

1. Description

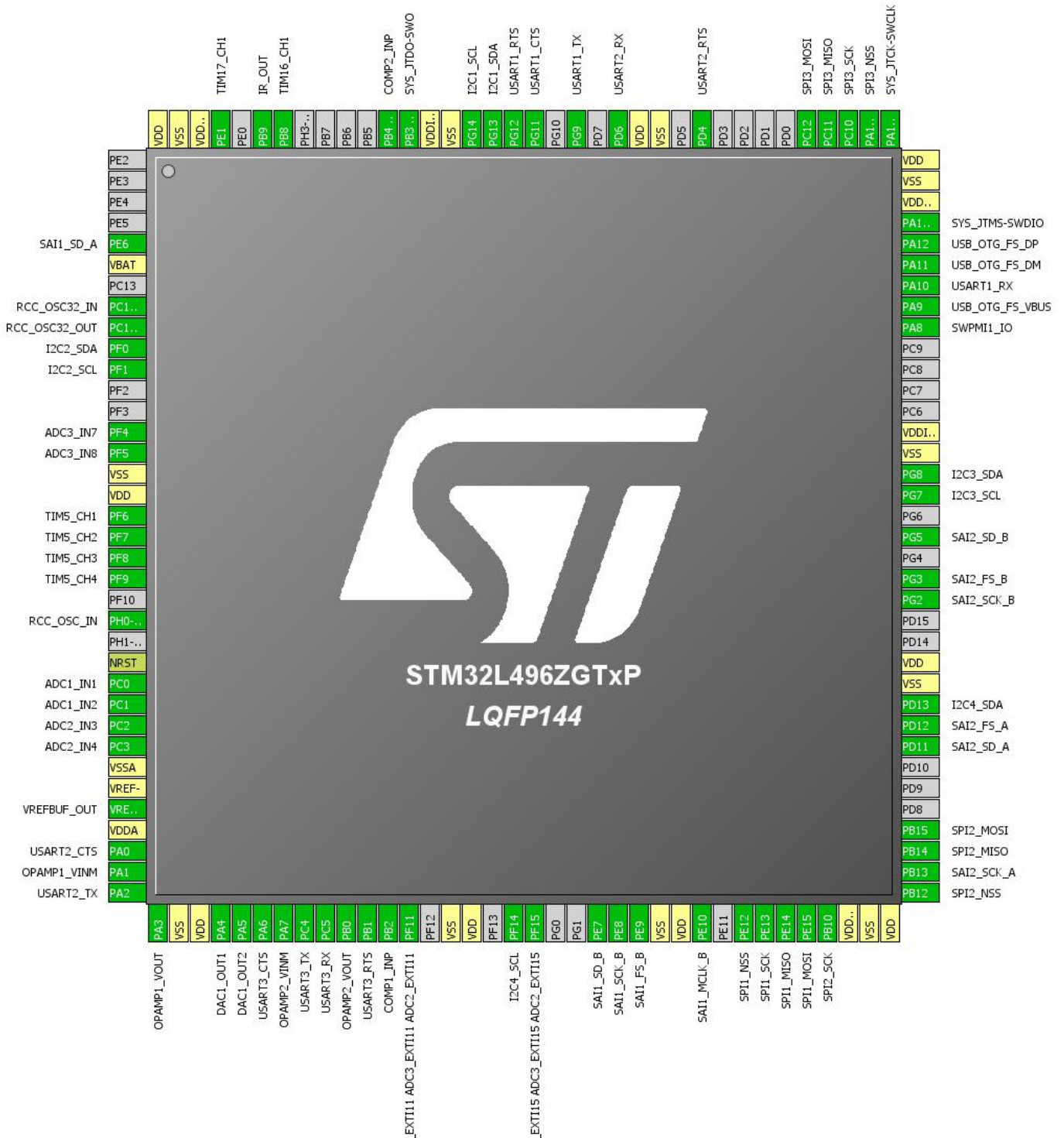
1.1. Project

| | |
|-----------------|--------------------|
| Project Name | TrueSTUDIO |
| Board Name | TrueSTUDIO |
| Generated with: | STM32CubeMX 4.24.0 |
| Date | 03/07/2018 |

1.2. MCU

| | |
|----------------|----------------|
| MCU Series | STM32L4 |
| MCU Line | STM32L4x6 |
| MCU name | STM32L496ZGTxP |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

2. Pinout Configuration



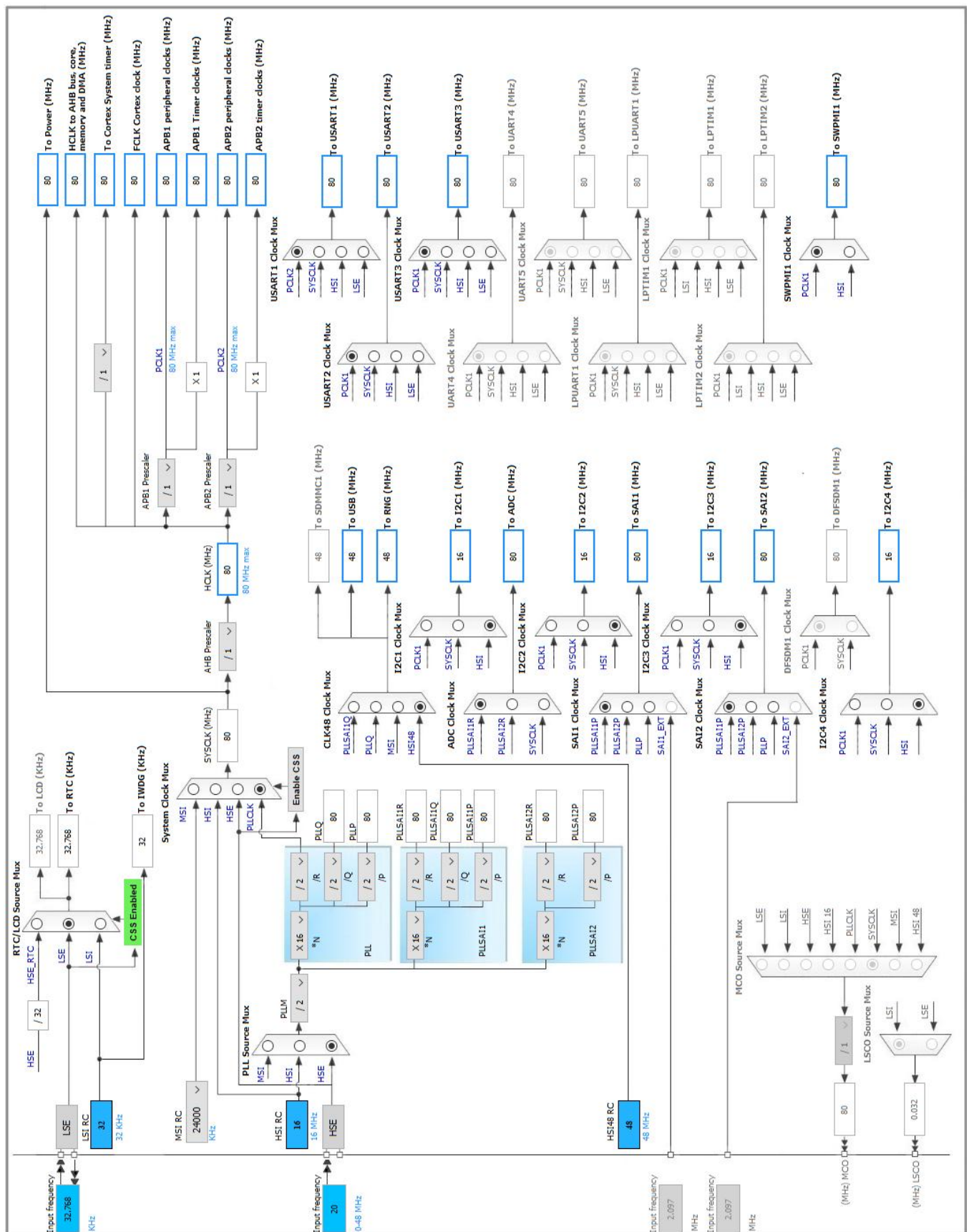
3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|-------|
| 5 | PE6 | I/O | SAI1_SD_A | |
| 6 | VBAT | Power | | |
| 8 | PC14-OSC32_IN (PC14) | I/O | RCC_OSC32_IN | |
| 9 | PC15-OSC32_OUT (PC15) | I/O | RCC_OSC32_OUT | |
| 10 | PF0 | I/O | I2C2_SDA | |
| 11 | PF1 | I/O | I2C2_SCL | |
| 14 | PF4 | I/O | ADC3_IN7 | |
| 15 | PF5 | I/O | ADC3_IN8 | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PF6 | I/O | TIM5_CH1 | |
| 19 | PF7 | I/O | TIM5_CH2 | |
| 20 | PF8 | I/O | TIM5_CH3 | |
| 21 | PF9 | I/O | TIM5_CH4 | |
| 23 | PH0-OSC_IN (PH0) | I/O | RCC_OSC_IN | |
| 25 | NRST | Reset | | |
| 26 | PC0 | I/O | ADC1_IN1 | |
| 27 | PC1 | I/O | ADC1_IN2 | |
| 28 | PC2 | I/O | ADC2_IN3 | |
| 29 | PC3 | I/O | ADC2_IN4 | |
| 30 | VSSA | Power | | |
| 31 | VREF- | Power | | |
| 32 | VREF+ | MonolO | VREFBUF_OUT | |
| 33 | VDDA | Power | | |
| 34 | PA0 | I/O | USART2_CTS | |
| 35 | PA1 | I/O | OPAMP1_VINM | |
| 36 | PA2 | I/O | USART2_TX | |
| 37 | PA3 | I/O | OPAMP1_VOUT | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 40 | PA4 | I/O | DAC1_OUT1 | |
| 41 | PA5 | I/O | DAC1_OUT2 | |
| 42 | PA6 | I/O | USART3_CTS | |
| 43 | PA7 | I/O | OPAMP2_VINM | |
| 44 | PC4 | I/O | USART3_TX | |
| 45 | PC5 | I/O | USART3_RX | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|---|-------|
| 46 | PB0 | I/O | OPAMP2_VOUT | |
| 47 | PB1 | I/O | USART3_RTS | |
| 48 | PB2 | I/O | COMP1_INP | |
| 49 | PF11 | I/O | ADC1_EXTI11, ADC3_EXTI11, ADC2_EXTI11 | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 54 | PF14 | I/O | I2C4_SCL | |
| 55 | PF15 | I/O | ADC1_EXTI15, ADC3_EXTI15, ADC2_EXTI15 | |
| 58 | PE7 | I/O | SAI1_SD_B | |
| 59 | PE8 | I/O | SAI1_SCK_B | |
| 60 | PE9 | I/O | SAI1_FS_B | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 63 | PE10 | I/O | SAI1_MCLK_B | |
| 65 | PE12 | I/O | SPI1_NSS | |
| 66 | PE13 | I/O | SPI1_SCK | |
| 67 | PE14 | I/O | SPI1_MISO | |
| 68 | PE15 | I/O | SPI1_MOSI | |
| 69 | PB10 | I/O | SPI2_SCK | |
| 70 | VDD12 | Power | | |
| 71 | VSS | Power | | |
| 72 | VDD | Power | | |
| 73 | PB12 | I/O | SPI2_NSS | |
| 74 | PB13 | I/O | SAI2_SCK_A | |
| 75 | PB14 | I/O | SPI2_MISO | |
| 76 | PB15 | I/O | SPI2_MOSI | |
| 80 | PD11 | I/O | SAI2_SD_A | |
| 81 | PD12 | I/O | SAI2_FS_A | |
| 82 | PD13 | I/O | I2C4_SDA | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 87 | PG2 | I/O | SAI2_SCK_B | |
| 88 | PG3 | I/O | SAI2_FS_B | |
| 90 | PG5 | I/O | SAI2_SD_B | |
| 92 | PG7 | I/O | I2C3_SCL | |
| 93 | PG8 | I/O | I2C3_SDA | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|-------|
| 94 | VSS | Power | | |
| 95 | VDDIO2 | Power | | |
| 100 | PA8 | I/O | SWPMI1_IO | |
| 101 | PA9 | I/O | USB_OTG_FS_VBUS | |
| 102 | PA10 | I/O | USART1_RX | |
| 103 | PA11 | I/O | USB_OTG_FS_DM | |
| 104 | PA12 | I/O | USB_OTG_FS_DP | |
| 105 | PA13 (JTMS/SWDIO) | I/O | SYS_JTMS-SWDIO | |
| 106 | VDDUSB | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 (JTCK/SWCLK) | I/O | SYS_JTCK-SWCLK | |
| 110 | PA15 (JTDI) | I/O | SPI3_NSS | |
| 111 | PC10 | I/O | SPI3_SCK | |
| 112 | PC11 | I/O | SPI3_MISO | |
| 113 | PC12 | I/O | SPI3_MOSI | |
| 118 | PD4 | I/O | USART2_RTS | |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 122 | PD6 | I/O | USART2_RX | |
| 124 | PG9 | I/O | USART1_TX | |
| 126 | PG11 | I/O | USART1_CTS | |
| 127 | PG12 | I/O | USART1_RTS | |
| 128 | PG13 | I/O | I2C1_SDA | |
| 129 | PG14 | I/O | I2C1_SCL | |
| 130 | VSS | Power | | |
| 131 | VDDIO2 | Power | | |
| 132 | PB3 (JTDO/TRACESWO) | I/O | SYS_JTDO-SWO | |
| 133 | PB4 (NJTRST) | I/O | COMP2_INP | |
| 138 | PB8 | I/O | TIM16_CH1 | |
| 139 | PB9 | I/O | IR_OUT | |
| 141 | PE1 | I/O | TIM17_CH1 | |
| 142 | VDD12 | Power | | |
| 143 | VSS | Power | | |
| 144 | VDD | Power | | |

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Differential

mode: Temperature Sensor Channel

mode: Vbat Channel

mode: Vrefint Channel

Conversion Trigger: Regular and Injected Conversion Trigger

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source EXTI Line11

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 1

Sampling Time 2.5 Cycles

Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

5.2. ADC2

IN3: IN3 Differential

Conversion Trigger: Regular and Injected Conversion Trigger

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source EXTI Line11

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 3

Sampling Time 2.5 Cycles

Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

5.3. ADC3

IN7: IN7 Differential

Conversion Trigger: Regular and Injected Conversion Trigger

5.3.1. Parameter Settings:

ADC_Settings:

| | |
|-------------------------------|--------------------------------------|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Low Power Auto Wait | Disabled |

ADC_Regular_ConversionMode:

| | |
|------------------------------------|--------------------------------------|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Disable |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | EXTI Line11 |
| External Trigger Conversion Edge | Trigger detection on the rising edge |
| <u>Rank</u> | 1 |
| Channel | Channel 7 |
| Sampling Time | 2.5 Cycles |
| Offset Number | No offset |

ADC_Injected_ConversionMode:

| | |
|-----------------------------|---------|
| Enable Injected Conversions | Disable |
|-----------------------------|---------|

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

5.4. COMP1

mode: Input [+]

Input [-]: 3/4 Internal VRef

5.4.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------|------------|
| Speed / Power Mode | High Speed |
| Trigger Mode | None |
| Hysteresis Level | None |

Output Configuration:

| | |
|-----------------|------------------------------------|
| Blanking Source | None |
| Output Pol | COMP output on GPIO isn't inverted |

5.5. COMP2

Input [+]: INP

Input [-]: 3/4 Internal VRef

5.5.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------|------------|
| Speed / Power Mode | High Speed |
| Trigger Mode | None |
| Hysteresis Level | None |

Output Configuration:

| | |
|-----------------|------------------------------------|
| Blanking Source | None |
| Output Pol | COMP output on GPIO isn't inverted |

5.6. CRC

mode: Activated

5.6.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------------|--------|
| Default Polynomial State | Enable |
| Default Init Value State | Enable |

Advanced Parameters:

| | |
|----------------------------|---------|
| Input Data Inversion Mode | None |
| Output Data Inversion Mode | Disable |
| Input Data Format | Bytes |

5.7. DAC1

OUT1 mode: Connected to external pin and to on chip-peripherals

OUT2 mode: Connected to external pin and to on chip-peripherals

5.7.1. Parameter Settings:

DAC Out1 Settings:

| | |
|-----------------|-----------------------|
| Output Buffer | Enable |
| Trigger | None |
| User Trimming | Factory trimming |
| Sample And Hold | Sampleandhold Disable |

DAC Out2 Settings:

| | |
|-----------------|-----------------------|
| Output Buffer | Enable |
| Trigger | None |
| User Trimming | Factory trimming |
| Sample And Hold | Sampleandhold Disable |

5.8. DMA2D

mode: Activated

5.8.1. Parameter Settings:

Basic Parameters:

| | |
|---------------|------------------|
| Transfer Mode | Memory to Memory |
| Color Mode | ARGB8888 |
| Output Offset | 0 |

Foreground layer Configuration:

| | |
|-------------------------|--|
| DMA2D Input Color Mode | ARGB8888 |
| DMA2D ALPHA MODE | No modification of the alpha channel value |
| Input Alpha | 0 |
| Input Offset | 0 |
| DMA2D ALPHA Inversion | Regular Alpha |
| DMA2D Red and Blue swap | Regular mode (RGB or ARGB) |

5.9. I2C1

I2C: I2C

5.9.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x0010061A * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.10. I2C2

I2C: I2C

5.10.1. Parameter Settings:

Timing configuration:

| | |
|---------------------------|--------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |

| | |
|-------------------------------|---------------------|
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x0010061A * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.11. I2C3

I2C: I2C

5.11.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x0010061A * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.12. I2C4

I2C: I2C

5.12.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x0010061A * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.13. IRTIM

mode: Activate

5.14. IWDG

mode: Activated

5.14.1. Parameter Settings:

Watchdog Clocking:

| | |
|--------------------------------|------|
| IWDG counter clock prescaler | 4 |
| IWDG window value | 4095 |
| IWDG down-counter reload value | 4095 |

5.15. OPAMP1

Mode: PGA Connected-DAC_OUT1-INP

5.15.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------|------------------------|
| Power Supply Range | Power Supply Range Low |
| Power Mode | Normal |
| PGA Gain | 2 |

| | |
|---------------|---------|
| User Trimming | Disable |
|---------------|---------|

5.16. OPAMP2

Mode: PGA Connected-DAC_OUT2-INP

5.16.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------|------------------------|
| Power Supply Range | Power Supply Range Low |
| Power Mode | Normal |
| PGA Gain | 2 |
| User Trimming | Disable |

5.17. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

CRS SYNC: CRS SYNC Source USB

5.17.1. Parameter Settings:

System Parameters:

| | |
|-------------------|--------------------|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Disabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 4 WS (5 CPU cycle) |

RCC Parameters:

| | |
|--------------------------------|-------------------------------------|
| HSI Calibration Value | 64 |
| MSI Calibration Value | 0 |
| MSI Auto Calibration | Disabled |
| HSE Startup Timeout Value (ms) | 100 |
| LSE Startup Timeout Value (ms) | 5000 |
| LSE Drive Capability | LSE oscillator low drive capability |

Power Parameters:

| | |
|-------------------------------|---------------------------------|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |
|-------------------------------|---------------------------------|

CRS Parameters:

| | |
|-------------------------------|-----------------------|
| CRS Synchro Divider | 1 |
| CRS Synchro Polarity | Active on rising edge |
| CRS Synchro Reload Value Type | Automatic |
| CRS Synchro frequency (Hz) | 1000 |
| Error limit Value | 34 |
| HSI48 Calibration Value | 32 |

5.18. RNG

mode: Activated

5.19. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

Alarm B: Internal Alarm B

WakeUp: Internal WakeUp

5.19.1. Parameter Settings:

General:

| | |
|-------------------------------|---------------|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 127 |
| Synchronous Predivider value | 255 |

Calendar Time:

| | |
|--|-----------------------------|
| Data Format | Binary data format * |
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Day Light Saving: value of hour adjustment | Daylightsaving None |
| Store Operation | Storeoperation Reset |

Calendar Date:

| | |
|----------|-------------|
| Week Day | Monday |
| Month | January |
| Date | 1 |
| Year | 80 * |

Alarm A:

| | |
|---------|---|
| Hours | 0 |
| Minutes | 0 |

| | |
|--------------------------|---------------------------------|
| Seconds | 0 |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Disable |
| Alarm Mask Hours | Disable |
| Alarm Mask Minutes | Disable |
| Alarm Mask Seconds | Disable |
| Alarm Sub Second Mask | All Alarm SS fields are masked. |
| Alarm Date Week Day Sel | Date |
| Alarm Date | 1 |

Alarm B:

| | |
|--------------------------|---------------------------------|
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Disable |
| Alarm Mask Hours | Disable |
| Alarm Mask Minutes | Disable |
| Alarm Mask Seconds | Disable |
| Alarm Sub Second Mask | All Alarm SS fields are masked. |
| Alarm Date Week Day Sel | Date |
| Alarm Date | 1 |

Wake UP:

| | |
|-----------------|-------------|
| Wake Up Clock | RTCCLK / 16 |
| Wake Up Counter | 0 |

5.20. SAI1

Mode: SPDIF TX Transmitter (IEC60958)

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

5.20.1. Parameter Settings:

SAI A:

Basic Parameters

| | |
|-----------------|--------------------|
| Protocol | SPDIF |
| Audio Mode | Master Transmit |
| Output Mode | Stereo |
| Companding Mode | No companding mode |

Clock Parameters

| | |
|--------------------------|----------|
| Audio Frequency | 48 KHz |
| Real Audio Frequency | 0 |
| Advanced Parameters | |
| Fifo Threshold | Empty |
| Output Drive | Disabled |
| Synchronization External | Disabled |

SAI B:

| | |
|------------------------------------|--------------------|
| Basic Parameters | |
| Audio Mode | Master Transmit |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| Protocol Parameters | |
| Protocol | I2S Standard |
| Data Size | 16 Bits |
| Number of Slots (only Even Values) | 2 |
| Clock Parameters | |
| Master Clock Divider | Enabled |
| Audio Frequency | 192 KHz |
| Real Audio Frequency | 0 |
| Error between Selected | 0 |
| Advanced Parameters | |
| Fifo Threshold | Empty |
| Output Drive | Disabled |
| Synchronization External | Disabled |

5.21. SAI2

Mode: Asynchronous Slave

Mode: Asynchronous Slave

mode: I2S/PCM Protocol

5.21.1. Parameter Settings:

SAI A:

| | |
|---------------------------------|---------------|
| Basic Parameters | |
| Protocol | Free |
| Audio Mode | Slave Receive |
| Frame Length (only Even Values) | 24 |
| Data Size | 24 Bits |
| Slot Size | DataSize |

| | |
|-----------------------------------|--------------------|
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| Frame Parameters | |
| First Bit | MSB First |
| Frame Synchro Active Level Length | 1 |
| Frame Synchro Definition | Start Frame |
| Frame Synchro Polarity | Active Low |
| Frame Synchro Offset | First Bit |
| Slot Parameters | |
| First Bit Offset | 0 |
| Number of Slots | 1 |
| Slot Active Final Value | 0x00000000 |
| Slot Active | Neither |
| Clock Parameters | |
| Clock Strobing | Falling Edge |
| Advanced Parameters | |
| Fifo Threshold | Empty |
| Output Drive | Disabled |
| Synchronization External | Disabled |

SAI B:

| | |
|------------------------------------|--------------------|
| Basic Parameters | |
| Audio Mode | Slave Receive |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| Protocol Parameters | |
| Protocol | I2S Standard |
| Data Size | 16 Bits |
| Number of Slots (only Even Values) | 2 |
| Clock Parameters | |
| Real Audio Frequency | 0 |
| Error between Selected | 0 |
| Advanced Parameters | |
| Fifo Threshold | Empty |
| Output Drive | Disabled |
| Synchronization External | Disabled |

5.22. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.22.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------------|
| Frame Format | Motorola |
| Data Size | 8 Bits * |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 4 * |
| Baud Rate | 20.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|-----------------|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Output Hardware |

5.23. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.23.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------------|
| Frame Format | Motorola |
| Data Size | 8 Bits * |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 4 * |
| Baud Rate | 20.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|----------|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |

NSS Signal Type

Output Hardware

5.24. SPI3

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.24.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------------|
| Frame Format | Motorola |
| Data Size | 8 Bits * |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 4 * |
| Baud Rate | 20.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|-----------------|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Output Hardware |

5.25. SWPMI1

Mode: Full-Duplex (normal mode)

5.25.1. Parameter Settings:

Basic Parameters:

| | |
|-----------------------------|--------------------|
| Voltage Class | Class B |
| Bit Rate Prescaler | 49 * |
| SWPMI Clock frequency | 80000 |
| Bit Rate | 400 |
| Transmission Buffering Mode | No Software buffer |
| Reception Buffering Mode | No Software buffer |

5.26. SYS

Debug: Trace Asynchronous Sw

Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)

VREFBUF Mode: Internal voltage reference

Timebase Source: TIM2

5.26.1. Parameter Settings:

Programmable_Voltage_Detector_Settings:

| | |
|---------------------|-------------------------|
| PVD detection Level | PWR PVD LEVEL 0 (2.0 V) |
| PWR PVD Mode | basic mode is used |

Voltage_Reference_Buffer_Settings:

| | |
|----------------------------------|-------------------------|
| Trimming Mode | Factory Trimming |
| Internal Voltage reference scale | SCALE 0: around 2.048 V |

5.27. TIM1

Clock Source : Internal Clock

5.27.1. Parameter Settings:

Counter Settings:

| | |
|---|-------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|-------------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

5.28. TIM5

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

5.28.1. Parameter Settings:

Counter Settings:

| | |
|---|-------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|------------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

Input Capture Channel 1:

| | |
|-----------------------------|-------------|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

Input Capture Channel 2:

| | |
|-----------------------------|-------------|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

Input Capture Channel 3:

| | |
|-----------------------------|-------------|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

Input Capture Channel 4:

| | |
|-----------------------------|-------------|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

5.29. TIM16

mode: Activated

Channel1: Output Compare CH1

5.29.1. Parameter Settings:

Counter Settings:

| | |
|---|-------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Break And Dead Time management - BRK Configuration:

| | |
|---------------------------|---------|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |
| BRK Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - DFSDM | Disable |

Break And Dead Time management - Output Configuration:

| | |
|--|---------|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

Output Compare Channel 1:

| | |
|-----------------------|-------------------------------|
| Mode | Frozen (used for Timing base) |
| Pulse (16 bits value) | 0 |
| CH Polarity | High |
| CH Idle State | Reset |

5.30. TIM17

mode: Activated

Channel1: Output Compare CH1

5.30.1. Parameter Settings:

Counter Settings:

| | |
|---|-------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

Break And Dead Time management - BRK Configuration:

| | |
|---------------------------|---------|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |
| BRK Sources Configuration | |
| - Digital Input | Disable |
| - COMP1 | Disable |
| - COMP2 | Disable |
| - DFSDM | Disable |

Break And Dead Time management - Output Configuration:

| | |
|--|---------|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

Output Compare Channel 1:

| | |
|-----------------------|-------------------------------|
| Mode | Frozen (used for Timing base) |
| Pulse (16 bits value) | 0 |
| CH Polarity | High |
| CH Idle State | Reset |

5.31. USART1

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.31.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |

| | |
|-------------------------------|----------------------|
| Stop Bits | 1 |
| Advanced Parameters: | |
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| Advanced Features: | |
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.32. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.32.1. Parameter Settings:

| | |
|-------------------------------|---------------------------|
| Basic Parameters: | |
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |
| Advanced Parameters: | |
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| Advanced Features: | |
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.33. USART3

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.33.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.34. USB_OTG_FS

Mode: Device_Only

Activate_VBUS: VBUS sensing

5.34.1. Parameter Settings:

| | |
|----------------------------|---------------------|
| Speed | Full Speed 12MBit/s |
| Endpoint 0 Max Packet size | 64 Bytes |
| Enable internal IP DMA | Enabled * |
| Low power | Disabled |
| Battery charging | Enabled |

| | |
|-------------------------------------|------------------|
| Link Power Management | Enabled * |
| Use dedicated end point 1 interrupt | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Disabled |

5.35. FREERTOS

mode: Enabled

5.35.1. Config parameters:

Versions:

| | |
|--------------------|-------|
| FreeRTOS version | 9.0.0 |
| CMSIS-RTOS version | 1.02 |

Kernel settings:

| | |
|-----------------------------------|-----------------|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |

Memory management settings:

| | |
|--------------------------|---------|
| Memory Allocation | Dynamic |
| TOTAL_HEAP_SIZE | 3000 |
| Memory Management scheme | heap_4 |

Hook function related definitions:

| | |
|------------------------|----------|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |

| | |
|------------------------------|----------|
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

Run time and task stats gathering related definitions:

| | |
|--------------------------------|----------|
| GENERATE_RUN_TIME_STATS | Disabled |
| USE_TRACE_FACILITY | Disabled |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

Co-routine related definitions:

| | |
|---------------------------|----------|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

Software timer definitions:

| | |
|------------|----------|
| USE_TIMERS | Disabled |
|------------|----------|

Interrupt nesting behaviour configuration:

| | |
|--|----|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

5.35.2. Include parameters:

Include definitions:

| | |
|-----------------------------|----------|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |

5.36. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.36.1. Parameter Settings:

Basic Parameters:

| | |
|--|------------------------------------|
| USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces) | 1 |
| USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration) | 1 |
| USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors) | 512 |
| USBD_SUPPORT_USER_STRING (Enable user string descriptor) | Disabled |
| USBD_SELF_POWERED (Enabled self power) | Enabled |
| USBD_DEBUG_LEVEL (USBD Debug Level) | 0: No debug message |
| USBD_LPM_ENABLED (Link Power Management) | 1: Link Power Management supported |

Class Parameters:

| | |
|------------------------|------|
| USB CDC Rx Buffer Size | 2048 |
| USB CDC Tx Buffer Size | 2048 |

5.36.2. Device Descriptor:

Device Descriptor:

| | |
|---|------------------------|
| VID (Vendor Identifier) | 1155 |
| LANGID_STRING (Language Identifier) | English(United States) |
| MANUFACTURER_STRING (Manufacturer Identifier) | STMicroelectronics |

Device Descriptor FS:

| | |
|---|-----------------------|
| PID (Product Identifier) | 22336 |
| PRODUCT_STRING (Product Identifier) | STM32 Virtual ComPort |
| SERIALNUMBER_STRING (Serial number) | 00000000001A |
| CONFIGURATION_STRING (Configuration Identifier) | CDC Config |
| INTERFACE_STRING (Interface Identifier) | CDC Interface |

* User modified value

6. System Configuration

6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|-------|--------------|-------------|--|-----------------------------|-------------|------------|
| ADC1 | PC0 | ADC1_IN1 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PC1 | ADC1_IN2 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PF11 | ADC1_EXTI11 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| | PF15 | ADC1_EXTI15 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| ADC2 | PC2 | ADC2_IN3 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PC3 | ADC2_IN4 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PF11 | ADC2_EXTI11 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| | PF15 | ADC2_EXTI15 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| ADC3 | PF4 | ADC3_IN7 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PF5 | ADC3_IN8 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | |
| | PF11 | ADC3_EXTI11 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| | PF15 | ADC3_EXTI15 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| COMP1 | PB2 | COMP1_INP | Analog mode | No pull-up and no pull-down | n/a | |
| COMP2 | PB4 (NJTRST) | COMP2_INP | Analog mode | No pull-up and no pull-down | n/a | |
| DAC1 | PA4 | DAC1_OUT1 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA5 | DAC1_OUT2 | Analog mode | No pull-up and no pull-down | n/a | |
| I2C1 | PG13 | I2C1_SDA | Alternate Function Open Drain | Pull-up | Very High * | |
| | PG14 | I2C1_SCL | Alternate Function Open Drain | Pull-up | Very High * | |
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | Pull-up | Very High * | |
| | PF1 | I2C2_SCL | Alternate Function Open | Pull-up | Very High | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|--------|-----------------------|---------------|-------------------------------|-----------------------------|-------------|------------|
| | | | Drain | | * | |
| I2C3 | PG7 | I2C3_SCL | Alternate Function Open Drain | Pull-up | Very High * | |
| | PG8 | I2C3_SDA | Alternate Function Open Drain | Pull-up | Very High * | |
| I2C4 | PF14 | I2C4_SCL | Alternate Function Open Drain | Pull-up | Very High * | |
| | PD13 | I2C4_SDA | Alternate Function Open Drain | Pull-up | Very High * | |
| IRTIM | PB9 | IR_OUT | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| OPAMP1 | PA1 | OPAMP1_VINM | n/a | n/a | n/a | |
| | PA3 | OPAMP1_VOUT | Analog mode | No pull-up and no pull-down | n/a | |
| OPAMP2 | PA7 | OPAMP2_VINM | n/a | n/a | n/a | |
| | PB0 | OPAMP2_VOUT | Analog mode | No pull-up and no pull-down | n/a | |
| RCC | PC14-OSC32_IN (PC14) | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT (PC15) | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | |
| SAI1 | PE6 | SAI1_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE7 | SAI1_SD_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE8 | SAI1_SCK_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE9 | SAI1_FS_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PE10 | SAI1_MCLK_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| SAI2 | PB13 | SAI2_SCK_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD11 | SAI2_SD_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PD12 | SAI2_FS_A | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PG2 | SAI2_SCK_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PG3 | SAI2_FS_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PG5 | SAI2_SD_B | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| SPI1 | PE12 | SPI1_NSS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PE13 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PE14 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|--------|---------------------|----------------|------------------------------|-----------------------------|-----------------------|------------|
| | PE15 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| SPI2 | PB10 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PB12 | SPI2_NSS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PB14 | SPI2_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PB15 | SPI2_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| SPI3 | PA15 (JTDI) | SPI3_NSS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PC10 | SPI3_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PC11 | SPI3_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PC12 | SPI3_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| SWPMI1 | PA8 | SWPMI1_IO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| SYS | VREF+ | VREFBUF_OUT | n/a | n/a | n/a | |
| | PA13 (JTMS/SWDIO) | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 (JTCK/SWCLK) | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| | PB3 (JTDO/TRACESWO) | SYS_JTDO-SWO | n/a | n/a | n/a | |
| TIM5 | PF6 | TIM5_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PF7 | TIM5_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PF8 | TIM5_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PF9 | TIM5_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM16 | PB8 | TIM16_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM17 | PE1 | TIM17_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USART1 | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PG9 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|------------|------|-----------------|------------------------------|-----------------------------|----------------|------------|
| | | | | | * | |
| | PG11 | USART1_CTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PG12 | USART1_RTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| USART2 | PA0 | USART2_CTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PA2 | USART2_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PD4 | USART2_RTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PD6 | USART2_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| USART3 | PA6 | USART3_CTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PC4 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PC5 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PB1 | USART3_RTS | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| USB_OTG_FS | PA9 | USB_OTG_FS_VBUS | Input mode | No pull-up and no pull-down | n/a | |
| | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Prefetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| TIM2 global interrupt | true | 0 | 0 |
| USB OTG FS global interrupt | true | 5 | 0 |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38 | unused | | |
| RTC tamper and time stamp, CSS on LSE interrupts through EXTI line 19 | unused | | |
| RTC wake-up interrupt through EXTI line 20 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1 and ADC2 interrupts | unused | | |
| TIM1 break interrupt and TIM15 global interrupt | unused | | |
| TIM1 update interrupt and TIM16 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM17 global interrupt | unused | | |
| TIM1 capture compare interrupt | unused | | |
| I2C1 event interrupt | unused | | |
| I2C1 error interrupt | unused | | |
| I2C2 event interrupt | unused | | |
| I2C2 error interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| USART2 global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| EXTI line[15:10] interrupts | unused | | |
| RTC alarm interrupt through EXTI line 18 | unused | | |
| ADC3 global interrupt | unused | | |
| TIM5 global interrupt | unused | | |
| SPI3 global interrupt | unused | | |
| TIM6 global interrupt, DAC channel1 and | unused | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|--------|----------------------|-------------|
| channel2 underrun error interrupts | | | |
| COMP1 and COMP2 interrupts through EXTI lines 21 and 22 | | unused | |
| I2C3 event interrupt | | unused | |
| I2C3 error interrupt | | unused | |
| SAI1 global interrupt | | unused | |
| SAI2 global interrupt | | unused | |
| SWPMI1 global interrupt | | unused | |
| HASH and RNG global interrupts | | unused | |
| FPU global interrupt | | unused | |
| CRS global interrupt | | unused | |
| I2C4 event interrupt | | unused | |
| I2C4 error interrupt | | unused | |
| DMA2D global interrupt | | unused | |

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|-----------|----------------|
| Series | STM32L4 |
| Line | STM32L4x6 |
| MCU | STM32L496ZGTxP |
| Datasheet | 029173_Rev2 |

7.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.6 |

7.3. SMPS Selection

| | |
|------------|----------|
| SMPS | SMPS1_ST |
| Vin | 3.0 V |
| Vout | 1.1 V |
| OffCurrent | 250.0 nA |
| QCurrent | 500.0 nA |
| Efficiency | 85 % |

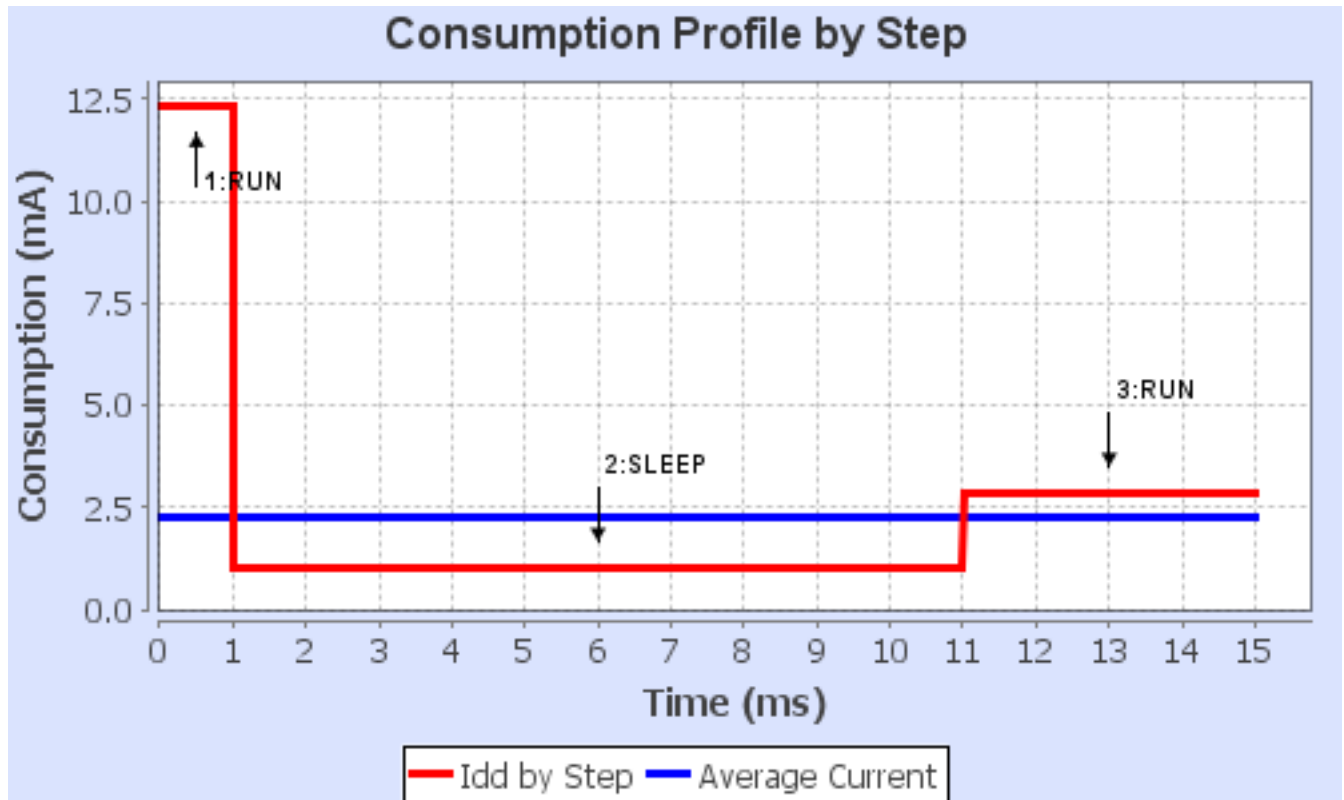
7.4. Sequence

| Step | Step1 | Step2 | Step3 |
|-------------------------------|---|--------------------------|---|
| Mode | RUN | SLEEP | RUN |
| SMPS | CONNECTED | CONNECTED | CONNECTED |
| Vdd | 3.6 | 3.6 | 3.6 |
| Voltage Source | Vbus | Vbus | Vbus |
| Range | Range1-High | Range1-High | Range1-High |
| Fetch Type | FLASH | FLASH | FLASH |
| Clock Configuration | HSE BYP PLL Flash-ON | HSE BYP PLL ART Flash-ON | HSE BYP Flash-ON |
| Clock Source Frequency | 4 MHz | 4 MHz | 16 MHz |
| CPU Frequency | 80 MHz | 80 MHz | 16 MHz |
| Peripherals | ADC1:fs_10_ksp AHB_APB1_Bridge AHB_APB2_Bridge CRC GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 I2C2 I2C3 I2C4 PVD/BOR RNG RTC SPI1 SPI2 SPI3 SYS- VREFBUF/COMP1:C OMP_OFF_VREFBU F_ON_Iload-0uA SYS- VREFBUF/COMP2:C OMP_OFF_VREFBU F_ON_Iload-0uA TIM2 TIM5 TIM16 TIM17 TSC USB_OTG_FS | | ADC1:fs_10_ksp AHB_APB1_Bridge AHB_APB2_Bridge CRC GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 I2C2 I2C3 I2C4 PVD/BOR RNG RTC SPI1 SPI2 SPI3 SYS- VREFBUF/COMP1:C OMP_OFF_VREFBU F_ON_Iload-0uA SYS- VREFBUF/COMP2:C OMP_OFF_VREFBU F_ON_Iload-0uA TIM2 TIM5 TIM16 TIM17 TSC USB_OTG_FS |
| Additional Cons. | 0 mA | 0 mA | 0 mA |
| Average Current | 12.31 mA | 1.02 mA | 2.86 mA |
| Duration | 1 ms | 10 ms | 4 ms |
| DMIPS | 0.0 | 0.0 | 0.0 |
| Ta Max | 103.58 | 104.88 | 104.67 |
| Category | Measurements | Measurements | Measurements |

7.5. RESULTS

| | | | |
|---------------|-------|-----------------|-------------|
| Sequence Time | 15 ms | Average Current | 2.26 mA |
| Battery Life | 0 | Average DMIPS | 78.67 DMIPS |

7.6. Chart



8. Software Project

8.1. Project Settings

| Name | Value |
|-----------------------------------|---|
| Project Name | TrueSTUDIO |
| Project Folder | \\.\psf\Home\nfs_ds_nfs\git\HFT-Core-Module__SW\SW\TrueSTUDIO |
| Toolchain / IDE | TrueSTUDIO |
| Firmware Package Name and Version | STM32Cube FW_L4 V1.11.0 |

8.2. Code Generation Settings

| Name | Value |
|---|---------------------------------------|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

9. Software Pack Report