

1. Description

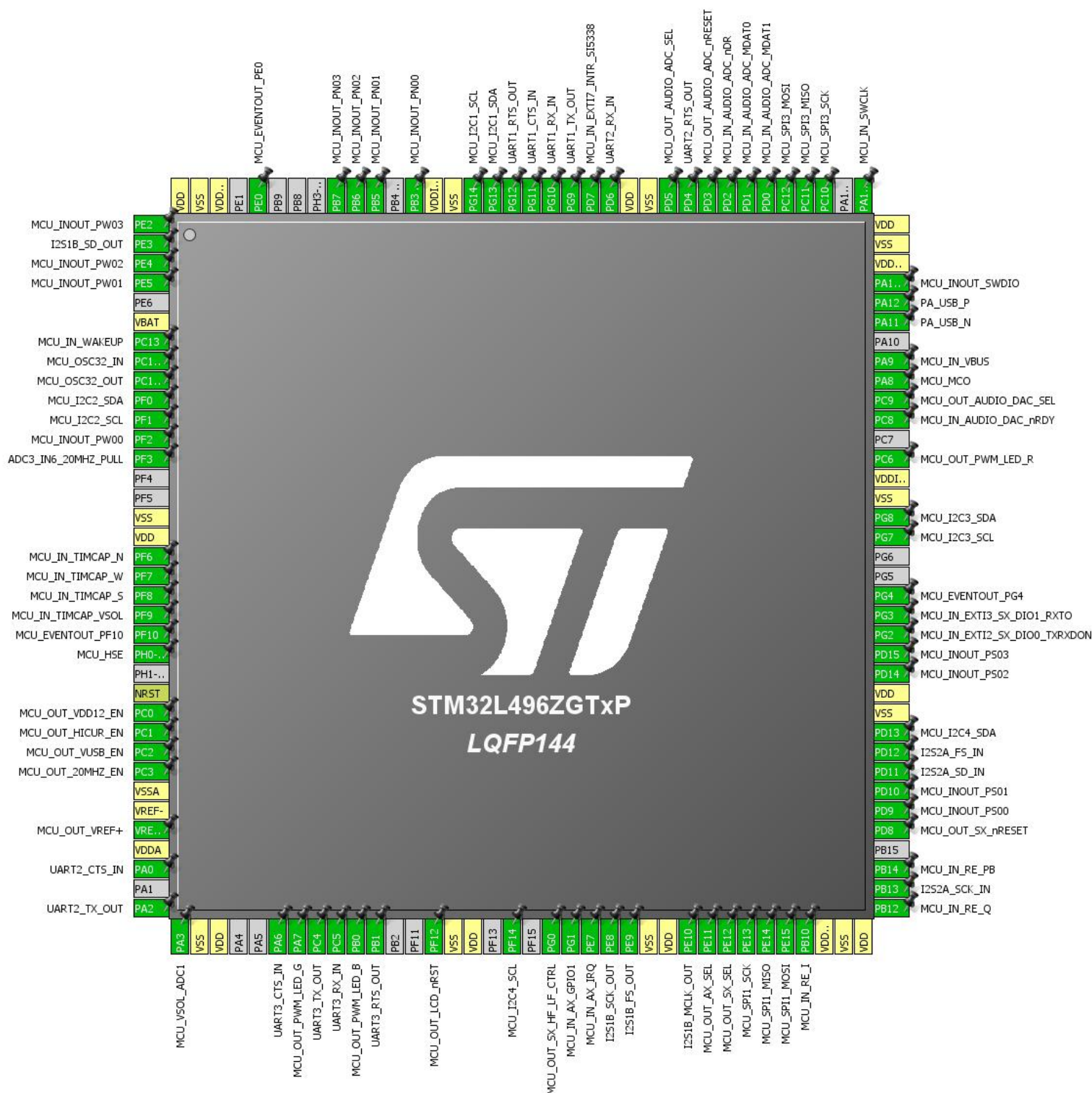
1.1. Project

| | |
|-----------------|----------------------------|
| Project Name | HFT-Core-Module_TrueSTUDIO |
| Board Name | HFT-Core-Module_TrueSTUDIO |
| Generated with: | STM32CubeMX 4.26.1 |
| Date | 10/07/2018 |

1.2. MCU

| | |
|----------------|----------------|
| MCU Series | STM32L4 |
| MCU Line | STM32L4x6 |
| MCU name | STM32L496ZGTxP |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

2. Pinout Configuration



3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|---------------------|
| 1 | PE2 * | I/O | GPIO_Input | MCU_INOUT_PW03 |
| 2 | PE3 | I/O | SAI1_SD_B | I2S1B_SD_OUT |
| 3 | PE4 * | I/O | GPIO_Input | MCU_INOUT_PW02 |
| 4 | PE5 * | I/O | GPIO_Input | MCU_INOUT_PW01 |
| 6 | VBAT | Power | | |
| 7 | PC13 | I/O | SYS_WKUP2 | MCU_IN_WAKEUP |
| 8 | PC14-OSC32_IN (PC14) | I/O | RCC_OSC32_IN | MCU_OSC32_IN |
| 9 | PC15-OSC32_OUT (PC15) | I/O | RCC_OSC32_OUT | MCU_OSC32_OUT |
| 10 | PF0 | I/O | I2C2_SDA | MCU_I2C2_SDA |
| 11 | PF1 | I/O | I2C2_SCL | MCU_I2C2_SCL |
| 12 | PF2 * | I/O | GPIO_Input | MCU_INOUT_PW00 |
| 13 | PF3 | I/O | ADC3_IN6 | ADC3_IN6_20MHZ_PULL |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PF6 | I/O | TIM5_CH1 | MCU_IN_TIMCAP_N |
| 19 | PF7 | I/O | TIM5_CH2 | MCU_IN_TIMCAP_W |
| 20 | PF8 | I/O | TIM5_CH3 | MCU_IN_TIMCAP_S |
| 21 | PF9 | I/O | TIM5_CH4 | MCU_IN_TIMCAP_VSOL |
| 22 | PF10 * | I/O | EVENTOUT | MCU_EVENTOUT_PF10 |
| 23 | PH0-OSC_IN (PH0) | I/O | RCC_OSC_IN | MCU_HSE |
| 25 | NRST | Reset | | |
| 26 | PC0 * | I/O | GPIO_Output | MCU_OUT_VDD12_EN |
| 27 | PC1 * | I/O | GPIO_Output | MCU_OUT_HICUR_EN |
| 28 | PC2 * | I/O | GPIO_Output | MCU_OUT_VUSB_EN |
| 29 | PC3 * | I/O | GPIO_Output | MCU_OUT_20MHZ_EN |
| 30 | VSSA | Power | | |
| 31 | VREF- | Power | | |
| 32 | VREF+ | MonoIO | VREFBUF_OUT | MCU_OUT_VREF+ |
| 33 | VDDA | Power | | |
| 34 | PA0 | I/O | USART2_CTS | UART2_CTS_IN |
| 36 | PA2 | I/O | USART2_TX | UART2_TX_OUT |
| 37 | PA3 | I/O | ADC2_IN8, ADC1_IN8 | MCU_VSOL_ADC1 |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 42 | PA6 | I/O | USART3_CTS | UART3_CTS_IN |
| 43 | PA7 | I/O | TIM3_CH2 | MCU_OUT_PWM_LED_G |

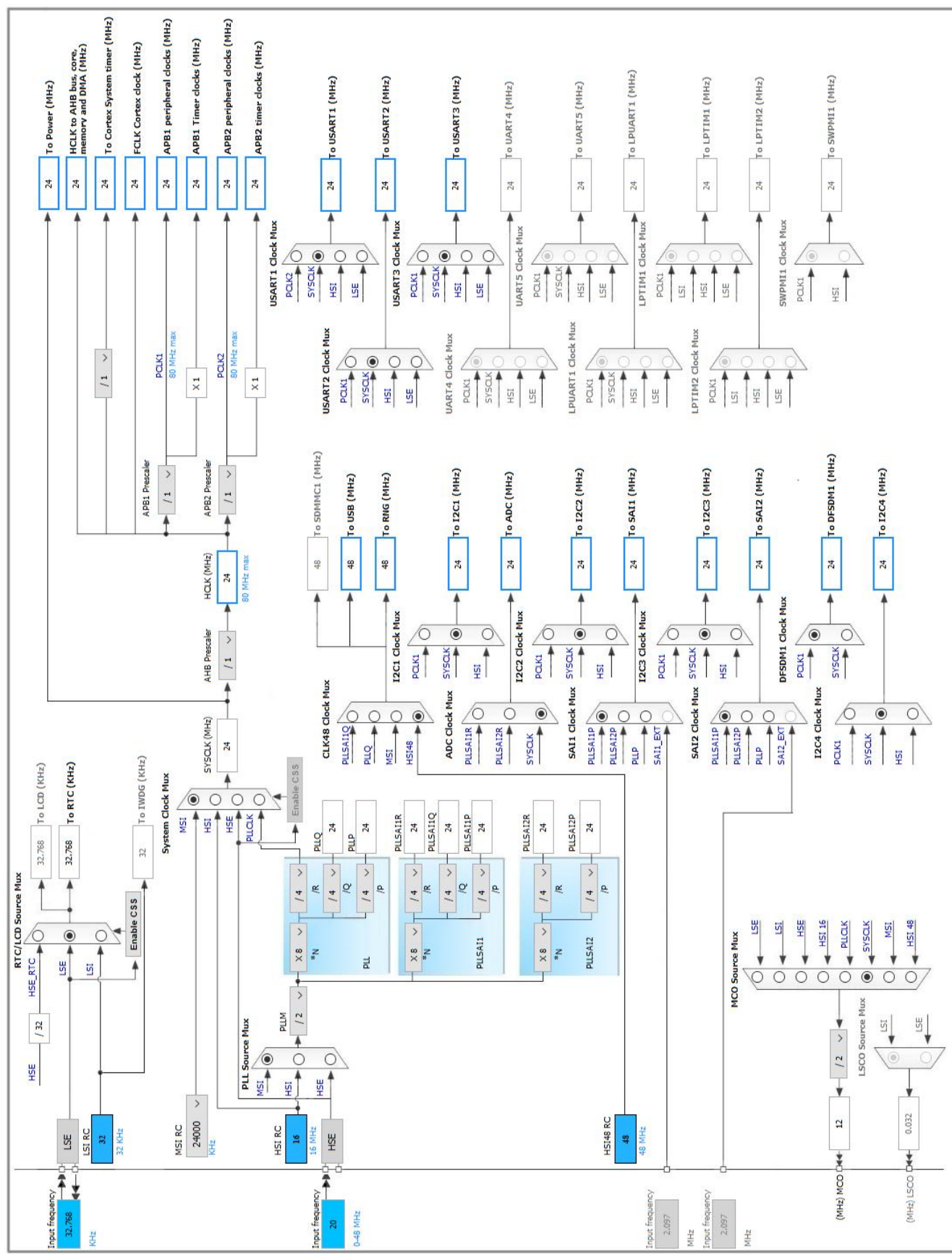
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|---------------------------|
| 44 | PC4 | I/O | USART3_TX | UART3_TX_OUT |
| 45 | PC5 | I/O | USART3_RX | UART3_RX_IN |
| 46 | PB0 | I/O | TIM3_CH3 | MCU_OUT_PWM_LED_B |
| 47 | PB1 | I/O | USART3_RTS | UART3_RTS_OUT |
| 50 | PF12 * | I/O | GPIO_Output | MCU_OUT_LCD_nRST |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 54 | PF14 | I/O | I2C4_SCL | MCU_I2C4_SCL |
| 56 | PG0 * | I/O | GPIO_Output | MCU_OUT_SX_HF_LF_CT RL |
| 57 | PG1 * | I/O | GPIO_Input | MCU_IN_AX_GPIO1 |
| 58 | PE7 * | I/O | GPIO_Input | MCU_IN_AX_IRQ |
| 59 | PE8 | I/O | SAI1_SCK_B | I2S1B_SCK_OUT |
| 60 | PE9 | I/O | SAI1_FS_B | I2S1B_FS_OUT |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 63 | PE10 | I/O | SAI1_MCLK_B | I2S1B_MCLK_OUT |
| 64 | PE11 * | I/O | GPIO_Output | MCU_OUT_AX_SEL |
| 65 | PE12 * | I/O | GPIO_Output | MCU_OUT_SX_SEL |
| 66 | PE13 | I/O | SPI1_SCK | MCU_SPI1_SCK |
| 67 | PE14 | I/O | SPI1_MISO | MCU_SPI1_MISO |
| 68 | PE15 | I/O | SPI1_MOSI | MCU_SPI1_MOSI |
| 69 | PB10 * | I/O | GPIO_Input | MCU_IN_RE_I |
| 70 | VDD12 | Power | | |
| 71 | VSS | Power | | |
| 72 | VDD | Power | | |
| 73 | PB12 * | I/O | GPIO_Input | MCU_IN_RE_Q |
| 74 | PB13 | I/O | SAI2_SCK_A | I2S2A_SCK_IN |
| 75 | PB14 * | I/O | GPIO_Input | MCU_IN_RE_PB |
| 77 | PD8 * | I/O | GPIO_Output | MCU_OUT_SX_nRESET |
| 78 | PD9 * | I/O | GPIO_Input | MCU_INOUT_PS00 |
| 79 | PD10 * | I/O | GPIO_Input | MCU_INOUT_PS01 |
| 80 | PD11 | I/O | SAI2_SD_A | I2S2A_SD_IN |
| 81 | PD12 | I/O | SAI2_FS_A | I2S2A_FS_IN |
| 82 | PD13 | I/O | I2C4_SDA | MCU_I2C4_SDA |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 85 | PD14 * | I/O | GPIO_Input | MCU_INOUT_PS02 |
| 86 | PD15 * | I/O | GPIO_Input | MCU_INOUT_PS03 |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|-----------------------------------|
| 87 | PG2 | I/O | GPIO_EXTI2 | MCU_IN_EXTI2_SX_DIO0_ TXRXDONE |
| 88 | PG3 | I/O | GPIO_EXTI3 | MCU_IN_EXTI3_SX_DIO1_ RXTO |
| 89 | PG4 * | I/O | EVENTOUT | MCU_EVENTOUT_PG4 |
| 92 | PG7 | I/O | I2C3_SCL | MCU_I2C3_SCL |
| 93 | PG8 | I/O | I2C3_SDA | MCU_I2C3_SDA |
| 94 | VSS | Power | | |
| 95 | VDDIO2 | Power | | |
| 96 | PC6 | I/O | TIM3_CH1 | MCU_OUT_PWM_LED_R |
| 98 | PC8 * | I/O | GPIO_Input | MCU_IN_AUDIO_DAC_nRD Y |
| 99 | PC9 * | I/O | GPIO_Output | MCU_OUT_AUDIO_DAC_S EL |
| 100 | PA8 | I/O | RCC_MCO | MCU_MCO |
| 101 | PA9 | I/O | USB_OTG_FS_VBUS | MCU_IN_VBUS |
| 103 | PA11 | I/O | USB_OTG_FS_DM | PA_USB_N |
| 104 | PA12 | I/O | USB_OTG_FS_DP | PA_USB_P |
| 105 | PA13 (JTMS/SWDIO) | I/O | SYS_JTMS-SWDIO | MCU_INOUT_SWDIO |
| 106 | VDDUSB | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 (JTCK/SWCLK) | I/O | SYS_JTCK-SWCLK | MCU_IN_SWCLK |
| 111 | PC10 | I/O | SPI3_SCK | MCU_SPI3_SCK |
| 112 | PC11 | I/O | SPI3_MISO | MCU_SPI3_MISO |
| 113 | PC12 | I/O | SPI3_MOSI | MCU_SPI3_MOSI |
| 114 | PD0 * | I/O | GPIO_Input | MCU_IN_AUDIO_ADC_MD AT1 |
| 115 | PD1 * | I/O | GPIO_Input | MCU_IN_AUDIO_ADC_MD AT0 |
| 116 | PD2 * | I/O | GPIO_Input | MCU_IN_AUDIO_ADC_nDR |
| 117 | PD3 * | I/O | GPIO_Output | MCU_OUT_AUDIO_ADC_n RESET |
| 118 | PD4 | I/O | USART2_RTS | UART2_RTS_OUT |
| 119 | PD5 * | I/O | GPIO_Output | MCU_OUT_AUDIO_ADC_S EL |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 122 | PD6 | I/O | USART2_RX | UART2_RX_IN |
| 123 | PD7 | I/O | GPIO_EXTI7 | MCU_IN_EXTI7_INTR_SI53 38 |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|------------------|
| 124 | PG9 | I/O | USART1_TX | UART1_TX_OUT |
| 125 | PG10 | I/O | USART1_RX | UART1_RX_IN |
| 126 | PG11 | I/O | USART1_CTS | UART1_CTS_IN |
| 127 | PG12 | I/O | USART1_RTS | UART1_RTS_OUT |
| 128 | PG13 | I/O | I2C1_SDA | MCU_I2C1_SDA |
| 129 | PG14 | I/O | I2C1_SCL | MCU_I2C1_SCL |
| 130 | VSS | Power | | |
| 131 | VDDIO2 | Power | | |
| 132 | PB3 (JTDO/TRACESWO) * | I/O | GPIO_Input | MCU_INOUT_PN00 |
| 134 | PB5 * | I/O | GPIO_Input | MCU_INOUT_PN01 |
| 135 | PB6 * | I/O | GPIO_Input | MCU_INOUT_PN02 |
| 136 | PB7 * | I/O | GPIO_Input | MCU_INOUT_PN03 |
| 140 | PE0 * | I/O | EVENTOUT | MCU_EVENTOUT_PE0 |
| 142 | VDD12 | Power | | |
| 143 | VSS | Power | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN8: IN8 Single-ended

mode: Temperature Sensor Channel

mode: Vbat Channel

mode: Vrefint Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling **Enable ***

Oversampling Right Shift No bit shift for oversampling

Oversampling Ratio **Oversampling ratio 16x ***

Regular Oversampling Mode Oversampling Continued Mode

Triggered Regular Oversampling Single trigger for all oversampled conversions

Number Of Conversion **4 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel Vrefint ***

Sampling Time **12.5 Cycles ***

Offset Number No offset

Rank **2 ***

Channel Channel 8

Sampling Time **12.5 Cycles ***

| | |
|-------------------------------------|-------------------------------------|
| Offset Number | No offset |
| <u>Rank</u> | 3 * |
| Channel | Channel Vbat * |
| Sampling Time | 247.5 Cycles * |
| Offset Number | No offset |
| <u>Rank</u> | 4 * |
| Channel | Channel Temperature Sensor * |
| Sampling Time | 12.5 Cycles * |
| Offset Number | No offset |
| ADC_Injected_ConversionMode: | |
| Enable Injected Conversions | Disable |
| Analog Watchdog 1: | |
| Enable Analog WatchDog1 Mode | false |
| Analog Watchdog 2: | |
| Enable Analog WatchDog2 Mode | false |
| Analog Watchdog 3: | |
| Enable Analog WatchDog3 Mode | false |

5.2. ADC3

IN6: IN6 Single-ended

5.2.1. Parameter Settings:

ADC_Settings:

| | |
|-------------------------------|--------------------------------------|
| Clock Prescaler | Asynchronous clock mode divided by 1 |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Enabled * |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | Overrun data preserved |
| Low Power Auto Wait | Disabled |

ADC_Regular_ConversionMode:

| | |
|-----------------------------|---------------------------------|
| Enable Regular Conversions | Enable |
| Enable Regular Oversampling | Enable * |
| Oversampling Right Shift | No bit shift for oversampling |
| Oversampling Ratio | Oversampling ratio 16x * |

| | |
|------------------------------------|--|
| Regular Oversampling Mode | Oversampling Continued Mode |
| Triggered Regular Oversampling | Single trigger for all oversampled conversions |
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| <u>Rank</u> | 1 |
| Channel | Channel 6 |
| Sampling Time | 2.5 Cycles |
| Offset Number | No offset |

ADC_Injected_ConversionMode:

| | |
|-----------------------------|---------|
| Enable Injected Conversions | Disable |
|-----------------------------|---------|

Analog Watchdog 1:

| | |
|------------------------------|-------|
| Enable Analog WatchDog1 Mode | false |
|------------------------------|-------|

Analog Watchdog 2:

| | |
|------------------------------|-------|
| Enable Analog WatchDog2 Mode | false |
|------------------------------|-------|

Analog Watchdog 3:

| | |
|------------------------------|-------|
| Enable Analog WatchDog3 Mode | false |
|------------------------------|-------|

5.3. CRC

mode: Activated

5.3.1. Parameter Settings:

Basic Parameters:

| | |
|--------------------------|--------|
| Default Polynomial State | Enable |
| Default Init Value State | Enable |

Advanced Parameters:

| | |
|----------------------------|---------|
| Input Data Inversion Mode | None |
| Output Data Inversion Mode | Disable |
| Input Data Format | Bytes |

5.4. DFSDM1

mode: Parallel input

mode: Parallel input

5.4.1. Filter 0:

regular channel selection:

regular channel selection

| | |
|-------------------------------------|------------------------|
| Continuous Mode | Channel 0 * |
| Trigger to start regular conversion | One Shot Mode * |
| Fast Mode | Software trigger |
| Dma Mode | Disable |
| | Disable |
| injected channel selection: | |
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |
| Filter parameters: | |
| Sinc Order | FastSinc filter type |
| Fosr | 1 |
| losr | 1 |

5.4.2. Filter 1:

| | |
|-------------------------------------|------------------------|
| regular channel selection: | Channel 1 * |
| regular channel selection | One Shot Mode * |
| Continuous Mode | Software trigger |
| Trigger to start regular conversion | Disable |
| Fast Mode | Disable |
| Dma Mode | Disable |
| injected channel selection: | |
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |
| Filter parameters: | |
| Sinc Order | FastSinc filter type |
| Fosr | 1 |
| losr | 1 |

5.4.3. Filter 2:

regular channel selection:

regular channel selection - None -

injected channel selection:

| | |
|------------------------------|---------|
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |

5.4.4. Filter 3:

regular channel selection:

regular channel selection - None -

injected channel selection:

| | |
|------------------------------|---------|
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |

5.4.5. Channel 0:

Channel 0 Parallel input selection:

Multiplexer_Internal_CH0 Data are taken from internal register

Channel 0 parameters:

| | |
|-----------------|----------------------------|
| Data Packing | Standard data packing mode |
| Right Bit Shift | 0x00 * |

5.4.6. Channel 1:

Channel 1 Parallel input selection:

Multiplexer_Internal_CH1 Data are taken from internal register

Channel 1 parameters:

Data Packing Standard data packing mode
Right Bit Shift **0x00 ***

5.5. I2C1

I2C: I2C

5.5.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 120 * |
| Fall Time (ns) | 25 * |
| Coefficient of Digital Filter | 3 * |
| Analog Filter | Enabled |
| Timing | 0x00500822 * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.6. I2C2

I2C: I2C

5.6.1. Parameter Settings:

Timing configuration:

| | |
|---------------------------|--------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 120 * |
| Fall Time (ns) | 25 * |

| | |
|-------------------------------|---------------------|
| Coefficient of Digital Filter | 3 * |
| Analog Filter | Enabled |
| Timing | 0x00500822 * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.7. I2C3

I2C: I2C

5.7.1. Parameter Settings:

Timing configuration:

| | |
|-------------------------------|---------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | 0x00200C28 * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.8. I2C4

I2C: I2C

5.8.1. Parameter Settings:

Timing configuration:

| | |
|---------------------------|--------------------|
| I2C Speed Mode | Fast Mode * |
| I2C Speed Frequency (KHz) | 400 |

| | |
|-------------------------------|---------------------|
| Rise Time (ns) | 120 * |
| Fall Time (ns) | 25 * |
| Coefficient of Digital Filter | 3 * |
| Analog Filter | Enabled |
| Timing | 0x00500822 * |

Slave Features:

| | |
|----------------------------------|----------|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

5.9. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Master Clock Output

CRS SYNC: CRS SYNC Source USB

5.9.1. Parameter Settings:

System Parameters:

| | |
|-------------------|--------------------|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled * |
| Data Cache | Enabled |
| Flash Latency(WS) | 3 WS (4 CPU cycle) |

RCC Parameters:

| | |
|--------------------------------|-------------------------------------|
| HSI Calibration Value | 64 |
| MSI Calibration Value | 0 |
| MSI Auto Calibration | Disabled |
| HSE Startup Timeout Value (ms) | 100 |
| LSE Startup Timeout Value (ms) | 5000 |
| LSE Drive Capability | LSE oscillator low drive capability |

Power Parameters:

| | |
|-------------------------------|--|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 2 * |
|-------------------------------|--|

CRS Parameters:

| | |
|-------------------------------|-----------------------|
| CRS Synchro Divider | 1 |
| CRS Synchro Polarity | Active on rising edge |
| CRS Synchro Reload Value Type | Automatic |

| | |
|----------------------------|------|
| CRS Synchro frequency (Hz) | 1000 |
| Error limit Value | 34 |
| HSI48 Calibration Value | 32 |

5.10. RNG

mode: Activated

5.11. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

Alarm B: Internal Alarm B

WakeUp: Internal WakeUp

5.11.1. Parameter Settings:

General:

| | |
|-------------------------------|---------------|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 31 * |
| Synchronous Predivider value | 1023 * |

Calendar Time:

| | |
|--|-----------------------------|
| Data Format | Binary data format * |
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Day Light Saving: value of hour adjustment | Daylightsaving None |
| Store Operation | Storeoperation Reset |

Calendar Date:

| | |
|----------|-------------|
| Week Day | Monday |
| Month | January |
| Date | 1 |
| Year | 18 * |

Alarm A:

| | |
|--------------------------|-----------------|
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Enable * |

| | |
|--------------------------|---------------------------------|
| Alarm Mask Hours | Enable * |
| Alarm Mask Minutes | Enable * |
| Alarm Mask Seconds | Enable * |
| Alarm Sub Second Mask | All Alarm SS fields are masked. |
| Alarm Date Week Day Sel | Date |
| Alarm Date | 1 |
| Alarm B: | |
| Hours | 0 |
| Minutes | 0 |
| Seconds | 0 |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Disable |
| Alarm Mask Hours | Disable |
| Alarm Mask Minutes | Disable |
| Alarm Mask Seconds | Disable |
| Alarm Sub Second Mask | All Alarm SS fields are masked. |
| Alarm Date Week Day Sel | Date |
| Alarm Date | 1 |
| Wake UP: | |
| Wake Up Clock | RTCCLK / 16 |
| Wake Up Counter | 0 |

5.12. SAI1

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

5.12.1. Parameter Settings:

SAI B:

| | |
|------------------------------------|--------------------|
| Basic Parameters | |
| Audio Mode | Master Transmit |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |
| Protocol Parameters | |
| Protocol | I2S Standard |
| Data Size | 16 Bits |
| Number of Slots (only Even Values) | 2 |
| Clock Parameters | |
| Master Clock Divider | Enabled |

| | |
|--------------------------|--------------------|
| Audio Frequency | 192 KHz |
| Real Audio Frequency | 93.75 KHz * |
| Error between Selected | -51.17 % * |
| Advanced Parameters | |
| Fifo Threshold | Half Full * |
| Output Drive | Disabled |
| Synchronization External | Disabled |

5.13. SAI2

Mode: Asynchronous Slave

mode: I2S/PCM Protocol

5.13.1. Parameter Settings:

SAI A:

Basic Parameters

| | |
|-------------------------|--------------------|
| Audio Mode | Slave Receive |
| Output Mode | Stereo |
| Companding Mode | No companding mode |
| SAI SD Line Output Mode | Driven |

Protocol Parameters

| | |
|------------------------------------|--------------|
| Protocol | I2S Standard |
| Data Size | 16 Bits |
| Number of Slots (only Even Values) | 2 |

Clock Parameters

Advanced Parameters

| | |
|--------------------------|---------------------------|
| Fifo Threshold | One Quarter Full * |
| Output Drive | Disabled |
| Synchronization External | Disabled |

5.14. SPI1

Mode: Full-Duplex Master

5.14.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------------|
| Frame Format | Motorola |
| Data Size | 8 Bits * |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | 12.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|-------------------|
| CRC Calculation | Disabled |
| NSSP Mode | Disabled * |
| NSS Signal Type | Software |

5.15. SPI3

Mode: Full-Duplex Master

5.15.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------------|
| Frame Format | Motorola |
| Data Size | 8 Bits * |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|-----------------------|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | 12.0 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|-------------------|
| CRC Calculation | Disabled |
| NSSP Mode | Disabled * |
| NSS Signal Type | Software |

5.16. SYS

Debug: Serial Wire

mode: System Wake-Up 2

Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)

VREFBUF Mode: Internal voltage reference

Timebase Source: TIM2

5.16.1. Parameter Settings:

Programmable_Voltage_Detector_Settings:

| | |
|---------------------|----------------------------------|
| PVD detection Level | PWR PVD LEVEL 5 (2.8 V) * |
| PWR PVD Mode | basic mode is used |

Voltage_Reference_Buffer_Settings:

| | |
|----------------------------------|-------------------------|
| Trimming Mode | User Trimming * |
| Trimming Value | 5 * |
| Internal Voltage reference scale | SCALE 0: around 2.048 V |

5.17. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

5.17.1. Parameter Settings:

Counter Settings:

| | |
|---|-----------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 65535 * |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Enable * |

Trigger Output (TRGO) Parameters:

| | |
|------------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

Clear Input:

| | |
|--------------------|---------|
| Clear Input Source | Disable |
|--------------------|---------|

PWM Generation Channel 1:

| | |
|-----------------------|------------|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

PWM Generation Channel 2:

| | |
|-----------------------|------------|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |

CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1
Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

5.18. TIM5

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

5.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 32 bits value) **1599999999 ***
Internal Clock Division (CKD) No Division
auto-reload preload **Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division
Input Filter (4 bits value) 0

Input Capture Channel 2:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division
Input Filter (4 bits value) 0

Input Capture Channel 3:

Polarity Selection Rising Edge
IC Selection Direct
Prescaler Division Ratio No division

| | |
|---------------------------------|-------------|
| Input Filter (4 bits value) | 0 |
| Input Capture Channel 4: | |
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

5.19. TIM16

mode: Activated

Channel1: Input Capture direct mode from Remap

5.19.1. Parameter Settings:

Counter Settings:

| | |
|---|-----------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 65535 * |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Enable * |

Input Capture Channel 1:

| | |
|----------------------------------|--|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |
| TI1 remap capabilities for TIM16 | TIM16 Channel 1 is connected to LSE * |

5.20. TIM17

mode: Activated

Channel1: Input Capture direct mode from Remap

5.20.1. Parameter Settings:

Counter Settings:

| | |
|---|----------------|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 65535 * |
| Internal Clock Division (CKD) | No Division |

| | |
|---|--|
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Enable * |
| Input Capture Channel 1: | |
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |
| TI1 remap capabilities for TIM17 | TIM17 Channel 1 is connected to MSI internal clock |

5.21. USART1

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.21.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 38400 * |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.22. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.22.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 38400 * |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.23. USART3

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.23.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 38400 * |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |

| | |
|-------------------------------|---------|
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

5.24. USB_OTG_FS

Mode: Device_Only

Activate_VBUS: VBUS sensing

5.24.1. Parameter Settings:

| | |
|-------------------------------------|---------------------|
| Speed | Full Speed 12MBit/s |
| Endpoint 0 Max Packet size | 64 Bytes |
| Enable internal IP DMA | Disabled |
| Low power | Disabled |
| Battery charging | Disabled * |
| Link Power Management | Enabled * |
| Use dedicated end point 1 interrupt | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Enabled * |

5.25. FREERTOS

mode: Enabled

5.25.1. Config parameters:

Versions:

| | |
|--------------------|-------|
| FreeRTOS version | 9.0.0 |
| CMSIS-RTOS version | 1.02 |

Kernel settings:

| | |
|--------------------|-----------------|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 32 * |
| USE_16_BIT_TICKS | Disabled |

| | |
|-----------------------------------|-------------------|
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Enabled * |
| QUEUE_REGISTRY_SIZE | 64 * |
| USE_APPLICATION_TASK_TAG | Enabled * |
| ENABLE_BACKWARD_COMPATIBILITY | Disabled * |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |

Memory management settings:

| | |
|--------------------------|-----------------|
| Memory Allocation | Dynamic |
| TOTAL_HEAP_SIZE | 0x8000 * |
| Memory Management scheme | heap_4 |

Hook function related definitions:

| | |
|------------------------------|------------------|
| USE_IDLE_HOOK | Enabled * |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Enabled * |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Option1 * |

Run time and task stats gathering related definitions:

| | |
|--------------------------------|------------------|
| GENERATE_RUN_TIME_STATS | Enabled * |
| USE_TRACE_FACILITY | Enabled * |
| USE_STATS_FORMATTING_FUNCTIONS | Enabled * |

Co-routine related definitions:

| | |
|---------------------------|----------|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

Software timer definitions:

| | |
|------------------------|-------------|
| USE_TIMERS | Enabled |
| TIMER_TASK_PRIORITY | 2 |
| TIMER_QUEUE_LENGTH | 16 * |
| TIMER_TASK_STACK_DEPTH | 256 |

Interrupt nesting behaviour configuration:

| | |
|--|----|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

5.25.2. Include parameters:

Include definitions:

| | |
|-----------------------------|-------------------|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Disabled * |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Enabled * |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Enabled * |
| xSemaphoreGetMutexHolder | Enabled * |
| pcTaskGetTaskName | Enabled * |
| uxTaskGetStackHighWaterMark | Enabled * |
| xTaskGetCurrentTaskHandle | Enabled * |
| eTaskGetState | Enabled * |
| xEventGroupSetBitFromISR | Enabled * |
| xTimerPendFunctionCall | Enabled * |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Enabled * |

5.26. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.26.1. Parameter Settings:

Basic Parameters:

| | |
|--|------------------------------------|
| USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces) | 1 |
| USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration) | 1 |
| USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors) | 512 |
| USBD_SUPPORT_USER_STRING (Enable user string descriptor) | Disabled |
| USBD_SELF_POWERED (Enabled self power) | Disabled * |
| USBD_DEBUG_LEVEL (USBD Debug Level) | 0: No debug message |
| USBD_LPM_ENABLED (Link Power Management) | 1: Link Power Management supported |

Class Parameters:

| | |
|------------------------|------|
| USB CDC Rx Buffer Size | 2048 |
| USB CDC Tx Buffer Size | 2048 |

5.26.2. Device Descriptor:

Device Descriptor:

| | |
|---|------------------------------|
| VID (Vendor Identifier) | 0x483 |
| LANGID_STRING (Language Identifier) | English(United States) |
| MANUFACTURER_STRING (Manufacturer Identifier) | HSMA HFT Laborities * |

Device Descriptor FS:

| | |
|---|--------------------------|
| PID (Product Identifier) | 0x5740 |
| PRODUCT_STRING (Product Identifier) | HFT-Core_Module * |
| SERIALNUMBER_STRING (Serial number) | 000000000001 * |
| CONFIGURATION_STRING (Configuration Identifier) | CDC Config |
| INTERFACE_STRING (Interface Identifier) | CDC Interface |

* User modified value

6. System Configuration

6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|------|-----------------------|---------------|--------------------------------|-----------------------------|-----------------|---------------------|
| ADC1 | PA3 | ADC1_IN8 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | MCU_VSOL_ADC1 |
| ADC3 | PF3 | ADC3_IN6 | Analog mode for ADC conversion | No pull-up and no pull-down | n/a | ADC3_IN6_20MHZ_PULL |
| I2C1 | PG13 | I2C1_SDA | Alternate Function Open Drain | Pull-up | Low | MCU_I2C1_SDA |
| | PG14 | I2C1_SCL | Alternate Function Open Drain | Pull-up | Low | MCU_I2C1_SCL |
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | Pull-up | Low | MCU_I2C2_SDA |
| | PF1 | I2C2_SCL | Alternate Function Open Drain | Pull-up | Low | MCU_I2C2_SCL |
| I2C3 | PG7 | I2C3_SCL | Alternate Function Open Drain | Pull-up | Low | MCU_I2C3_SCL |
| | PG8 | I2C3_SDA | Alternate Function Open Drain | Pull-up | Low | MCU_I2C3_SDA |
| I2C4 | PF14 | I2C4_SCL | Alternate Function Open Drain | Pull-up | Low | MCU_I2C4_SCL |
| | PD13 | I2C4_SDA | Alternate Function Open Drain | Pull-up | Low | MCU_I2C4_SDA |
| RCC | PC14-OSC32_IN (PC14) | RCC_OSC32_IN | n/a | n/a | n/a | MCU_OSC32_IN |
| | PC15-OSC32_OUT (PC15) | RCC_OSC32_OUT | n/a | n/a | n/a | MCU_OSC32_OUT |
| | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | MCU_HSE |
| | PA8 | RCC_MCO | Alternate Function Push Pull | Pull-down * | Low | MCU_MCO |
| SAI1 | PE3 | SAI1_SD_B | Alternate Function Push Pull | Pull-down * | Medium * | I2S1B_SD_OUT |
| | PE8 | SAI1_SCK_B | Alternate Function Push Pull | Pull-down * | Medium * | I2S1B_SCK_OUT |
| | PE9 | SAI1_FS_B | Alternate Function Push Pull | Pull-down * | Medium * | I2S1B_FS_OUT |
| | PE10 | SAI1_MCLK_B | Alternate Function Push Pull | Pull-down * | Medium * | I2S1B_MCLK_OUT |
| SAI2 | PB13 | SAI2_SCK_A | Alternate Function Push Pull | Pull-down * | Medium * | I2S2A_SCK_IN |
| | PD11 | SAI2_SD_A | Alternate Function Push Pull | Pull-down * | Medium * | I2S2A_SD_IN |
| | PD12 | SAI2_FS_A | Alternate Function Push Pull | Pull-down * | Medium * | I2S2A_FS_IN |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|--------|----------------------|----------------|------------------------------|------------------------|--------------------|--------------------|
| SPI1 | PE13 | SPI1_SCK | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI1_SCK |
| | PE14 | SPI1_MISO | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI1_MISO |
| | PE15 | SPI1_MOSI | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI1_MOSI |
| SPI3 | PC10 | SPI3_SCK | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI3_SCK |
| | PC11 | SPI3_MISO | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI3_MISO |
| | PC12 | SPI3_MOSI | Alternate Function Push Pull | Pull-down * | Very High * | MCU_SPI3_MOSI |
| SYS | PC13 | SYS_WKUP2 | n/a | n/a | n/a | MCU_IN_WAKEUP |
| | VREF+ | VREFBUF_OUT | n/a | n/a | n/a | MCU_OUT_VREF+ |
| | PA13 (JTMS/SWDIO) | SYS_JTMS-SWDIO | n/a | n/a | n/a | MCU_INOUT_SWDIO |
| | PA14 (JTCK/SWCLK) | SYS_JTCK-SWCLK | n/a | n/a | n/a | MCU_IN_SWCLK |
| TIM3 | PA7 | TIM3_CH2 | Alternate Function Push Pull | Pull-down * | Low | MCU_OUT_PWM_LED_G |
| | PB0 | TIM3_CH3 | Alternate Function Push Pull | Pull-down * | Low | MCU_OUT_PWM_LED_B |
| | PC6 | TIM3_CH1 | Alternate Function Push Pull | Pull-down * | Low | MCU_OUT_PWM_LED_R |
| TIM5 | PF6 | TIM5_CH1 | Alternate Function Push Pull | Pull-down * | Low | MCU_IN_TIMCAP_N |
| | PF7 | TIM5_CH2 | Alternate Function Push Pull | Pull-down * | Low | MCU_IN_TIMCAP_W |
| | PF8 | TIM5_CH3 | Alternate Function Push Pull | Pull-down * | Low | MCU_IN_TIMCAP_S |
| | PF9 | TIM5_CH4 | Alternate Function Push Pull | Pull-down * | Low | MCU_IN_TIMCAP_VSOL |
| USART1 | PG9 | USART1_TX | Alternate Function Push Pull | Pull-up * | Low | UART1_TX_OUT |
| | PG10 | USART1_RX | Alternate Function Push Pull | Pull-up * | Low | UART1_RX_IN |
| | PG11 | USART1_CTS | Alternate Function Push Pull | Pull-down * | Low | UART1_CTS_IN |
| | PG12 | USART1_RTS | Alternate Function Push Pull | Pull-down * | Low | UART1_RTS_OUT |
| USART2 | PA0 | USART2_CTS | Alternate Function Push Pull | Pull-down * | Low | UART2_CTS_IN |
| | PA2 | USART2_TX | Alternate Function Push Pull | Pull-up * | Low | UART2_TX_OUT |
| | PD4 | USART2_RTS | Alternate Function Push Pull | Pull-down * | Low | UART2_RTS_OUT |
| | PD6 | USART2_RX | Alternate Function Push Pull | Pull-up * | Low | UART2_RX_IN |
| USART3 | PA6 | USART3_CTS | Alternate Function Push Pull | Pull-down * | Low | UART3_CTS_IN |
| | PC4 | USART3_TX | Alternate Function Push Pull | Pull-up * | Low | UART3_TX_OUT |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|------------|------|-----------------|--|------------------------|--------------------|-------------------------------|
| | PC5 | USART3_RX | Alternate Function Push Pull | Pull-up * | Low | UART3_RX_IN |
| | PB1 | USART3_RTS | Alternate Function Push Pull | Pull-down * | Low | UART3_RTS_OUT |
| | | | | | | |
| USB_OTG_FS | PA9 | USB_OTG_FS_VBUS | Input mode | Pull-down * | n/a | MCU_IN_VBUS |
| | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | Pull-down * | High * | PA_USB_N |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | Pull-down * | High * | PA_USB_P |
| GPIO | PE2 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PW03 |
| | PE4 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PW02 |
| | PE5 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PW01 |
| | PF2 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PW00 |
| | PF10 | EVENTOUT | Alternate Function Push Pull | Pull-down * | Low | MCU_EVENTOUT_PF10 |
| | PC0 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_VDD12_EN |
| | PC1 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_HICUR_EN |
| | PC2 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_VUSB_EN |
| | PC3 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_20MHZ_EN |
| | PF12 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_LCD_nRST |
| | PG0 | GPIO_Output | Output Push Pull | Pull-up * | Low | MCU_OUT_SX_HF_LF_CTRL |
| | PG1 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_IN_AX_GPIO1 |
| | PE7 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_IN_AX_IRQ |
| | PE11 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | MCU_OUT_AX_SEL |
| | PE12 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | MCU_OUT_SX_SEL |
| | PB10 | GPIO_Input | Input mode | Pull-up * | n/a | MCU_IN_RE_I |
| | PB12 | GPIO_Input | Input mode | Pull-up * | n/a | MCU_IN_RE_Q |
| | PB14 | GPIO_Input | Input mode | Pull-up * | n/a | MCU_IN_RE_PB |
| | PD8 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_SX_nRESET |
| | PD9 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PS00 |
| | PD10 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PS01 |
| | PD14 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PS02 |
| | PD15 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PS03 |
| | PG2 | GPIO_EXTI2 | External Interrupt Mode with Rising edge trigger detection | Pull-down * | n/a | MCU_IN_EXTI2_SX_DIO0_TXRXDONE |
| | PG3 | GPIO_EXTI3 | External Interrupt Mode with | | n/a | MCU_IN_EXTI3_SX_DIO1 |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|----|------------------------|-------------|--|------------------------|--------------------|--------------------------|
| | | | Rising edge trigger detection | Pull-down * | | _RXTO |
| | PG4 | EVENTOUT | Alternate Function Push Pull | Pull-down * | Low | MCU_EVENTOUT_PG4 |
| | PC8 | GPIO_Input | Input mode | Pull-up * | n/a | MCU_IN_AUDIO_DAC_nRDY |
| | PC9 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | MCU_OUT_AUDIO_DAC_SEL |
| | PD0 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_IN_AUDIO_ADC_MDAT1 |
| | PD1 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_IN_AUDIO_ADC_MDAT0 |
| | PD2 | GPIO_Input | Input mode | Pull-up * | n/a | MCU_IN_AUDIO_ADC_nDR |
| | PD3 | GPIO_Output | Output Push Pull | Pull-down * | Low | MCU_OUT_AUDIO_ADC_nRESET |
| | PD5 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | MCU_OUT_AUDIO_ADC_SEL |
| | PD7 | GPIO_EXTI7 | External Interrupt Mode with Rising edge trigger detection | Pull-down * | n/a | MCU_IN_EXTI7_INTR_SI5338 |
| | PB3 (JTDO/TRACESWO) | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PN00 |
| | PB5 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PN01 |
| | PB6 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PN02 |
| | PB7 | GPIO_Input | Input mode | Pull-down * | n/a | MCU_INOUT_PN03 |
| | PE0 | EVENTOUT | Alternate Function Push Pull | Pull-down * | Low | MCU_EVENTOUT_PE0 |

6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|-------------|---------------|----------------------|----------|
| SAI2_A | DMA1_Channel6 | Peripheral To Memory | Low |
| SAI1_B | DMA2_Channel7 | Memory To Peripheral | Low |
| ADC1 | DMA1_Channel1 | Peripheral To Memory | Low |
| ADC3 | DMA1_Channel3 | Peripheral To Memory | Low |
| SPI3_RX | DMA2_Channel1 | Peripheral To Memory | Low |
| SPI3_TX | DMA2_Channel2 | Memory To Peripheral | Low |
| SPI1_RX | DMA1_Channel2 | Peripheral To Memory | Low |
| SPI1_TX | DMA2_Channel4 | Memory To Peripheral | Low |

SAI2_A: DMA1_Channel6 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Word
Memory Data Width: Word

SAI1_B: DMA2_Channel7 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Word
Memory Data Width: Word

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

ADC3: DMA1_Channel3 DMA request Settings:

Mode: Normal

Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

SPI3_RX: DMA2_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

SPI3_TX: DMA2_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

SPI1_RX: DMA1_Channel2 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

SPI1_TX: DMA2_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|--|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Prefetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| EXTI line2 interrupt | true | 5 | 0 |
| EXTI line3 interrupt | true | 5 | 0 |
| DMA1 channel1 global interrupt | true | 5 | 0 |
| DMA1 channel2 global interrupt | true | 5 | 0 |
| DMA1 channel3 global interrupt | true | 5 | 0 |
| DMA1 channel6 global interrupt | true | 5 | 0 |
| ADC1 and ADC2 interrupts | true | 5 | 0 |
| TIM2 global interrupt | true | 0 | 0 |
| I2C1 event interrupt | true | 5 | 0 |
| I2C1 error interrupt | true | 5 | 0 |
| I2C2 event interrupt | true | 5 | 0 |
| I2C2 error interrupt | true | 5 | 0 |
| RTC alarm interrupt through EXTI line 18 | true | 5 | 0 |
| ADC3 global interrupt | true | 5 | 0 |
| DMA2 channel1 global interrupt | true | 5 | 0 |
| DMA2 channel2 global interrupt | true | 5 | 0 |
| DMA2 channel4 global interrupt | true | 5 | 0 |
| USB OTG FS global interrupt | true | 5 | 0 |
| DMA2 channel7 global interrupt | true | 5 | 0 |
| I2C3 event interrupt | true | 5 | 0 |
| I2C3 error interrupt | true | 5 | 0 |
| SAI1 global interrupt | true | 5 | 0 |
| SAI2 global interrupt | true | 5 | 0 |
| HASH and RNG global interrupts | true | 5 | 0 |
| I2C4 event interrupt | true | 5 | 0 |
| I2C4 error interrupt | true | 5 | 0 |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38 | unused | | |
| RTC wake-up interrupt through EXTI line 20 | unused | | |
| Flash global interrupt | unused | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|--|--------|----------------------|-------------|
| RCC global interrupt | | unused | |
| EXTI line[9:5] interrupts | | unused | |
| TIM1 update interrupt and TIM16 global interrupt | | unused | |
| TIM1 trigger and commutation interrupts and TIM17 global interrupt | | unused | |
| TIM3 global interrupt | | unused | |
| SPI1 global interrupt | | unused | |
| USART1 global interrupt | | unused | |
| USART2 global interrupt | | unused | |
| USART3 global interrupt | | unused | |
| TIM5 global interrupt | | unused | |
| SPI3 global interrupt | | unused | |
| DFSDM1 filter0 global interrupt | | unused | |
| DFSDM1 filter1 global interrupt | | unused | |
| FPU global interrupt | | unused | |
| CRS global interrupt | | unused | |

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|-----------|----------------|
| Series | STM32L4 |
| Line | STM32L4x6 |
| MCU | STM32L496ZGTxP |
| Datasheet | 029173_Rev2 |

7.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.6 |

7.3. SMPS Selection

| | |
|------------|------------|
| SMPS | SMPS1_User |
| Vin | 3.3 V |
| Vout | 1.2 V |
| OffCurrent | 250.0 nA |
| QCurrent | 500.0 nA |
| Efficiency | 85 % |

7.4. Sequence

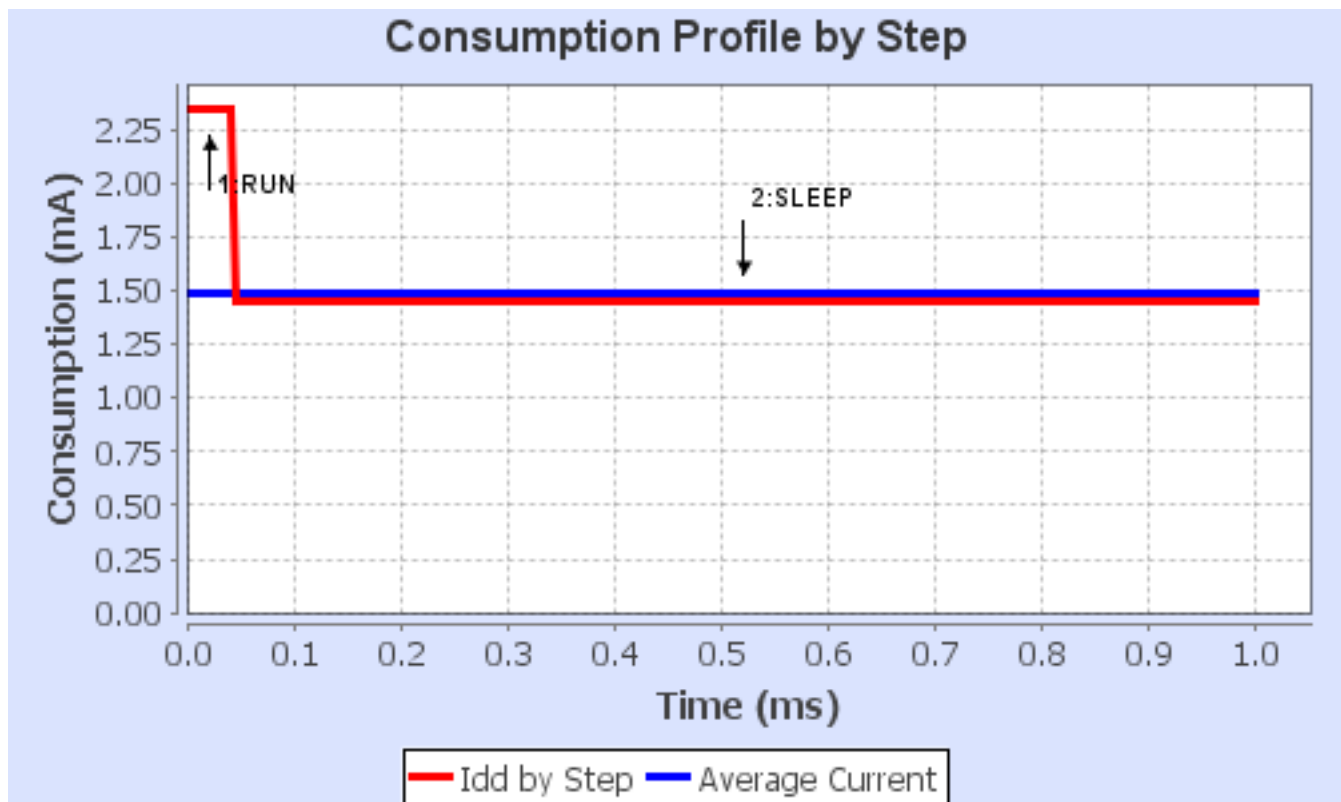
| | | |
|-------------|-------|-------|
| Step | Step1 | Step2 |
|-------------|-------|-------|

| | | |
|-------------------------------|--|--|
| Mode | RUN | SLEEP |
| SMPS | CONNECTED | CONNECTED |
| Vdd | 3.6 | 3.6 |
| Voltage Source | Battery | Battery |
| Range | Range2-Medium | Range2-Medium |
| Fetch Type | FLASH | FLASH |
| Clock Configuration | HSE BYP ART Flash-ON | HSE BYP ART Flash-ON |
| Clock Source Frequency | 24 MHz | 24 MHz |
| CPU Frequency | 24 MHz | 24 MHz |
| Peripherals | ADC1:fs_10_ksp ADC3:fs_10_ksp CRC DFSDM1 GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 I2C2 I2C3 I2C4 RNG RTC SAI1 SAI2 SPI1 SPI3 SYS- VREFBUF/COMP1:COMP_H igh_Speed- Square_VREFBUF_OFF TIM3 TIM5 TIM16 TIM17 USART1 USART2 USART3 USB_OTG_FS | ADC1:fs_10_ksp ADC3:fs_10_ksp CRC DFSDM1 GPIOA GPIOB GPIOC GPIOD GPIOE GPIOF GPIOG GPIOH I2C1 I2C2 I2C3 I2C4 RNG RTC SAI1 SAI2 SPI1 SPI3 SYS- VREFBUF/COMP1:COMP_H igh_Speed- Square_VREFBUF_OFF TIM3 TIM5 TIM16 TIM17 USART1 USART2 USART3 USB_OTG_FS |
| Additional Cons. | 0 mA | 0 mA |
| Average Current | 2.34 mA | 1.45 mA |
| Duration | 0.04 ms | 0.96 ms |
| DMIPS | 0.0 | 0.0 |
| Ta Max | 104.73 | 104.83 |
| Category | Measurements | Measurements |

7.5. RESULTS

| | | | |
|---------------|------|-----------------|------------|
| Sequence Time | 1 ms | Average Current | 1.49 mA |
| Battery Life | 0 | Average DMIPS | 30.0 DMIPS |

7.6. Chart



8. Software Project

8.1. Project Settings

| Name | Value |
|-----------------------------------|---|
| Project Name | HFT-Core-Module_TrueSTUDIO |
| Project Folder | Z:\nfs_ds_nfs\git\HFT-Core-Module__SW\SW\HFT-Core-Module_TrueSTUDIO |
| Toolchain / IDE | TrueSTUDIO |
| Firmware Package Name and Version | STM32Cube FW_L4 V1.12.0 |

8.2. Code Generation Settings

| Name | Value |
|---|---------------------------------------|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | Yes |

9. Software Pack Report