

RedPitaya

FPGA memory map

Written by	Revision Description	Version	Date
Matej Oblak	Initial	0.1	08/11/13
Matej Oblak	Release1 update	0.2	16/12/13
Matej Oblak	ASG - added burst mode ASG - buffer read pointer readout		Dec. 2014 Jan. 2015
Matej Oblak	AXI master documented		Feb. 2015
Iztok Jeras	Added debounce delay register		Mar. 2015
Iztok Jeras	Added digital loopback, pre trigger status		Apr. 2015
Iztok Jeras	Removed XADC registers GPIO[0] is now R/W		Avg. 2015
Ulrich Habel	RadioBox added	0.3	Dec. 2015
Ulrich Habel	RadioBox receiver path added	0.31	Jan. 2016

Table of Contents

About Document.....3

FPGA Memory Map.....3

Red Pitaya Modules.....3

 Housekeeping.....4

 Oscilloscope.....5

 Arbitrary Signal Generator (ASG).....7

 PID Controller.....9

 Analog Mixed Signals (AMS).....11

 Daisy Chain.....13

 Power Test.....14

About Document

Red Pitaya HDL design has multiple functions, which are configured by registers. It also uses memory locations to store capture data and generate output signals. All of this are described in this document. Memory location is written in a way that is seen by SW.

FPGA Memory Map

The table describes address space partitioning implemented on FPGA via AXI GP0 interface. All registers have offsets aligned to 4 bytes and are 32-bit wide. Granularity is 32-bit, meaning that minimum transfer size is 4 bytes. The organization is little-endian .

The memory block is divided into 8 parts. Each part is occupied by individual IP core. Address space of individual application is described in the subsection below. The size of each IP core address space is 4MByte.

For additional informations and better understanding check other documents (schematics, specifications...).

	Start	End	Module Name
CS[0]	0x40000000	0x400FFFFFF	Housekeeping
CS[1]	0x40100000	0x401FFFFFF	Oscilloscope
CS[2]	0x40200000	0x402FFFFFF	Arbitrary signal generator (ASG)
CS[3]	0x40300000	0x403FFFFFF	PID controller
CS[4]	0x40400000	0x404FFFFFF	Analog mixed signals (AMS)
CS[5]	0x40500000	0x405FFFFFF	(not assigned)
CS[6]	0x40600000	0x406FFFFFF	RadioBox (RB)
CS[7]	0x40700000	0x407FFFFFF	(not assigned)

Red Pitaya Modules

Here are described submodules used in Red Pitaya FPGA logic.

Housekeeping

offset	description	bits	R/W
0x0	ID		
	<i>Reserved</i>	<i>31:4</i>	<i>R</i>
	Design ID 0-prototype0, 1-release1	3:0	R
0x4	DNA part1		
	DNA[31:0]	31:0	R
0x8	DNA part2		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	DNA[56:32]	24:0	R
0xC	Digital Loopback		
	<i>Reserved</i>	<i>31:1</i>	<i>R</i>
	digital_loop	0	R/W
0x10	Expansion connector direction P		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	Direction for P lines 1-out 0-in	7:0	R/W
0x14	Expansion connector direction N		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	Direction for N lines 1-out 0-in	7:0	R/W
0x18	Expansion connector output P		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	P pins output	7:0	R/W
0x1C	Expansion connector output N		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	N pins output	7:0	R/W
0x20	Expansion connector input P		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	P pins input	7:0	R
0x24	Expansion connector input N		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>
	N pins input	7:0	R
0x30	LED control		
	<i>Reserved</i>	<i>31:8</i>	<i>R</i>

	LEDs 7-0	7:0	R/W
--	----------	-----	-----

Oscilloscope

offset	description	bits	R/W
0x0	Configuration		
	<i>Reserved</i>	31:3	R
	Trigger status before acquire ends (0 – pre trigger, 1 – post trigger)	2	R
	Reset write state machine	1	W
	Start writing data into memory (ARM trigger).	0	W
0x4	Trigger source		
	Selects trigger source for data capture. When trigger delay is ended value goes to 0.		
	<i>Reserved</i>	31:4	R
	Trigger source: 1-trig immediately 2-ch A threshold positive edge 3-ch A threshold negative edge 4-ch B threshold positive edge 5-ch B threshold negative edge 6-external trigger positive edge - DIO0_P pin 7-external trigger negative edge 8-arbitrary wave generator application positive edge 9-arbitrary wave generator application negative edge	3:0	R/W
0x8	Ch A threshold		
	<i>Reserved</i>	31:14	R
	Ch A threshold, makes trigger when ADC value cross this value	13:0	R/W
0xC	Ch B threshold		
	<i>Reserved</i>	31:14	R
	Ch B threshold, makes trigger when ADC value cross this value	13:0	R/W
0x10	Delay after trigger		
	Number of decimated data after trigger written into memory	31:0	R/W
0x14	Data decimation		
	Decimate input data, uses data average		
	<i>Reserved</i>	31:17	R
	Data decimation, supports only this values: 1,8, 64,1024,8192,65536. If other value is written data will NOT be correct.	16:0	R/W
0x18	Write pointer - current		
	<i>Reserved</i>	31:14	R
	Current write pointer	13:0	R
0x1C	Write pointer - trigger		
	<i>Reserved</i>	31:14	R

	Write pointer at time when trigger arrived	13:0	R
0x20	Ch A hysteresis		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	Ch A threshold hysteresis. Value must be outside to enable trigger again.	13:0	R/W
0x24	Ch B hysteresis		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	Ch B threshold hysteresis. Value must be outside to enable trigger again.	13:0	R/W
0x28	Other		
	<i>Reserved</i>	<i>31:1</i>	<i>R</i>
	Enable signal average at decimation	0	R/W
0x2C	PreTrigger Counter		
	This unsigned counter holds the number of samples captured between the start of acquire and trigger. The value does not overflow, instead it stops incrementing at 0xffffffff.	31:0	R
0x30	CH A Equalization filter		
	<i>Reserved</i>	<i>31:18</i>	<i>R</i>
	AA Coefficient	17:0	R/W
0x34	CH A Equalization filter		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	BB Coefficient	24:0	R/W
0x38	CH A Equalization filter		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	KK Coefficient	24:0	R/W
0x3C	CH A Equalization filter		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	PP Coefficient	24:0	R/W
0x40	CH B Equalization filter		
	<i>Reserved</i>	<i>31:18</i>	<i>R</i>
	AA Coefficient	17:0	R/W
0x44	CH B Equalization filter		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	BB Coefficient	24:0	R/W
0x48	CH B Equalization filter		
	<i>Reserved</i>	<i>31:25</i>	<i>R</i>
	KK Coefficient	24:0	R/W
0x4C	CH B Equalization filter		

	<i>Reserved</i>	31:25	R
	PP Coefficient	24:0	R/W
0x50	CH A AXI lower address		
	Starting writing address	31:0	R/W
0x54	CH A AXI upper address		
	Address where it jumps to lower	31:0	R/W
0x58	CH A AXI delay after trigger		
	Number of decimated data after trigger written into memory	31:0	R/W
0x5C	CH A AXI enable master		
	<i>Reserved</i>	31:1	R
	Enable AXI master	0	R/W
0x60	CH A AXI write pointer - trigger		
	Write pointer at time when trigger arrived	31:0	R
0x64	CH A AXI write pointer - current		
	Current write pointer	31:0	R
0x70	CH B AXI lower address		
	Starting writing address	31:0	R/W
0x74	CH B AXI upper address		
	Address where it jumps to lower	31:0	R/W
0x78	CH B AXI delay after trigger		
	Number of decimated data after trigger written into memory	31:0	R/W
0x7C	CH B AXI enable master		
	<i>Reserved</i>	31:1	R
	Enable AXI master	0	R/W
0x80	CH B AXI write pointer - trigger		
	Write pointer at time when trigger arrived	31:0	R
0x84	CH B AXI write pointer - current		
	Current write pointer	31:0	R
0x90	Trigger debouncer time		
	Number of ADC clock periods trigger is disabled after activation reset value is decimal 62500 or equivalent to 0.5ms	19:0	R/W
0xA0	Accumulator data sequence length		
	<i>Reserved</i>	31:14	R
0xA4	Accumulator data offset corection ChA		
	<i>Reserved</i>	31:14	R
	signed offset value	13:0	R/W
0xA8	Accumulator data offset corection ChB		
	<i>Reserved</i>	31:14	R

	signed offset value	13:0	R/W
0x10000 to 0x1FFFC	Memory data (16k samples)		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	Captured data for ch A	15:0	R
0x20000 to 0x2FFFC	Memory data (16k samples)		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	Captured data for ch B	15:0	R

Arbitrary Signal Generator (ASG)

offset	description	bits	R/W
0x0	Configuration		
	<i>Reserved</i>	31:25	R
	ch B external gated repetitions	24	R/W
	ch B set output to 0	23	R/W
	ch B SM reset	22	R/W
	<i>Reserved</i>	21	R/W
	ch B SM wrap pointer (if disabled starts at address 0)	20	R/W
	ch B trigger selector: (don't change when SM is active) 1-trig immediately 2-external trigger positive edge - DIO0_P pin 3-external trigger negative edge	19:16	R/W
	<i>Reserved</i>	15:9	R
	ch A external gated bursts	8	R/W
	ch A set output to 0	7	R/W
	ch A SM reset	6	R/W
	<i>Reserved</i>	5	R/W
	ch A SM wrap pointer (if disabled starts at address 0)	4	R/W
	ch A trigger selector: (don't change when SM is active) 1-trig immediately 2-external trigger positive edge - DIO0_P pin 3-external trigger negative edge	3:0	R/W
0x4	Ch A amplitude scale and offset		
	out = (data*scale)/0x2000 + offset		
	<i>Reserved</i>	31:30	R
	Amplitude offset	29:16	R/W
	<i>Reserved</i>	15:14	R
	Amplitude scale. 0x2000 == multiply by 1. Unsigned	13:0	R/W
0x8	Ch A counter wrap		
	<i>Reserved</i>	31:30	R
	Value where counter wraps around. Depends on SM wrap setting. If it is 1 new value is get by wrap, if value is 0 counter goes to offset value. 16 bits for decimals.	29:0	R/W
0xC	Ch A start offset		
	<i>Reserved</i>	31:30	R
	Counter start offset. Start offset when trigger arrives. 16 bits for decimals.	29:0	R/W

0x10	Ch A counter step		
	<i>Reserved</i>	31:30	R
	Counter step. 16 bits for decimals.	29:0	R/W
0x14	Ch A buffer current read pointer		
	<i>Reserved</i>	31:16	R
	Read pointer	15:2	R/W
	<i>Reserved</i>	1:0	R
0x18	Ch A number of read cycles in one burst		
	<i>Reserved</i>	31:16	R
	Number of repeats of table readout. 0=infinite	15:0	R/W
0x1C	Ch A number of burst repetitions		
	<i>Reserved</i>	31:16	R
	Number of repetitions. 0=disabled	15:0	R/W
0x20	Ch A delay between burst repetitions		
	Delay between repetitions. Granularity=1us	31:0	R/W
0x24	Ch B amplitude scale and offset		
	out = (data*scale)/0x2000 + offset		
	<i>Reserved</i>	31:30	R
	Amplitude offset	29:16	R/W
	<i>Reserved</i>	15:14	R
	Amplitude scale. 0x2000 == multiply by 1. Unsigned	13:0	R/W
0x28	Ch B counter wrap		
	<i>Reserved</i>	31:30	R
	Value where counter wraps around. Depends on SM wrap setting. If it is 1 new value is get by wrap, if value is 0 counter goes to offset value. 16 bits for decimals.	29:0	R/W
0x2C	Ch B start offset		
	<i>Reserved</i>	31:30	R
	Counter start offset. Start offset when trigger arrives. 16 bits for decimals.	29:0	R/W
0x30	Ch B counter step		
	<i>Reserved</i>	31:30	R
	Counter step. 16 bits for decimals.	29:0	R/W
0x34	Ch B buffer current read pointer		
	<i>Reserved</i>	31:16	R
	Read pointer	15:2	R/W
	<i>Reserved</i>	1:0	R
0x38	Ch B number of read cycles in one burst		

	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	Number of repeats of table readout. 0=infinite	15:0	R/W
0x3C	Ch B number of burst repetitions		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	Number of repetitions. 0=disabled	15:0	R/W
0x40	Ch B delay between burst repetitions		
	Delay between repetitions. Granularity=1us	31:0	R/W
0x10000 to 0x1FFFC	Ch A memory data (16k samples)		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	ch A data	13:0	R/W
0x20000 to 0x2FFFC	Ch B memory data (16k samples)		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	ch B data	13:0	R/W

PID Controller

offset	description	bits	R/W
0x0	Configuration		
	<i>Reserved</i>	<i>31:4</i>	<i>R</i>
	PID22 integrator reset	3	R/W
	PID21 integrator reset	2	R/W
	PID12 integrator reset	1	R/W
	PID11 integrator reset	0	R/W
0x10	PID11 set point		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID11 set point	13:0	R/W
0x14	PID11 proportional coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID11 Kp	13:0	R/W
0x18	PID11 integral coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID11 Ki	13:0	R/W
0x1C	PID11 derivative coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID11 Kd	13:0	R/W
0x20	PID12 set point		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID12 set point	13:0	R/W
0x24	PID12 proportional coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID12 Kp	13:0	R/W
0x28	PID12 integral coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID12 Ki	13:0	R/W
0x2C	PID12 derivative coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID12 Kd	13:0	R/W
0x30	PID21 set point		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID21 set point	13:0	R/W

0x34	PID21 proportional coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID21 Kp	13:0	R/W
0x38	PID21 integral coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID21 Ki	13:0	R/W
0x3C	PID21 derivative coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID21 Kd	13:0	R/W
0x40	PID22 set point		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID22 set point	13:0	R/W
0x44	PID22 proportional coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID22 Kp	13:0	R/W
0x48	PID22 integral coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID22 Ki	13:0	R/W
0x4C	PID22 derivative coefficient		
	<i>Reserved</i>	<i>31:14</i>	<i>R</i>
	PID22 Kd	13:0	R/W

Analog Mixed Signals (AMS)

offset	description	bits	R/W
0x0	XADC AIF0		
	<i>Reserved</i>	<i>31:12</i>	<i>R</i>
	AIF0 value	11:0	R
0x4	XADC AIF1		
	<i>Reserved</i>	<i>31:12</i>	<i>R</i>
	AIF1 value	11:0	R
0x8	XADC AIF2		
	<i>Reserved</i>	<i>31:12</i>	<i>R</i>
	AIF2 value	11:0	R
0xC	XADC AIF3		
	<i>Reserved</i>	<i>31:12</i>	<i>R</i>
	AIF3 value	11:0	R
0x10	XADC AIF4		
	<i>Reserved</i>	<i>31:12</i>	<i>R</i>
	AIF4 value (5V power supply)	11:0	R
0x20	PWM DAC0		
	<i>Reserved</i>	<i>31:24</i>	<i>R</i>
	PWM value (100% == 156)	23:16	R/W
	Bit select for PWM repetition which have value PWM+1	15:0	R/W
0x24	PWM DAC1		
	<i>Reserved</i>	<i>31:24</i>	<i>R</i>
	PWM value (100% == 156)	23:16	R/W
	Bit select for PWM repetition which have value PWM+1	15:0	R/W
0x28	PWM DAC2		
	<i>Reserved</i>	<i>31:24</i>	<i>R</i>
	PWM value (100% == 156)	23:16	R/W
	Bit select for PWM repetition which have value PWM+1	15:0	R/W
0x2C	PWM DAC3		
	<i>Reserved</i>	<i>31:24</i>	<i>R</i>
	PWM value (100% == 156)	23:16	R/W
	Bit select for PWM repetition which have value PWM+1	15:0	R/W

RadioBox (RB)

offset	description	bits	R/W
0x000	RB_CTRL Control register		
	<i>Reserved</i>	<i>31:29</i>	<i>R</i>
	<i>RX_MOD_OSC RESYNC</i> '1' stops incrementing the accumulating phase register. That holds the oscillator just there, where it is. With '0' the RX_MOD_OSC resumes operation.	28	R/W
	<i>RX_AFC ENABLE</i> '1' enables RX_CAR_OSC automatic frequency correction. '0' disabled the AFC feature.	27	R/W
	<i>Reserved</i>	<i>26:21</i>	<i>R</i>
	<i>RX_CAR_OSC RESYNC</i> '1' stops incrementing the accumulating phase register. That holds the oscillator just there, where it is. With '0' the RX_CAR_OSC resumes operation.	20	R/W
	<i>Reserved</i>	<i>19</i>	<i>R</i>
	<i>RX_MOD_OSC RESET</i> '1' resets the RX_MOD_OSC (modulation oscillator) to its initial state, like the accumulating phase register.	18	R/W
	<i>RX_CAR_OSC RESET</i> '1' resets the RX_CAR_OSC (carrier oscillator) to its initial state, like the accumulating phase register.	17	R/W
	<i>Reserved</i>	<i>16</i>	<i>R</i>
	<i>TX_RF_AMP_Q_EN</i> '1' enables the TX_CAR_QMIX Q path for the SSB modulation.	15	R/W
	<i>TX_MOD_OSC OFS SRC STREAM</i> '1' places input MUXer for TX_MOD_OSC DDS offset input to the second streamed input pipe. '0' places MUXer to registers "TX_MOD_OSC OFS HI" and "TX_MOD_OSC OFS LO".	14	R/W
	<i>TX_MOD_OSC INC SRC STREAM</i> '1' places input MUXer for TX_MOD_OSC DDS increment input to the second streamed input pipe. '0' places MUXer to registers "TX_MOD_OSC INC HI" and "TX_MOD_OSC INC LO".	13	R/W
	<i>TX_MOD_OSC RESYNC</i> '1' stops incrementing the accumulating phase register. That holds the oscillator just there, where it is. With '0' the TX_CAR_OSC resumes operation.	12	R/W
	<i>Reserved</i>	<i>11:7</i>	<i>R</i>

0x000 cont'd	<i>TX_CAR_OSC_OFS_SRC_STREAM</i> '1' places input MUXer for TX_CAR_OSC DDS offset input to the first streamed input pipe. '0' places MUXer to registers "TX_CAR_OSC_OFS_HI" and "TX_CAR_OSC_OFS_LO".	6	R/W
	<i>TX_CAR_OSC_INC_SRC_STREAM</i> '1' places input MUXer for TX_CAR_OSC DDS increment input to the first streamed input pipe. '0' places MUXer to registers "TX_CAR_OSC_INC_HI" and "TX_CAR_OSC_INC_LO".	5	R/W
	<i>TX_CAR_OSC_RESYNC</i> '1' stops incrementing the accumulating phase register. That holds the oscillator just there, where it is. With '0' the TX_CAR_OSC resumes operation.	4	R/W
	<i>Reserved</i>	3	R
	<i>TX_MOD_OSC_RESET</i> '1' resets the TX_MOD_OSC (modulation oscillator) to its initial state like the accumulating phase register.	2	R/W
	<i>TX_CAR_OSC_RESET</i> '1' resets the TX_CAR_OSC (carrier oscillator) to its initial state like the accumulating phase register.	1	R/W
	<i>RB_ENABLE</i> '1' enables the RadioBox sub-module. DDS-Oscillators, multipliers, LED handling are turned on. The DAC and LEDs are connected to this sub-module when enabled.	0	R/W
0x004	RB_STATUS Status register		
	<i>STAT_LED7_ON</i> '1' RadioBox LED7 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	31	R/W
	<i>STAT_LED6_ON</i> '1' RadioBox LED6 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	30	R/W
	<i>STAT_LED5_ON</i> '1' RadioBox LED5 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	29	R/W
	<i>STAT_LED4_ON</i> '1' RadioBox LED4 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	28	R/W
	<i>STAT_LED3_ON</i> '1' RadioBox LED3 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	27	R/W
	<i>STAT_LED2_ON</i> '1' RadioBox LED2 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	26	R/W

0x004 cont'd	<i>STAT_LED1_ON</i> '1' RadioBox LED1 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	25	R/W
	<i>STAT_LED0_ON</i> '1' RadioBox LED0 driver that is shown at the diodes, when STAT_LEDS_EN is '1'.	24	R/W
	<i>Reserved</i>	<i>23:18</i>	<i>R</i>
	<i>STAT_RX_MOD_OSC_VALID</i> '1' RX_MOD_OSC output equals zero. This state is based on the output of the DDS oscillator itself.	17	R/W
	<i>STAT_RX_MOD_OSC_ZERO</i> '1' RX_MOD_OSC output is valid. After turning this sub-module active it needs some clocks going into valid state.	16	R/W
	<i>Reserved</i>	<i>15:14</i>	<i>R</i>
	<i>STAT_RX_CAR_OSC_VALID</i> '1' RX_CAR_OSC output equals zero. This state is based on the output of the DDS oscillator itself.	13	R/W
	<i>STAT_RX_CAR_OSC_ZERO</i> '1' RX_CAR_OSC output is valid. After turning this sub-module active it needs some clocks going into valid state.	12	R/W
	<i>Reserved</i>	<i>11:10</i>	<i>R</i>
	<i>STAT_TX_MOD_OSC_VALID</i> '1' TX_MOD_OSC output is valid. After turning this sub-module active it needs some clocks going into valid state.	9	R/W
	<i>STAT_TX_MOD_OSC_ZERO</i> '1' TX_MOD_OSC output equals zero. This state is based on the output of the DDS oscillator itself.	8	R/W
	<i>Reserved</i>	<i>7:6</i>	<i>R</i>
	<i>STAT_TX_CAR_OSC_VALID</i> '1' TX_CAR_OSC output is valid. After turning this sub-module active it needs some clocks going into valid state.	5	R/W
	<i>STAT_TX_CAR_OSC_ZERO</i> '1' TX_CAR_OSC output equals zero. This state is based on the output of the DDS oscillator itself.	4	R/W
	<i>Reserved</i>	<i>3</i>	<i>R</i>
	<i>STAT_LEDS_EN</i> '1' RadioBox LEDs state is shown at the diodes, any other output register is discarded.	2	R/W
	<i>STAT_RESET</i> '1' reset of the RadioBox sub-system is active (clears phase accumulators).	1	R/W

0x004 cont'd	<i>STAT_CLK_EN</i> '1' clock of the RadioBox sub-system is enabled (power up sub-module).	0	R/W
0x008	RB_ICR Interrupt control register (reserved)		
	<i>Reserved</i>	<i>31:0</i>	<i>R</i>
0x00C	RB_ICR Interrupt status register (reserved)		
	<i>Reserved</i>	<i>31:0</i>	<i>R</i>
0x010	RB_DMA_CTRL DMA control register (reserved)		
	<i>Reserved</i>	<i>31:0</i>	<i>R</i>
0x01C	RB_SRC_CON_PNT output connection matrix for RB_LEDs, RFOUT1 and RFOUT2		
	<i>Reserved</i>	<i>31:30</i>	<i>R</i>
	RF Output 2 (SMA) source position: 0-silence 1-silence 4-ADC selector input 5-TX modulation amplifier input 6-TX modulation amplifier output 8-TX_MOD_OSC I output at stage 1 9-TX_MOD_OSC Q output at stage 1 10-TX_MOD_QMIX I output at stage 1 11-TX_MOD_QMIX Q output at stage 1 12-TX_MOD_QMIX I output at stage 2 13-TX_MOD_QMIX Q output at stage 2 14-TX_MOD_QMIX I output at stage 3 15-TX_MOD_QMIX Q output at stage 3 16-TX_MOD_CIC I output 17-TX_MOD_CIC Q output 18-TX_MOD_FIR I output 19-TX_MOD_FIR Q output 20-TX_CAR_CIC I output 41.664 MHz 21-TX_CAR_CIC Q output 41.664 MHz 24-TX_CAR_OSC I output 25-TX_CAR_OSC Q output 26-TX_CAR_QMIX I output 27-TX_CAR_QMIX Q output 28-TX_AMP_RF output (** RF output **)	29:24	R/W

	<p>32-RX_CAR_OSC I output 33-RX_CAR_OSC Q output 34-RX_CAR_QMIX I output 35-RX_CAR_QMIX Q output 36-RX_CAR_CIC1 I output 37-RX_CAR_CIC1 Q output 38-RX_CAR_CIC2 I output 39-RX_CAR_CIC2 Q output</p> <p>40-RX_MOD_FIR1 I output 41-RX_MOD_FIR1 Q output 42-RX_MOD_OSC I output 43-RX_MOD_OSC Q output 44-RX_MOD_HLD I output 45-RX_MOD_HLD Q output 46-RX_MOD_QMIX I output 47-RX_MOD_QMIX Q output 48-RX_MOD_FIR2 I output 49-RX_MOD_FIR2 Q output 50-RX_MOD_CIC2 I output 51-RX_MOD_CIC2 Q output</p> <p>56-RX_MOD_ADD output (** Audio output **)</p> <p>58-RX_AFC_FIR I output 59-RX_AFC_FIR Q output 60-RX_AFC_CORDIC magnitude output 61-RX_AFC_CORDIC phase output</p> <p>63-test vector as signal, look for current assignments within the <i>red_pitaya_radiobox.sv</i> file</p>		
0x01C cont'd	<i>Reserved</i>	23:22	R
	<p>RF Output 1 (SMA) source position: 0-silence 1-silence</p> <p>4-ADC selector input 5-TX modulation amplifier input 6-TX modulation amplifier output</p> <p>8-TX_MOD_OSC I output at stage 1 9-TX_MOD_OSC Q output at stage 1 10-TX_MOD_QMIX I output at stage 1 11-TX_MOD_QMIX Q output at stage 1 12-TX_MOD_QMIX I output at stage 2 13-TX_MOD_QMIX Q output at stage 2 14-TX_MOD_QMIX I output at stage 3 15-TX_MOD_QMIX Q output at stage 3</p>	21:16	R/W

	16-TX_MOD_CIC I output 17-TX_MOD_CIC Q output 18-TX_MOD_FIR I output 19-TX_MOD_FIR Q output 20-TX_CAR_CIC I output 41.664 MHz 21-TX_CAR_CIC Q output 41.664 MHz 24-TX_CAR_OSC I output 25-TX_CAR_OSC Q output 26-TX_CAR_QMIX I output 27-TX_CAR_QMIX Q output 28-TX_AMP_RF output (** RF output **) 32-RX_CAR_OSC I output 33-RX_CAR_OSC Q output 34-RX_CAR_QMIX I output 35-RX_CAR_QMIX Q output 36-RX_CAR_CIC1 I output 37-RX_CAR_CIC1 Q output 38-RX_CAR_CIC2 I output 39-RX_CAR_CIC2 Q output 40-RX_MOD_FIR1 I output 41-RX_MOD_FIR1 Q output 42-RX_MOD_OSC I output 43-RX_MOD_OSC Q output 44-RX_MOD_HLD I output 45-RX_MOD_HLD Q output 46-RX_MOD_QMIX I output 47-RX_MOD_QMIX Q output 48-RX_MOD_FIR2 I output 49-RX_MOD_FIR2 Q output 50-RX_MOD_CIC2 I output 51-RX_MOD_CIC2 Q output 56-RX_MOD_ADD output (** Audio output **) 58-RX_AFC_FIR I output 59-RX_AFC_FIR Q output 60-RX_AFC_CORDIC magnitude output 61-RX_AFC_CORDIC phase output 63-test vector as signal, look for current assignments within the <i>red_pitaya_radiobox.sv</i> file		
0x01C cont'd	<i>Reserved</i>	15:6	R
	LEDs magnitude scope (logarithmic) source position: 0-RadioBox does not touch the LED state of the other sub-module(s) 1-all LEDs are driven off	5:0	R/W

<p>4-ADC selector input 5-TX modulation amplifier input 6-TX modulation amplifier output</p> <p>8-TX_MOD_OSC I output at stage 1 9-TX_MOD_OSC Q output at stage 1 10-TX_MOD_QMIX I output at stage 1 11-TX_MOD_QMIX Q output at stage 1 12-TX_MOD_QMIX I output at stage 2 13-TX_MOD_QMIX Q output at stage 2 14-TX_MOD_QMIX I output at stage 3 15-TX_MOD_QMIX Q output at stage 3</p> <p>16-TX_MOD_CIC I output 17-TX_MOD_CIC Q output 18-TX_MOD_FIR I output 19-TX_MOD_FIR Q output 20-TX_CAR_CIC I output 41.664 MHz 21-TX_CAR_CIC Q output 41.664 MHz</p> <p>24-TX_CAR_OSC I output 25-TX_CAR_OSC Q output 26-TX_CAR_QMIX I output 27-TX_CAR_QMIX Q output</p> <p>28-TX_AMP_RF output (** RF output **)</p> <p>32-RX_CAR_OSC I output 33-RX_CAR_OSC Q output 34-RX_CAR_QMIX I output 35-RX_CAR_QMIX Q output 36-RX_CAR_CIC1 I output 37-RX_CAR_CIC1 Q output 38-RX_CAR_CIC2 I output 39-RX_CAR_CIC2 Q output</p> <p>40-RX_MOD_FIR1 I output 41-RX_MOD_FIR1 Q output 42-RX_MOD_OSC I output 43-RX_MOD_OSC Q output 44-RX_MOD_HLD I output 45-RX_MOD_HLD Q output 46-RX_MOD_QMIX I output 47-RX_MOD_QMIX Q output 48-RX_MOD_FIR2 I output 49-RX_MOD_FIR2 Q output 50-RX_MOD_CIC2 I output 51-RX_MOD_CIC2 Q output</p> <p>56-RX_MOD_ADD output (** Audio output **)</p>		
---	--	--

	58-RX_AFC_FIR I output 59-RX_AFC_FIR Q output 60-RX_AFC_CORDIC magnitude output 61-RX_AFC_CORDIC phase output 63-test vector as signal, look for current assignments within the <i>red_pitaya_radiobox.sv</i> file		
0x020	RB_TX_CAR_OSC_INC_LO DDS TX_CAR_OSC, phase increment register @ 125 MHz		
	LSB of TX_CAR_OSC phase increment register	31:0	R/W
0x024	RB_TX_CAR_OSC_INC_HI DDS TX_CAR_OSC, phase increment register @ 125 MHz		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	MSB of TX_CAR_OSC phase increment register	15:0	R/W
0x028	RB_TX_CAR_OSC_OFS_LO DDS TX_CAR_OSC, phase offset register @ 125 MHz		
	LSB of TX_CAR_OSC phase offset register	31:0	R/W
0x02C	RB_TX_CAR_OSC_OFS_HI DDS TX_CAR_OSC, phase offset register @ 125 MHz		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	MSB of TX_CAR_OSC phase offset register	15:0	R/W
0x030	RB_TX_AMP_RF_GAIN TX AMP RF gain register		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	SIGNED 16 bit – TX amplifier RF gain setting	15:0	R/W
0x038	RB_TX_AMP_RF_OFS TX AMP RF offset register		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	SIGNED 16 bit – TX Amplifier RF offset value	15:0	R/W
0x040	RB_TX_MOD_OSC_INC_LO DDS TX_MOD_OSC, phase increment register		
	LSB of TX_MOD_OSC phase increment register	31:0	R/W
0x044	RB_TX_MOD_OSC_INC_HI DDS TX_MOD_OSC, phase increment register		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	MSB of TX_MOD_OSC phase increment register	15:0	R/W
0x048	RB_TX_MOD_OSC_OFS_LO DDS TX_MOD_OSC, phase offset register		
	LSB of TX_MOD_OSC phase offset register	31:0	R/W

0x04C	RB_TX_MOD_OSC_OFS_HI DDS TX_MOD_OSC, phase offset register		
	<i>Reserved</i>	31:16	R
	MSB of TX_CAR_OSC phase offset register	15:0	R/W
0x050	RB_TX_MOD_QMIX_GAIN TX_MOD_QMIX gain setting (stage 2)		
	<i>Reserved</i>	31:16	R
	SIGNED 16 bit - TX_MOD_QMIX output amplitude	15:0	R/W
0x058	RB_TX_MOD_QMIX_OFS_LO TX_MOD_QMIX offset value (stage 3)		
	LSB of TX_MOD_QMIX offset value	15:0	R/W
0x05C	RB_TX_MOD_QMIX_OFS_HI TX_MOD_QMIX offset value (stage 3)		
	<i>Reserved</i>	31:16	R
	MSB of TX_MOD_QMIX offset value	15:0	R/W
0x060	RB_TX_MUXIN_SRC Source signal for the TX analog input MUXer		
	<i>Reserved</i>	31:6	R
	Source position: 0-no external signal used, TX_MOD_OSC used instead 3-Vp_Vn, mapped to: vin[4] 16-XADC CH#0, mapped to: AI1 17-XADC CH#1, mapped to: AI0 24-XADC CH#8, mapped to: AI2 25-XADC CH#9, mapped to: AI3 32-ADC0, mapped to: RF Input 1 33-ADC1, mapped to: RF Input 2	5:0	R/W
0x064	RB_TX_MUXIN_GAIN Source signal gain for TX_MUXIN output amplifier		
	<i>Reserved</i>	31:18	R
	input booster – realized as left shift value: (7 .. 0) gives amplification of: (128x .. 1x)	18:16	R/W
	SIGNED 16 bit - TX_MUXIN mixer amplitude	15:0	R/W
0x120	RB_RX_CAR_OSC_INC_LO DDS RX_CAR_OSC, phase increment register @ 125 MHz		
	LSB of RX_CAR_OSC phase increment register	31:0	R/W
0x124	RB_RX_CAR_OSC_INC_HI DDS RX_CAR_OSC, phase increment register @ 125 MHz		
	<i>Reserved</i>	31:16	R
	MSB of RX_CAR_OSC phase increment register	15:0	R/W
0x128	RB_RX_CAR_OSC_OFS_LO DDS RX_CAR_OSC, phase offset register @ 125 MHz		
	LSB of RX_CAR_OSC phase offset register	31:0	R/W

0x12C	RB_RX_CAR_OSC_OFS_HI DDS RX_CAR_OSC, phase offset register @ 125 MHz		
	<i>Reserved</i>	31:16	R
	MSB of TX_CAR_OSC phase offset register	15:0	R/W
0x130	RB_RX_MOD_ADD_GAIN RX_MOD_ADD decoder gain register		
	<i>Reserved</i>	31:16	R
	SIGNED 16 bit – RX MOD decoder gain setting	15:0	R/W
0x138	RB_RX_MOD_ADD_OFS RX_MOD_ADD decoder offset register		
	<i>Reserved</i>	31:16	R
	SIGNED 16 bit – RX MOD decoder offset value	15:0	R/W
0x140	RB_RX_MOD_OSC_INC_LO DDS RX_MOD_OSC, phase increment register @ 125 MHz		
	LSB of RX_MOD_OSC phase increment register	31:0	R/W
0x144	RB_RX_MOD_OSC_INC_HI DDS RX_MOD_OSC, phase increment register @ 125 MHz		
	<i>Reserved</i>	31:16	R
	MSB of RX_MOD_OSC phase increment register	15:0	R/W
0x148	RB_RX_MOD_OSC_OFS_LO DDS RX_MOD_OSC, phase offset register @ 125 MHz		
	LSB of RX_MOD_OSC phase offset register	31:0	R/W
0x14C	RB_RX_MOD_OSC_OFS_HI DDS RX_MOD_OSC, phase offset register @ 125 MHz		
	<i>Reserved</i>	31:16	R
	MSB of RX_MOD_OSC phase offset register	15:0	R/W
0x160	RB_RX_MUXIN_SRC RX_MUXIN audio signal input selector		
	<i>Reserved</i>	31:6	R
	Source position: 0-no external signal used 1-ADC0, mapped to: RF Input 1 2-ADC1, mapped to: RF Input 2	5:0	R/W
0x164	RB_RX_MUXIN_GAIN (not yet implemented) Audio signal source gain for RX_MUXIN input amplifier		
	<i>Reserved</i>	31:19	R
	input booster – realized as left shift value: (7 .. 0) gives amplification of: (128x .. 1x)	18:16	R/W
	SIGNED 16 bit - TX_MUXIN mixer amplitude	15:0	R/W

0x170	RB_RX_AFC_CORDIC_MAG AFC_CORDIC magnitude value register		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	SIGNED 16 bit - RX_AFC_CORDIC magnitude value	15:0	R/O
0x174	RB_RX_AFC_CORDIC_PHS AFC_CORDIC phase value register		
	<i>Reserved</i>	<i>31:16</i>	<i>R</i>
	SIGNED 16 bit - RX_AFC_CORDIC phase value	15:0	R/O