ROACH-2 DATASHEET

Introduction

ROACH (Reconfigurable Open Architecture Computing Hardware) was developed by the SKA SA as part of a CASPER (Centre for Astronomy Signal Processing and Electronic Research) collaboration to be used as a general purpose hardware platform for radio astronomy signal processing.
ROACH-2 is a high performance reconfigurable hardware board based on the Xilinx® Virtex-6 LX-T and SX-T ranges of platform FPGAs. An onboard AMCC PowerPC 440EPx provides system control and monitoring functionality. ROACH-2 makes provision for high speed ADC / DACs, DSP functions, memory bandwidth and high speed data transfer.

Key Features

- Xilinx Virtex-6 FPGA
- AMCC PowerPC 440EPx
- QDRII+ FPGA Memory
- DDR3 FPGA Memory
- 2 x high data rate LVDS interfaces
- 2 x Multi Gigabit Transceivers (MGT) mezzanine cards supporting up to 8 10Ge ports.
- 1Ge Control and Monitoring Interface
- Standard 1U ATX form factor
- Multipurpose test and debug USB port using an FTDI FT4232 chip.

Applications

- Radio Astronomy
    - Correlators
    - Beam-formers
    - Spectrometers
- DSP
    - FFT
    - Matrix transpose
    - Filter banks
- High Speed Data transfer
    - 10Ge Ethernet
    - Packetization

General Description

The primary component of ROACH-2 is a Xilinx Virtex 6 FPGA. The FPGA could either be a LX550T for logic-intensive applications or SX475T for DSP-intensive applications. A number of other devices, as listed in the "FPGA Device Options" in the specifications table, can be used with some loss in functionality. An independent PowerPC runs software used to control the board, program the FPGA, allow interfacing between the FPGA resources and external devices using 1Ge Ethernet, USB and RS232.

Four 36-bit QDRII+ SRAMs provide high-speed, medium-capacity memory. One DDR3 DIMM provides high-capacity memory for the FPGA. The PowerPC has independent DDR2 SDRAM to run control software.

The two Z-DOK+ connectors allow ADC, DAC and other interface cards to be attached to the FPGA. 32 of the FPGA's MGTs are available on two mezzanine card interfaces. This enables the user to configure ROACH-2 to provide a maximum of 8 x 10 Gb/s Ethernet connection over whichever physical protocol the mezzanine card supports. There is an additional 1Gb Ethernet accessible from the FPGA.

An FDTI FT4232 provides a test and debug interface via USB. All JTAG devices can be programmed and debugged from this interface. This device provides IIC and serial UART interfaces. System health data is provided by IIC monitoring devices.

A Block diagram of the system is shown in Figure 1 on page 5 and a specifications table is shown below.

Table 1: ROACH 2 Specifications

Specifications			
Product Name	ROACH 2		
FPGA Device Options	XC6VSX475T, XC6VLX550T, XC6VSX315T[1], XC6VLX365T[1], XC6VLX240T[1] Footprint - 1FFG1759C		
FPGA Resources	Logic Cells	476k	
	DSP Slices	2016	
	BRAM	38Mb	
FPGA Memory	4 x 36-bit QDRII +	72Mb 144Mb[2]	400MHz
	DDR3 (Registered DIMM)	Up to 16GB	400MHz
FPGA Network Interface	32 MGT (8 x 10Ge ports) accessible on mezzanine breakout connectors [1] 1 x 1Gb Ethernet (RJ45)		
FPGA Clocks Options	Onboard 100MHz System Clock ZDOK Clock inputs External SMA Clock input		
ADC/ DAC Interface	2 ports with 40 LVDS pairs (1.25Gb/s) Connect to Z-DOK+ connectors		
General Purpose I/O	12 FPGA GPIO 4 Power PC GPIOs		
On Board Processor	AMCC Power PC 440EPx	667MHz	
PowerPC Memory	DDR2 SDRAM	512 MB(4 x 1024Mb)	166MHz
	Boot loader Flash	128MB	
PowerPC External Memory Interface	External SD/MMC Flash Mass Storage (USB)		
Power PC Communication	1Gb Ethernet (RJ45) USB RS232 (on board header)		
Software	UBoot Linux with BORPH support BusyBox/GNU-Linux		
Debug	JTAG and Boundary Scan via USB using FTDI FT4232HL chip		
Power	Power Supply	Standard ATX	
	Power Consumption	80-100W (typ.)	125W (max)
Environmental	T.B.A.		
Physical	Board Dimensions	ATX motherboard (305x244mm)	
	Chassis Height	1U	
	Width	Compatible with 19'' rack	

1 Fitment of these devices will result in limited functionality (see Table 2 for details)
2 Refer to manufacturer's roadmap

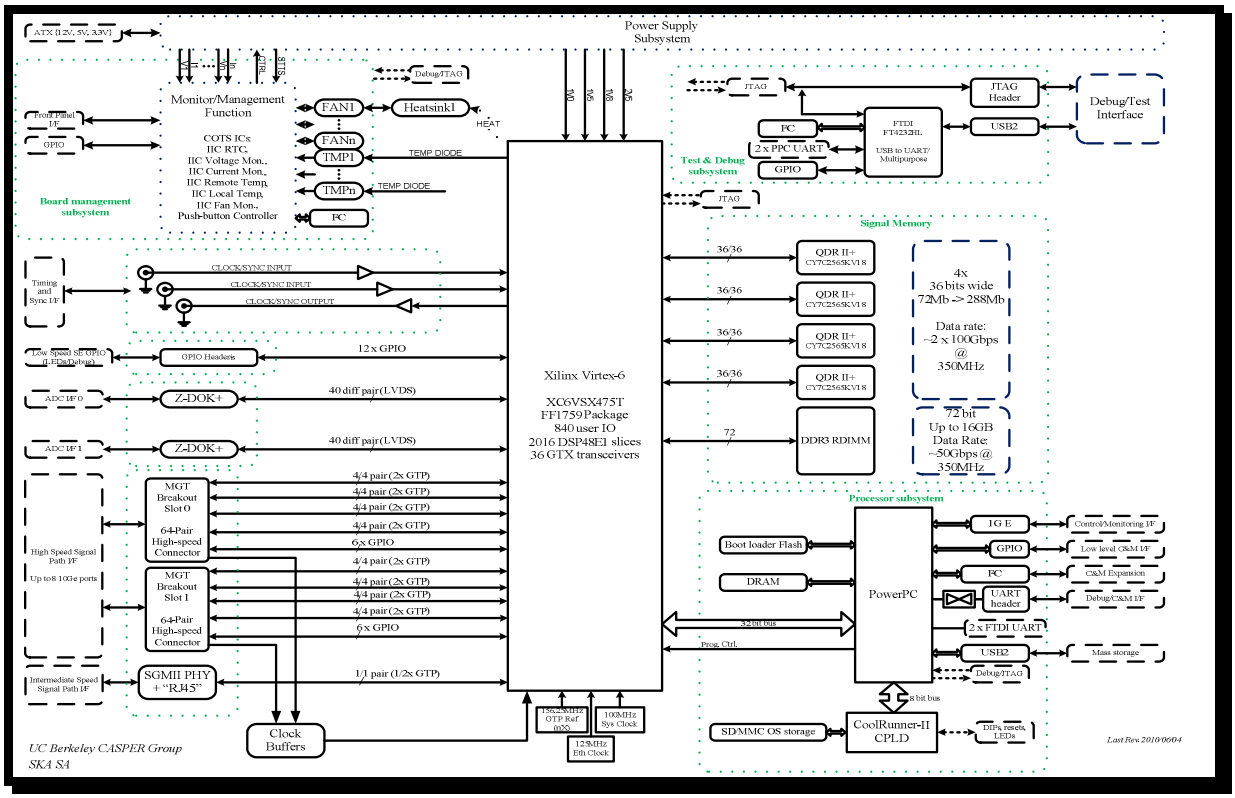

Figure1. ROACH-2 Block Diagram

Table 2: ROACH 2 Build Options

Build Options and Limitations							
Xilinx FPGA	FPGA Limitations		ROACH II Limitations				
	GTX	IO	Signal Path Interface			GPIO	QDRII+
			MGTs	10Ge	1Ge		
XC6VLX240T	24	720	24	6	0	8	2
XC6VLX365T	24	720	24	6	0	8	2
XC6VLX550T	36	840	36	8	1	12	4
XC6VSX315T	24	720	24	6	0	8	2
XC6VSX475T	36	840	36	8	1	12	4

ROACH 2 was designed for SX47ST and LXSS0T. LX240T, LX36ST and SX31ST devices can be used with the loss of:

- 1 Full QDR Memory, 18 Bits of a QDR
- 3 GTX tiles: lose 2 x 10Ge ports and SGMII port
- 4 x Single-ended GPIO