Design Principles of Batteryless Transponder for Vehicular DSRC at 5.8 GHz

Marco Passafiume, *Member, IEEE*, Giovanni Collodi, *Member, IEEE*, and Alessandro Cidronali, *Senior Member, IEEE*

***Abstract*—This article presents design principles for a totally batteryless and cost-effective wireless transponder, based on commercially-of-the-shelf (COTS) components. The transponder architecture is compliant with the physical layers of most common vehicular dedicated short range communications (DSRC) applications operating at 5.8 GHz. The paper is organized in two parts. We discuss firstly the design principles and system architecture, which includes both the energy harvesting and the back-scattering modes. The second part introduces a batteryless transponder prototype for vehicular DSRC, as result of the discussed design principles. In this part of the article reports a full set of experimental results, illustrating the consistency with the design principles, as well as the effective performance in terms of power consumption, energy efficiency and radio communication capabilities. In particular we report that at the distance of 1.05 m, a legacy road-side unit can establish both the down-link and up-link, with the latter requiring 37 s of charging time to enable 68 ms of data link at 8 Mbps.**

***Index Terms*—Energy harvesting, batteryless transponder, low power communications, wireless sensors, vehicular communications, DSRC.**

I. Introduction

THE NEW paradigms of mobile communications postulate the use of small mobile nodes widely spread through the physical environment, for both pervasive networking and distributed monitoring. Furthermore, upcoming technologies, such as 5G mobile communications, make use of network topologies based on a dense distribution of small routers (e.g., pico-cells), enabling connectivity for low-power devices; examples of these paradigms are the Internet-of-things (IoT) and the vehicular communications, [1]. It is a matter of fact that low-power network nodes have been developed for minimal power consumption, though they rely on a power source (or rather, a battery). This requirement is dictated by the need to minimize the battery capacity requirements and thus the cost, the size, the maintenance, and overall the risk related to their use in critical environments like a vehicle or in space applications [2]. Thus the new pervasive communications paradigms might trigger issues of environmental sustainability, [3], as well as high maintenance costs, [4], [5].

These issues could be partially solved by introducing wireless transponder technologies supported by energy harvesting techniques, and innovative devices with exceptionally low supply voltage requirements, [6], [7], [8]. Energy harvesting implementations in RFIDs (Radio Frequency Identifiers), [9], and WSN (Wireless Sensor Network) nodes, [10], [11], is a wide spread topic in the literature, much less, if not absent, in the vehicular communications area.

Henceforth we refer to the "on-demand" attribute, as the capability of a wireless node to provide a synchronous answer in response to an asynchronous query [5], [12].

Batteryless WSN nodes have been developed to establish either synchronous or asynchronous packet transmissions, whenever they have stored enough energy to do this, [11]. As a consequence, such nodes, missing the on-demand query capability, can not be considered neither a point-to-point network node nor a device suitable for vehicle communications.

To the best knowledge of the authors, in the literature only [13] and [14] pursue the goal of developing a full batteryless back-scattering wireless node able to perform on-demand communications. The results shown in [14] are very promising, reporting high energy conversion efficiencies with very low input power levels (≈ -14 dBm), in this case the operating frequency is 868 MHz, significantly lower than that considered in the present paper. In general these technologies, including also the so called wireless identification and sensing platforms (WISP), [15], need for customized integrated circuits (IC) and thus cannot be compared straightforwardly with commercial off-the-shelf (COTS) device developments, which is the object of this work. In addition, WISP are not commonly adopted to build 2.4 GHz and 5.8 GHz backscatter systems because the WISP RF analog front end is designed for operating around 915 MHz, [16].

In [2] the authors address the task of developing a 5.8 GHz energy harvesting tag with significant energy conversion capability, although it requires longer charging time if compared with this work, and does not report the back-scattering features.

This article aims at providing the design principles assessment and the consequent development, of a full batteryless back-scattering wireless transponder suited for on-demand

Manuscript received February 24, 2020; revised July 17, 2020 and August 12, 2020; accepted August 24, 2020. Date of publication September 2, 2020; date of current version November 23, 2020. This work was supported in part by Regione Toscana POR CreO FESR 2014–2020 Action 1.1.5.a3–Bando FAR–FAS 2014 under Project "SUMA-*Struttura Urbana Multifunzionale Attiva*" and Project POR-FSE 2014–2020 "*asse – A*," and in part by the Joint Research Laboratory on *Systems and Technologies for Info-Mobility* at the University of Florence, Italy. This paper is an extended version of "Optimum Design of Low Energy Harvesting Detector at 5.8 GHz suitable for COTS devices" from the 2019 IEEE International Conference on RFID Technology and Applications, Pisa, Italy, Sep. 2019. *(Corresponding author: Alessandro Cidronali.)*

The authors are with the Department of Information Engineering, University of Florence, 50139 Florence, Italy (e-mail: alessandro.cidronali@unifi.it).

Digital Object Identifier 10.1109/JRFID.2020.3020398

communications, compliant with the physical layer of the 5.8 GHz vehicular dedicated short-range communications (DSRC) radio access technologies, [17], [18], [19].

A notable objective of the present paper is a detailed analysis of this type of transponder and its validation by the development of a prototype, which makes use only of COTS devices. According to the literature related to energy harvesting techniques, [14], [20], [21], the "system load" that has to be powered by RF to DC converter blocks is often considered as having a very high impedance (e.g., kOhms [10]). This relies on a misconception, that the energy harvesting is a problem that should be faced by employing integrated technologies and ultra-low power optimized digital stages. Surely this is the best case scenario, but the high expenses required to develop a proprietary fully integrated system as well as the tight time-to-market constraints, make attractive a COTS based development. Making energy harvesting practical also with not so low-powered COTS devices, such as conventional EEPROMs, [22], or not optimized but cheaper uCs, [23], can give smaller competitors a chance to get into the IoT market.

These considerations motivated the present paper, which is an extension of the work presented in [24] where the authors presented preliminary results about the optimum energy harvesting design technique with COTS devices, for radio communications at 5.8 GHz. In this article, we extend those results to a more complete set of design principles including also the transmitting section, and the entire digital section. Thus transforming the module described in [24] into a fully operative battery-less transponder; the first of its class for vehicular DSRC.

The paper is organized as it follows. The description of the battery-less transponder architecture, along with the detailed derivation of its design principles are discussed in Section II. The Section III provides the design details about a battery-less transponder prototype operating at 5.8 GHz, implementing COTS devices, while Section IV discusses the experimental validation with reference to a vehicular DSRC scenario.

II. Principles of the Transponder Architecture and Design

The transponder system architecture proposed in the present paper, Fig. 1, describes a complete and functional device. The harvester section, (A), is based on the one proposed in [24], here anlysed in detail. In addition, with respect to [24], an RF back-scattering modulator stage, (C), and a fully functional digital section, (B), have been added. The back-scattering modulator stage, (C), has been introduced between the antenna section and the energy harvesting stage (A). In order to reduce the complexity of the system, only one antenna for both the harvesting and back-scattering functions has been employed, representing an unique feature of this development compared to the existing literature, at the operative frequency of 5.8 GHz. In Fig. 1, the component C_{BAT} represents the charge storing capacitor. Although in many energy harvesting applications this component is either replaced by a battery or a super-capacitor, in the present work these solutions are not suitable due to the fast recharge time required by the applicative

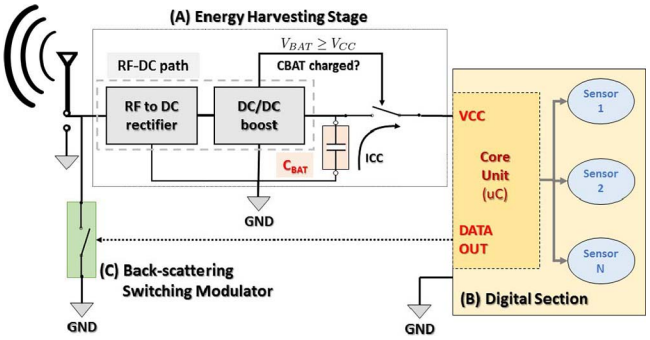


Fig. 1. Architecture of the proposed batteryless transponder system.

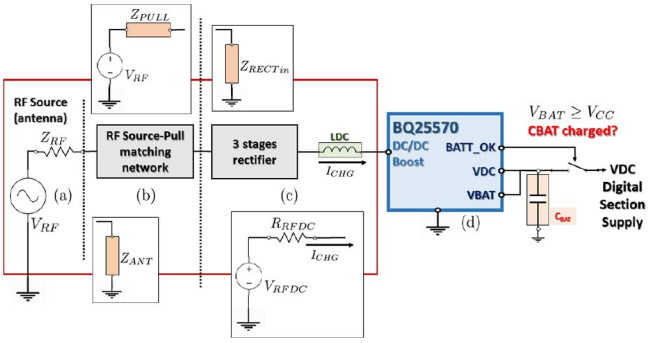


Fig. 2. Architecture of the energy harvesting and conceptual stages input/output impedances.

scenario. The whole system has been fully implemented on a plastic laminate by an industrial printed circuit board (PCB) technology. The design guidelines for each block are described in detail in the following subsection.

A. Energy Harvesting Stage (Block A)

The energy harvesting stage consists of an input matching network, (b) in Fig. 2, an n-stage ladder rectifier, (c) in Fig. 2, and a DC/DC converter, (d) in Fig. 2, that is fed by the rectifier. It is worth to note that the step-up DC/DC block reports the pins name of the functional diagram provided by the vendor. With respect to the architecture proposed in [24], a series 5.8 GHz inductor L_{DC} is introduced after the rectifier DC output to remove the high order spurious harmonics generated by the intrinsic rectifier's non-linear behavior.

The implemented DC/DC converter is expected to have the capabilities of Maximum Power Point Tracking (MPPT) and power-state monitoring. The latter is of primary importance to correctly control the system's operational mode with respect to the actual charge state of energy storage.

From the harvesting section point of view, the on-demand answering capability of the whole system is achieved when the ratio between the required energy harvesting time (the charging time) and the entire communication time window is low enough; this corresponds to the case of a single answer to a single query request. In [24], the authors reported the following simplified formula for estimating the charging time.

$$\Delta T_{CHG} = \left(\frac{V_{BAT\max}}{V_{RFDC}}\right)^2 \frac{R_{RFDC} C_{BAT}}{\eta_{DCDC}}, \tag{1}$$

Here, η_{DCDC} is the efficiency of the DC/DC converter, $V_{BAT\max} = V_{BAT}(0)$ is the full-charge voltage level for the storage capacitor, V_{RFDC} is the open circuit DC output voltage as given by the rectifier stage, R_{RFDC} is the equivalent output impedance for the rectifier stage, and C_{BAT} is the chosen energy storage capacitance. The digital section is made active only when $V_{BAT}(t) \geq V_{DC\min}$, where $V_{DC\min}$ is equal to the minimum required DC supply voltage to ensure correct digital stage operation.

Taking R_{LOAD} as the load impedance fed by the C_{BAT} capacitor, the digital section maximum operational time window is

$$\Delta T_{ON} = \left[\ln\left(\frac{V_{BAT\max}}{V_{DC\min}}\right)\right] R_{LOAD} C_{BAT}, \tag{2}$$

The communication slot is defined as the overall time window between the beginning of a query to the node, including the energy transfer time, and the reception of its answer. Following this the duty-cycle of device node operation within a communication slot can be written as

$$D_{SYS} = \frac{\Delta T_{ON}}{\Delta T_{ON} + \Delta T_{CHG}} = \frac{R_{LOAD}}{R_{LOAD} + K R_{RFDC}}, \tag{3}$$

where the parameter K is

$$K = \frac{1}{\eta_{DCDC}} \left(\frac{V_{BAT\max}}{V_{RFDC}}\right)^2 \left[\ln\left(\frac{V_{BAT\max}}{V_{DC\min}}\right)\right]^{-1} \tag{4}$$

In (3), the parameter K depends on the voltages related to the specific implemented ICs. In the present paper, we employ the BQ25570 DC/DC, which provides a $V_{BAT\max} = 5.0$ V as typical full charge C_{BAT} voltage [25], so when $V_{BAT}(t) \geq 5.0$ V, the "battery OK" control signal is asserted and the digital section is switched to the ON condition (Fig. 1). Considering actual implemented EEPROM, in (2) we can assume $V_{DC\min} = 3.0$ V [22].

Reducing R_{RFDC} improves the efficiency of the communication link increasing the node operation duty-cycle within a single communication slot, thus increasing the ratio between node operational time respect charging time. This can be effectively traded-off by considering that a rectifier with a low number of stages is required to reduce the R_{RFDC} parameter [24], [26], while inceasing the number of stages increases V_{RFDC}, at the same input power, so it leads to

$$K >> 1 \tag{5}$$

and as a consequence one has

$$D_{SYS} < D_{SYS\max} = \frac{R_{LOAD}}{R_{LOAD} + R_{RFDC}}. \tag{6}$$

Eq. (6) provides an upper limit for the D_{SYS} operation duty-cycle and makes clear the importance of providing an R_{RFDC} rectifier output impedance comparable with the R_{LOAD} digital section load impedance. Note that the absolute time delay between query and answer depends only on parameter ΔT_{CHG}, so to improve node reactivity lowering (1) is of main concern.

In the harvester block, the DC/DC acts as a step-up converter which behaves, in the charging phase, as a feedback controlled current sink [27]. As a consequence it drains an I_{CHG} current as high as possible from the rectifier stage, preventing its DC input (or rather, the output of the rectifier stage) from becoming lower than the threshold voltage V_{TH}. This behavior has been successfully modeled in [24].

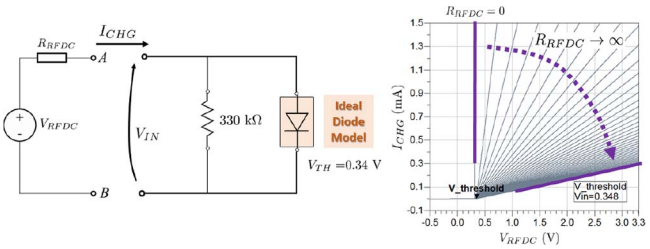


Fig. 3. The DC/DC boost behavioral model.

The application of the DC/DC behavioral model shown in Fig. 3, taking into account that the BQ25570 requires a minimum DC input voltage $V_{IN} > V_{TH} = 0.34$ V, [25], and following the definitions in Fig. 2, leads to the result

$$\begin{cases} V_{RFDC} > V_{TH} \\ V_{RFDC} - R_{RFDC} \cdot I_{CHG} = V_{TH} \end{cases} \tag{7}$$

or, rather,

$$I_{CHG} = \frac{V_{RFDC} - V_{TH}}{R_{RFDC}}. \tag{8}$$

If $\Delta T_{CHG\max}$ is the maximum acceptable charge time, merging the above with (1) results in

$$\left(\frac{V_{BAT\max}}{V_{RFDC}}\right)^2 \frac{R_{RFDC} C_{BAT}}{\eta_{DCDC}} \leq \Delta T_{CHG\max} \tag{9}$$

or, rather,

$$R_{RFDC} \leq \frac{\eta_{DCDC} \Delta T_{CHG\max}}{C_{BAT}} \left(\frac{V_{RFDC}}{V_{BAT\max}}\right)^2 = R_{RFDC\max}. \tag{10}$$

Furthermore, it is possible to estimate an equivalent condition for the minimum required charge current, $I_{CHG} \geq I_{CHG\min}$, if a maximum answer delay $\Delta T_{CHG\max}$ is set

$$I_{CHG} \geq \left(\frac{V_{BAT\max}}{V_{RFDC}}\right)^2 \frac{(V_{RFDC} - V_{TH}) C_{BAT}}{\eta_{DCDC} \Delta T_{CHG\max}} \tag{11}$$

Considering (6), (10), and (11) leads to two fundamental design principles, as proposed in [24]:

- the aim of increasing the overall duty cycle lowering R_{RFDC} is more important than achieving higher V_{RFDC}. As a consequence, since the output resistance of a ladder RF–DC voltage multiplier is proportional to the number of its diodes [26], detectors with fewer stages should be preferred;
- the aim of reducing the charging time ΔT_{CHG} by increasing I_{CHG} is the main optimization goal.

As previously suggested, the DC/DC converter input voltage must be always greater than the minimum voltage threshold to start and maintain the charging process. This means that the entire device is able to operate only when the conditions defined in (7) are met.

Concerning the RF to DC converter, (b) and (c) of Fig. 2, it is possible to describe the power at the rectifier output P_{RFDC} as a function of P_{RF}, which is the power (RF) at the input of the whole harvester stage. According to this, with η_{DCDC}

being the efficiency of the DC/DC converter and η_{RFDC} the efficiency of the RF to DC converter block, it is possible to write

$$P_{RFDC} = V_{TH} \cdot I_{CHG} = \eta_{RFDC} \cdot P_{RF}; \tag{12}$$

assuming that the DC/DC lowers its input voltage to $V_{RFDC} = V_{TH}$. As a consequence

$$I_{CHG} = \frac{\eta_{RFDC} \cdot P_{RF}}{V_{TH}}. \tag{13}$$

To fulfill the condition on the maximum answer delay, $\Delta T_{CHG} \leq \Delta T_{CHG\max}$, Eq. (11) must be verified, so one can impose

$$\frac{\eta_{RFDC} \cdot P_{RF\min}}{V_{TH}} \geq I_{CHG\min} \tag{14}$$

or, rather,

$$\Delta T_{CHG} \geq \frac{V_{BAT\max}^2 \cdot V_{TH}(V_{RFDC} - V_{TH}) \cdot C_{BAT}}{V_{RFDC}^2 \cdot P_{RF\min} \cdot \eta_{RFDC} \cdot \eta_{DCDC}}. \tag{15}$$

If (10) and (15) are satisfied for any power level greater than $P_{RF\min}$, the answer delay is lower than the imposed $\Delta T_{CHG\max}$ limit. Eq. (15) gives an estimation of the minimum ΔT_{CHG} achievable for a specific configuration.

These have as a consequence that the rectifier topology can be chosen in advance, estimating its R_{RFDC} output impedance using (6). Despite this, (15) is strictly dependent on the power conversion efficiency, thus an effective tuning must be made by carefully analyzing the η_{RFDC} efficiency term. Considering now the RF to DC converter stage, as shown in Fig. 2, the efficiency parameter η_{RFDC} can be written as

$$\eta_{RFDC} = |\mathrm{T_{POW_{ab}}}|^2 \cdot |\mathrm{T_{POW_{bc}}}|^2 \cdot \eta_{RFDC0} \cdot |\mathrm{T_{POW_{cd}}}|^2, \tag{16}$$

where the power transmission coefficients $\left|\mathrm{T_{POW_{ij}}}\right|^2$ model any possible power loss due to mismatches between the sections, as described in Fig. 2, while η_{RFDC0} is equal to the ideal RF to DC power conversion efficiency, without considering any mismatch between section interfaces. Without the need of further developing such simple model, it is straightforward that a comprehensive optimization process based on circuit simulations must be done, with the goal of maximizing the mean DC/DC input current I_{CHG}.

The maximization of the $|\mathrm{T_{POW_{cd}}}|^2$ power coupling term is strictly related to the MPPT feature implemented within the DC/DC feedback control unit [25]. Briefly, the MPPT algorithm tries to identify the best working point (or the best V_{IN} input voltage and I_{CHG} input current) for the DC/DC block, thus making the DC/DC converter a time-variant variable load. The DC/DC input port acts like a current sink while the DC/DC logic continuously verifies the voltage at the input port: if it decreases the logic control, it increases the DC/DC supply input resistance, reducing the current sinking. The model proposed in Fig. 3, although fairly simplified, describes quite accurately the behavior of the DC/DC supply input when the DC/DC logic driving it is in "high absorption" mode (with $V_{IN} = V_{TH}$ [25]).

According to the BQ25570 operation principle, [25], the DC/DC continuously tries to increase its current absorption, using the voltage at its $V_{IN} = V_{RFDC}$ input pin as feedback control. The average current absorption is modulated by varying the DC/DC switching duty cycle and when voltage on V_{IN} begins to rise, the duty cycle is reduced to restore the steady condition. On this basis, it behaves as a feedback controlled device, which always tends to reach its steady condition of maximum current absorption by keeping $V_{IN} = V_{TH}$. The proposed model in Fig. 3 effectively reproduces the behavior of the DC/DC stage, and it was validated by comparison with experimental measurements by setting voltage source levels with fixed maximum output current.

As a consequence we can assume that the harvester optimization, carried out on the basis of the proposed equivalent model, ensures that the system works in such a condition.

Having imposed $|\mathrm{T_{POW_{cd}}}|^2 = 1$, because of the particular choice of the DC/DC model, the energy harvesting stage optimization problem relies on maximizing the $|\mathrm{T_{POW_{bc}}}|^2$ power transmission coefficient and the η_{RFDC0} power conversion efficiency.

The DC/DC converter input charge current I_{CHG} can be maximized through a source-pull optimization, implementing a simulation based on a model composed by the rectifier stage, (c) in Fig. 2, and the behavioral model of the DC/DC, Fig. 3. As stated in (7), when charging, the converter DC input voltage is fixed at V_{TH}. In this way, the goal, namely, maximizing the I_{CHG} charge current, exactly matches the goal of maximizing the DC/DC input power P_{RFDC} (12) and power conversion efficiency η_{RFDC0}. The source-pull finds the optimal RF source impedance Z_{PULL} to be shown to rectifier input port to maximize the RF to DC power conversion efficiency, thus maximizing the $|\mathrm{T_{POW_{bc}}}|^2$ power transmission coefficient, or, rather, it looks for the optimal $Z_{\mathrm{PULL}} = Z_{\mathrm{RECT_{opt}}}^*$ which minimizes the power reflection coefficient

$$\Gamma_{\mathrm{POW_{bc}}} = \frac{Z_{\mathrm{RECT_{opt}}} - Z_{\mathrm{PULL}}^*}{Z_{\mathrm{RECT_{opt}}} + Z_{\mathrm{PULL}}^*} \quad \text{with } |\mathrm{T_{POW_{bc}}}|^2 = 1 - |\Gamma_{\mathrm{POW_{bc}}}|^2. \tag{17}$$

Because the RF to DC stage is nonlinear, different values of Z_{PULL} lead to highly different energy distributions in the output harmonics, thus dramatically varying the magnitude of the DC output current I_{CHG}. This leads to $Z_{\mathrm{PULL}} \neq Z_{\mathrm{RECT_{in}}}^*$, which is different than it should be with a linear stage. A harmonic balance simulation engine must be used to simulate the entire span of feasible values of Z_{PULL}, looking for the maximum output current I_{CHG}.

Note that considering the standard small-signal reflection coefficient definition at network output port

$$\Gamma_{\mathrm{bc}} = \frac{Z_{\mathrm{RECT_{in}}} - Z_{\mathrm{PULL}}^*}{Z_{\mathrm{RECT_{in}}} + Z_{\mathrm{PULL}}^*} \tag{18}$$

the source-pull matching network does not provide a small-signal matching between its output and the rectifier input impedances, because what results is $Z_{\mathrm{RECT_{opt}}} \neq Z_{\mathrm{RECT_{in}}}$.

Further theoretical analysis could be implemented by modeling nonlinear diodes (e.g., [28], [29], [30], [31]) nevertheless, for this specific work, source-pull turns out to be a straightforward approach for finding the optimal values.

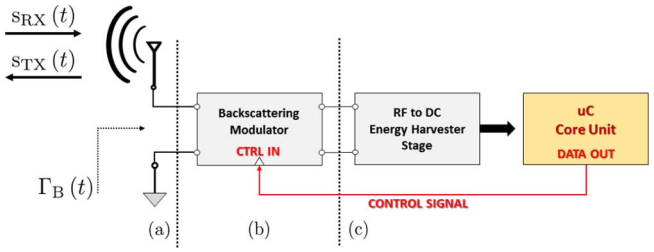


Fig. 4. Architecture of series back-scatterer modulator.

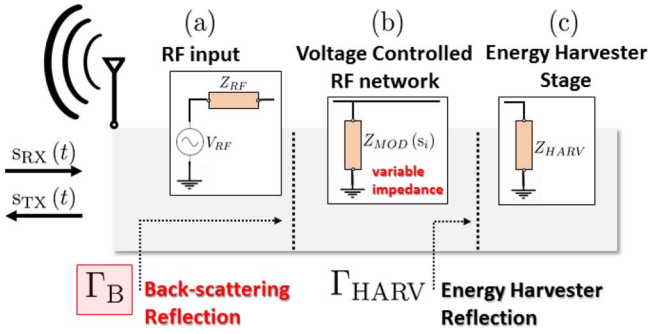


Fig. 5. Conceptual diagram of stages chain.

B. Digital Section (Block B)

From the point of view of the system analysis and design of the harvesting sub-block, the digital section input, B in Fig. 1, can be modeled as a resistor of value R_{LOAD}; note that its value can vary significantly on the basis of the specific adopted IC. The main structural features of the harvesting architecture, in particular, the number of rectifier stages, can also be exploited to determine the best choice for the integrated DC/DC converter, following (6), (10) and (15).

Because all the step-up converters share the same architecture, they may be described by the behavioral model shown in Fig. 3 and described in [24]–[27]. To increase the compactness and efficiency of the system, the use of an IC capable of internal clock generation is strongly suggested, in order to reduce the overall power consumption.

C. Back-Scattering Modulator (Block C)

The system technology under consideration adopts an uplink communication implemented by a back-scattering scheme, thus exploiting the same impinging RF power for sending radio network answers without wasting the collected power, [28], [32], [33]. The concept of a back-scattering modulator is well-known in the literature, but the proposed architecture makes use of a single antenna for both harvesting and back-scattering in order to reduce the size of the device.

With reference to Fig. 4, the back-scatterer sends back its own radio signal based on a modulation of the impinging RF power (19)

$$s_{TX}(t) = \Gamma_B(t) \cdot s_{RX}(t) \tag{19}$$

thus the RF signal modulation is achieved through the variation of the reflection coefficient term $\Gamma_0(t)$. It is worth noting that wave reflection can introduce both amplitude and phase variation in the reflected signal: $\Gamma_0(t)$ can be a complex quantity, thus any kind of modulation scheme can be implemented (e.g., amplitude, phase or combined modulation [33]). The constraint of having a single antenna for both harvesting and back-scattering imposes a signal chain as shown in Fig. 4. This requires the simultaneous fulfillment of two different requirements for the modulator stage: first it must be able to achieve the required modulation parameters, and the second consists of allowing the maximization of the power delivery between the RF input and the energy harvesting stage during its standby state.

To correctly design the back-scattering modulator, we define design parameters on the basis of proper modulation index. It allows also the estimation of the data-link robustness and the link budget under physical channel conditions [32], [34], [35]. For this purpose, the analytical forms of modulation indexes for a two-symbols ASK and a two-symbols PSK modulation schemes are hereby derived, and further on adopted to determine feasible design parameters for the modulator stage.

The modulation is achieved by varying the electrical parameters of the modulator stage. As a consequence, the stage can be modeled as a variable load connected between the RF input and the harvester stage (Fig. 5). Following this model, the overall reflection coefficient can be expressed as a function of the modulator impedance $Z_{MOD_i} = Z_{MOD}(s_i)$, so by imposing some conditions on the modulation index, the Z_{MOD} modulator impedance can be extracted.

With a two-symbol (s_0 "low", s_1 "high") modulation scheme, it is possible to define the symbol ratio as

$$m = \frac{s_{TX}(s_1)}{s_{TX}(s_0)} = \frac{\Gamma_B(s_1)}{\Gamma_B(s_0)} \tag{20}$$

thus the modulation depth for an ASK or a PSK modulation scheme can be defined as a function of the symbol ratio, which is a function of back-scattering coefficients for each symbol state condition.

At the modulation state "zero" the RF source available power must be entirely delivered to the harvester stage, in such condition the delivered power can be written as

$$P_{RF} = \frac{V_B^2}{2(Z_{MOD0} || Z_{HARV})} \tag{21}$$

where V_B is the voltage at the back-scattering to antenna interface section. The power delivered to the Z_{HARV} load is

$$P_{HARV} = \frac{V_B^2}{2Z_{HARV}} \tag{22}$$

and the actual goal is to achieve

$$\frac{P_{RF}}{P_{HARV}} = 1 + \frac{Z_{HARV}}{Z_{MOD0}} \approx 1; \tag{23}$$

so it should result

$$\left|\frac{Z_{HARV}}{Z_{MOD0}}\right| \to 0 \quad \Rightarrow \quad |Z_{MOD}(s_0)| >> |Z_{HARV}|. \tag{24}$$

Using the flow graph method [36], the input signal reflection coefficient Γ_B for the cascade of stages can be defined as

$$\Gamma_B = S_{11} + \frac{S_{12}S_{21}\Gamma_{HARV}(s_0)}{1 - S_{22}\Gamma_{HARV}(s_0)}, \tag{25}$$

with

$$\Gamma_{\mathrm{HARV}}(\mathrm{s}_0) = \frac{Z_{\mathrm{HARV}} - Z_{\mathrm{RF}}}{Z_{\mathrm{HARV}} + Z_{\mathrm{RF}}}, \tag{26}$$

where $\Gamma_{\mathrm{HARV}}(\mathrm{s}_0)$ is the signal reflection coefficient at the energy harvester input interface during the s_0 state or rather, during the energy harvesting process. The S_{ij} are the terms of the matrix of *S*-parameter matrix characterizing the modulator, normalized at Z_{RF}, which turn out to be

$$\mathrm{S}_{11} = \mathrm{S}_{22} = \frac{(Z_{\mathrm{MOD}}(\mathrm{s}_i)||Z_{\mathrm{RF}}) - Z_{\mathrm{RF}}}{(Z_{\mathrm{MOD}}(\mathrm{s}_i)||Z_{\mathrm{RF}}) + Z_{\mathrm{RF}}}$$
$$\mathrm{S}_{12} = \mathrm{S}_{21} = 1 - \mathrm{S}_{11}$$

that are,

$$\mathrm{S}_{11} = \mathrm{S}_{22} = -\frac{Z_{\mathrm{RF}}}{2Z_{\mathrm{MOD}}(\mathrm{s}_i) + Z_{\mathrm{RF}}} \tag{27}$$

$$\mathrm{S}_{12} = \mathrm{S}_{21} = \frac{2Z_{\mathrm{MOD}}(\mathrm{s}_i)}{2Z_{\mathrm{MOD}}(\mathrm{s}_1) + Z_{\mathrm{RF}}} \tag{28}$$

merging (27) and (26) with (25) one obtains

$$\Gamma_{\mathrm{B}}(\mathrm{s}_i) = \frac{(2Z_{\mathrm{MOD}i} - Z_{\mathrm{RF}})\Gamma_{\mathrm{HARV}}(\mathrm{s}_0) - Z_{\mathrm{RF}}}{(2Z_{\mathrm{MOD}i} + Z_{\mathrm{RF}}) + Z_{\mathrm{RF}}\Gamma_{\mathrm{HARV}}(\mathrm{s}_0)}. \tag{29}$$

Let us to note that the disable state of the modulator corresponds to its "zero" (s_0) state. Considering the modulator stage, the equivalent input impedance for the harvester stage becomes

$$Z_{\mathrm{RF,MOD}} = (Z_{\mathrm{RF}}||Z_{\mathrm{MOD}0}) = Z_{\mathrm{RF}}\left(1 + \frac{Z_{\mathrm{RF}}}{Z_{\mathrm{MOD}0}}\right)^{-1} \tag{30}$$

but the source-pull network is designed to maximize the RF–DC power conversion given an input impedance Z_{RF}. To achieve this during the symbol s_0 state, one must have

$$Z_{\mathrm{RF,MOD}} \approx Z_{\mathrm{RF}} \tag{31}$$

so it is trivial that one must have

$$\left|\frac{Z_{\mathrm{RF}}}{Z_{\mathrm{MOD}0}}\right| \to 0 \quad \Rightarrow \quad |Z_{\mathrm{MOD}}(\mathrm{s}_0)| >> |Z_{\mathrm{RF}}| \tag{32}$$

Merging (24) and (32) a mandatory condition for "zero" state modulator impendance results

$$|Z_{\mathrm{MOD}}(\mathrm{s}_0)| >> \max\left(|Z_{\mathrm{HARV}}|, |Z_{\mathrm{RF}}|\right) \tag{33}$$

If the condition in (33) is verified, $\Gamma_{\mathrm{B}}(\mathrm{s}_0)$ can be simplified to

$$\Gamma_{\mathrm{B}}(\mathrm{s}_0) \approx \Gamma_{\mathrm{HARV}}(\mathrm{s}_0) = \frac{Z_{\mathrm{HARV}} - Z_{\mathrm{RF}}}{Z_{\mathrm{HARV}} + Z_{\mathrm{RF}}} \tag{34}$$

and, as expected, the modulator stage does not affect the signal propagation. Following (20) and employing (34), the symbol ratio is

$$\mathrm{m} = \frac{\Gamma_{\mathrm{B}1}}{\Gamma_{\mathrm{B}0}} \approx \left(\frac{1}{\Gamma_{\mathrm{B}0}}\right)\frac{(2Z_{\mathrm{MOD}1} - Z_{\mathrm{RF}})\Gamma_{\mathrm{B}0} - Z_{\mathrm{RF}}}{(2Z_{\mathrm{MOD}1} + Z_{\mathrm{RF}}) + Z_{\mathrm{RF}}\Gamma_{\mathrm{B}0}} \tag{35}$$

where $\Gamma_{\mathrm{B}i}$ represents the corresponding $\Gamma_{\mathrm{B}}(\mathrm{s}_i)$. The (35) can be simplified by noting that maximizing the power transfer from the RF input source to the harvester implies the condition $|\Gamma_{\mathrm{B}0}|^2 << 1$, thus the symbol ratio can be approximated by

$$\mathrm{m} \approx -\left(\frac{1}{\Gamma_{\mathrm{B}0}}\right)\left(\frac{Z_{\mathrm{RF}}}{2Z_{\mathrm{MOD}}(\mathrm{s}_1) + Z_{\mathrm{RF}}}\right) \tag{36}$$

where $\Gamma_{\mathrm{B}0}$ is independent of $Z_{\mathrm{MOD}}(\mathrm{s}_i)$ and is already given by the energy harvester stage simulation after the source-pull optimization, as shown in Section II-A.

Conventionally a two-symbols ASK modulation index can be defined as

$$\mathrm{m}_{\mathrm{ASK}} = \frac{|A_1 - A_0|}{\max\left(|A_1|, |A_0|\right)} \tag{37}$$

where each A_i is the carrier amplitude related to the i-th symbol [34]. Considering the back-scattering modulator it leads to

$$\mathrm{m}_{\mathrm{ASK}} = \frac{|\Gamma_{\mathrm{B}1} - \Gamma_{\mathrm{B}0}|}{\max\left(|\Gamma_{\mathrm{B}1}|, |\Gamma_{\mathrm{B}0}|\right)} \tag{38}$$

and considering the symbol ratio definition in (36) it results

$$\mathrm{m}_{\mathrm{ASK}} = \begin{cases} 1 - |\mathrm{m}|^{-1} & \text{if } |\mathrm{m}| \geq 1 \\ 1 - |\mathrm{m}| & \text{if } |\mathrm{m}| < 1 \end{cases} \tag{39}$$

Merging (36) and (39) the final ASK modulation index becomes

$$\mathrm{m}_{\mathrm{ASK}} = \begin{cases} 1 - |\Gamma_{\mathrm{B}0}|\left|2\frac{Z_{\mathrm{MOD}}(\mathrm{s}_1)}{Z_{\mathrm{RF}}} + 1\right| & \text{if } |\Gamma_{\mathrm{B}1}| \geq |\Gamma_{\mathrm{B}0}| \\ 1 - \left|\frac{1}{\Gamma_{\mathrm{B}0}}\right|\left|\frac{Z_{\mathrm{RF}}}{2Z_{\mathrm{MOD}}(\mathrm{s}_1) + Z_{\mathrm{RF}}}\right| & \text{otherwise.} \end{cases} \tag{40}$$

Note that the condition $|\Gamma_{\mathrm{B}1}| < |\Gamma_{\mathrm{B}0}|$ is absolutely not feasible because it would lead to a very low signal amplitude for the symbol "s_1". With this, (40) should be rewritten for final calculations as

$$\mathrm{m}_{\mathrm{ASK}} = 1 - |\Gamma_{\mathrm{B}0}|\left|2\frac{Z_{\mathrm{MOD}}(\mathrm{s}_1)}{Z_{\mathrm{RF}}} + 1\right| \quad \text{with} \quad |\mathrm{m}| \geq 1 \tag{41}$$

thus maintaining only the suitable subdomain.

In a similar way, defining ϑ_i as the signal carrier phase displacement (in radians) respect reference signal for each i-th symbol, the PSK modulation index can be defined as

$$\mathrm{m}_{\mathrm{PSK}} = \frac{|[(\vartheta_1 - \vartheta_0) - \pi] \bmod 2\pi - \pi|}{\pi} \tag{42}$$

or rather

$$\mathrm{m}_{\mathrm{PSK}} = \frac{|\vartheta_1 - \vartheta_0|}{\pi} \quad \text{with} \quad |\vartheta_1 - \vartheta_0| < \pi, \forall i \tag{43}$$

Considering the back-scattering modulator it equals to

$$\mathrm{m}_{\mathrm{PSK}} = \frac{|\angle\Gamma_{\mathrm{B}1} - \angle\Gamma_{\mathrm{B}0}|}{\pi} = \frac{|\angle\mathrm{m}|}{\pi} \quad \text{with} \quad |\angle m| < \pi \tag{44}$$

thus considering (36) the PSK modulation index results

$$\mathrm{m}_{\mathrm{PSK}} = \frac{|\angle Z_{\mathrm{RF}} - \angle(2 \cdot Z_{\mathrm{MOD}}(\mathrm{s}_1) + Z_{\mathrm{RF}}) - \angle\Gamma_{\mathrm{B}0}|}{\pi}. \tag{45}$$

Assuming $|Z_{\mathrm{MOD}}(\mathrm{s}_1)| >> |Z_{\mathrm{RF}}|$ and a real Z_{RF} impedance, (45) can be simplified as

$$\mathrm{m}_{\mathrm{PSK}} = \frac{|\angle Z_{\mathrm{MOD}}(\mathrm{s}_1) + \angle\Gamma_{\mathrm{B}0}|}{\pi} \tag{46}$$

The design of the modulator exploits the degrees of freedom dictated by the (41) and (46), respectively suitable to implement either an ASK or a PSK back-scatterer modulation scheme; having fixed $|\Gamma_{\mathrm{B}0}|^2 << 1$, these result to be related mainly to design value of $Z_{\mathrm{MOD}}(\mathrm{s}_1)$.

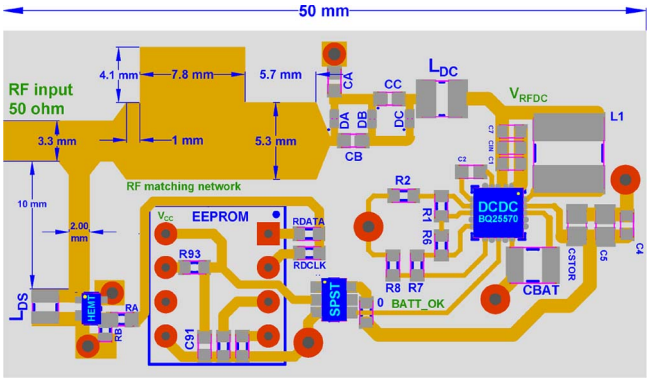


Fig. 6. Top layer of implemented PCB on ISOLA FR408 1.52 mm.

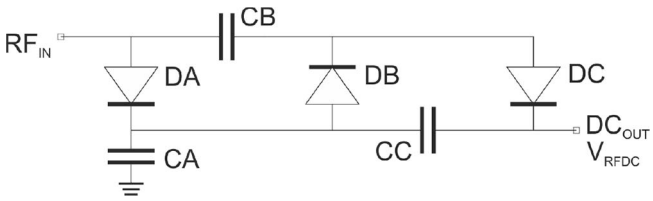


Fig. 7. Schematic of implemented 3-stage RF–DC converter.

III. The Design of the Batteryless Subsystems

The design and implementation of a 5.8 GHz batteryless back-scattering transponder with on-demand answer capability will now be covered in detail, applying the design principles described in Section II.

In Fig. 6 we present the layout of the batteryless transponder. The device is implemented as a standard two-layer PCB on ISOLA FR408 1.52 mm laminate. This does not allow a particularly refined routing solution, thus forcing us to choose a simple PDIP version for the digital IC. This solution has the drawback of having higher power requirements (as stated for instance in [22]), thus the PDIP version represents the low cost development scenario aimed at in this article.

In the following, we present the detailed design process and considerations for each block.

A. Energy Harvesting Stage (Block A)

With reference to the topology shown in Fig. 2, the energy harvesting block is based on a 3-stage rectifier (Fig. 7) which feeds a commercially available DC/DC converter (namely the BQ25570) which operates in step-up/boost configuration [25]. The BQ25 DC/DC converter family is well-known in the literature (see [14], [37]) because of its ease of integration and its advanced capabilities of MPPT tracking and power-state monitoring.

The number of RF to DC rectifier stages was chosen using the equations discussed in Section II-A, and considering a minimum input power of $P_{RF} = -5$ dBm.

The configuration shown in Fig. 7 is the same as proposed in [24]. Anyway the previous rectifier was implemented using Infineon BAT-1503W Schottky diodes with a forward voltage $V_F = 0.25$ V with $I_F = 1$ mA forward current [38]. In the present work we adopted zero-bias diodes in order to cope

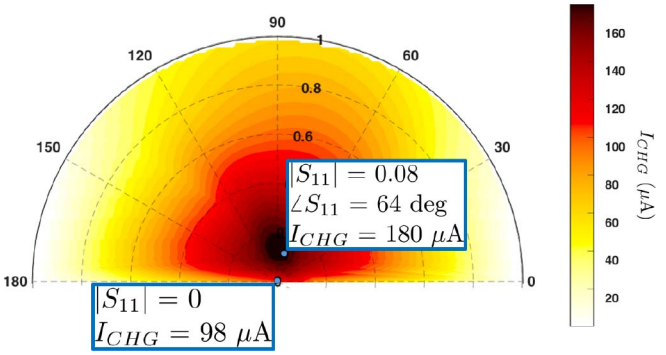


Fig. 8. Simulated charge current values throughout the domain of the RF–DC input reflection coefficients.

with lower level of minimum impinging power at the rectifier input port, thus improving the sensitivity of the transponder. The implementation of the rectifier is based on Skyworks SMS7630-061 Zero-Bias Schottky diodes with a forward voltage $V_F = 0.18$ V at forward current $I_F = 1$ mA [39]. As energy storage a tank capacitor $C_{BAT} = 100$ uF has been used. Assuming an RF input power level of -5 dBm at the rectifier input section (Fig. 7), a complete set of simulations were carried out to simulate the system cascade shown in Fig. 2; this was achieved without inserting the source-pull matching network block, and uniformly sweeping the entire domain of the reflection coefficient seen by the matching network, this latter having output impedance Z_{PULL}. As a consequence of the above setting, the equivalent Z_{PULL} source output impedance can be calculated as

$$Z^*_{\mathrm{PULL}} = Z_{\mathrm{RECTin}}\left(\frac{1-\mathrm{S}_{11}}{1+\mathrm{S}_{11}}\right) \tag{47}$$

where S_{11} is the independent variable of the source-pull analysis, and $Z_{\mathrm{RECTin}} = (8.2 + j91.95)\Omega$ is the estimated input impedance of the rectifier and the DC/DC cascade. The simulated results for the charge current I_{CHG} are plotted in Fig. 8, showing a doubling of the power conversion efficiency with respect to a typical $|\mathrm{S}_{11}| = 0$ small-signal matching.

From Fig. 8, one can see that this source-pull analysis leads to the optimal source output impedance

$$Z_{\mathrm{PULL}} = 19.8512 - j83.7706\,\Omega,$$

which can be conveniently implemented in microstrip technology.

Thus considering a typical RF source input impedance of 50Ω, the source-pull matching network is designed as in Fig. 6. The simulation with the source-pull matching network and an RF input power of -5 dBm provided the following data.

$$\begin{gathered} I_{CHG} = 180\ \mu\mathrm{A},\ V_{RFDC} = 1.05\ \mathrm{V} \\ |\Gamma_{\mathrm{B0}}| = 0.319,\ \angle\Gamma_{\mathrm{B0}} = -140\ \mathrm{deg} \\ \text{expected } \eta_{RFDC} = 0.21,\ \eta_{DCDC} = 0.60 \end{gathered} \tag{48}$$

where the DC/DC efficiency η_{DCDC} has been extrapolated from the BQ25570 datasheet [25].

Note that terminating the source-pull network on the actual rectifier input impedance $Z_{\mathrm{RECTin}} \neq Z_{\mathrm{PULL}}$ leads to a non-zero signal reflection coefficient at the RF input port. Despite

this, the source-pull ensures that at the interface between the source-pull network and the rectifier, the power reflection coefficient is minimized, thus increasing the power transfer with respect to a small-signal matching network.

The comparison between different matching conditions with respect to the estimated charge currents I_{CHG}, is presented in (49), for an input power of -5 dBm.

$$I_{CHG} = \begin{cases} 98\ \mu\text{A} & \text{small-signal matching} \\ 141\ \mu\text{A} & \text{with source-pull network} \end{cases} \tag{49}$$

From (49) we can conclude that the source-pull analysis provides the impedance termination that optimize of RF-to-DC conversion, with respect to the conventional case of impedance matching between the antenna and the RF-DC converter block. A further and conclusive analysis permits to reveal the impact of the matching network losses; indeed simulating the I_{CHG} by assuming the RF source having an internal impedance equal to Z_{PULL}, we would achieve $I_{CHG} = 180\ \mu$A. Thus removing the losses introduced by the matching network, the result shows a significant additional improvement.

B. Digital Section (Block B)

In Section I we highlighted how the proposed design principles allow achieving a good system efficiency, also dealing with non–power-optimized COTS ICs. To demonstrate this, the digital section is actually implemented with a very cheap EEPROM in a PDIP package intended to be integrated in a PCB containing the entire system. Considering the for instance the commercially available EEPROM, Atmel AT17LV512A 3.3 V 256 kbit on PDIP package [22], it is equivalent to the harvesting load

$$R_{LOAD} = \frac{V_{DC}}{I_{DC}} = \frac{3.0\ \text{V}}{5\ \text{mA}} \approx 600\Omega \tag{50}$$

thus it is much lower than the kΩ load resistance typically considered in similar works, which deal with very low-power or integrated CMOS digital stages [2], [4], [14], [21].

This EEPROM features also the MSM (Master-Serial-Mode) operating mode, thus it is able to output its entire bit stream together with a matched clock without needing any sort of boot-up procedure [22]. Dealing with an RFID-like application scenario, this solution is actually the simplest one and it removes the need for writing specific firmware for testing purposes.

Using the simulation results in (48) it is possible to estimate a feasible value for the energy storage capacitor C_{BAT} (Fig. 2). Taking $V_{BAT\max} = 5.0$ V, an input power of -5 dBm, and that the EEPROM internal clock shows an average data throughput $f_{\text{CLK}} \approx 8$ Mbps [22], using (2) and (15) the operation time window and charging time can be approximated as

$$\begin{aligned} \Delta T_{ON} &\approx \left(2.5 \cdot 10^2\right) C_{BAT} \\ \Delta T_{CHG} &\approx \left(2.0 \cdot 10^5\right) C_{BAT} \end{aligned} \tag{51}$$

The entire memory has size $N_{\text{BITS}} = 256$ kbits so to transmit the entire data the minimum operation time window must be

$$\Delta T_{ON} \geq \frac{N_{\text{BITS}}}{f_{\text{CLK}}} \approx 40\ \text{ms} \tag{52}$$

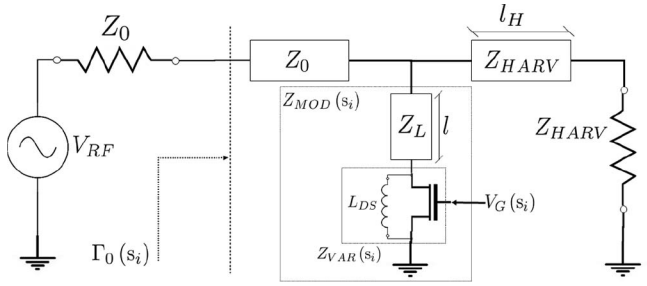


Fig. 9. Simplified schematic diagram of the back-scatterer block.

thus the energy storage capacitor must be $C_{BAT} \geq 200$ uF. With $C_{BAT} = 200$ uF, estimated charging time is $\Delta T_{CHG} \approx 40$ s.

From its specifications, it is expected that a DC/DC converter could isolate, electrically, the DC output port from its DC input [27], so the final load should not affect the charging process. For the BQ25570 converter, this condition is not verified because the DC output port is enabled also during charging state. To overcome this drawback, an integrated switch is placed, as seen in Fig. 2: the BQ25570 "ready state" signal is used as a control signal for a NC7SZ66 single-pole single-throw SPST COTS switch, [40], Fig. 6.

C. Back-Scattering Modulator (Block C)

The modulator block input and output impedances are defined following the principles described in Section II-C and employing the optimal source-pull power matching network as designed above. A simple topology for the back-scattering modulator is shown in Fig. 9, which assumes a typical $Z_0 = 50\Omega$ line impedance and RF source. The transmission line, of length l_H, has a characteristic impedance Z_{HARV} line impedance to maintain the same impedance at the modulator section and thus verify all the conditions explained in Section II. Note that this assumption requires that Z_{HARV} has not a significant imaginary component.

Note that an L_{DS} inductor is placed in parallel with the transistor to make it operate in the cold-FET region. In addition, this allows a DC current path for the harvester block and consequently for the DC/DC converter input. This is required because when connecting an antenna, it constitutes an open circuit for any DC signal, so there would not be a DC closed loop that includes the harvester block input. By this, the variable load is

$$Z_{\text{VAR}}(s_i) = \left(Z_{\text{DS}}(s_i) || Z_{L_{DS}}\right), \tag{53}$$

where $Z_{\text{DS}}(s_i)$ is the voltage controlled drain-source impedance of the transistor while $Z_{L_{DS}}$ is the resulting impedance of the L_{DS} inductor.

The transistor, which acts as an on–off switch, selected for This work is an ATF-58143 high-electron mobility transistor, [41], which is a normally-on high frequency transistor (i.e., an E-PHEMT) operating as cold-FET because of the inductor L_{DS} (LQW2UAS4R7J00 4.7 uH). All the simulations were calculated using the Keysight Technology - Advanced System

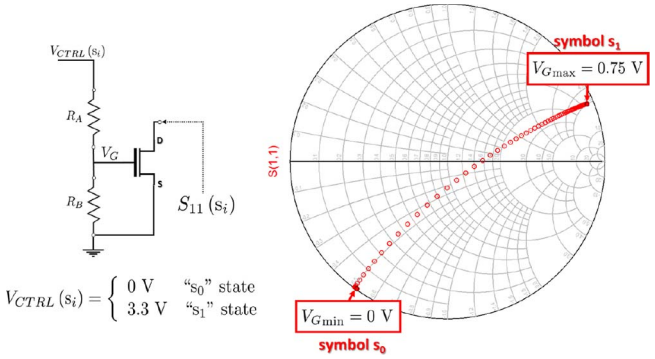


Fig. 10. Schematic diagram of the variable load Z_{VAR} (left) and corresponding simulated impedance at 5.8 GHz (right) as a function of E-PHEMT gate voltage for Vds = 0 V.

Design simulation tool, and using CAD models available from the vendors for all the circuit components.

The modulation is made directly connecting the transistor gate $V_G(s_i)$ to the EEPROM data output through resistor R_{DATA} (see Fig. 6). To correctly scale the EEPROM high level output voltage $V_H = V_{DC} = 3.3$ V to the maximum feasible gate voltage of 0.75 V, [41], a resistive divider is implemented on the PCB with resistances $R_A = 6.8$ MΩ and $R_B = 2.2$ MΩ (Fig. 10 and Fig. 6). The simulation yields $Z_{VAR}(s_i)$ impedances for each binary logic level (s_0, s_1) of

$$Z_{VAR}(V_G) = \begin{cases} 0.25 - j25.80 & V_G = 0\text{ V} \quad \text{state “s}_0\text{”} \\ 32.6 + j246.3 & V_G = 0.7\text{ V state “s}_1\text{”} \end{cases} \quad (54)$$

As stated in Section II-C (33), the maximum power transfer for the configuration shown in Fig. 9 requires

$$|Z_{MOD}(s_0)| >> \max(|Z_0|, |Z_{HARV}|) \quad \text{with} \quad Z_0 = 50\Omega,\ Z_{HARV} = 28.35 - j13.20\ \Omega \quad (55)$$

but observing the simulated Z_{VAR} impedances in (54), it is clear that this condition must be reached. Without adding components, a way to further introduce degrees of freedom to Z_{MOD} is to add a section of line before the variable load. As in Fig. 9, $Z_{MOD}(s_i)$ equals

$$Z_{MOD}(s_i) = Z_L \cdot \frac{Z_{VAR}(s_i) + jZ_L \tan\left(\frac{2\pi}{\lambda_{RF}} l\right)}{Z_L + jZ_{VAR}(s_i) \tan\left(\frac{2\pi}{\lambda_{RF}} l\right)} \quad (56)$$

so tuning the line impedance Z_L and line length l, the modulator load can be set as needed. To check for the achievable values of Z_{MOD}, a sweep over the entire feasible domain for the width (w) of Z_L as well as it length (l) can be performed by simulating the circuit configuration described in Fig. 11.

Considering the mechanical constraints and the wavelength on the actual PCB substrate, the sweep domain is set as

$$l \in [1\text{ mm}, 26\text{ mm}], w \in [1\text{ mm}, 10\text{ mm}] \quad (57)$$

The Fig. 12 shows the magnitudes for the estimated Z_{MOD} impedances throughout the sweep domain for the sizes of the transmission line, for both states of the modulator. To fulfill the maximum power transfer condition defined in (33), one must have

$$|Z_{MOD}(s_0)| >> |Z_{RF}| \quad \rightarrow \quad |Z_{MOD}(s_0)| \geq 500\Omega \quad (58)$$

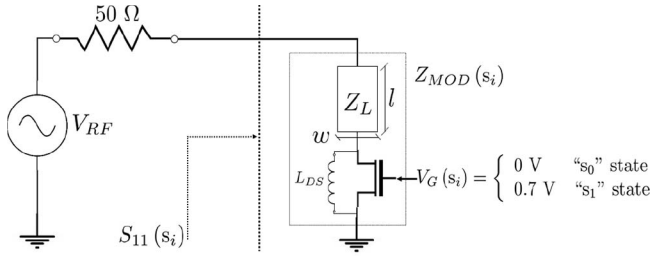


Fig. 11. Simulation model for evaluating Z_{MOD} impedances.

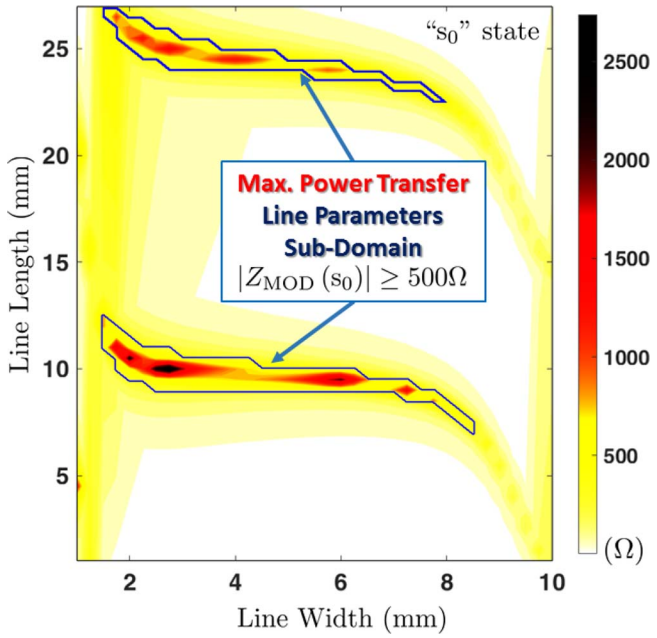


Fig. 12. Magnitudes of simulated Z_{MOD} impedances for energy harvesting “s$_0$” state, for Z_L line width and length parameters.

so a subdomain of feasible Z_L line parameters is defined, shown as a light closed line in Fig. 12. The final line physical parameters must lie within this subdomain to ensure that during the modulator standby state the maximum power transfer is achieved. Shorter Z_L line lengths are preferable to reduce the final PCB dimensions, so we put $l \leq 15$ mm.

As the final step, the modulation index must be investigated. Using the Γ_{B0} parameter calculated after the source-pull optimization, see the (48), and having the entire set of values for $Z_{MOD}(s_i)$, an estimation for both ASK and PSK modulation depths can be done applying the (36)–(46). The numerical estimations of the expected modulation depths functions are given in Fig. 13. We can see from the data the best set of dimensions for the transmission line Z_L, looking for the required depths within the admissible subdomain. According to the theoretical bit error rate versus E_b/N_0 for ASK and PSK modulation, which establish that for distance a BER $= 10^{-}3$ is achieved at $E_b/N_0 = 10$ dB for ASK and at $E_b/N_0 = 6.6$ dB for PSK, the latter modulation scheme is preferable for backscattering radio link with low SNRs margin to preserve a sufficiently good link quality. Note that a pure PSK modulation would require having the same signal amplitude for both symbols ($|\Gamma_{B1}| = |\Gamma_{B0}|$) but, being $|\Gamma_{B0}|^2 << 1$, this condition

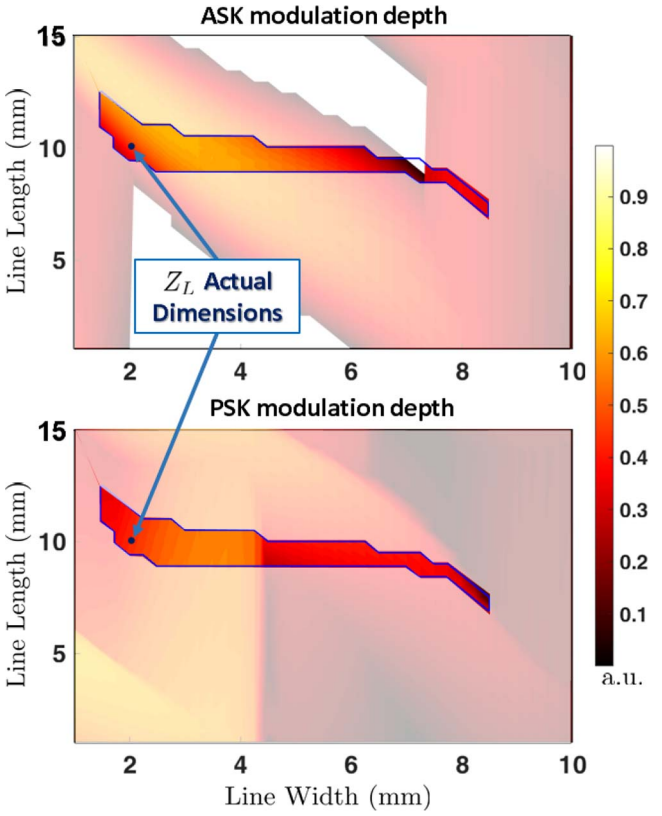


Fig. 13. Estimated ASK (top) and PSK (bottom) modulation depths for Z_L line width and length parameters.

would lead to a constant low amplitude for the retransmitted signal. Hence, a good working point should be one which maximizes both the ASK and the PSK modulation indexes. Considering the plots in Fig. 13, a feasible dimensions set for the transmission line Z_L is

$$\begin{cases} l = 10 \text{ mm} \\ w = 2 \text{ mm} \end{cases} \tag{59}$$

thus, following Fig. 13, leading to modulation indexes

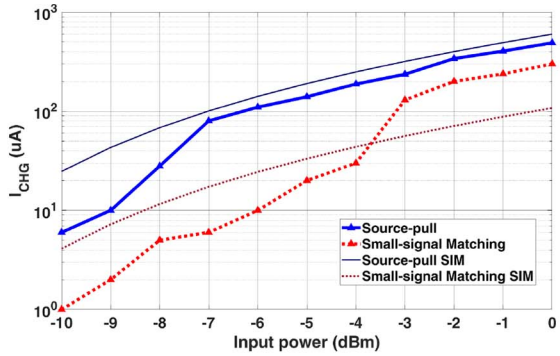
$$\text{m} = 2.5\angle 0.52\pi, \quad \text{m}_{\text{ASK}} = 0.60, \quad \text{m}_{\text{PSK}} = 0.50 \tag{60}$$

The above set of design parameters for the modulator was implemented in the PCB design, see Fig. 6.

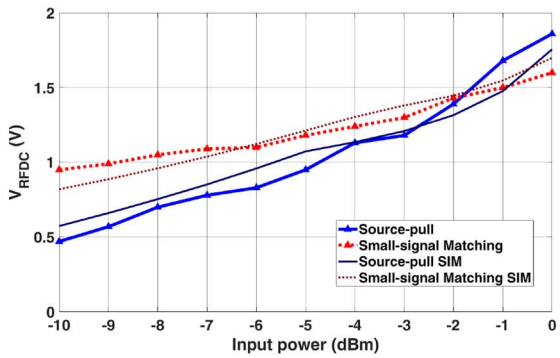
IV. Experimental Validation of the Batteryless Transponder Design Principles

In this section we provide the results of an experimental validation of the analysis and design principles for the batteryless transponder operating at 5.8 GHz which is suitable for vehicular communications; it considers both the down-link and the up-link communications. The down-link is dominated by the energy harvesting capability and specifically the charging time and the transponder latency to answer to an interrogation, while the second is discussed in terms of the back-scattering capability.

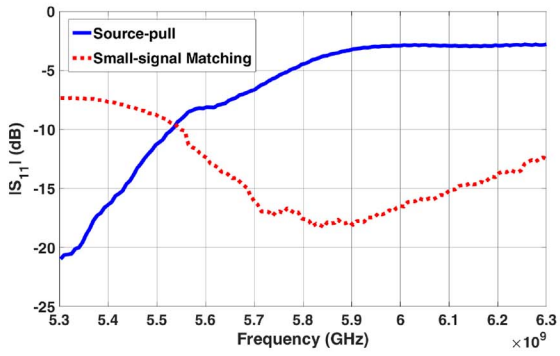
The experiments are provided for both the conducted and radiated operative conditions.



(a) Measured and simulated Charge Current I_{CHG}, versus P_{RF}.



(b) Measured and simulated open-circuit output voltage V_{RFDC}, versus P_{RF}.



(c) Measured S_{11}, versus frequency.

Fig. 14. Measured and simulated electrical parameters for source-pull and small-signal matching PCBs at various input power levels.

A. Energy Harvesting Mode

The evaluation of the performance of the energy harvester block was carried out by a set of measurements employing two different samples, each one equipped with coaxial RF connectors but without the EEPROM installed. One PCB follows the design in Fig. 6, while the other implements the small-signal conjugate matching network. It is worth to note that this lead to the design of two different circuits, differentiated only by the matching network between the antenna section and the RF-DC converter. This approach allows to assess the performance improvements due to the source-pull optimization, with respect to the conventional impedance matching. Tee Fig. 14(b) shows the comparison between measured and simulated charge current I_{CHG}, and the open-circuit DC output voltage V_{RFDC}. The

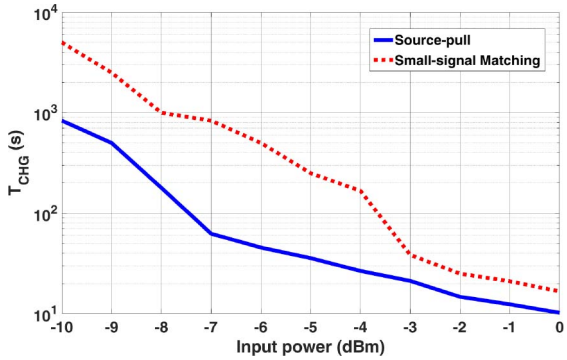
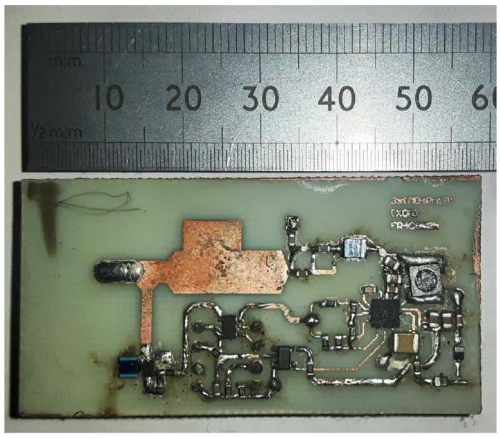


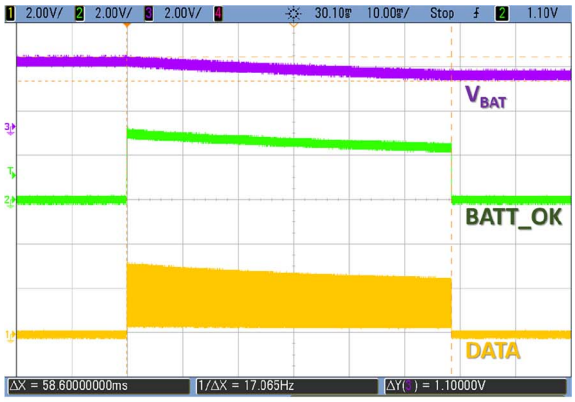
Fig. 15. Measured charging time ΔT_{CHG} for source-pull and small-signal matched PCBs, versus P_{RF}.



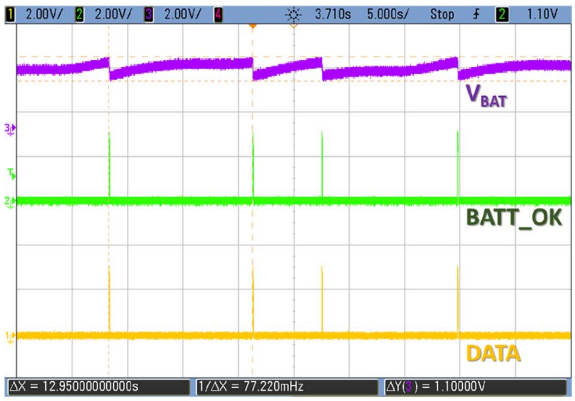
(a) Front Side

(b) Back Side

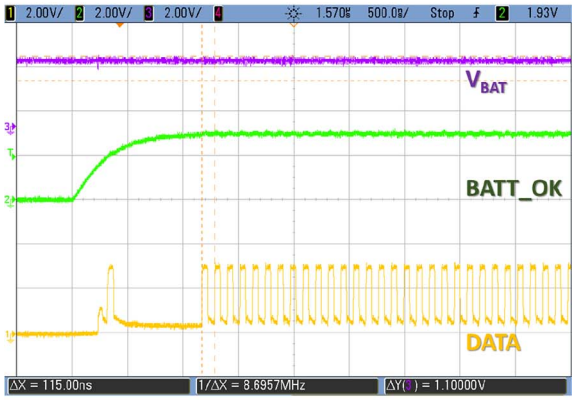
Fig. 16. Photograph of complete 5.8 GHz batteryless transponder prototype.



(a) Single Packet Transmission



(b) Cyclic Packet Transmission



(c) Transient at beginning of transmitted packet

Fig. 17. Oscilloscope traces acquired with $P_{RF} = -5$ dBm.

same figure reports also the comparison between the measured reflection coefficient S_{11} for the two implementations.

It is noteworthy that the source-pull PCB shows a lower matching with respect to the impedance matching implementation (as discussed in Section III-A), nevertheless exhibits a power conversion efficiency that is higher by about a factor of six. This has a great impact on the transponder communication capability, as it allows dramatically decreasing the charging time (Fig. 15). Note that for an RF input power of -5 dBm, the charging time is consistent with what was estimated in Section III-B, applying (2) and (15).

B. Back-Scattering Mode

We now analyze the transponder up-link capability, by considering the back-scattering modulation parameters in the context of batteryless operation. For this purpose the batteryless transponder prototype was integrated with a dielectric cost-effective linear-polarized COTS antenna (Taoglas WLP-12C, [42]) which exhibits an antenna gain of $G_{TAG} = 6$ dB. The picture of the complete transponder prototype is shown in Fig. 16.

The Fig. 17(c) shows the oscilloscope traces about the transmission process after the first cold-start of the system, that is, when $V_{BAT} = 0V$, with an input power level of -5 dBm. During the cold-start, the energy storage capacitor must be totally filled to reach the $V_{BAT\max}$ ready voltage, so the latency for the first query answer is the longest during the communications cycle and such duration is equal to the charging time

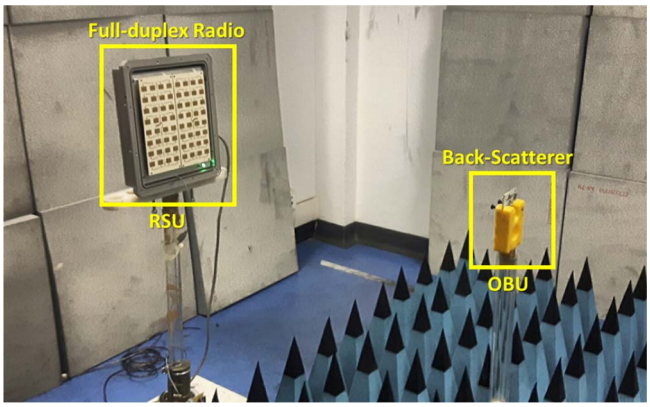


Fig. 18. Vehicular DSRC characterization setup.

ΔT_{CHG} measured in Fig. 15. The duration of the transmission window is shown in Fig. 17(a); after enabling the transmission, determined by the level of *BATT_OK*, the packet stored in the memory is sent to the modulator in the meantime, the voltage at the capacitor C_{BAT} decreases to a given threshold and then the transmission enabling goes down. Fig. 17(c)a shows that the transmission time window lasts 58 ms which is comparable with the estimation given in (52). Successive requests exhibits an increase in the packet rate and a recharge time less than ΔT_{CHG}, as shown in Fig. 17(c)b. The recharge time is not constant, because during transmission, the node is able to continue the harvesting process during the "s_0" low symbol states, as described in Section III-A. Fig. 17(b) shows in detail the header of the transmitted packet; we can clearly see a spurious transient before the beginning of the transmission due to the setting of the switch between the memory and modulator, and the payload represented by a sequence of bits at approximately 8.7 MHz.

C. Vehicular DSRC Characterization

In view of the possible exploitation of the developed battery-less transponder in vehicular DSRC, hereinafter we discuss its capability to establish both the down-link and up-link with a legacy reader for this specific application. For this purpose, we adopted a roadside unit (RSU) that fulfills the ETSI ES 200-674 standard requirements for electronic toll collection, [17]. This testing RSU provides an EIRP of 37 dBm at 5.8 GHz, and its digital-IF receiver is equipped with two 16-bit ADCs working at a sampling rate of 78.125 MHz. The experimental setup was arranged in a semi-anechoic chamber, with the RSU and the back-scatterer prototype of Fig. 16 on line of sight (see Fig. 18); both units were oriented in their direction of maximum radiation, with the antenna matched in polarization, and placed at different distances.

In down-link mode, the received transponder RF power can be estimated by the following linear-scale link budget, [32],

$$P_{RF} = \frac{EIRP\, G_{TAG}\, \lambda^2}{(4\pi r)^2 \Theta\, B\, F} \xi \left(1 - |\Gamma_{B0}|^2\right) \tag{61}$$

where λ is the wavelength of the radiated signal and r the reader-to-transponder distance. The (61) includes also other parameters that can be set to unity in the following experiments, these are: ξ the polarization mismatch, Θ the antenna gain penalty, B the path blockage, and F the fade margin. In (61) the mismatch loss term can't be neglected and from Fig. 14(a) it is estimated in -1.5 dB. On this latter aspect, by (61) results that poor impedance matching would lead to high value of Γ_B, and thus reducing the received transponder RF power P_{RF}. Nevertheless, the proposed source pull method is aimed at increasing the overall P_{RFDC} DC power supplied to the DC/DC converter thus the goal, applying the (12), results

$$P_{RFDC} = \eta_{RFDC} P_{RF} \propto \left(1 - |\Gamma_{B0}|^2\right) \eta_{RFDC}. \tag{62}$$

From (62) we can conclude that the source pull optimization finds the better design parameters for which Γ_B and η_{RFDC} lead to the maximum DC power supplied to the DC/DC converter, thus increasing the I_{CHG} charge current (13).

TABLE I
MEASURED RADIATED TRANSPONDER CHARGING CURRENT AND CHARGING TIME

Distance (m)	Estimated Incident Power (dBm)	Charge Current I_{CHG} (uA)	Charging Time ΔT_{CHG} (s)
0.30	5.74	714	7
0.60	0.28	358	14
0.90	-3.80	167	30
1.05	-5.14	135	37
1.20	-6.30	111	45
1.50	-8.24	50	100

In Table I we list the charge current, I_{CHG}, and the corresponding charging times ΔT_{CHG} at various distances; the estimated RF power at the transponder input section was estimated by (61).

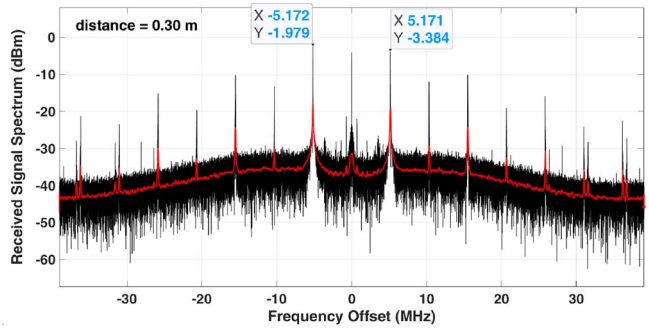
The ratios between the charge times and the estimated input powers comply with the conducted power measurements shown in Fig. 15, thus confirming the coherence of the data between the radiated and conducted measurements.

To verify the modulation index, we considered the base band signal received by the RSU receiver, during the sequence of down- and up-link data packet exchanges. The base-band signal spectrum of the back-scatterer up-link and the corresponding symbol constellation in the complex IQ plane are shown in Figs. 19–20.

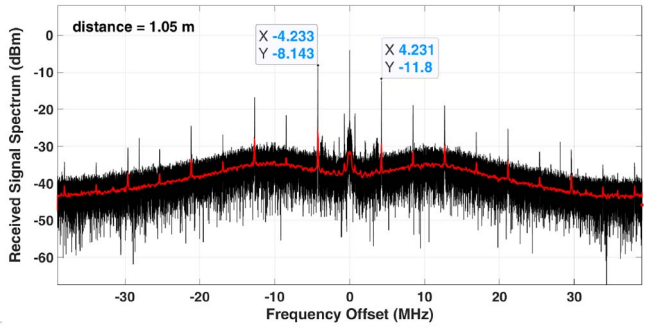
In up-link mode the RSU's received modulated back-scattered power, consistently with (61) is given by the following

$$P_{RX} = \frac{EIRP\, G_{RSU} G_{TAG}^2\, \lambda^4}{4(4\pi r)^4 \Theta^2\, B^2\, F} \xi^2 |\Gamma_{B0}|^2 |\mathrm{m} - 1|^2 \tag{63}$$

where, $|\Gamma_{B0}| = 0.32$, $\mathrm{m} = 2.5 \angle 0.52\pi$ and $G_{RSU} = 17\ dB$, while the remaining parameters are those already definite in (61). The Fig. 19 shows the corresponding referred to the RSU antenna connector section, for the two RSU-transponder distances of $0.3\,m$ and $1.05\,m$. For this purpose, we calibrated the RSU chain gain and the FFT scaling using a 0 dBm calibration tone at 1 MHz. It is possible to show that the data are consistent with the (63). The transponder back-scatters the RSU carrier impressing a PSK modulation. The RSU spectra clearly show that the 5.8 GHz carrier, removed by the zero-IF RSU receiver and DC filter in the RSU receive chain, is modulated by a square wave with a 2-PSK modulation scheme.



(a) Back-Scatterer at 0.30 m



(b) Back-Scatterer at 1.05 m

Fig. 19. Spectra of received radio messages.

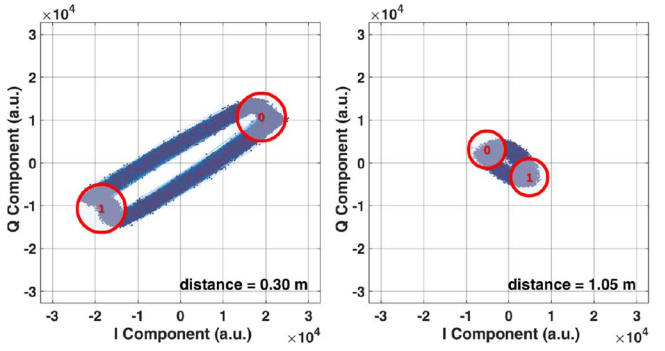


Fig. 20. DC filtered 16-bit quantized IQ plane representation of received radio messages with symbol constellation map.

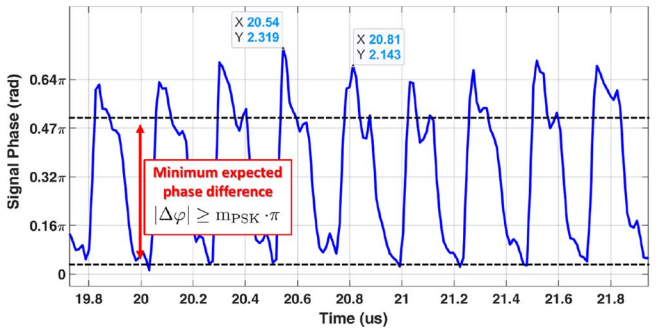


Fig. 21. Phase of received signal without DC filtering at a distance of 1.05 m.

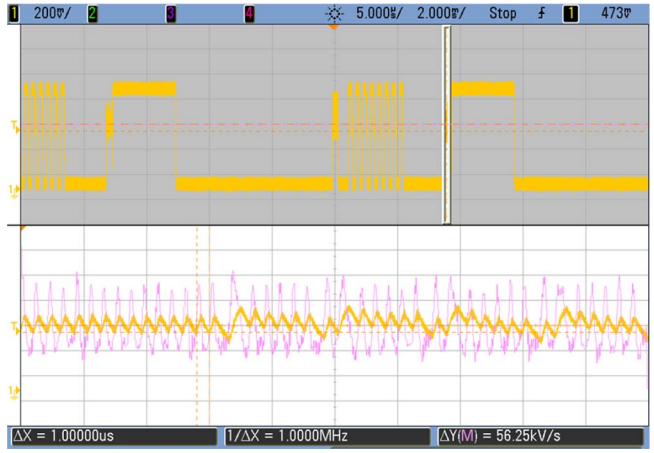


Fig. 22. Down-link detected signal at the transponder V_{RFDC} node with an incident power level of -5 dBm at the RF_{input} node (see Fig. 6).

The spectra show a square wave characteristic frequency of about 5 MHz, comparable with the measurements plotted in Fig. 17(c), the slight difference is to be attributed to the EEPROM data bit-rate drift given by voltage supply decrease. The associated ASK modulation can be observed evaluating the received signal phase, shown in Fig. 21: note that dealing with a varying complex back-scattering reflection coefficient, the resulting modulation comprises both modulation schemes, having expected modulation indexes as indicated in (60).

It is worth noting that, on comparing Fig. 17(c) and the spectra in Fig. 19, the EEPROM seems to generate a data stream with different f_{CLK} clock frequencies. This is consistent with the characteristics of EEPROM as depicted in [22] where the internally generated clock frequency is described as being dependent on the actual EEPROM supply voltage. As shown in Fig. 17(c), the V_{BAT} supply voltage constantly decreases during communication due to the discharge of the capacitor C_{BAT}, thus leading to a decreasing symbol frequency throughout the communication window. Such a drawback can be overcome by applying a data coding scheme (e.g., Manchester or NRZI coding) or including a voltage regulator before the EEPROM supply input.

The Fig. 20 shows on IQ plots of the RSU received signal for the two corresponding RSU-transponder distances, at a highly oversampled acquisition of the phase plane (with a sample rate of 78.125 Msps): from the plots the corresponding two symbols are clearly detectable. Note that scattered points on IQ plots are not grouped in two symbol groups due to narrow band filtering applied on receive chain, which softens level transitions on modulated signal but decreases overall noise level. Nevertheless, a synchronous sampling can easily reconstruct the 2-PSK symbols

From these plots we can observe that there is a significant margin of detection up to more than 1 m. In particular, from Fig. 21, we observe an achieved 2-PSK modulation depth in excess of 0.6 at a distance of 1.05 m.

Finally, we report the test of the transponder receiving properties in down-link, by considering the standard down-link signal in real vehicular DSRC operation conditions. According to [17], this is composed of a 8 pulse at the rate of 9.6 KHz, adopted to wake-up the OBU, to which follows the payload data at the rate of 921,6 kbps. In Fig. 22, we show the time domain waveform acquired at the output of the RF-DC converter, thus representing the V_{RFDC} node of the circuit represented in Fig. 6; the test was conducted with an estimated

TABLE II
HARVESTING PERFORMANCES AT COMPARISON WITH THE STATE-OF-THE-ART

Design	Harvesting Load and Conditions	Measured P_{DC} (μW)	η	I_{CHG}; ΔT_{CHG}
[43]	DC/DC, Current Sink 868 MHz, -5 dBm	-	-	-; 2.5 s
[4]	100 Ω, fixed load 2.4 GHz, -5 dBm	40.1	13%	118 μA; -
[2]	3000 Ω, fixed load 5.8 GHz, -5 dBm	72.7	23%	145 μA; -
[2]	DC/DC, Current Sink 5.8 GHz, 1 dBm	-	-	-; 140 s
This work	DC/DC, Current Sink 5.8 GHz, -5 dBm	51.0	16%	135 μA; 37 s
This work	DC/DC, Current Sink 5.8 GHz, -8 dBm	17.0	11%	50 μA; 100 s

incident power level at the RF_{input} of -5 dBm. The picture in the lower section reports an expanded vision of the time-basis by which it is observable the detected signal and its post-process version by a derivative operator to make more distinguishable the signal. The post processed signal get the amplitude of about 600 mV, and permits to observe the 7E hexadecimal code. Although the post processing was not included in the transponder prototype, we can assess that a 16-bit general purpose micro-controller could effectively accomplish the task of the receiver signal acquisition and detection.

V. CONCLUSION

This article has analyzed the design principles of a battery-less transponder suited for the implementation of vehicular DSRC physical layers operating at 5.8 GHz. We have analyzed the optimum design of the matching network with respect to the speed of charging, the optimum design of the modulation block capable of preserving harvesting capabilities and, for either ASK or 2-PSK, providing optimized back-scattering properties. The experimental validation of the design principles was carried out by conducted and radiated measurements, the latter by considering a legacy RSU developed for vehicular DSRC at 5.8 GHz.

Table II summarizes the results achieved for the harvesting stage compared with the available state-of-the-art.

From the table we can observe that only [4] describes a complete system based on COTS devices, but working in the 2.4 GHz ISM band and using two different antennas for harvesting and back-scattering, while similar literature for devices compliant with vehicular communication specifications are not available. While at the frequency of 5.8 GHz the literature reports the work in [2], that performs comparably to the present work but misses of data related to the back-scattering functions.

It is noteworthy that this work considers a digital section based on not power-optimized and not low-voltage COTS devices. The (50) establishes that the equivalent impedance of the actual implemented EEPROM results to be very low, in order of hundreds of ohms, while needing a voltage supply of $V_{DC} = 3.3$ V leading to high currents compared to supplied currents by RF rectifier.

Note that the device proposed in [2] implements a digital section, which requires an overall power of 559 μW. The present work has implemented an EEPROM device with a power requirement of 16.5 mW [22], about 30 times higher compared to power provided by [2], By this, the resulting operating time window width of [2] is increased, while the charge process is not dependent on the power requirements of the digital section stage.

Following this approach, the comparison with [4] might appear not completely consistent because such work does not consider the power requirements of a necessary digital section. Nevertheless, to the knowledge of the authors in literature only these two works resemble the concept of building a totally battery-less system based on COTS devices, operating above the UHF band. The Table II includes for comparison also a WISP based device, namely reported in [43]; it is based on an MSP430 low-power microprocessor requiring less than 1 mW of supply power. It implements a 98 uF storage capacitor and each data packet carries only up to 28 bits at 436 kbps, very far below the packet size of 256 kbits transmitted at 8 Mbps by the device proposed in this work. In [16] the authors clearly point how the WISP analog front-end, as implemented in [43], [44] and further works, actually shows poor performances when implemented in systems operating above the UHF band. Considering the results shown in Table II, this work provides design principles allowing to overcome several actual limitations in developing WISP-like devices on higher ISM bands.

REFERENCES

[1] A. Cidronali, S. Maddio, M. Passafiume, and G. Manes, "Car talk: Technologies for vehicle-to-roadside communications," *IEEE Microw. Mag.*, vol. 17, no. 11, pp. 40–60, Oct. 2016.
[2] C. Qi *et al.*, "A 5.8 GHz energy harvesting tag for sensing applications in space," in *Proc. 6th IEEE Int. Conf. Wireless Space Extreme Environ. (WiSEE)*, 2018, pp. 218–223.
[3] C. Grey and J. Tarascon, "Sustainability and *in situ* monitoring in battery development," *Nat. Mater.*, vol. 16, no. 1, p. 45, 2017.
[4] H. J. Visser and R. J. Vullers, "RF energy harvesting and transport for wireless sensor network applications: Principles and requirements," *Proc. IEEE*, vol. 101, no. 6, pp. 1410–1423, Apr. 2013.
[5] G. Manes *et al.*, "Realtime gas emission monitoring at hazardous sites using a distributed point-source sensing infrastructure," *Sensors*, vol. 16, no. 1, p. 121, 2016.
[6] A. Cidronali *et al.*, "MMIC applications of heterostructure interband tunnel devices," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 4, pp. 1351–1367, 2003.
[7] A. Cidronali *et al.*, "Ultralow DC power VCO based on InP-HEMT and heterojunction interband tunnel diode for wireless applications," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 12, pp. 2938–2946, Dec. 2002.
[8] R. K. Krishnamurthy and H. Kaul, "Ultra-low voltage technologies for energy-efficient special-purpose hardware accelerators," *Intel Technol. J.*, vol. 13, no. 4, pp. 102–117, 2009.
[9] R. M. Ferdous, A. W. Reza, and M. F. Siddiqui, "Renewable energy harvesting for wireless sensors using passive RFID tag technology: A review," *Renew. Sustain. Energy Rev.*, vol. 58, pp. 1114–1128, May 2016.
[10] M. Cansiz, D. Altinel, and G. K. Kurt, "Efficiency in RF energy harvesting systems: A comprehensive review," *Energy*, vol. 174, pp. 292–309, May 2019.
[11] T. Kavitha and S. Silas, "A survey on energy harvesting routing protocol for WSN," in *Proc. IEEE 3rd Int. Conf. Trends Electron. Informat. (ICOEI)*, 2019, pp. 572–575.
[12] M. Passafiume, S. Maddio, and A. Cidronali, "An improved approach for RSSI-based only calibration-free real-time indoor localization on IEEE 802.11 and 802.15. 4 wireless networks," *Sensors*, vol. 17, no. 4, p. 717, 2017.
[13] A. Okba, A. Takacs, and H. Aubert, "Compact rectennas for ultra-low-power wireless transmission applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 5, pp. 1697–1707, Mar. 2019.

[14] A. Okba, D. Henry, A. Takacs, and H. Aubert, "Autonomous RFID sensor node using a single ISM band for both wireless power transfer and data communication," *Sensors*, vol. 19, no. 15, p. 3330, 2019.
[15] A. P. Sample, D. J. Yeager, P. S. Powledge, A. V. Mamishev, and J. R. Smith, "Design of an RFID-based battery-free programmable sensing platform," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 11, pp. 2608–2615, Nov. 2008.
[16] C. Xu and P. Zhang, "Open-source software and hardware platforms for building backscatter systems," *Mobile Comput. Commun.*, vol. 23, no. 1, pp. 16–20, 2019.
[17] *V2.4.1 (Part 1): Intelligent Transport Systems (ITS); Road Transport and Traffic Telematics (RTTT); Dedicated Short Range Communications (DSRC)*, ETSI Standard ES 200 674-1, May 2013.
[18] *V2.1.1 Transport and Traffic Telematics (TTT); Dedicated Short Range Communication (DSRC) Transmission Equipment (500 Kbit/s/250 kbit/s) Operating in the 5795 MHz to 5815 MHz Frequency Band*, ETSI Standard EN 300 674-2-2, Nov. 2016.
[19] *Intelligent Transport Systems (ITS); Vehicular Communications; Basic Set of Applications; Definitions*, ETSI Standard 102 638, Jun. 2009.
[20] P. Kaur, B. Sohi, and P. Singh, "Recent advances in MAC protocols for the energy harvesting based WSN: A comprehensive review," *Wireless Pers. Commun.*, vol. 104, no. 1, pp. 423–440, 2019.
[21] L. M. Borges, R. Chávez-Santiago, N. Barroca, F. J. Velez, and I. Balasingham, "Radio-frequency energy harvesting for wearable sensors," *Healthcare Technol. Lett.*, vol. 2, no. 1, pp. 22–27, 2015.
[22] *AT17LV512A-10PU EEPROM Datasheet (DocID:102014). Microchip Technology, Inc. Chandler, Arizona, United States*. Accessed: 2020. [Online]. Available: https://www.microchip.com/
[23] *CC2530 Datasheet (DOCID:SWRS081B). Texas Instruments, Inc. Texas, United States*. Accessed: 2020. [Online]. Available: http://www.ti.com/
[24] M. Passafiume, G. Collodi, and A. Cidronali, "Optimum design of low energy harvesting detector at 5.8 GHz suitable for COTS devices," in *Proc. IEEE Int. Conf. RFID Technol. Appl. (RFID-TA)*, 2019, pp. 6–10.
[25] *BQ25570 DC/DC Converter Datasheet (DocID:SLUSBH2E). Texas Instruments, Inc. Texas, United States*. Accessed: 2020. [Online]. Available: http://www.ti.com/
[26] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," *IEEE Trans. Circuits Syst.*, vol. CS-24, no. 10, pp. 517–530, Oct. 1977.
[27] F. L. Luo and H. Ye, *Advanced DC/DC Converters*. Hoboken, NJ, USA: CRC Press, 2016.
[28] A. Cidronali, S. Maddio, G. Collodi, and G. Manes, "Design trade-off for a compact 5.8 GHz DSRC transponder front-end," *Microw. Opt. Technol. Lett.*, vol. 57, no. 5, pp. 1187–1191, 2015.
[29] A. S. Boaventura, A. R. Testera, N. B. Carvalho, and M. F. Barciela, "Using X-parameters to model diode-based RF power probes," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2011, pp. 1–4.
[30] A. J. Boaventura and N. B. Carvalho, "Using X-parameters to model RFID energy harvesting circuits," in *Proc. IEEE 5th Eur. Conf. Antennas Propag. (EUCAP)*, 2011, pp. 2819–2822.
[31] A. Cidronali, K. Gupta, J. Jargon, K. Remley, D. DeGroot, and G. Manes, "Extraction of conversion matrices for P-HEMTs based on vectorial large-signal measurements," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2, 2003, pp. 777–780.
[32] J. D. Griffin and G. D. Durgin, "Complete link budgets for backscatter-radio and RFID systems," *IEEE Antennas Propag. Mag.*, vol. 51, no. 2, pp. 11–25, Apr. 2009.
[33] C. Boyer and S. Roy, "Backscatter communication and RFID: Coding, energy, and MIMO analysis," *IEEE Trans. Commun.*, vol. 62, no. 3, pp. 770–785, Dec. 2013.
[34] E. McCune, *Practical Digital Wireless Signals*. Cambridge, U.K.: Cambridge Univ. Press, 2010.
[35] J. G. Proakis, M. Salehi, N. Zhou, and X. Li, *Communication Systems Engineering*, vol. 2. Upper Saddle River, NJ, USA: Prentice-Hall, 1994.
[36] J. Dobrowolski, *Microwave Network Design Using the Scattering Matrix*. London, U.K.: Artech House, 2010.
[37] N. A. Eltresy *et al.*, "RF energy harvesting IoT system for museum ambience control with deep learning," *Sensors*, vol. 19, no. 20, p. 4465, 2019.
[38] *BAT15–03W Schottky Diode Datasheet. Infineon Technologies AG. Germany, Europe*. Accessed: 2020. [Online]. Available: https://www.infineon.com/cms/en/product/rf-wireless-control/rf-diode/rf-mixer-and-detector-schottky-diode/bat15-03w/
[39] *SMS7630-061 Zero-Bias Schottky Detector Diode Datasheet. Texas Instruments, Inc. Texas, United States*. Accessed: 2020. [Online]. Available: https://www.skyworksinc.com/products/diodes/sms7630-061
[40] *NC7SZ66 Low Voltage Single SPST Normally Open Bus Switch Datasheet*. Accessed: 2020. [Online]. Available: https://www.onsemi.com/products/interfaces/analog-switches/nc7sz66
[41] *ATF-58143 Low Noise Enhancement Mode Pseudomorphic HEMT. Broadcom Inc. San Jose, California, United States*. [Online]. Available: https://docs.broadcom.com/docs/AV02-0672EN
[42] *Taoglas WLP.4958.12.4.A.02 4900-5825MHz 12 * 11.8 * 4 mm Patch Antenna. Taoglas. Ireland, Europe*. Accessed: 2020. [Online]. Available: https://www.taoglas.com/product/wlp-4958-12-4-a-02-49005825mhz-patch-antenna-12mm/
[43] D. Fabbri, E. Berthet-Bondet, D. Masotti, A. Costanzo, D. Dardari, and A. Romani, "Long range battery-less UHF-RFID platform for sensor applications," in *Proc. IEEE Int. Conf. RFID Technol. Appl. (RFID-TA)*, 2019, pp. 80–85.
[44] S. J. Thomas, "RFID for everyone: Design of an easily-accessible, experimental UHF RFID platform," in *Proc. IEEE Int. Conf. RFID (RFID)*, 2019, pp. 1–6.

Marco Passafiume (Member, IEEE) was born in Florence, Italy, in February 6, 1987. He received the Laurea and Ph.D. degrees in electronic engineering (*cum laude*) from the University of Florence, Italy, in 2012, where he is working with the Microelectronics and HF Research Group. His research activities covers developing of software defined radios and digital systems for communication (also working with private institutes, like Autostrade Tech., for development of new info-mobility systems), highly integrated SoC/SiP and human interface devices. Actually he is studying deeply new development technologies based on FPGA and he covers in depth various aspects related to computer science evolution and digital communications/software defined radios. His scientific interests also cover the area of data elaboration methodologies, with particular attention to algorithmic development.

Giovanni Collodi (Member, IEEE) was born in Florence, Italy, in 1966. He received the M.S. (Hons.) degree in electronic engineering and Ph.D. degree in computer science and telecommunication engineering from the University of Florence, Florence, in 1996 and 2002, respectively. His doctoral work focused on MMIC circuit design and device modeling. From 2001 to 2004, he was a Postdoctoral Researcher with the Arcetri Astrophysical Observatory, where he was involved in the ATACAMA large millimeter array radio telescope project (integrated circuit design) and Department of Information Engineering, University of Florence. In 2002, he was a Visiting Researcher with the Physical Sciences Research Lab Motorola, Tempe, AZ, USA, and he was a Contract Professor of electronics with the University of Florence. In 2005, he was an Assistant Professor with the Department of Information Engineering, University of Florence, where he was involved in developing systems for wireless applications. In 2006, he began his involvement also with the Interdepartmental Centre Technology and Microsystems for Quality and Environmental Safety. Since 2007, he has been teaching a course on technology and systems for wireless application. In 2015, started teaching a second course on high frequency electronic microsystem. His current research interests include the development of microwave systems and circuit with a particular emphasis on MMIC.

Alessandro Cidronali (Senior Member, IEEE) received the Laurea and Ph.D. degrees in electronics engineering from the University of Florence, Florence, Italy, in 1992 and 1997, respectively, where he was an Assistant Professor with the Department of Electronics and Telecommunications, from 1999 to 2011. From 1999 to 2003, he was a Visiting Researcher with the Motorola Physics Science Research Laboratory. From 2002 to 2005, he was a Guest Researcher with the Non-Linear Device Characterization Group, Electromagnetic Division, National Institute of Standards and Technology. Under the frame of the IST-EU FP6 Network TARGET (IST-1-507893-NOE), he served as Workpackage Leader for the transmitters modeling/architectures for wireless broadband access work packages. He is currently an Associate Professor with the Department of Information Engineering, University of Florence, where he teaches courses on electron devices and integrated microwave circuits. His research activities concern the study of analysis and synthesis methods for nonlinear microwave circuits, the design of broadband microwave integrated circuits and the development of computer-aided design modeling for microwave devices and circuits. He was a recipient of the Best Paper Award presented at the 61st ARFTG Conference, and the IEEE MIcrowave Magazine 2016 Best Paper Award. From 2004 to 2006, he was an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is currently a member of IEEE Microwave Theory and Techniques Society TC-20 Wireless Communications and TC-27 Vehicular Technologies and Communications.