Instruction Encodings

INSTRUCTION	32-BIT ENCODING																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOVE INSTRUCTIONS	**Opcode (4b)**				**Op (5b)**					**Cond (3b)**			**4b**				**16b**															
MOV rA k	0	0	0	1	0	0	0	0	0	0	0	0	r	A			0	0	0	0	0	0	0	0	k							
MOVE rA k	0	0	0	1	0	0	0	0	0	0	0	1	r	A			0	0	0	0	0	0	0	0	k							
MOVNE rA k	0	0	0	1	0	0	0	0	0	0	1	0	r	A			0	0	0	0	0	0	0	0	k							
MOVC rA k	0	0	0	1	0	0	0	0	0	0	1	1	r	A			0	0	0	0	0	0	0	0	k							
MOVNC rA k	0	0	0	1	0	0	0	0	0	1	0	0	r	A			0	0	0	0	0	0	0	0	k							
MOVL rA k	0	0	0	1	0	0	0	0	0	1	0	1	r	A			0	0	0	0	0	0	0	0	k							
MOVG rA k	0	0	0	1	0	0	0	0	0	1	1	0	r	A			0	0	0	0	0	0	0	0	k							
MOV rA rB	0	0	0	1	1	0	0	0	0	0	0	0	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVE rA rB	0	0	0	1	1	0	0	0	0	0	0	1	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVNE rA rB	0	0	0	1	1	0	0	0	0	0	1	0	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVC rA rB	0	0	0	1	1	0	0	0	0	0	1	1	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVNC rA rB	0	0	0	1	1	0	0	0	0	1	0	0	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVL rA rB	0	0	0	1	1	0	0	0	0	1	0	1	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
MOVG rA rB	0	0	0	1	1	0	0	0	0	1	1	0	r	A			r	B			0	0	0	0	0	0	0	0	0	0	0	0
ALU INSTRUCTIONS	**Opcode (4b)**				**Op (5b)**					**WB (2b)**		**Carry (1b)**	**4b**				**16b**															
ADD rA k	0	0	1	0	0	0	0	0	0	0	1	0	r	A			0	0	0	0	0	0	0	0	k							
ADDC rA k	0	0	1	0	0	0	0	0	1	0	1	1	r	A			0	0	0	0	0	0	0	0	k							
AND rA k	0	0	1	0	0	0	0	1	0	0	1	0	r	A			0	0	0	0	0	0	0	0	k							
CMP rA k	0	0	1	0	0	0	0	1	1	0	0	0	r	A			0	0	0	0	0	0	0	0	k							
MVN rA k	0	0	1	0	0	0	1	0	0	0	1	0	r	A			0	0	0	0	0	0	0	0	k							

NOT rA k	0 0 1 0	0 0 1 0 1	0 1	0	rA	0 0 0 0 0 0 0 0	k
OR rA k	0 0 1 0	0 0 1 1 0	0 1	0	rA	0 0 0 0 0 0 0 0	k
SUB rA k	0 0 1 0	0 0 1 1 1	0 1	0	rA	0 0 0 0 0 0 0 0	k
SUBC rA k	0 0 1 0	0 1 0 0 0	0 1	1	rA	0 0 0 0 0 0 0 0	k
TEST rA k	0 0 1 0	0 1 0 0 1	0 0	0	rA	0 0 0 0 0 0 0 0	k
XOR rA k	0 0 1 0	0 1 0 1 0	0 1	0	rA	0 0 0 0 0 0 0 0	k
ADD rA rB	0 0 1 0	1 0 0 0 0	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
ADDC rA rB	0 0 1 0	1 0 0 0 1	0 1	1	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
AND rA rB	0 0 1 0	1 0 0 1 0	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
CMP rA rB	0 0 1 0	1 0 0 1 1	0 0	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
MVN rA rB	0 0 1 0	1 0 1 0 0	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
NOT rA rB	0 0 1 0	1 0 1 0 1	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
OR rA rB	0 0 1 0	1 0 1 1 0	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
SUB rA rB	0 0 1 0	1 0 1 1 1	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
SUBC rA rB	0 0 1 0	1 1 0 0 0	0 1	1	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
TEST rA rB	0 0 1 0	1 1 0 0 1	0 0	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
XOR rA rB	0 0 1 0	1 1 0 1 0	0 1	0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
SL0 rA	0 0 1 0	1 1 0 1 1	0 1	0	rA	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
SL1 rA	0 0 1 0	1 1 1 0 0	0 1	0	rA	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
SR0 rA	0 0 1 0	1 1 1 0 1	0 1	0	rA	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
SR1 rA	0 0 1 0	1 1 1 1 0	0 1	0	rA	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
BRANCHING INSTRUCTIONS	**Opcode (4b)**	**Op (5b)**	**Cond (3b)**		**4b**	**16b**	
JMP k	0 0 1 1	0 0 0 0 0	0 0 0		0 0 0 0	0 0 0 0 0 0 0 0	k
JE k	0 0 1 1	0 0 0 0 0	0 0 1		0 0 0 0	0 0 0 0 0 0 0 0	k
JNE k	0 0 1 1	0 0 0 0 0	0 1 0		0 0 0 0	0 0 0 0 0 0 0 0	k
JL k	0 0 1 1	0 0 0 0 0	1 0 1		0 0 0 0	0 0 0 0 0 0 0 0	k

JG k	0 0 1 1	0 0 0 0 0	1 1 0	0 0 0 0	0 0 0 0 0 0 0 0	k
CALL k	0 1 1 0	0 0 0 0 0	0 0 0	0 0 0 0	0 0 0 0 0 0 0 0	k
MEMORY INSTRUCTIONS	**Opcode (4b)**	**Op (5b)**	**Cond (3b)**	**4b**	**16b**	
FETCH rA k	1 0 1	0 0 0 0 1	0 0 0	rA	0 0 0 0 0 0 0 0	k
STORE rA k	1 0 1	0 0 0 1 0	0 0 0	rA	0 0 0 0 0 0 0 0	k
FETCH rA rB	1 0 1	1 0 0 0 1	0 0 0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
STORE rA rB	1 0 1	1 0 0 1 0	0 0 0	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
SPECIAL INSTRUCTIONS	**Opcode (4b)**	**Op (5b)**	**Cond (3b)**	**4b**	**16b**	
HALT	1 1 1	0 0 0 0 0	0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
NOP	0 0 0	0 0 0 0 0	0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
RETURN	0 1 1 0	0 0 0 0 1	0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	