Theory of operation for MAX14662 analog switch array

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Description

The MAX14662 is a serially controlled 8 x SPST switch for general purpose signal switching applications. …This part features Beyond-The-Rails™capability so that ±5.5V signals can be passed with any single supply between +1.6V and +5.5V.The serial control is selectable between I2C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. …The SPI mode includes a DOUT pin that can be used to chain multiple devices together with a single select signal.

-From the datasheet for the MAX14662

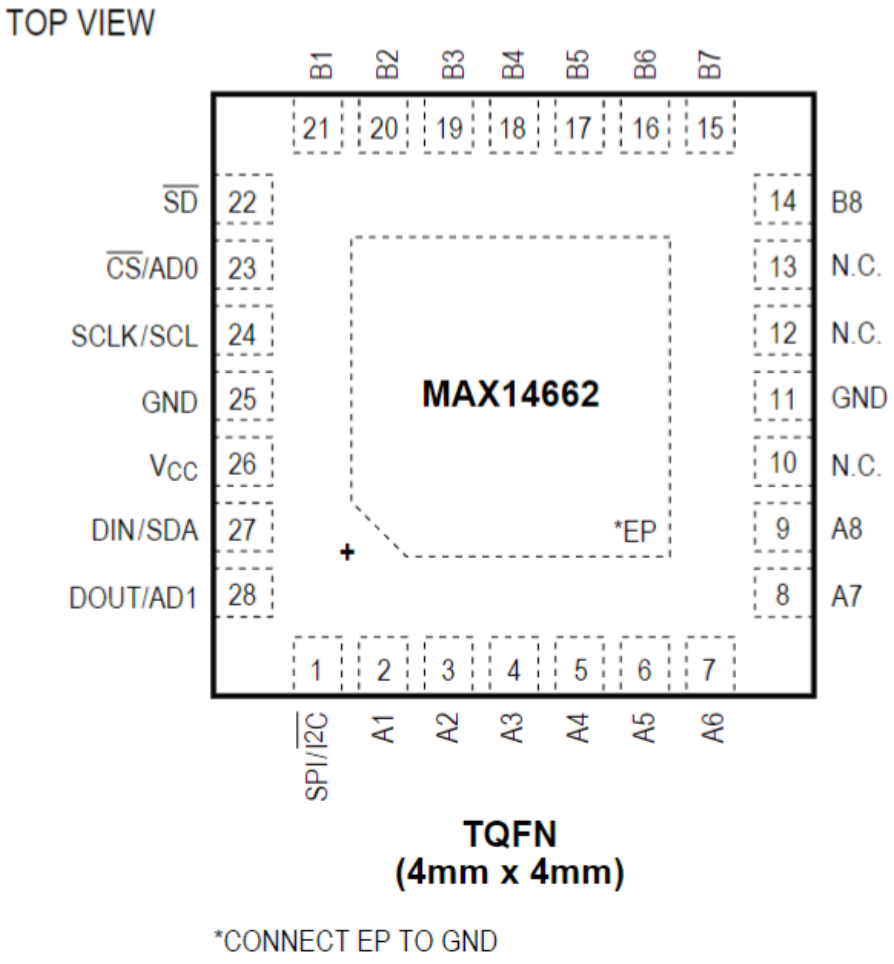

Figure 1: Pinout of MAX14662

Basic Operation

The MAX14662 is being used to replace the mechanical switches present in the original amplifier. Each switch module contains 8 independent switches, with inputs A1-A8 and outputs B1-B8. A1 corresponds to B1, A2 to B2, etc. 4 switch modules, totaling 32 individual switches,

are used, but switches 6,7,and 8 of switch module 4 are not used. The switches are controlled via SPI; to reduce controller I/O requirements, the switches are set up in a chain configuration, so that 3 wires from the controller are sufficient to control all switches. The Clock and ~Chip Select signals are connected to all switches in parallel, and the Data signal is connected to the DIN/SDA pin of the first switch, and that switch's DOUT/AD1 pin is connected to the DIN/SDA pin of the second switch, and so on, as seen in Figure 2.

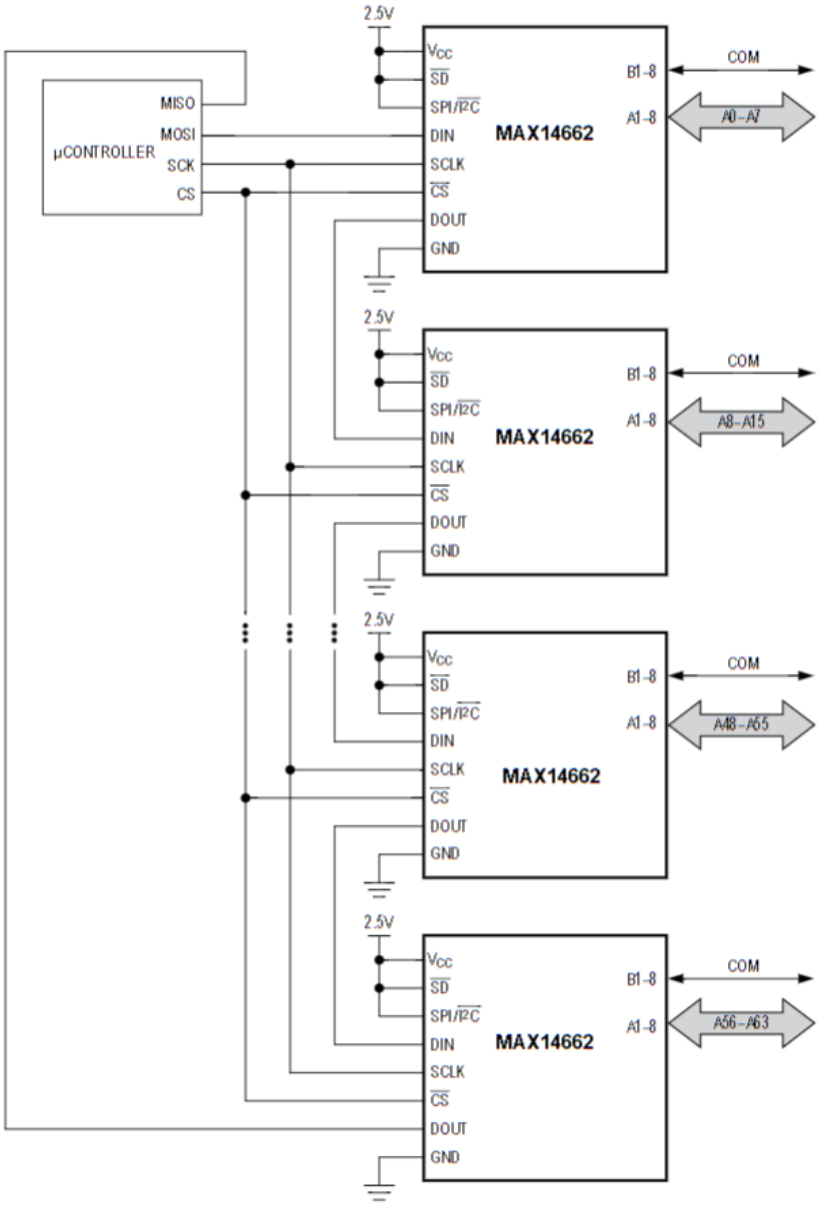

Figure 2: Chained switch configuration

Each individual switch functions as an 8-bit shift register, where the MSB corresponds to A8/B8 and the LSB corresponds to A1/B1. A ‘0’ in a bit position means the switch is off, a ‘1’ means it is on.

BYTE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Data	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1

Figure 3: SPI data format

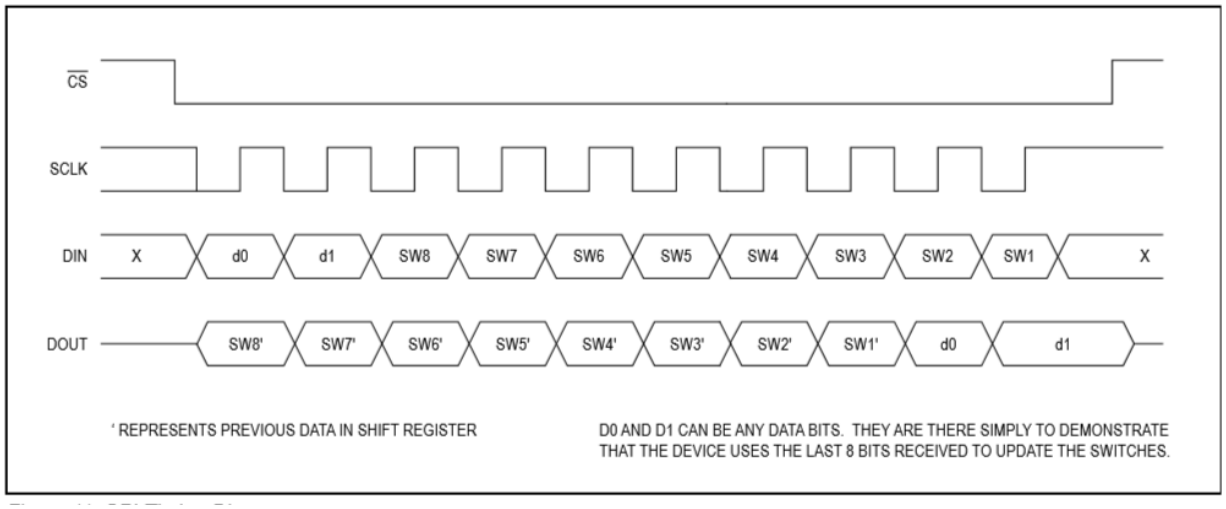

Figure 4: SPI timing diagram

When ~Chip Select (~CS) is asserted, then a rising clock edge will shift the data one bit to the left. BIT0 is replaced with the current value of DIN/SDA, and DOUT/AD0 takes the value of BIT7. When ~CS is deasserted, the switches are set according to the current value of the register, *if and only if* there have been ≥ 8 clock pulses while ~CS was asserted. While ~CS is deasserted, the clock has no effect. The flow of data through the switches is illustrated in

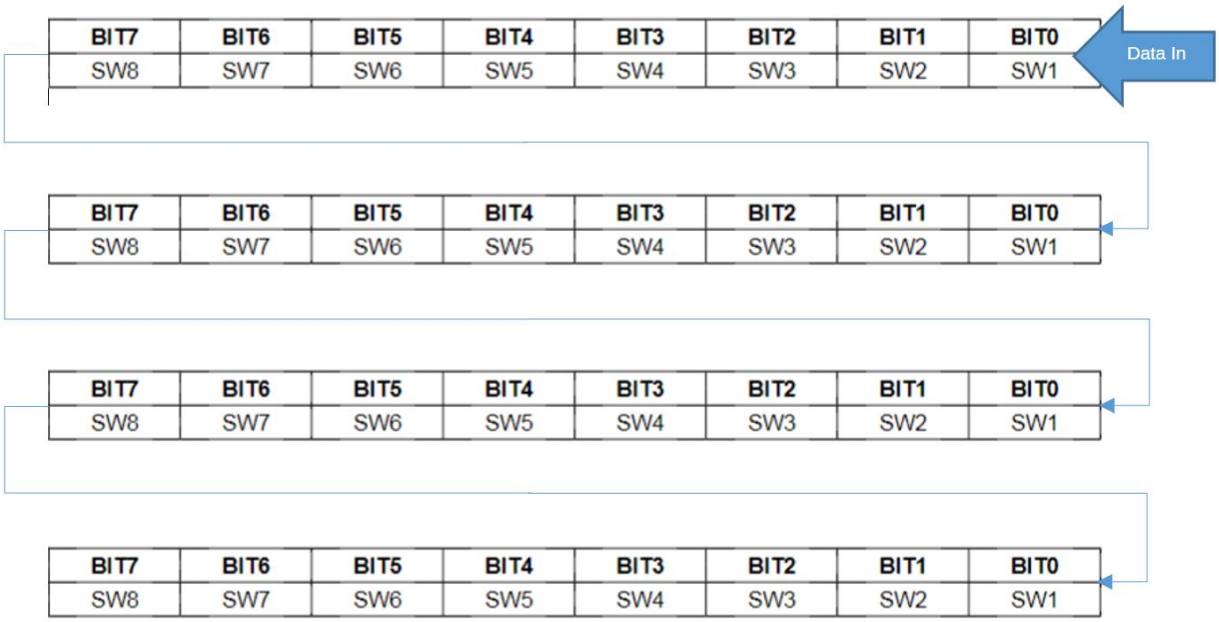
BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1
Data In
BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1
BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1
BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0
SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1

Figure 6.

Control data format

To avoid setting the switches to unwanted positions, 32 bits of data must be sent during one ~CS pulse. As shown in Figure 5, U1 is connected to the data from the controller, and U4 is the last switch in the chain.

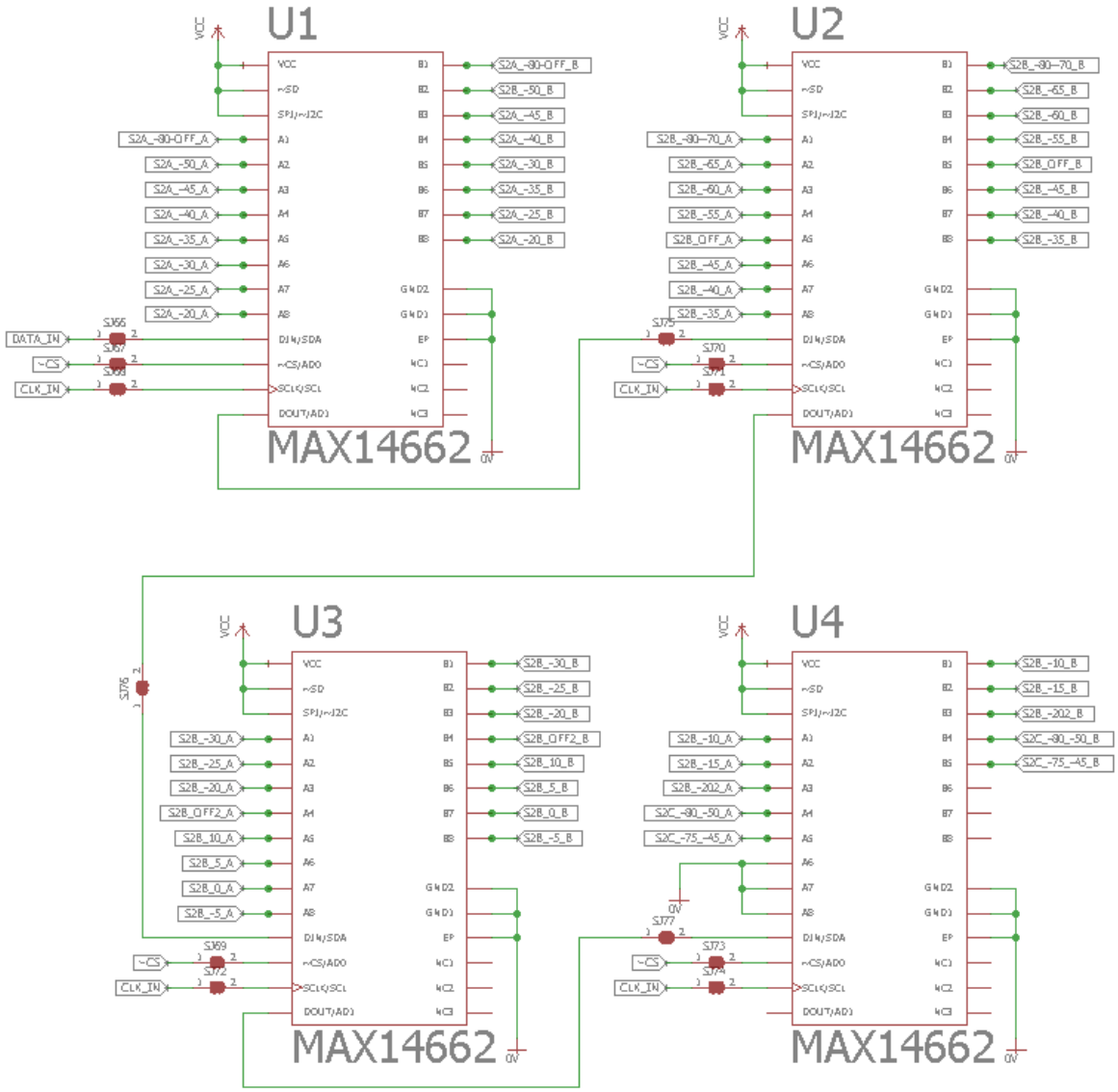

Figure 5: Schematic of switch arrays

This arrangement means that, after 32 clock cycles, the first bit sent will be in BIT7 of U4, and the last bit sent will be in BIT0 of U1.

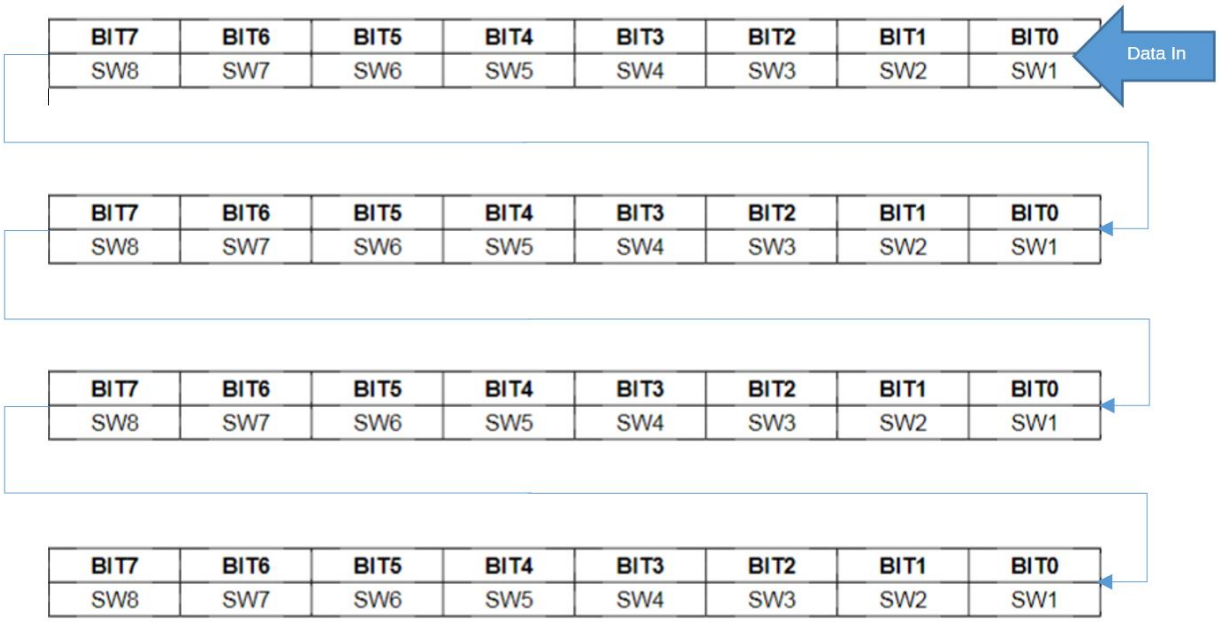

Figure 6: Data flow through switches, U1 on top, U4 on bottom

Switch\Bit	0	1	2	3	4	5	6	7
U1	S2A_-80-OFF	S2A_-50	S2A_-45	S2A_-40	S2A_-35	S2A_-30	S2A_-25	S2A_-20
U2	S2B_-80--70	S2B_-65	S2B_-60	S2B_-55	S2B_OFF	S2B_-45	S2B_-40	S2B_-35
U3	S2B_-30	S2B_-25	S2B_-20	S2B_OFF2	S2B_10	S2B_5	S2B_0	S2B_-5
U4	S2B_-10	S2B_-15	S2B_-202	S2C_-80_-50	S2C_-75_-45	N/A	N/A	N/A

Figure 7: Named signals and corresponding bits