DHANASANKAR K

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ASPIRATION

Aspiring and enthusiastic VLSI Design Verification Engineer with hands-on experience in Verilog, SystemVerilog, and UVM methodology. Skilled in testbench development, functional verification, and waveform analysis using Vivado and other EDA tools. Passionate about ensuring design quality and functional correctness through efficient verification strategies. Seeking a challenging role in a reputed organization to apply my skills and contribute to the success of advanced FPGA/ASIC design projects.

EDUCATION

- **B.E in Electronics and Communication Engineering**, Government College of Engineering, Erode ***2021 – 2025***
  CGPA: 7.6
- **Higher Secondary Education**,Government Boys Higher Secondary School, Gandarvakkottai, Pudukottai (State Board) ***2021***
  Percentage: 76.8

TECHNICAL SKILLS

HDL	Verilog
Verification Languages	SystemVerilog
Verification Methodology	UVM (Universal Verification Methodology)
Simulation Tools	Vivado 2019.2 (IP Integrator, Block Design), I Verilog, GTKWave
FPGA Platforms	Xilinx Artix-7 (EDGE Artix-7 board)
Communication Protocols	UART, I²C, SPI
Bus Protocols	AMBA APB, AMBA AHB, AXI4
Operating System	Linux, Windows

INTERNSHIP EXPERIENCE

- **Silicon Craft VLSI Training and Research Institute, Chennai** - Design Verification Trainee ***Feb 2025 – Present***
  - Gained strong understanding of digital design concepts including combinational and sequential logic.
  - Explored Verilog and SystemVerilog RTL coding for counters, FSMs, and data path designs.
  - Practiced RTL-to-gate-level synthesis, debugging, and waveform analysis using industry tools.
  - Implemented and verified communication protocols (UART, SPI, I2C, APB) with testbenches, including an APB-to-I2C bridge.
- **Silicon Craft VLSI Training and Research Institute, Chennai** - VLSI Intern ***Jul – Aug 2024***
  - Learned FPGA design flow, testbench creation, and waveform debugging.
  - Gained experience in RTL synthesis, bitstream generation, and hardware testing.
  - Designed digital circuits (logic gates, MUX, decoders, flip-flops) using Verilog.
  - Contributed to a secure digital voting machine through counters and control logic design.
- **TechVolt Pvt. Ltd, Coimbatore** - Embedded Systems and IoT ***Jun – Jul 2023***
  - Gained hands-on experience in microcontroller programming and IoT development.
  - Interfaced sensors and actuators using ESP8266, ESP32, and NodeMCU boards.
  - Built real-time data acquisition systems with Arduino and NodeMCU for temperature, humidity, and motion sensing.

PROJECTS

- **AXI4 to SPI Bridge with CDC and UVM-based Verification**
  - Designed an AXI4-to-SPI bridge with Clock Domain Crossing (CDC) for reliable multi-clock data transfer.
  - Integrated AXI4 Master, AXI-SPI Bridge, SPI Master, and SPI Slave modules for end-to-end communication.
  - Built a UVM verification environment with agents, sequencers, drivers, monitors, and scoreboard to validate functionality.
  - Verified SPI read/write operations and CDC stability using directed/random tests, SVA checks, and Questa/Vivado simulation.
- **I²C Protocol Design and Implementation using Verilog**
  - Designed and implemented an I²C Master controller in Verilog supporting communication with multiple slave devices. Verified FSM-based control for serial data transfer and acknowledgment handling.
  - Integrated one master with five slave modules, each configured with a unique 7-bit address for selective communication. Demonstrated accurate data exchange between master and targeted slave.
  - Verified correct protocol operations including start, stop, read, write, and ACK/NACK sequences through functional simulation. Analyzed SCL and SDA waveforms to confirm timing accuracy.
  - Ensured correct data transfer on shared SCL and SDA lines without signal conflicts.
  - Packaged the I²C Master controller as a reusable Custom IP in Vivado for FPGA projects.
- **UART Loopback Communication as Custom IP**
  - Designed a UART-based loopback system with FSM-controlled TX and RX modules in Verilog for reliable serial communication.
  - Implemented full-duplex data transfer where transmitted bytes were echoed back to verify correct reception.
  - Simulated and verified UART functionality using a structured testbench and GTKWave waveform analysis.
  - Developed the UART master as a reusable Custom IP in Vivado for FPGA-based communication designs.
  - Validated start, data, and stop bit timing to ensure accurate and error-free data transmission.

ACADEMIC PROJECTS

- **Dual Axis Solar Tracker**
  - Developed a solar tracking system to align panels with the sun's movement using dual-axis rotation.
  - Enhanced energy efficiency by continuously optimizing panel orientation based on real-time light intensity.
  - Implemented LDR (Light Dependent Resistor) sensing and servo motor control logic using Arduino.
  - Designed and debugged the embedded control algorithm for automatic solar panel alignment.
- **Color-Based Product Sorting**
  - Built an automated sorting system using TCS3200 color sensor and servo-based diverter mechanism.
  - Programmed the system to detect object color and classify items into specific output bins.
  - Utilized Arduino microcontroller for sensor interfacing and actuator control logic.
  - Demonstrated application in industries such as food processing, recycling, and packaging.

CO-CURRICULAR ACTIVITIES

- **Achieved Rank 1 on HDLBits:** Solved all digital design problems on the HDLBits platform using Verilog and organized all solutions in a dedicated GitHub repository.
- **Extensive Coding Practice:** Practiced numerous digital design problems in Verilog, creating well-structured GitHub repositories with topics organized by module, testbench, and functionality.