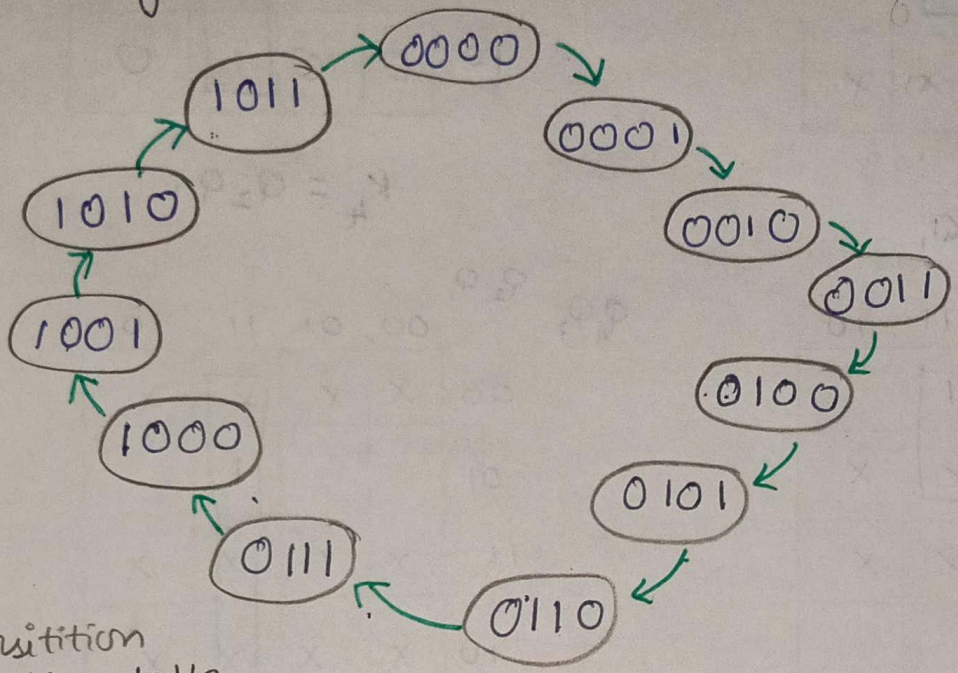
Synchronous Counter

Design of a Synchronous Module-12 up/~~down~~ Counter

a) state diagram



Transition

b) ~~Exitation~~ table.

Present state				Next State				Required excitations.							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	J_4	K_4	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	0	0	0	0	X	1	0	X	X	1	X	1

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00				
01			1	
11	X	X	X	X
10	X	X	X	X

$J_4 = Q_3 Q_2 Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

$K_4 = Q_2 Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00			1	
01	X	X	X	X
11	X	X	X	X
10				

$J_3 = Q_2 Q_1 \bar{Q}_4$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	X	X	X	X
01			1	
11	X	X	X	X
10	X	X	X	X

$K_3 = Q_2 Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10		1	X	X

$J_2 = Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	1	

$K_2 = Q_1$

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

Q_4Q_3 \ Q_2Q_1	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$J_1 = 1$ $\quad K_1 = 1$

$J_2 = Q_1$ $\quad K_2 = Q_1$

$J_3 = Q_2 Q_1 \bar{Q}_4$ $\quad K_3 = Q_2 Q_1$

$J_4 = Q_3 Q_2 Q_1$ $\quad K_4 = Q_2 Q_1$