HUPUF2X8A

Technical Documentation

Hutech - PulseForge Series

May 15, 2025

Contents

1
Introduction

1.1 Purpose and Scope

The HUPUF2X8A (Hutech PulseForge Stereo 2x8b Analog) is an audio synthesis chip designed for embedded systems requiring flexible and efficient sound generation. This technical documentation provides comprehensive information on the architecture, configuration, and usage of the HUPUF2X8A APU. It is intended for hardware developers, embedded software engineers, and audio system integrators who aim to incorporate the APU into audio processing applications.

1.2 Features

The HUPUF2X8A offers the following key features:

- Dual-channel stereo output with 8-bit resolution per channel.
- Support for up to 8 audio channels:
  - 6 Segmented Channels (2 High-Quality, 2 Medium-Quality, 2 Low-Quality).
  - 2 Sampled Channels for raw audio playback.
- Integrated waveform generation, including square, triangle, pulse, sawtooth, and noise.
- Modulation capabilities: Amplitude, Delta, Noise, and Period modulation.
- Dynamic mixing with individual channel volume control and stereo balancing.
- Flexible configuration via parallel register interface.
- Efficient handling of segmented waveforms, enabling the creation of complex audio patterns.
- Compact DIP-20 package with low power consumption.

1.3 Scope of the Document

This document covers the following aspects:

- APU Architecture: Detailed block diagrams and functional module descriptions.
- Register Map: Comprehensive guide to configuring the APU.
- Performance Characteristics: Channel capacity, latency, and power consumption.
- Integration Guidelines: Recommendations for audio output circuitry and signal conditioning.
- Usage and Programming: Initialization routines and real-time control methods.
- Debugging and Testing: Diagnostic features and troubleshooting tips.

1.4 Target Audience

This document is designed for:

- Audio hardware designers integrating the APU into embedded systems.
- Firmware developers writing control code for audio synthesis.
- System integrators looking to optimize audio performance.
- Quality assurance teams validating audio output quality and stability.

1.5 Packaging and Pinout

The HUPUF2X8A APU is available in a DIP-20 package. The table below describes the pin functions and directions:

Pin(s)	**Name**	**Direction**	**Description**	**Usage**
RA0-RA3	Register Address	In	Register Access Address	Exposed Registers
RD0-RD7	Register Data	In/Out	Register Access Data	Exposed Registers
RRW	Register R/W	In	Register Access Read/Write Control	Exposed Registers
RAE	Register Enable	In	Register Access Enable Signal	Exposed Registers
L	Left	Out	Sound Left Analog Signal	Sound Output
R	Right	Out	Sound Right Analog Signal	Sound Output
CLK	Master Clock	In	Master clock input	Clock
RST	Reset	In	Reset signal	Boot
VSS	Ground	-	Ground connection	Power supply
VDD	Power	-	Positive power supply	Power supply

Table 1: Pinout of HUPUF2X8A - DIP-20 Package

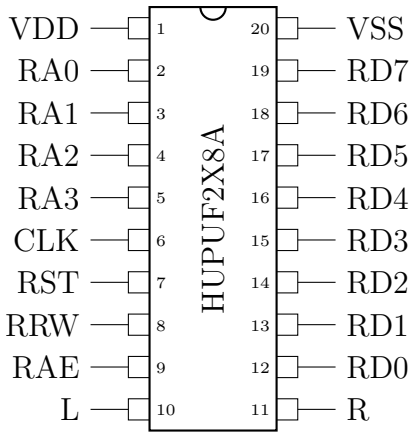

Figure 1: Pinout of HUPUF2X8A - DIP-20 Package

2

Architecture Overview

2.1 High-Level Description

The HUPUF2X8A Audio Processing Unit (APU) is a compact and versatile chip designed for generating high-quality stereo audio in embedded systems. The architecture leverages a modular design to accommodate a wide range of audio synthesis requirements while maintaining low power consumption and efficient processing.

The APU supports up to 8 audio channels:

- 6 Segmented Channels (2 High-Quality, 2 Medium-Quality, 2 Low-Quality)
- 2 Sampled Channels (configurable for raw audio playback and modulation)

The core of the APU is a pipeline-based audio engine that synthesizes sound by processing discrete segments or samples through specialized channels. Each channel can be independently configured for waveform generation, modulation, and mixing, allowing for complex audio patterns and dynamic effects.

The APU directly outputs analog signals through two dedicated stereo pins (L and R), providing high-quality sound at 8-bit resolution per channel.

2.2 Block Diagram

The following diagram provides an overview of the internal architecture of the HUPUF2X8A APU:

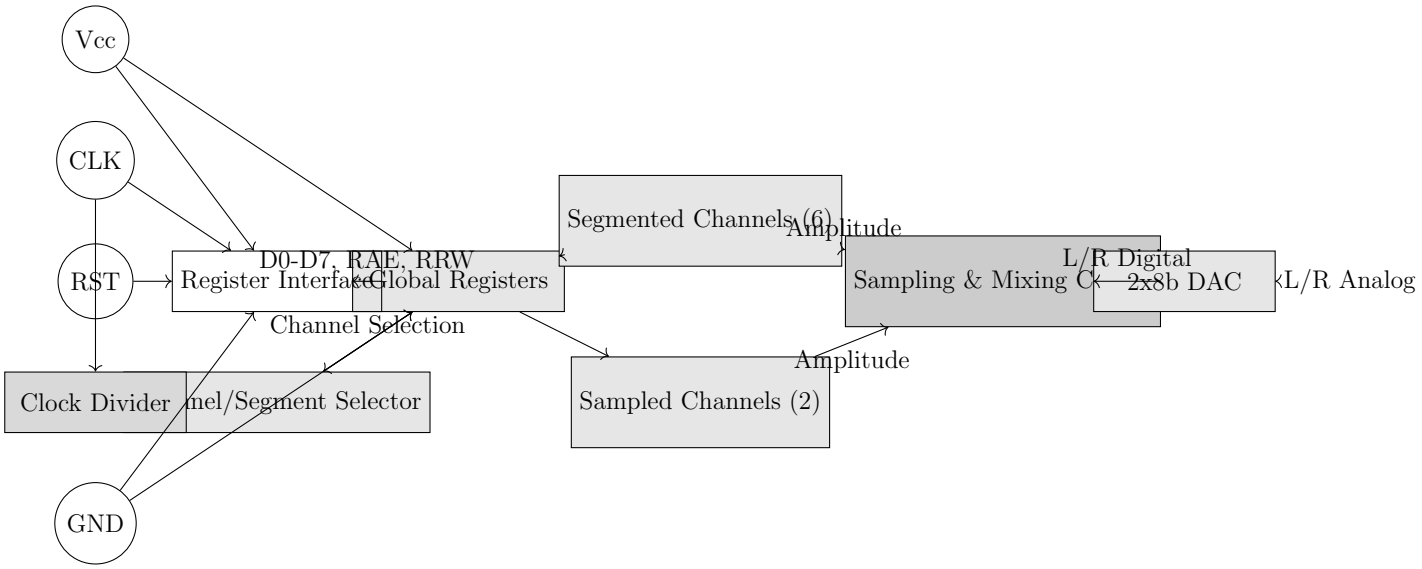

Figure 2: Block Diagram of HUPUF2X8A - APU

2.3 Signal Flow

The APU operates through a sequence of audio processing steps as follows:

1. **Clock and Reset Management:** The system clock synchronizes all internal operations, while the reset line initializes the APU state.
2. **Channel Configuration:** Each of the 8 channels can be independently configured through dedicated registers. Segmented channels generate complex waveforms, while sampled channels handle raw audio data.

3. **Waveform Generation:** The segmented channels utilize a series of amplitude steps to create dynamic audio patterns. Sampled channels output audio directly from stored data.

4. **Mixing and Output:** The outputs of all active channels are summed and balanced by the mixer, which can independently control the volume and stereo positioning of each channel.

5. **Digital-to-Analog Conversion:** The mixed digital audio signals are converted to analog output via a dual-channel DAC, feeding the left and right audio lines.

2.4 Audio Processing Pipeline

The audio processing pipeline is designed to handle multiple channels concurrently, optimizing resource usage while maintaining audio fidelity. The pipeline consists of:

- **Waveform Generation Stage:** Produces digital audio signals based on the selected waveform configuration.
- **Modulation and Mixing Stage:** Combines audio signals with volume scaling and stereo distribution.
- **Digital-to-Analog Conversion Stage:** Outputs the final mixed signal through the DAC.

The modular nature of the pipeline allows for fine-tuned control of each channel, including volume adjustment, waveform modulation, and stereo balancing, making it suitable for a wide range of audio applications.

3
Functional Modules

3.1 Oscillators and Tone Generators

Description of tone generation mechanisms.

3.2 Segmented Channels

Detailed description and configuration.

3.3 Sampled Channels

Handling of sampled audio data.

3.4 Modulation Techniques

Types: Amplitude, Frequency, Noise, Delta.

3.5 Mixer and Output

Mixing process, stereo configuration, volume control.

4

Register Map and Configuration

4.1 Global Registers

Listing and description of global control registers.

4.2 Per-Channel Registers

Detailed mapping of registers for each channel type.

4.3 Access Mechanism

How to interact with registers.

4.4 Programming Examples

Example configurations and setups.

5

Clock and Timing

5.1 Master Clock

Description of clock source and synchronization.

5.2 Sampling Rate

Relation between clock speed and audio output.

5.3 Latency and Constraints

Expected processing delays.

6
Performance Characteristics

6.1 Channel Capacity

Max simultaneous channels and tone generation.

6.2 Latency

Measured delays from input to output.

6.3 Power Consumption

Energy efficiency and expected consumption.

7

Integration and Usage

7.1 Wiring Diagrams

Example wiring for headphones and RCA output.

7.2 Usage Scenarios

Step-by-step setup for basic sound generation.

7.3 Programming Interface

Methods to program and interact with the APU.

8

Debugging and Testing

8.1 Built-in Diagnostics

Test modes and validation procedures.

8.2 Signal Validation

Test signals and output expectations.

8.3 Troubleshooting

Common issues and their resolutions.

A
Electrical Characteristics

Power and signal specifications.

B

Example Code

Sample scripts and configurations.

C
Revision History

Track changes and updates to the document.