ECE 571

INTRO TO SYSTEM VERILOG

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A PROJECT REPORT

TEAM-17

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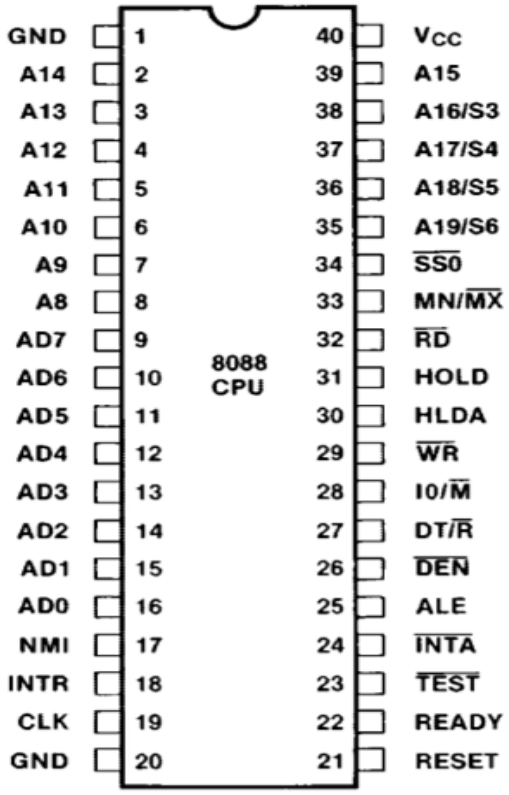
TABLE OF CONTENT

S.NO	CONTENTS	PAGES
1.	INTRODUCTION	3
2.	OBJECTIVE	4
3.	BLACKBOX	5
4.	METHOD	5-6
5.	TESTCASES	7
6.	OUTWAVEFORMS	9
7.	CHALLENGES	7

INTRODUCTION:



The Intel 8088 microprocessor architecture combines features of both 8-bit and 16-bit microprocessors, offering high performance and compatibility with existing software and hardware. In this report, we delve into the technical specifications and functionalities of the Intel 8088.

The Intel 8088 microprocessor boasts several key features:

8-Bit Data Bus Interface: While internally it operates with a 16-bit architecture, externally it interfaces with an 8-bit data bus.
16-Bit Internal Architecture: Internally, the processor operates on a 16-bit architecture, providing enhanced processing capabilities.
Direct Addressing Capability: The processor supports direct addressing to up to 1 Mbyte of memory, enabling efficient memory access.

Software Compatibility: It is directly compatible with software written for the Intel 8086 CPU, ensuring seamless migration for existing applications.

Register Set: The processor includes a 14-word by 16-bit register set with symmetrical operations, facilitating efficient data manipulation.

Operand Addressing Modes: It supports 24 operand addressing modes, offering flexibility in accessing data.

Functional Description: The 8088 microprocessor operates with a 20-bit address bus, enabling access to a memory space of up to 1 Mbyte. Memory is logically divided into segments, including code, data, extra data, and stack segments, each with specific attributes and addressing rules.

External Interface: The processor features various pins and control signals for interfacing with external components. It supports both minimum and maximum modes of operation, offering flexibility in system design. In minimum mode, it can be used with a multiplexed or demultiplexed bus, while maximum mode employs the 8288-bus controller for enhanced bus control.
Bus Operation: The processor's bus operation involves time-multiplexed address and data lines, with distinct cycles for address emission and data transfer. It supports various bus cycles, including memory and I/O operations, interrupt acknowledgment, and halt states.

SIGNIFICANCE:

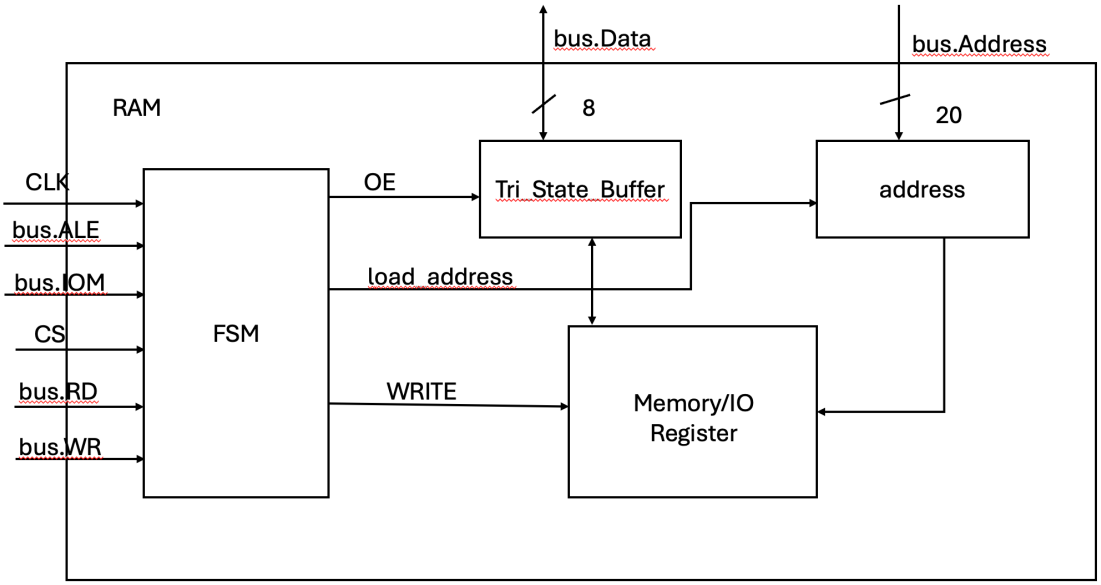
Exploring the operation of the pins and control signals of the 8088 processor by simulating and observing waveform patterns.

OBJECTIVE:

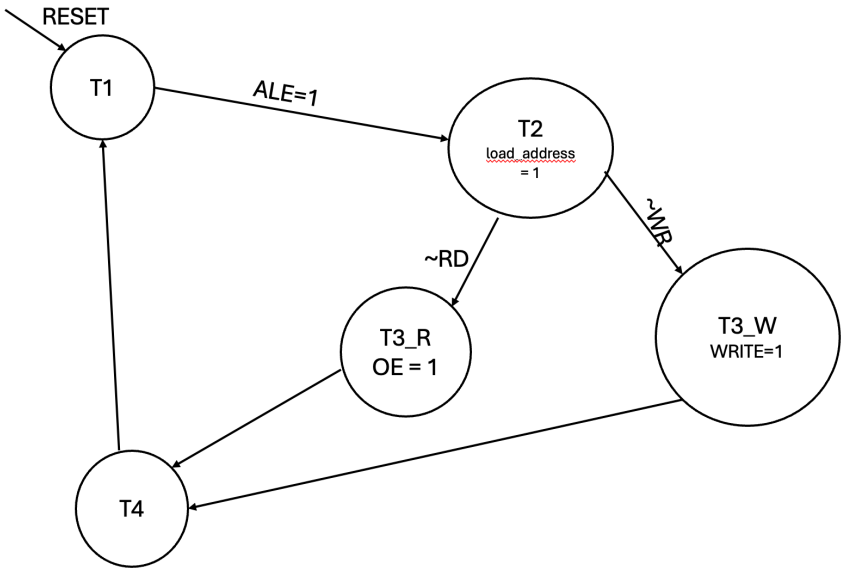
The main objective of this project is to design a controller which captures the signals from the processor and do the following memory and I/O operations.

This Intel's' 8088 microprocessor with 20-bit address for memory and 16-bit address for I/O modules. As the 8088.svp only triggers the read and write operation to the memory and I/O modules we use the following signals CLK, ALE, IOM, CS, WR, address and data as in out.
In this project, we designed a synthesizable FSM for 8088 bus-compatible memory or I/O modules, incorporating CS and OE inputs. And implemented the FSM as a one-hot Moore machine. Modified the top-level module to instantiate two 512KiB memories and two I/O devices and adjusted the busops.txt file accordingly. Created an interface for 8088 pins with Processor and Peripheral mod ports and modified the top-level module to instantiate and use this interface.

BLACKBOX:



METHODS:



The above states are taken for read and write operations. Our System Verilog module has the following.

Module Parameters:

- IOM: Parameter specifying the I/O memory size.

Interface Ports:

- Intel8088Pins.Peripheral in: Interface with the Intel 8088 processor peripheral.
- input CS: Chip Select signal.
- input [19:0] Address: Address input.
- inout [7:0] Data: Data bus.

FSM States:

- IDLE: Initial state, waiting for control signals.
- FETCH_ADDRESS: State for fetching the memory address.
- READ: State for reading data from memory.
- WRITE: State for writing data to memory.
- END: End state, transitioning back to IDLE.

Internal Signals:

- current_state, next_state: FSM state registers.
- OE, Write, LoadAddress: Control signals.
- memory: Memory array for storing data.
- addr: Memory address register.

Functional Description:

- Memory Address and Data Handling:
- Address and data are stored in registers for manipulation.
- Address is loaded into the addr register when LoadAddress signal is asserted.
- Data is written to memory on the rising edge of the clock when Write signal is asserted.
- FSM State Transition:
- FSM state transitions occur on the rising edge of the clock.
- State transitions are determined by the current state and input control signals.
- Reset condition sets the FSM to the IDLE state.
- State-Dependent Control Signals:
- Control signals (Load Address, OE, Write) are set based on the current state.
- These signals control address loading, data output enables, and write enable respectively.
- Initial Memory Loading:
- Initial memory content is loaded from a hex file (tracefile1.txt) using $readmemh() function.

TESTCASES:

we have created 3 busops files

busopsl

100	I	R	0x01C00
104	I	R	0x0FF04
205	I	R	0x6FF04
350	I	R	0x1F00F
405	I	W	0x41C01
420	I	R	0x01D00
555	I	W	0x0FF0F
601	I	W	0x1F005
657	I	R	0xFF004
680	I	R	0x0F005

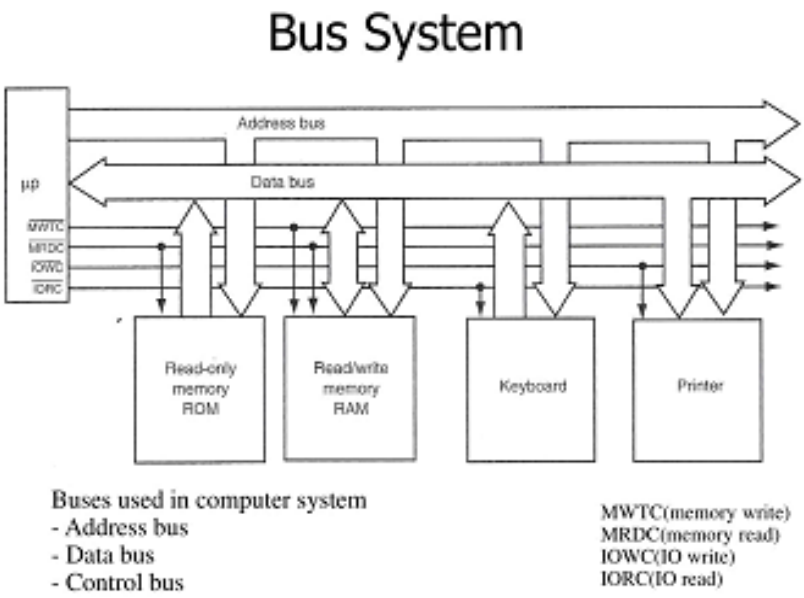
Busops

100	M	R	0x21D05
101	M	R	0x44333
200	M	W	0x3FF04
250	M	R	0x3FF04
255	M	R	0x0F020
352	M	W	0x21F04
353	M	W	0x00302
380	M	R	0x21D04
500	I	R	0x2FF0D
625	I	W	0x2DF03
701	I	R	0x2DF03
765	I	R	0x21E02
801	I	W	0x44422
835	I	R	0x44422

Busopsm

100	M	R	0x00F33
101	M	R	0x20507
200	M	W	0x003F2
250	M	R	0x00505
355	M	R	0x90505
452	M	W	0x44FFF
553	M	W	0x5F605
600	M	R	0xF3444
753	M	R	0x00500

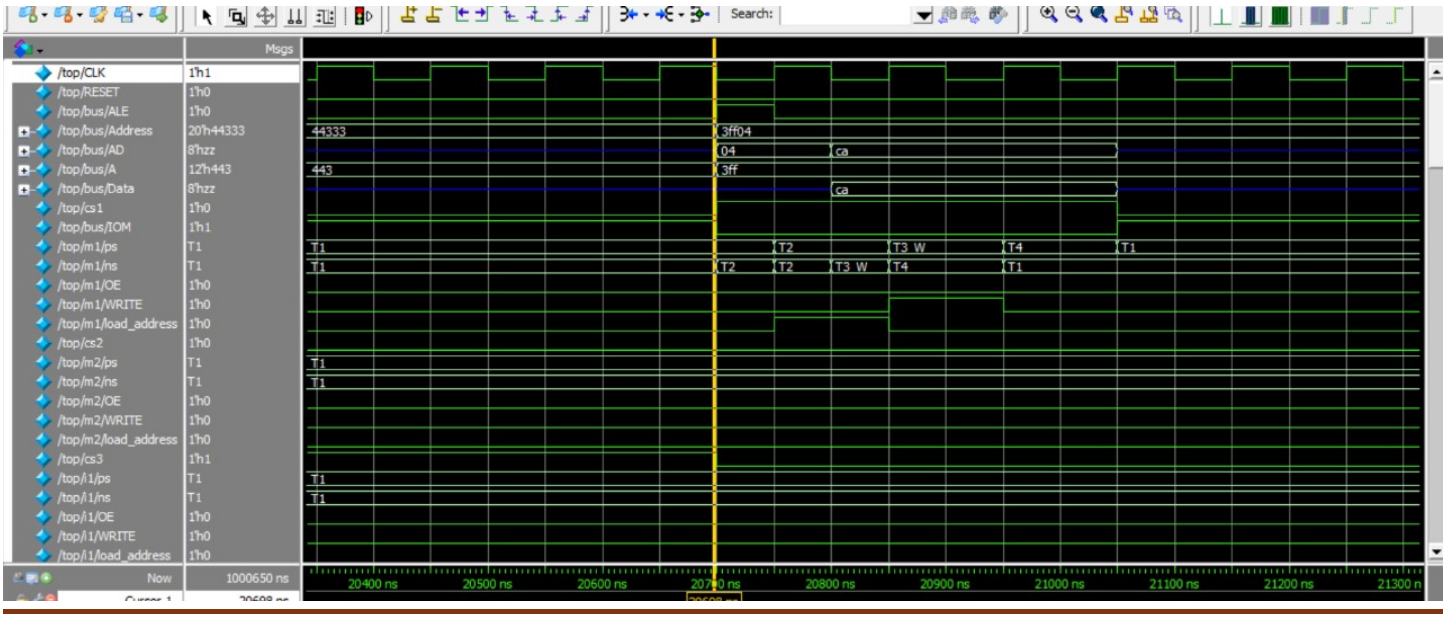
INTERFACE:



Module Components:

- Processor Interface:
- Input signals (CLK, RESET) are connected to the Intel8088Pins module to synchronize operation with the processor clock and handle reset conditions.
- I/O Memory FSM Instances:
- Four instances of the IOMFSM module (dut1 to dut4) are instantiated, each with its chip select (CS) signal, address, and **data connections:**
- Address and Data Signals:
- Address: 20-bit wide signal for memory address.
- Data: 8-bit wide signal for data communication.
- Control Signals:
- Chip select signals (CS1 to CS4) are used to enable memory access for specific devices.

WAVEFORMS:



CHALLENGES:

we faced so many issues while doing with interfaces, it was challenged for us. Now we gained great knowledge on how to perform code. We succeed it.

GITHUB REPOSITORY LINK:

https://github.com/DHUSHYANTHDHARMAVARAPU?tab=projects