

### **General Description**

The MAX5383/MAX5384/MAX5385 low-cost, 8-bit digitalto-analog converters (DACs) in miniature 6-pin SOT23 packages have a simple 3-wire, SPITM/QSPITM/ MICROWIRE™-compatible serial interface that operates up to 10MHz. The MAX5383 has an internal +2V reference and operates from a +2.7V to +3.6V supply. The MAX5384 has an internal +4V reference and operates from a +4.5V to +5.5V supply. The MAX5385 operates over the full +2.7V to +5.5V supply range and has an internal reference equal to 0.9 × V<sub>DD</sub>.

The MAX5383/MAX5384/MAX5385 require an extremely low supply current of only 150µA (typ) and provide a buffered voltage output. These devices power up at zero code and remain there until a new code is written to the DAC registers. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5383/MAX5384/ MAX5385 include a 1µA, low-power shutdown mode that features software-selectable output loads of  $1k\Omega$ ,  $100k\Omega$ , or  $1M\Omega$  to ground.

### **Applications**

Automatic Tuning (VCO) Power Amplifier Bias Control Programmable Threshold Levels Automatic Gain Control Automatic Offset Adjustment

SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

## **Features**

- ♦ 8-Bit Resolution in a Miniature 6-Pin SOT23 **Package**
- ♦ Wide +2.7V to +5.5V Supply Range (MAX5385)
- ♦ <1µA Shutdown Mode
- **♦** Software-Selectable Output Resistance During Shutdown
- **♦** Buffered Output Drives Resistive Loads
- ♦ Low-Glitch Power-On Reset to Zero DAC Output
- **♦ 3-Wire SPI/QSPI/MICROWIRE-Compatible Interface**
- ♦ < ±5% Full-Scale Error (MAX5385)
- ♦ < ±1LSB max INL/DNL
- ♦ Low 230µA (max) Supply Current

### **Ordering Information**

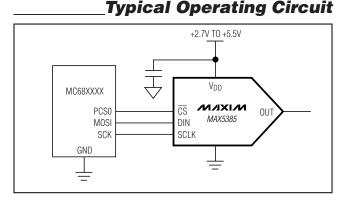
		_	
PART	TEMP RANGE	PIN- PACKAGE	SOT TOP MARK
MAX5383EUT+T	-40°C to +85°C	6 SOT23	AADF
MAX5383EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAH
MAX5384EUT+T	-40°C to +85°C	6 SOT23	AADH
MAX5384EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAI
MAX5385EUT+T	-40°C to +85°C	6 SOT23	AADJ
MAX5385EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAJ

<sup>+</sup>Denotes lead(Pb)-free/RoHS-compliant package. T = Tape and reel.

### **Selector Guide**

PART	INTERNAL REFERENCE
MAX5383	2V
MAX5384	4V
MAX5385	$0.9 \times V_{DD}$

## **Pin Configuration**



TOP VIEW		
OUT 1	+	6
GND 2	MAX5383 MAX5384 MAX5385	5 SCLK
V <sub>DD</sub> 3		4 DIN
	SOT23	ı

MIXIM

Maxim Integrated Products 1

#### **ABSOLUTE MAXIMUM RATINGS**

V <sub>DD</sub> to GND0.3V to +6V	Operating Temperature Range40°C to +85°C
OUT0.3V to (V <sub>DD</sub> + 0.3V)	Storage Temperature Range65°C to +150°C
CS, SCLK, DIN to GND0.3V to +6V	Maximum Junction Temperature+150°C
Maximum Current into Any Pin50mA	Lead Temperature (soldering, 10s)+300°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
6-Pin SOT23 (derate 8.7mW/°C above +70°C)696mW	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD}=+2.7V\ to\ +3.6V\ (MAX5383),\ V_{DD}=+4.5V\ to\ +5.5V\ (MAX5384),\ V_{DD}=+2.7V\ to\ +5.5V\ (MAX5385),\ R_L=10k\Omega,\ C_L=50pF,\ T_A=T_{MIN}\ to\ T_{MAX},\ unless\ otherwise\ noted.$  Typical values are  $T_A=+25^{\circ}C.)$ 

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
STATIC ACCURACY								
Resolution				8			Bits	
Integral Linearity Error	INL	(Note 1)				±1	LSB	
Differential Linearity Error	DNL	Guaranteed monotoni	С			±1	LSB	
Offset Error	Vos	(Note 2)			±1	±25	mV	
Offset Error Supply Rejection		MAX5385 (Notes 2, 3)				60	dB	
Offset Error Temperature		MAX5383/MAX5384			3		nnm/0C	
Coefficient		MAX5385			1		ppm/°C	
Full-Scale Error		Code = 255, no load	MAX5383/MAX5384			10	% of	
Full-Scale Error		Code = 255, no load	MAX5385			5	ideal FS	
Full-Scale Error Supply Rejection		Code = 255 (Note 4)	MAX5383/MAX5384			50	dB	
Full-Scale Error Temperature		0 1 055	MAX5383/MAX5384		±40		/00	
Coefficient		Code = 255 MAX5385			±10		ppm/°C	
DAC OUTPUT								
		MAX5383		1.8	2	2.2		
Internal Reference Voltage	REF	MAX5384		3.6	4	4.4		
(Note 5)	REF	MAX5385		0.85 × V <sub>DD</sub>	0.9 × V <sub>DD</sub>	0.95 × V <sub>DD</sub>	V	
Outrot I and Deputation		Code = 255, 0µA to 1	00μΑ		0.5		1.00	
Output Load Regulation		Code = 0, $0\mu$ A to 100	μΑ		0.5		LSB	
			[D13, D12] = 0, 1		1k			
Shutdown Output Resistance to GND		$V_{OUT} = 0$ to $V_{DD}$	[D13, D12] = 1, 0		100k		Ω	
		[D13, D12] = 1, 1		1M			]	
DYNAMIC PERFORMANCE								
Voltage Output Slew Rate		Positive and negative			0.4		V/µs	
Output Settling Time		To 1/2 LSB, $50$ k $\Omega$ and	50pF load (Note 6)		20		μs	
Digital Feedthrough		Code = 0, all digital in	puts from 0 to V <sub>DD</sub>		2		nVs	

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD}=+2.7V\ to\ +3.6V\ (MAX5383),\ V_{DD}=+4.5V\ to\ +5.5V\ (MAX5384),\ V_{DD}=+2.7V\ to\ +5.5V\ (MAX5385),\ R_L=10k\Omega,\ C_L=50pF,\ T_A=T_{MIN}\ to\ T_{MAX},\ unless\ otherwise\ noted.$  Typical values are  $T_A=+25^{\circ}C.)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-Analog Glitch Impulse		Code 127 to 128		40		nVs
Wake-Up Time		From software shutdown		50		μs
POWER REQUIREMENTS						
		MAX5383	2.7		3.6	
Supply Voltage	$V_{DD}$	MAX5384	4.5		5.5	V
		MAX5385	2.7		5.5	
Supply Current	I <sub>DD</sub>	No load, all digital inputs at 0 or $V_{DD}$ , code = 255		150	230	μА
		Shutdown mode			1	
DIGITAL INPUTS						
Input Low Voltage	V <sub>IL</sub>				$0.3 \times V_{DD}$	V
Input High Voltage	VIH		0.7 × V <sub>DD</sub>			V
Input Hysteresis	VH			0.05 × V <sub>DD</sub>		V
Input Capacitance	CIN	(Note 7)		10		рF
Input Leakage Current	IIN				±1	μΑ

#### TIMING CHARACTERISTICS

(Figures 3 and 4,  $V_{DD}$  = +2.7V to +3.6V (MAX5383),  $V_{DD}$  = +4.5V to +5.5V (MAX5384),  $V_{DD}$  = +2.7V to +5.5V (MAX5385),  $V_{DD}$  = 10k $\Omega$ ,  $C_L$  = 50pF,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are  $T_A$  = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period	tcp		100			ns
SCLK Pulse Width High	tcH		40			ns
SCLK Pulse Width Low	t <sub>CL</sub>		40			ns
CS Fall to SCLK Rise Setup Time	tcss		40			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	tcsh		0			ns
DIN Setup Time	t <sub>DS</sub>		40			ns
DIN Hold Time	tDH		0			ns
SCLK Rise to CS Fall Delay	t <sub>CS0</sub>		10			ns

### **TIMING CHARACTERISTICS (continued)**

(Figures 3 and 4,  $V_{DD}$  = +2.7V to +3.6V (MAX5383),  $V_{DD}$  = +4.5V to +5.5V (MAX5384),  $V_{DD}$  = +2.7V to +5.5V (MAX5385),  $V_{DD}$  = 10k $\Omega$ ,  $C_L$  = 50pF,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are  $T_A$  = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS Rise to SCLK Rise Hold	tCS1		40			ns
CS Pulse Width High	tcsw		100			ns

Note 1: Guaranteed from code 5 to code 255.

Note 2: The offset value extrapolated from the range over which the INL is guaranteed.

Note 3: MAX5385 tested at 5V  $\pm$ 10%.

Note 4: MAX5383 tested at 3V  $\pm$ 10%; MAX5384 tested at 5V  $\pm$ 10%.

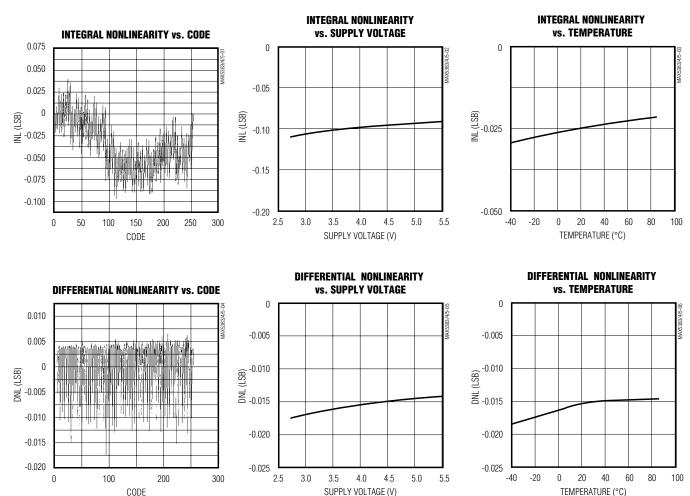
**Note 5:** Actual output voltages at full-scale are  $255/256 \times V_{REF}$ .

Note 6: Output settling time is measured by stepping from code 5 to code 255, and from code 255 to code 5.

Note 7: Guaranteed by design.

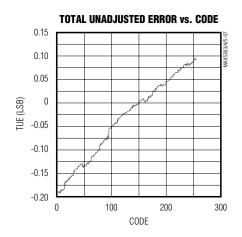
### Typical Operating Characteristics

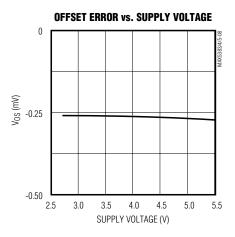
 $(V_{DD} = +3.0V (MAX5383), V_{DD} = +5.0V (MAX5384/MAX5385), T_{A} = +25^{\circ}C, unless otherwise noted.)$ 

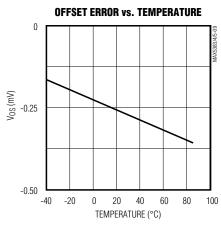


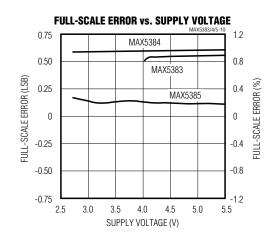
### Typical Operating Characteristics (continued)

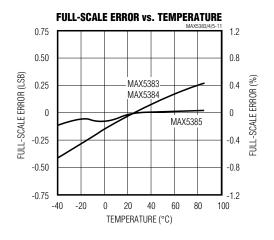
 $(V_{DD} = +3.0V \text{ (MAX5383)}, V_{DD} = +5.0V \text{ (MAX5384/MAX5385)}, T_{A} = +25^{\circ}\text{C}, \text{ unless otherwise noted.)}$ 

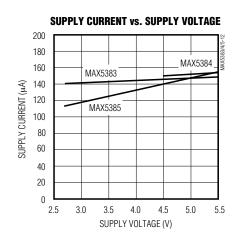


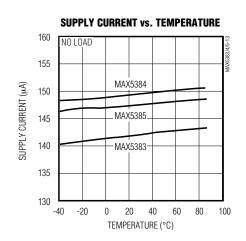






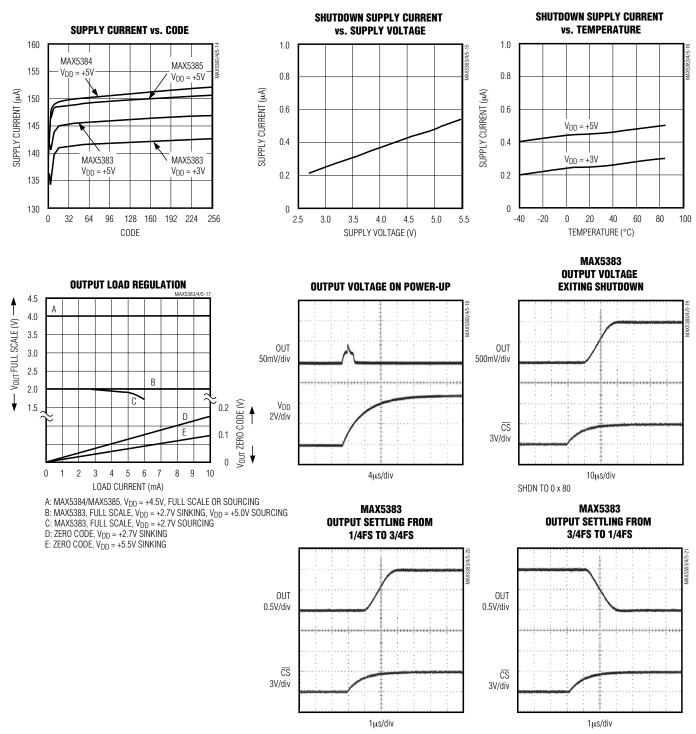






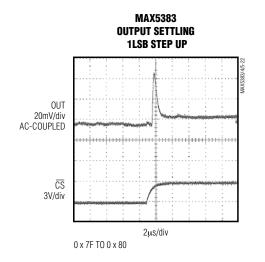
### Typical Operating Characteristics (continued)

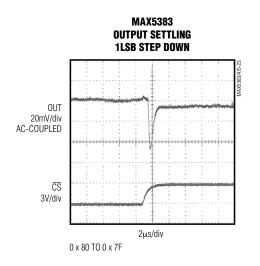
 $(V_{DD} = +3.0 \text{V (MAX5383)}, V_{DD} = +5.0 \text{V (MAX5384/MAX5385)}, T_{A} = +25 ^{\circ}\text{C}, \text{ unless otherwise noted.})$ 



### Typical Operating Characteristics (continued)

 $(V_{DD} = +3.0 \text{V (MAX5383)}, V_{DD} = +5.0 \text{V (MAX5384/MAX5385)}, T_{A} = +25 ^{\circ}\text{C}$ , unless otherwise noted.)





### **Pin Description**

PIN	NAME	DESCRIPTION		
1	OUT	DAC Voltage Output		
2	GND	Ground		
3	V <sub>DD</sub>	Power-Supply Input		
4	DIN	Serial Data Input		
5	SCLK	Serial Clock Input		
6	CS	Chip-Select Input		

### **Detailed Description**

The MAX5383/MAX5384/MAX5385 voltage-output, 8-bit DACs ensure monotonic performance by offering full 8-bit performance with less than 1LSB integral nonlinearity error and less than 1LSB differential nonlinearity error. The devices use a simple 3-wire, SPI/QSPI/MICROWIRE-compatible serial interface that operates up to 10MHz. They include an internal reference, an output buffer, and three low-current shutdown modes, making these devices ideal for low-power, highly integrated applications. Figure 1 shows the devices' functional diagram.

### **Analog Section**

The MAX5383/MAX5384/MAX5385 employ a current-steering DAC topology as shown in Figure 2. At the core of the DAC is a reference voltage-to-current converter (V/I) that generates a reference current. This current is mirrored to 255 equally weighted current sources. DAC switches control the outputs of these current mirrors so that only the desired fraction of the total current-mirror currents is steered to the DAC output. The current is then converted to a voltage across a resistor, and this voltage is buffered by the output buffer amplifier.

#### Output Voltage

Table 1 shows the relationship between the DAC code and the analog output voltage. The 8-bit DAC code is binary unipolar with 1LSB = ( $V_{REF}/256$ ). The MAX5383/MAX5384 have a full-scale output voltage of (+2V - 1LSB) and (+4V - 1LSB), set by the internal references. The MAX5385 has a full-scale output voltage of (0.9 ×  $V_{DD}$  - 1LSB).

#### Output Buffer

The DAC voltage output is an internally buffered unity-gain follower that slews up to  $\pm 0.4 \text{V/}\mu\text{s}$ . The output can swing from 0 to full scale. With a 1/4FS to 3/4FS output transition, the amplifier outputs typically settle to 1/2LSB in less than 5 $\mu$ s when loaded with 10k $\Omega$  in parallel with 50pF. The buffer amplifiers are stable with any

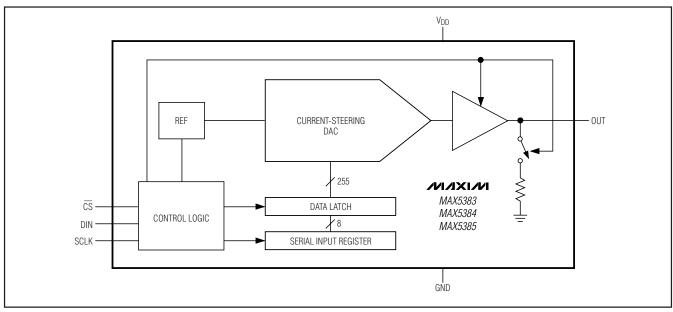


Figure 1. Functional Diagram

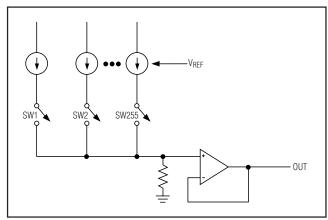


Figure 2. Current-Steering DAC Topology

### **Table 1. Unipolar Code Output Voltage**

DAC CODE	OUTPUT VOLTAGE				
[D11–D4]	MAX5383	MAX5384	MAX5385		
1111 1111	2V × (255/256)	4V × (255/256)	0.9 × V <sub>DD</sub> × (255/256)		
1000 0000	1V	2V	0.9 × V <sub>DD</sub> / 2		
0000 0001	7.8mV	15.6mV	0.9 × V <sub>DD</sub> / 256		
0000 0000	0	0	0		

combination of resistive loads >10k $\!\Omega$  and capacitive loads <50pF.

#### Power-On Reset

The MAX5383/MAX5384/MAX5385 have a power-on reset circuit to set the DAC's output to 0 when  $V_{DD}$  is first applied or when  $V_{DD}$  dips below 1.7V (typ). This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. The output glitch on startup is typically less than 50mV.

#### Shutdown Mode

The MAX5383/MAX5384/MAX5385 include three software-controlled shutdown modes that reduce the supply current to <1 $\mu$ A. All internal circuitry is disabled, and a known impedance is placed from OUT to GND to ensure 0V while in shutdown. Table 2 details the three shutdown modes of operation.

### **Digital Section**

#### **3-Wire Serial Interface**

The MAX5383/MAX5384/MAX5385s' digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The chip-select input (CS) frames the serial data loading at the data-input pin (DIN). Immediately following CS's high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial

8 \_\_\_\_\_\_ *NIXIM* 

input register, it transfers its contents to the DAC latch on  $\overline{CS}$ 's low-to-high transition (Figure 3). Note that if  $\overline{CS}$  is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word. The serial clock (SCLK) can idle either high or low between transitions. Figure 4 shows the complete 3-wire serial interface transmission. Table 3 lists serial interface mapping.

### Applications Information

### **Device Powered by an External Reference**

Since the MAX5385 generates an output voltage proportional to V<sub>DD</sub>, a noisy power supply will affect the accuracy of the on-board reference, thereby affecting the overall accuracy of the DAC. The circuit in Figure 5 rejects this power-supply noise by powering the device directly with a precision voltage reference, improving overall system accuracy. The MAX6103 (+3V, 75ppm) or the MAX6105 (+5V, 75ppm) precision voltage references are ideal choices due to the low power requirements of the MAX5385. This solution is also useful when the required full-scale output voltage is different from the available supply voltages.

#### **Digital Inputs and Interface Logic**

The digital interface for the 8-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and MICROWIRE interfaces. The three digital inputs  $\overline{(CS, DIN, and SCLK)}$  load the digital input serially into the DAC.

All the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5383/MAX5384/MAX5385 without additional external logic. The digital inputs are compatible with CMOS logic levels and can be driven with voltages up to +5.5V regardless of the supply voltage.

#### **Power-Supply Bypassing and Layout**

Careful PC board layout is important for best system performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. To ensure that the ground return from GND to the supply ground is short and low impedance, a ground plane is recommended. Bypass  $V_{DD}$  with a  $0.1\mu F$  capacitor to ground as close as possible to the device. If the supply is excessively noisy, connect a  $10\Omega$  resistor in series with the supply and  $V_{DD}$  and add additional capacitance.

**Table 2. Shutdown Modes** 

DAC CODE [D13 AND D12]	MODE	OUTPUT RESISTANCE TO GROUND ( $\Omega$ )	MAXIMUM SUPPLY CURRENT (μA)
01	Shutdown	1k	1
10	Shutdown	100k	1
11	Shutdown	1M	1

**Table 3. Serial Interface Mapping** 

	16-BIT SER	IAL WORD		ANALOG	FUNCTION
MSB			LSB	OUTPUT	FUNCTION
XX00	0000	0000	XXXX	OV	Normal operation
XX00	1111	1111	XXXX	V <sub>REF</sub> × (255/256)	Normal operation
XX00	0000	0001	XXXX	V <sub>REF</sub> × (1/256)	Normal operation
XX00	1000	0000	XXXX	V <sub>REF</sub> × (128/256)	Normal operation
XX01	XXXX	XXXX	XXXX	OV	Shutdown, $1$ k $\Omega$ to GND
XX10	XXXX	XXXX	XXXX	OV	Shutdown, 100kΩ to GND
XX11	XXXX	XXXX	XXXX	OV	Shutdown, 1MΩ to GND

X = Don't care

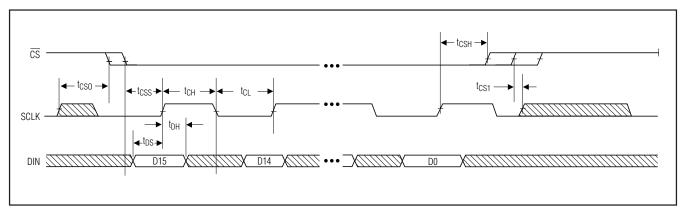


Figure 3. 3-Wire Serial Interface Timing Diagram

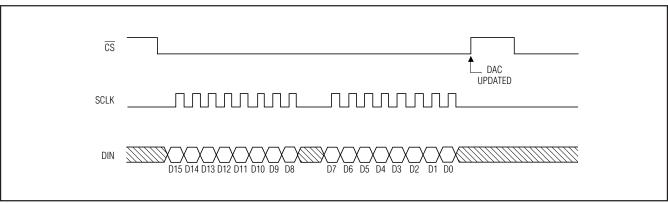


Figure 4. Complete 3-Wire Serial Interface Transmission

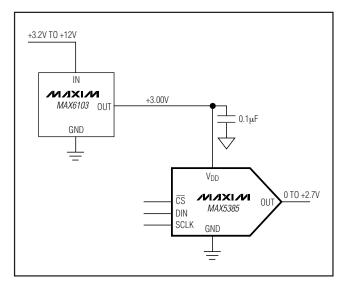


Figure 5. Powering the MAX5385 with a Precision Voltage Reference

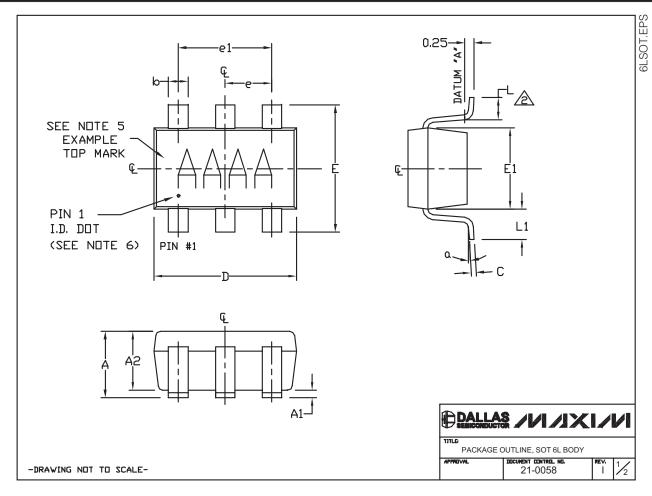
\_Chip Information

TRANSISTOR COUNT: 2160

### **Package Information**

For the latest package outline information and land patterns, go to <a href="www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SOT23	U6-4	<u>21-0058</u>
6 SOT23-Thin	Z6-1	<u>21-0114</u>



### Package Information (continued)

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#### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A &

- 3. PACKAGE DUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR, MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
- 4. PACKAGE DUTLINE INCLUSIVE OF SOLDER PLATING.
- 5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
- 6. PIN 1 I.D. DOT IS 0.3mm Ø MIN. LOCATED ABOVE PIN 1.
- 7. MEETS JEDEC MO178, VARIATION AB.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
- 9. LEAD TO BE COPLANAR WITHIN 0.1mm.
- 10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- 11. MARKING IS FOR PACKAGE DRIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX			
Α	0.90	1,25	1.45			
A1	0.00	0.05	0.15			
A2	0.90	1.10	1.30			
م	0.35	0.40	0.50			
C	0.08	0.15	0.20			
D	2.80	2.90	3.00			
Ε	2.60	2.80	3.00			
E1	1.50	1.625	1.75			
Г	0.35	0.45	0.60			
L1	0.60 REF.					
el	1.90 BSC.					
е	0.95 BSC.					
۵	0*	2.5*	10°			
פאכ כטובסי						

U6-1, U6-2, U6-4, U6C-8, U6SN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6

PACKAGE OUTLINE, SOT 6L BODY

APPROVAL

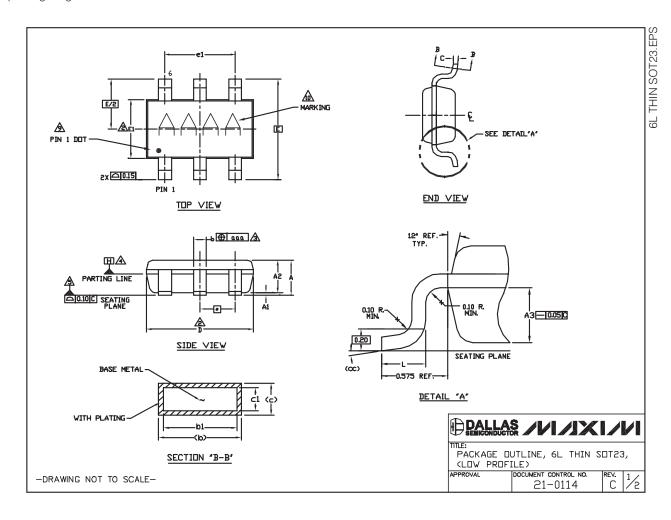
21-0058

REV. 2/2

-DRAWING NOT TO SCALE-

### Package Information (continued)

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#### NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.



'D' AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.



THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.



A. DATUM PLANE "H" LUCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.



THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. DINE PLANE IS THE SEATING PLANE, DATUM (-C-J) AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM (-C-J) IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO DINE ANOTHER WITH 0.10mm AT SEATING PLANE.

- THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
- 8. VARPAGE SHALL NOT EXCEED 0.10mm



9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.



10 MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS					
	MIN	NDM	MAX		
Α	-	-	1.10		
A1	0.00	0.075	0.10		
A2	0.85	0.88	0.90		
A3	0.50 BSC				
b	0.30	-	0.45		
b1	0.25	0.35	0.40		
c	0.15	-	0.20		
<b>c</b> 1	0.12	0.127	0.15		
D	2.80	2.90	3.00		
E	2.75 BSC				
E1	1.55	1.60	1.65		
L	0.30	0.40	0.50		
e1	1.90 BSC				
e	0.95 BSC				
$\infty$	0*	4*	8*		
aaa		0.20			
Pkg. codesi Z6-1; Z6-2					



PACKAGE DUTLINE, 6L THIN SDT23, (LOW PROFILE)

21-0114

С

-DRAWING NOT TO SCALE-

### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	1/09	Added lead-free designation to parts in the <i>Ordering Information</i> and added 21-0058 package diagram	1, 11

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