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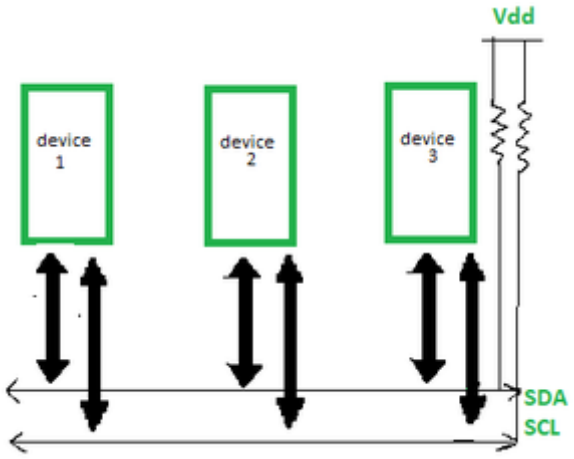
1. I2C PROTOCOL

I2C stands for Inter-Integrated Circuit**.** It is a bus interface connection protocol incorporated into devices for serial communication. It was originally designed by Philips Semiconductor in 1982. Recently, it is a widely used protocol for short-distance communication. It is also known as Two Wired Interface (TWI).

Working of I2C Communication Protocol :
It uses only 2 bi-directional open-drain lines for data communication called SDA and SCL. Both these lines are pulled high.
Serial Data (SDA) – Transfer of data takes place through this pin.
Serial Clock (SCL) – It carries the clock signal.

I2C operates in 2 modes –

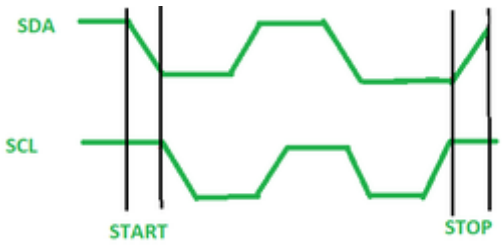
(i)Master mode
(ii)Slave mode
Each data bit transferred on SDA line is synchronized by a high to the low pulse of each clock on the SCL line.



According to I2C protocols, the data line can not change when the clock line is high, it can change only when the clock line is low. The 2 lines are open drain, hence a pull-up resistor is required so that the lines are high since the devices on the I2C bus are active low. The data is transmitted in the form of packets which comprises 9 bits. The sequence of these bits are –

1. **Start Condition** – 1 bit
2. **Slave Address** – 8 bit
3. **Acknowledge** – 1 bit

Start and Stop Conditions :
START and STOP can be generated by keeping the SCL line high and changing the level of SDA. To generate START condition the SDA is changed from high to low while keeping the SCL high. To generate STOP condition SDA goes from low to high while keeping the SCL high, as shown in the figure below.



Start and Stop Condition

Repeated Start Condition :
Between each start and stop condition pair, the bus is considered as busy and no master can take control of the bus. If the master tries to initiate a new transfer and does not want to release the bus before starting the new transfer, it issues a new START condition. It is called a REPEATED START condition.

Read/Write Bit :
A high Read/Write bit indicates that the master is sending the data to the slave, whereas a low Read/Write bit indicates that the master is receiving data from the slave.

ACK/NACK Bit :
After every data frame, follows an ACK/NACK bit. If the data frame is received successfully then ACK bit is sent to the sender by the receiver.

Addressing :
The address frame is the first frame after the start bit. The address of the slave with which the master wants to communicate is sent by the master to every slave connected with it. The slave then compares its own address with this address and sends ACK.

I2C Packet Format :
In the I2C communication protocol, the data is transmitted in the form of packets. These packets are 9 bits long, out of which the first 8 bits are put in SDA line and the 9th bit is reserved for ACK/NACK i.e. Acknowledge or Not Acknowledge by the receiver.

START condition plus **address packet** plus one more **data packet** plus **STOP condition** collectively form a complete **Data transfer.**

Features of I2C Communication Protocol :

- **Half-duplex Communication Protocol –**
  Bi-directional communication is possible but not simultaneously.
  - synchronous communication
    The data is transferred in the form of frames or blocks.
- Can be configured in a multi-master configuration.
- **Clock Stretching –**
  The clock is stretched when the slave device is not ready to accept more data by holding the SCL line low, hence disabling the master to raise the clock line. Master will not be able to raise the clock line because the wires are AND wired and wait until the slave releases the SCL line to show it is ready to transfer next bit.
- **Arbitration** –
  I2C protocol supports multi-master bus system but more than one bus can not be used simultaneously. The SDA and SCL are monitored by the masters. If the SDA is found high when it was supposed to be low it will be inferred that another master is active and hence it stops the transfer of data.
- Serial transmission
  I2C uses serial transmission for transmission of data.
- Used for low-speed communication

Advantages :

- Can be configured in multi-master mode.
- Complexity is reduced because it uses only 2 bi-directional lines (unlike SPI Communication).
- Cost-efficient.
- It uses ACK/NACK feature due to which it has improved error handling capabilities.

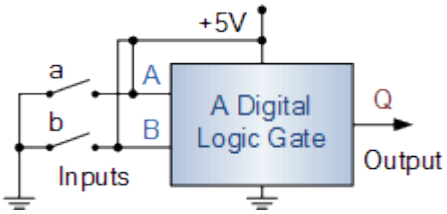
Limitations :

- Slower speed.
- Half-duplex communication is used in the I2C communication protocol

2. (A) PULL- UP RESISTOR

The most common method of ensuring that the inputs of digital logic gates and circuits can not self-bias and float about is to either connect the unused pins directly to ground (0V) for a

constant low “0” input, (OR and NOR gates) or directly to Vcc (+5V) for a constant high “1” input (AND and NAND gates). Ok, lets look again at our two switched inputs from above.



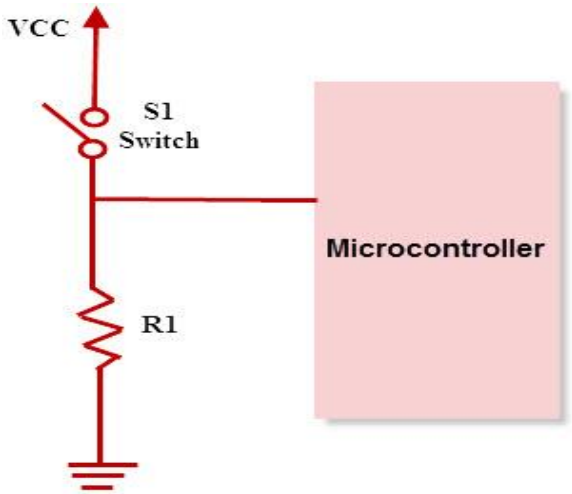
This time, to stop the two inputs, A and B, from “floating” about when the corresponding switches, “a” and “b” are open (OFF), the two inputs are connected to +5V supply.

You may think that this would work fine as when switch “a” is open (OFF), the input is connected to Vcc (+5V) and when the switch is closed (ON), the input is connected to ground as before, then inputs “A” or “B” always have a default state regardless of the position of the switch.

However, this is a bad condition because when either of the switches are closed (ON), there will be a direct short circuit between the +5V supply and ground, resulting in excessive current flow either blowing a fuse or damaging the circuit which is not good news. One way to overcome this issue is to use a pull-up resistor connected between the input pin and the +5V supply rail.

(B) PULL-DOWN RESISTOR

As pull up resistors, Pull-down resistors also works in the same way. But, they pull the pin to a low value. Pull-down resistors are connected between a particular pin on a microcontroller and the ground terminal. An example of a pull down resistor is a digital circuit shown in the figure below. A switch is connected between the VCC and the microcontroller pin. When the switch is closed in the circuit, the input of the microcontroller is logic 1,but when the switch is open in a circuit, the pull down resistor pulls down the input voltage to the ground (logic 0 or logic low value). The pull down resistor should have a higher resistance than the impedance of the logic circuit.



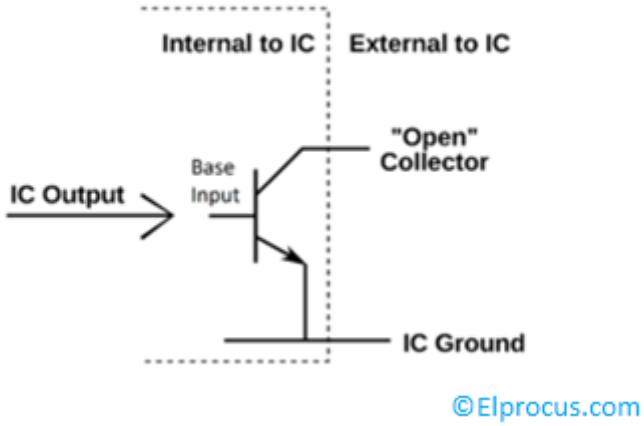
Pull-down Resistor

(C) OPEN DRAIN

An open-drain or open-collector output pin is simply a transistor that is connected to the ground. Whenever we apply high input at the gate, drain, and source are shorted. Whenever we apply low input at the gate, drain, and source are disconnected. To make it simple, open-drain is like a switch that will get connected or disconnected basing on the input signal given.

Open-Drain Input/Output Configuration

An open-drain is commonly found in many integrated circuits. This helps multiple devices to connect with the usage of single wire which is in a mode of pull-down operation. This single wire is also a bi-directional one so its bidirectional nature will gain so much importance to the circuit due to the interconnection of many devices on a common line. Coming to the configuration it is having programmable output configuration with push-pull. The operating of digital output is done in two modes one is a push-pull mode and another one is an open-drain mode.



(D)ACTIVE LOW AND ACTIVE HIGH

When working with ICs and microcontrollers, you'll likely encounter pins that are active-low and pins that are active-high. Simply put, this just describes how the pin is activated. If it's an active-low pin, you must "pull" that pin LOW by connecting it to ground. For an active high pin, you connect it to your HIGH voltage (usually 3.3V/5V).

For example, let's say you have a shift register that has a chip enable pin, CE. If you see the CE pin anywhere in the datasheet with a line over it like this, CE, then that pin is active-low. The CE pin would need to be pulled to GND in order for the chip to become enabled. If, however, the CE pin doesn't have a line over it, then it is active high, and it needs to be pulled HIGH in order to enable the pin.

Many ICs will have both active-low and active-high pins intermingled. Just be sure to double check for pin names that have a line over them. The line is used to represent NOT (also known as bar). When something is NOTTED, it changes to the opposite state. So if an active-high input is NOTTED, then it is now active-low

3. ROLE OF KERNEL IN LINUX

The **kernel** is often referred to as the core of any operating system, **Linux** included. It has complete control over everything in your system. In this stage of the **boot process**, the **kernel** that was selected by GRUB first mounts the root file system that's specified in the grub. conf file

4. FIRST IMPRESSION IN ZEPHYR RTOS

It is a free open source RTOS software that aims to be safety – certified.

The Zephyr Project aims to meet this need and plans to be the first in this category to submit its core OS, encompassing the kernel and OS services of the long term support (LTS) release for certification. These certificates are important as they indicate a product has undergone careful review and testing and is deemed trustworthy in safety-related systems.