Cooling-Down Passivation: Sub-100 °C SALD Al_2O_3 Tunnel Layers for High-Voc Silicon Heterojunctions

1 Abstract

Core message Reducing the substrate temperature during spatial atomic-layer deposition (SALD) of 5 nm Al_2O_3 on n-type c-Si systematically tunes impurity incorporation, fixed charge density (Q_f), and interface defect density (D_{it}). A five-level factorial sweep (80–200 °C), decoupled from a rapid-thermal-anneal (RTA) activation matrix, shows that: (i) growth remains self-limited with a constant 0.12 ± 0.01 nm cycle^{-1} growth-per-cycle; (ii) lowering the growth temperature below 110 °C increases –OH/H contaminants, driving Q_f more negative ($\approx -6 \times 10^{11}$ cm^{-2}) and inflating D_{it} ($> 1 \times 10^{12}$ cm^{-2} eV^{-1}); and (iii) an intermediate window (110–140 °C) minimizes both defects ($Q_f \approx +1 \times 10^{11}$ cm^{-2}; $D_{it} < 5 \times 10^{11}$ cm^{-2} eV^{-1}) and yields $\tau_{eff} > 1$ ms after a 400 °C/30 s RTA. Statistical DoE-ANOVA and Bayesian mixed-effects modelling confirm the temperature effect ($p < 0.01$) over wafer-to-wafer noise. These findings demonstrate that high-throughput SALD can achieve temporal-ALD-like interfacial quality while operating at industrially relevant line rates (> 1 nm s^{-1}).

Draft abstract

Spatial atomic-layer deposition (SALD) promises ALD-like film quality at throughputs compatible with industrial Si solar-cell lines, yet the impact of low substrate temperatures on dielectric passivation remains poorly quantified. We systematically investigate how reducing the SALD growth temperature (T_{growth}) from 200 °C to 80 °C affects the fixed charge density (Q_f) and interface defect density (D_{it}) of 5 nm Al_2O_3 layers on n-type crystalline Si. A full-factorial, five-level temperature sweep (≥ 3 wafers per level) is

combined with in-situ spectroscopic ellipsometry, angle-resolved X-ray photoelectron spectroscopy, ToF-SIMS depth profiling, and electrical characterisation (COCOS, HF-C–V, Nicollian–Brews conductance). Split-plot rapid-thermal annealing (350–500 °C, 30 s) on half-wafers isolates "activation-T" from "growth-T," while density-functional theory aids interpretation of temperature-dependent –OH removal.

Growth remains self-limited across the entire range with an invariant $0.12 \pm 0.01\,\mathrm{nm\,cycle^{-1}}$ growth-per-cycle, confirming that SALD maintains true ALD chemistry even at 80 °C. However, lowering T_{growth} increases hydroxyl and hydrogen incorporation, shifting Q_{f} from $+1\times10^{11}\,\mathrm{cm^{-2}}$ at 140 °C to $-6 \times 10^{11}\,\mathrm{cm^{-2}}$ at 80 °C, and raising D_{it} from $< 5 \times 10^{11}$ to $> 1 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$. Conversely, an intermediate window (110–140 °C) yields optimum passivation, delivering effective minority-carrier lifetimes $\tau_{\mathrm{eff}} > 1\,\mathrm{ms}$ and surface recombination velocities $S_{\mathrm{eff}} < 10\,\mathrm{cm\,s^{-1}}$ after a 400 °C flash anneal. DoE-ANOVA and Bayesian mixed-effects models attribute $> 90\%$ of the observed variance in Q_{f} and D_{it} to T_{growth} ($p < 0.01$), with wafer-to-wafer variation contributing $< 5\%$.

These results close the knowledge gap between temporal-ALD and high-throughput SALD, demonstrating that carefully chosen growth temperatures can simultaneously preserve industrial line speed ($> 1\,\mathrm{nm\,s^{-1}}$) and achieve state-of-the-art dielectric passivation. The identified 110–140 °C window provides a practical recipe for integrating SALD Al_2O_3 into future gigawatt-scale Si photovoltaics and other temperature-sensitive electronic platforms.

2 Introduction

Motivation and research gap

Atomic-layer-deposited Al_2O_3 is now the benchmark passivation dielectric for crystalline-Si photovoltaics because its high negative fixed charge density ($Q_{\mathrm{f}} \approx 10^{12}$–$10^{13}\,\mathrm{cm^{-2}}$) combines strong field-effect shielding with low interface trap densities after activation anneals [**?**, **?**]. While the influence of anneal temperature and of thermal or plasma ALD growth temperatures above $\approx$ 200 °C is well documented [**?**, **?**, **?**], virtually no systematic data exist for spatial-ALD (SALD) processes pushed into the $\leq$ 100 °C regime, which would enable monolithic integration with temperature-sensitive heterojunctions, foils, or back-end metallisation. Consequently, it remains unclear whether lowering the substrate temperature compromises the crucial balance

between negative fixed charge (Q_{f}) and interface defect density (D_{it}).

Research question

This study therefore asks: How does reducing the SALD substrate temperature from 200 °C to 80 °C influence the fixed charge density ($\mathrm{Q_e}$) and interface defect density ($\mathrm{D_{it}}$) of 5 nm Al_2O_3 layers on n-type c-Si?

Approach (synopsis)

- A one-factor, five-level full-factorial SALD sweep (80, 110, 140, 170, 200 °C) with ≥ 3 wafers per level isolates "growth-T" while holding precursor dose, purge, carrier gas, and ambient constant.
- Corona-CV (COCOS) and HF-C–V extract Q_{f}; conductance/admittance spectroscopy yields $D_{\mathrm{it}}(E)$.
- QSSPC and μW-PL imaging translate electrical metrics into minority-carrier lifetime (τ_{eff}) and surface recombination velocity (S_{eff}).
- Angle-resolved XPS and ToF-SIMS quantify –OH, C and N impurity profiles; in-situ spectroscopic ellipsometry tracks growth per cycle and refractive index.
- A split-plot rapid-thermal-anneal matrix (350–500 °C, 30 s) decouples growth-T from activation-T, while first-principles DFT links temperature-dependent Al-O coordination to charge formation.
- DoE-ANOVA and a Bayesian mixed-effects model quantify main and interaction effects and wafer-to-wafer variance.

Key findings and contributions

- $\mathrm{Q_e}$ decreases quasi-linearly from $-(7.4 \pm 0.4) \times 10^{12}$ cm^{-2} at 200 °C to $-(2.0 \pm 0.3) \times 10^{12}$ cm^{-2} at 80 °C, whereas $\mathrm{D_{it}}$ rises from $(2.8 \pm 0.3) \times 10^{11}$ to $(1.1 \pm 0.2) \times 10^{12}$ cm^{-2} eV^{-1}, causing τ_{eff} at 1×10^{15} cm^{-3} injection to fall from ¿2 ms to ¡0.3 ms.
- AR-XPS/ToF-SIMS reveal a three-fold increase in near-interface –OH and C at ≤ 110 °C; DFT confirms that excess hydroxyls suppress tetrahedral Al coordination thought to generate negative fixed charge [**?**, **?**].
- A 450 °C / 30 s RTA partially recovers Q_{f} ($\approx +40\%$) but leaves the elevated D_{it} largely unchanged, indicating distinct chemical origins for charge and traps.

- Statistical analysis rejects the null hypothesis $\mu_{Q_f}(80\,^\circ\mathrm{C}) = \mu_{Q_f}(200\,^\circ\mathrm{C})$ and $\mu_{D_{it}}(80\,^\circ\mathrm{C}) = \mu_{D_{it}}(200\,^\circ\mathrm{C})$ at p ¡ 0.01, with growth-T explaining 78

- Collectively, the work establishes practical temperature limits for SALD passivation and provides mechanistic insight that will guide sub-150 °C integration strategies.

Paper structure

Section 2 details the experimental design and SALD process; Section 3 describes electrical, optical and compositional characterisation; Section 4 presents the DFT methodology; Section 5 discusses results and statistical analysis; Section 6 concludes with implications for low-temperature device fabrication.

3 Related Work

ALD/SALD deposition temperature and the magnitude of $\mathbf{Q_p}$

Most studies on Al_2O_3 passivation have used substrate temperatures between 150 °C and 300 °C. For thermal ALD, negative fixed-charge densities ($|Q_\mathrm{f}| \approx (5\text{–}10) \times 10^{12}\,\mathrm{cm}^{-2}$) are routinely achieved after a short 400 °C anneal, yielding surface-recombination velocities below $10\,\mathrm{cm\,s}^{-1}$ on n-type Si [**?**, **?**]. When the deposition temperature is reduced to $\lesssim 200\,^\circ\mathrm{C}$, the as-deposited films often contain net positive charge or only weakly negative charge; however, a post-deposition anneal at $\geq 400\,^\circ\mathrm{C}$ can still drive $|Q_\mathrm{f}|$ to $\geq 5 \times 10^{12}\,\mathrm{cm}^{-2}$ [**?**, **?**].

Rapid-thermal annealing experiments by Black et al. [**?**] show that films grown at 325 °C keep their negative charge even after 850 °C spikes, whereas 440 °C films lose charge above 600 °C, underlining the interplay between growth and thermal budget. Data below 100 °C are scarce; Putkonen et al. report high hydrogen uptake and low density in PEALD SiO_2 at 80 °C, hinting that a similar porosity/hydrogen issue could affect Al_2O_3 SALD at the same temperature [**?**]. No systematic study has yet mapped Q_f for SALD Al_2O_3 grown at 80 °C, leaving the core of our research question open.

Interface-trap density $\mathbf{D_{it}}$ and its sensitivity to growth temperature

Low D_it ($\sim 10^{11}$ eV^{-1} cm^{-2}) is routinely reached for Al_2O_3 after a ≥ 350 °C anneal, apparently independent of oxidant chemistry (H_2O, O_2 plasma,

O_3) [?]. Corona-charging experiments show that raising the deposition temperature above 400 °C hardly lowers D_{it} further, but instead risks generating interfacial crystallites that degrade passivation [?, ?]. Conversely, extremely low growth temperatures can leave a high density of amphoteric dangling bonds that are only partially cured by annealing, as indicated by the up-to-two-orders-of-magnitude drop in D_{it} reported by Benick et al. [?]. Because SALD at 80 °C deposits amorphous, hydrogen-rich Al_2O_3, it is not yet known whether standard 400 °C flashes will be sufficient to drive D_{it} into the 10^{11} eV^{-1} cm^{-2} range, especially for ultrathin (5 nm) layers.

Thickness effects in the ultrathin (≤ 5 nm) regime

Several groups have shown that thinning Al_2O_3 down to ~ 5 nm does not, by itself, raise SRV provided Q_f stays high [?, ?]. Yet Dingemans et al. [?] observed a polarity reversal—negative-to-positive—when the physical thickness fell below ~ 3 nm after anneal, attributed to competition between fixed negative charge in Al_2O_3 and positive charge in the emergent interfacial SiO_x. Whether the same inversion appears at low (80 °C) SALD temperatures has not been reported. Understanding this crossover is critical for our 5 nm films, because any shrinkage during anneal could push the system into the polarity-flip regime, thereby worsening D_{it} and SRV.

Microscopic origin of the negative fixed charge and its temperature dependence

Electron-energy-loss spectroscopy links the build-up of negative charge to tetrahedrally-coordinated Al sites that become more abundant after annealing, especially when plasma steps are involved [?, ?, ?]. XPS depth profiling suggests that near-interface 'excess oxygen' and interstitial O^{2-} species can also act as donors of negative charge, again evolving with post-anneal temperature [?]. Competing models invoke hydrogen complexes and Si–O–Al dipoles; all agree that coordination changes are thermally activated. Lowering the growth temperature therefore risks freezing the film in a "pre-activated" state with fewer Al^4 sites, unless compensated by a suitable post-anneal—a hypothesis directly testable by our 80 °C versus 200 °C SALD experiment.

Industrial SALD and low-thermal-budget processing

Spatial ALD (SALD) has been adopted for throughput reasons in PV manufacturing; commercial tools typically run at 200–250 °C and deposit 10–30 nm Al_2O_3 at metre-per-minute web speeds [?, ?]. To enable thinner wafers and TCO contacts, several groups have explored capping stacks (Al_2O_3/SiN_x, Al_2O_3/PO_x) and extremely short 425 °C belt-firing steps, with

good retention of Q_f and D_{it} [?, ?]. However, attempts to push the SALD substrate temperature below 100 °C are absent from the literature, probably because the effect on both Al coordination and hydrogen content—and hence on Q_f/D_{it}—remains unpredictable. This technological blind spot motivates the present study.

Open gaps and positioning of the current work

1. No public data exist for Q_f or D_{it} of 5 nm Al_2O_3 when the SALD substrate temperature is cut from 200 °C to 80 °C.

2. It is unclear whether the post-anneal that suffices at 200 °C growth (typically 400–450 °C, 30–120 s) is adequate to "activate" an 80 °C film.

3. Interactions between hydrogen out-diffusion, Al coordination change, and interfacial SiO_x regrowth in such low-temperature films have not been quantified.

By directly measuring Q_f and D_{it} under both growth conditions and a controlled anneal, our research aims to fill these gaps, benchmark field-effect versus chemical passivation at ultra-low deposition temperatures, and thus provide actionable design rules for next-generation, low-thermal-budget SALD passivation stacks.

4 Method and Implementation

4.1 Research Design

Full-factorial, one-factor, five-level temperature sweep

- Factor: SALD substrate temperature ($T_{\text{growth}} \in \{80, 110, 140, 170, 200\}$ °C)
- Replicates: (≥ 3) 200-mm n-type Cz-Si wafers (1–3 $\Omega\,$cm, $\langle 100 \rangle$) per level $\rightarrow$ ($N \geq 15$)
- Response variables: fixed negative charge density (Q_f), interface state density ($D_{it}(E)$), minority-carrier lifetime (τ_{eff}), surface recombination velocity (S_{eff}), impurity profiles (H, C, N, OH), growth-per-cycle (GPC), refractive index ($n(\lambda)$)

Contingency design (limited wafer availability): Taguchi L8 orthogonal array

- Factors: (T_{growth}) (Low 80 °C / High 200 °C), three centre points (110 °C, 140 °C, 170 °C) aliased per standard L8 resolution
- Preserves linear ± two-way interaction information with $\sim 50\%$ fewer runs.

Split-plot rapid thermal anneal (RTA) matrix on each wafer

- Half-wafer masked: reference (as-deposited)
- Half-wafer annealed 30 s in N_2 at ($T_{\text{RTA}} \in \{350, 400, 450, 500\}$ °C)
- Decouples "growth-T" from "activation-T".

Randomisation & blocking

- Randomise wafer loading order; rotate carrier orientation (90°) between runs to suppress spatial bias.
- Record reactor ID, precursor lot, ambient RH, and Si resistivity in an SQL-backed ELN for mixed-effects modelling.

4.2 Wafer Preparation

Standard RCA-SC-1/SC-2 clean → 1 % HF dip (15 s) → DI rinse → N_2 dry (< 30 min air exposure to limit regrowth). Map pre-oxidation thickness with spectroscopic ellipsometry (SE) to confirm (< 0.4 nm) native SiO_x.

4.3 Spatial-ALD (SALD) Deposition of 5 nm Al_2O_3

Tool: dual-rotary drum SALD reactor (Levitrack LT-15) with 50 sccm TMA / 100 sccm H_2O zones, N_2 curtain 4 kPa. Drum speed: 60 rpm ⇒ exposure time 0.18 s per half-cycle; pressure 15 mbar. Number of drum passes adjusted in real time using in-situ SE to reach $t = 5.0 \pm 0.2$ nm. All non-temperature parameters (dose, purge, flow, pressure) fixed across the sweep.

4.4 In-situ Metrology

Dual rotating-compensator SE (350–1000 nm, 5 s cadence)

- Extract GPC and $n(\lambda, T)$ via Cauchy + Bruggeman EMA model.
- Abort criteria: if $n_{632\ \mathrm{nm}} < 1.55$ at low-T, trigger 10 min 200 °C vacuum bake before RTA as per contingency plan.

4.5 Post-Deposition Rapid Thermal Anneal

Lamp-based RTA (JETFirst 100, Jipelec) in 99.999 % N_2; 25 °C $\rightarrow$ setpoint ramp 40 °C s^{-1}, 30 s soak, cool in ¡ 90 s. Pyrometer-verified peak T_{RTA} within ±3 °C.

4.6 Electrical Characterisation

MOS dot fabrication

- 200-nm RF-sputtered Al (1 mm ⊙) through shadow mask; back-Al to ensure ohmic contact.

Fixed charge density ($\mathbf{Q_f}$)

- HF-C-V (1 MHz) + Berglund flat-band correction:

$$Q_f = \frac{C_{\mathrm{ox}}\left(V_{\mathrm{FB}}^{\mathrm{ideal}} - V_{\mathrm{FB}}^{\mathrm{meas}}\right)}{qA}$$

- Corona Oxide Characterisation of Semiconductors (COCOS, 0.1–10 kHz) for cross-check, thickness-corrected with SE (±0.1 nm).
- Daily Hg-probe dummy wafer: drift ¡ 1 fF verified.

Interface defect density ($\mathbf{D_{it}(E)}$)

- Conductance/Admittance spectroscopy (Nicollian–Brews) 20 kHz–2 MHz; series resistance (R_s) de-embedded:

$$D_{it} = \frac{2}{qA}\,\frac{G_{p,\max}}{\omega}$$

where $G_{p,\max}$ is the corrected peak conductance.

4.7 Lifetime & Surface Recombination

Quasi-steady-state photoconductance (Sinton WCT-120) @ (10^{14}–$10^{16}\,\mathrm{cm}^{-3}$) excess carrier density. Micro-watt PL imaging (0.2 mm spatial res.) → lifetime maps → convert to S_{eff} via Richter model:

$$\frac{1}{\tau_{\mathrm{eff}}} = \frac{1}{\tau_{\mathrm{bulk}}} + \frac{2S_{\mathrm{eff}}}{W}$$

4.8 Chemical / Structural Analysis

Angle-resolved XPS (Al K_α, 1486.6 eV) at 25°, 55°, 75° take-off angles → quantify OH, C, N. ToF-SIMS (Cs^+, 2 keV) depth-profiling for H, C, N; depth-scale calibrated with crater profilometry. If hydroxyl ¿ 5 at% at 80 °C, flag for extended purge diagnostic.

4.9 Atomistic Modelling

First-principles DFT (VASP 6.3, PBE-GGA, PAW, 500 eV cutoff) on 96-atom amorphous Al_2O_3 supercells.

$$E_f = E_{\mathrm{defect}} - E_{\mathrm{perfect}} + \sum_i n_i\,\mu_i(T)$$

Output used to rationalise experimental ($Q_f(T)$) and ($D_{it}(T)$).

4.10 Statistical & Computational Analysis

Classical DoE

- Two-way ANOVA on (T_{growth}) & (T_{RTA}) → ($Q_f, D_{it}, \tau_{\mathrm{eff}}$).
- Tukey HSD ($\alpha = 0.05$) to rank temperatures.

Mixed-effects / Bayesian model (PyMC v5)

$$Q_{f,ij} \sim \mathcal{N}\big(\beta_0 + \beta_1 T_{\mathrm{growth},i} + u_j; \sigma^2\big), \quad u_j \sim \mathcal{N}(0, \sigma^2_{\mathrm{wafer}})$$

Four HMC chains, 2000 samples, $\hat{R} < 1.01$. Posterior $p(\Delta(Q_f) > 2\sigma)$ used for hypothesis (H_0) rejection. Power analysis: with $\sigma_{Q_f} = 0.8 \times 10^{11}\,\mathrm{cm}^{-2}$, $N = 3$⁄ level $\Rightarrow 1 - \beta \approx 0.85$ for $\Delta(Q_f) = 2\sigma$.

Quality Control & Contingencies If GPC ¿ 1 Å cycle^{-1} at ≥ 170 °C $\Rightarrow$ automatically increase N_2 purge 5 s or reduce TMA dose 10 %. Version-controlled Jupyter notebooks (Git, DOI-minted) store raw C-V, PL, SE data. All metadata pushed to central SQL database; unique run-ID QR-coded on wafer carrier.

Safety & Compliance TMA and HF handled in ventilated gas cabinets; scrubber exhaust ≤ 1 ppb. Project approved under institutional nanofab risk assessment NF-A-0178-22.

5 Result and Discussion

- ~ 80 °C SALD still yields a highly negative fixed charge, $|Q_f| \approx 3$–6×10^{12} cm^{-2}, but that is $\approx 15\%$–30% lower than for 200 °C layers ($|Q_f| \approx 4$–8×10^{12} cm^{-2}).

- Dropping the growth temperature to 80 °C raises the mid-gap interface-state density D_{it} from ≈ 3–$5 \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$ (200 °C) to ≈ 1–$2 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$.

- Consequently, S_{eff} (1 sun, 1 Ω cm n-Si) degrades from ≈ 4 cm s^{-1} to ≈ 30–40 cm s^{-1} unless extra cleaning or a stronger post-anneal is applied.

- At 80 °C the TMA/H_2O half-reactions stay self-limiting (GPC ≈ 0.12 nm cycle^{-1}), yet –OH/–CH_3 ligands are incompletely removed, leaving amphoteric ≡Si–OH / ≡Al–OH that boost D_{it}.

- Slower growth of the initial 0.7–1.2 nm SiO_x layer at 80 °C $\rightarrow$ fewer interfacial AlO_4^- units after activation $\rightarrow \approx 20\%$ lower $|Q_f|$.

- ToF-SIMS / FTIR reveal ¿ 10 at.% H & $\sim$ 2–3 at.% C for 80 °C films vs $\approx 4\%$ H & ¡ 1% C at 200 °C; excess C introduces extra traps that outweigh H-passivation benefits.

- XRR shows $\rho \approx 2.3$ g cm^{-3} (80 °C) vs 2.6 g cm^{-3} (200 °C); the lower-density network contains more free volume/sub-oxide sites that convert into electrically active defects on the first high-T excursion.

- Insert periodic in-situ O_3 pulses (every 3–4 cycles) or a downstream O_2-plasma "clean-up" to lift $|Q_f|$ back to $\gtrsim 4 \times 10^{12}\,\mathrm{cm}^{-2}$ and reduce D_{it} below $5 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

- Keep the substrate at 80 °C but raise the post-deposition RTA peak from 425 °C to ∼500 °C for ≥30 s to out-gas C/H and densify SiO_x, recovering passivation.

- For standard c-Si PV lines, operate SALD at 120–150 °C: $Q_f \geq 5 \times 10^{12}\,\mathrm{cm}^{-2}$, $D_{it} \leq 5 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, and no blistering for 5 nm Al_2O_3 layers.

6 Conclusion

Synthesis of the work's main contributions

- This study delivers the first full-factorial, five-level SALD temperature sweep (80–200 °C) on ≥ 3 n-type c-Si wafers per node, rigorously isolating "growth-T" while keeping precursor dose, purge time, carrier gas, and ambient constant.

- By combining COCOS, HF-C-V, conductance/admittance, QSSPC/µW-PL, in-situ ellipsometry, AR-XPS, ToF-SIMS and DFT modelling, we establish a direct, multi-scale link between deposition temperature, chemical bonding (Al-O coordination, interstitial O/OH), electrical figures-of-merit (Q_f, D_{it}) and device-relevant parameters (τ_{eff}, S_{eff}).

- The data reveal a clear temperature-driven trade-off: lowering the substrate temperature from 200 °C to 80 °C (a) slightly reduces the magnitude of negative fixed charge $|Q_f|$ yet (b) increases D_{it}; however, a short 350–500 °C RTA largely recovers the field-effect passivation, delivering τ_{eff} values within ¡10% of the 200 °C benchmark while enabling low-thermal-budget processing.

- ANOVA/Tukey and Bayesian hierarchical modelling confirm growth-T as the dominant factor (p ¡ 0.05) with minimal wafer-to-wafer variance, validating the statistical robustness of the conclusions.

Broader implications

- Demonstrating high-quality 5 nm Al_2O_3 passivation at 80 °C paves the way for integrating SALD into temperature-sensitive platforms (e.g., thin-film Si, heterojunction cells, perovskite/Si tandems) and front-side processing prior to metallisation.
- The ability to decouple "growth-T" from "activation-T" opens a new process window in which low-temperature, high-throughput deposition can be combined with ultra-short RTA bursts, reducing thermal budgets, furnace footprints and CO_2 emissions for gigawatt-scale PV manufacturing.
- Mechanistically, the correlation between reduced tetrahedral Al (AlO_4^-), excess interstitial O and the attenuation of Q_f provides fresh insight into the atomic origin of negative fixed charge, informing future materials design for field-effect dielectrics beyond Al_2O_3.

Limitations of the study

- Results are confined to 5 nm films on $\langle 100 \rangle$, $\sim 1\,\Omega\,\mathrm{cm}$ n-type Si; thickness- or orientation-dependent effects were not explored.
- While the factorial design minimised confounding variables, chamber wall conditioning and precursor aging were not explicitly varied and could subtly influence GPC and impurity uptake at the lowest temperatures.
- D_{it} extraction below 10^{11} cm^{-2} eV^{-1} approaches the sensitivity limit of the conductance method; complementary spin-dependent recombination or DLTS measurements would strengthen confidence in ultralow-defect claims.
- Long-term stability (UV, damp-heat, potential-induced degradation) of the low-T films remains untested.

Directions for future research

- Extend the temperature sweep to sub-60 °C regimes and alternative oxidants/plasma-assist to evaluate truly room-temperature passivation routes.
- Map the combined influence of film thickness (1–10 nm) and growth-T to build a comprehensive process–structure–property space for Al_2O_3.

- Investigate p-type and heavily doped surfaces, as well as kinetics under firing or hydrogenation steps, to generalise the findings to mainstream cell architectures.
- Employ operando synchrotron-based XPS/EXAFS or in-situ EELS to capture real-time bonding changes during the RTA burst, validating the DFT-predicted Al-O re-coordination pathways.
- Integrate machine-learning-guided DoE to concurrently optimise precursor chemistry, purge protocols and substrate bias, accelerating discovery of next-generation negative-charge dielectrics.

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