

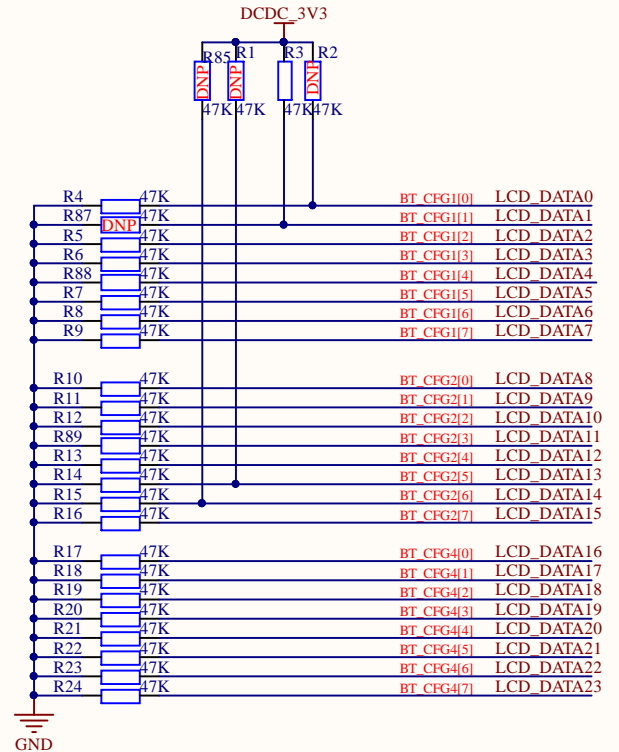
BOOT MAP

	0/1	0/1	0/1	1	0	0	0	0
TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved	DDRSMP: "000" : Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDMC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Self for SDR50 and SDR104 only 0 - through SD pad 1 - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Self for SDR50 and SDR104 only 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE	Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		NAND Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		NAND Row address, bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

	0	0	0	0	1	0	0	0
TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	Half Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock	Full Speed Delay selection 00 - 1 01 - 2 10 - 4 11 - Reserved	Full Speed Phase Selection 0 - select sampling at non-inverted clock 1 - select sampling at inverted clock	Full Speed Delay selection 00 - 1 01 - 2 10 - 4 11 - Reserved	Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A-D[16] 01 - A-DH 10 - A-DL 11 - Reserved	OneWord Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved		Reserved	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step "00" - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 100 - 16-bit 101 - 32-bit 110 - 64-bit 111 - 128-bit Else - reserved		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved		Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Reserved
NAND	Toggle Mode (SMBus Prescaler Delay, Read Latency): "00" - 16 GPMACIA cycles "001" - 1 GPMACIA cycles "010" - 2 GPMACIA cycles "011" - 3 GPMACIA cycles "100" - 4 GPMACIA cycles "101" - 5 GPMACIA cycles "110" - 6 GPMACIA cycles "111" - 7 GPMACIA cycles		BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Boot Frequencies (ARM/DSP) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Read Time 0 - 12ms 1 - 22ms (LBA NAND)	Reserved	Reserved

TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
0x450	Infnit-Loop (Debug USE only) 0 - Disable 1 - Enable	EEPROM Recovery Enable "0" - Disabled "1" - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Port Select: 000 - eCSPI0 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
0x460	L2_HW_INVALIDATE_DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460	Reserved (DDR3 config options)							
0x460	JTAG_SMODE[1:0]	WDG_ENABLE "0" - Disabled "1" - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved	Reserved
0x460	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x470	DLL Override: 0 - DLL Slave Mode for SD/eMMC 1 - DLL Override Mode for SD/eMMC	Reserved	SD2 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved	Disable SDRAM Manufacture mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT MMU_DISABLE	Override Pad Settings (using PAD_SETTINGS value)
0x470	Reserved for unexpected requirements	eMMC 4.4 - RESET TO PRE-IDLE STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 22K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	USDHC_IOMUX_SION_BIT_ENABLE 0 - Disable 1 - Enable	USDHC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470	USDHC_CMD_OE_PRE_EN (SD/MMC debug)	LPB_BOOT (Core / DDR - Bus) "00" - LPB Disable "01" - 1 GPIO (def freq) "10" - Div by 2 "11" - Div by 4	BT_LPB_POLARITY (GPIO polarity)		POWER_MNG_CFG (LDO's DCDC's) (Reserved - NOT USED)			
0x470	Override NAND Pad Settings (using PAD_SETTINGS value)	MMC_DLL_DLY[6:0] Delay target for SD/eMMC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						

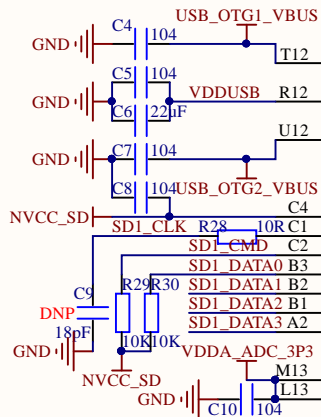
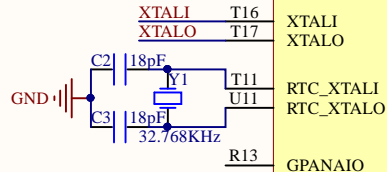
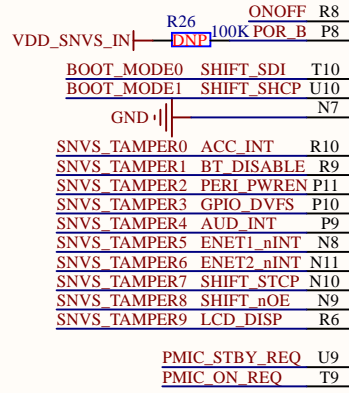
#Boot map pictures reference from the NXP I.MX6ULL EVK Board Schematic



BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot(Development)
11	Reserved

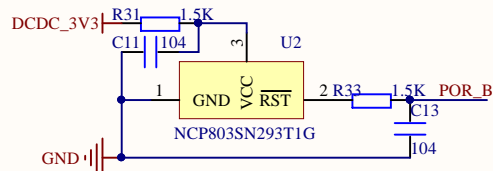
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Date: 2019-12-03	File: IMX6ULL_CORE_BOOT.SchDoc	
Revision: *	Version: V1.0	

IMX6ULL

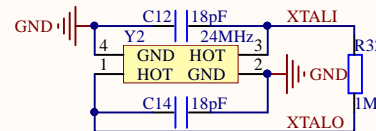


MCIMX6Y2CVM05AB

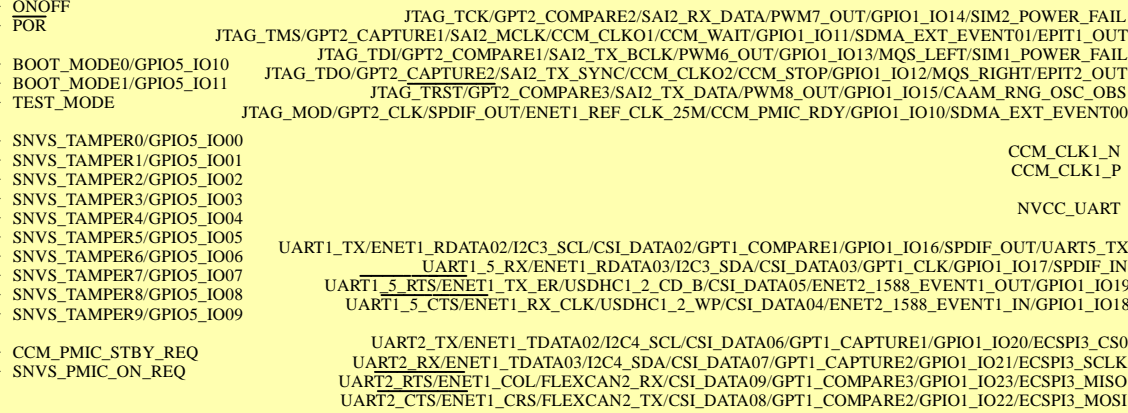
RESET



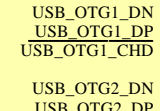
XTAL



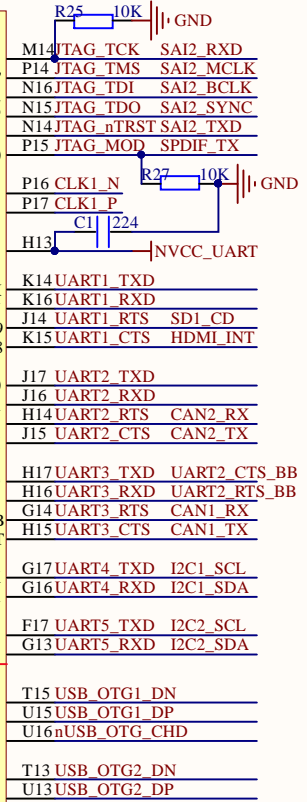
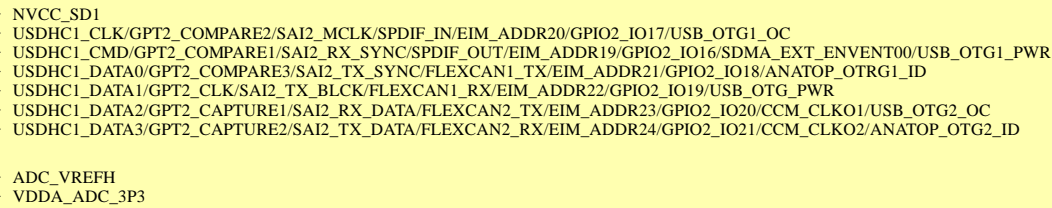
IMX6ULL-CONTROL



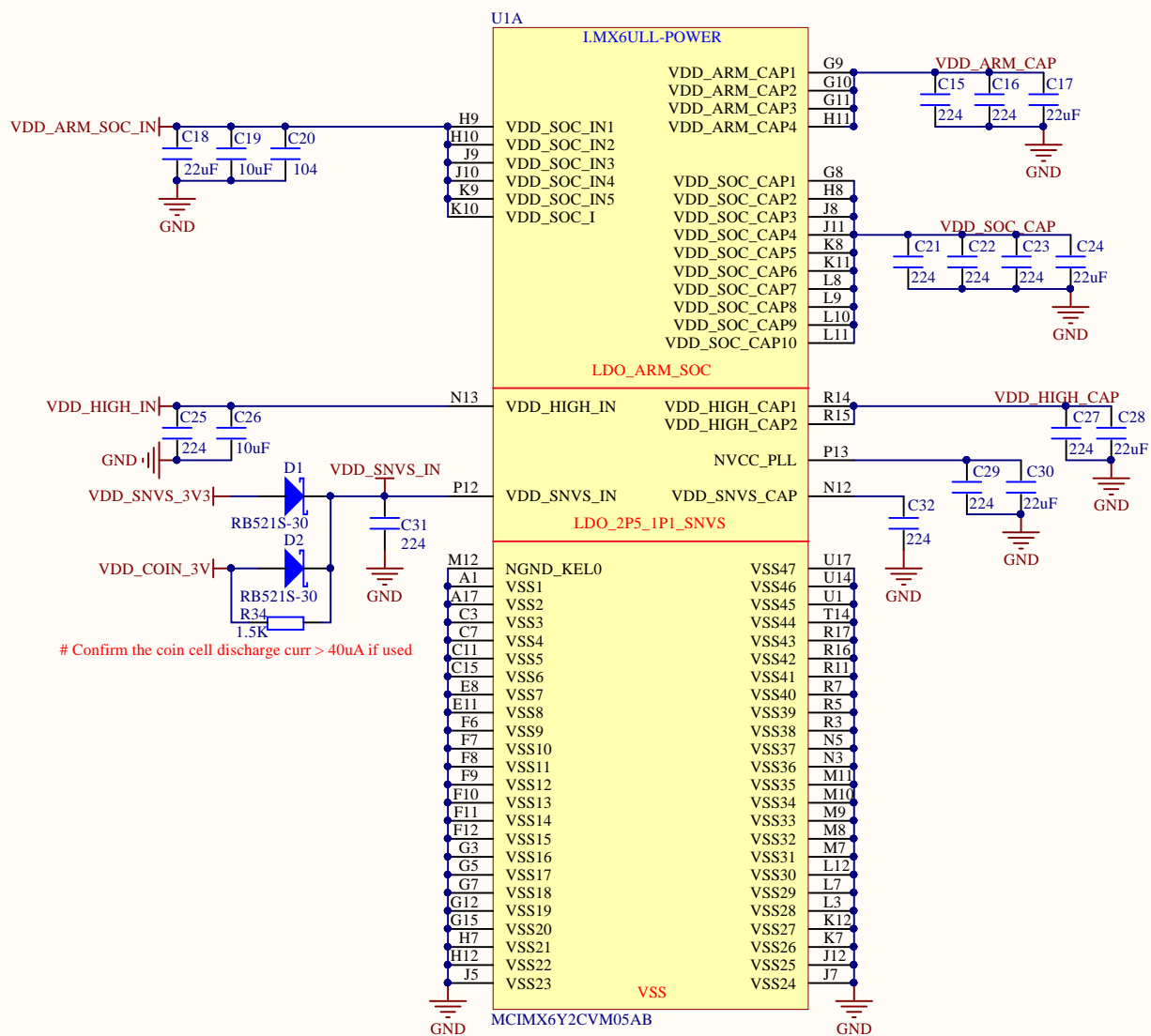
IMX6ULL-USB



IMX6ULL-SD1\ADC

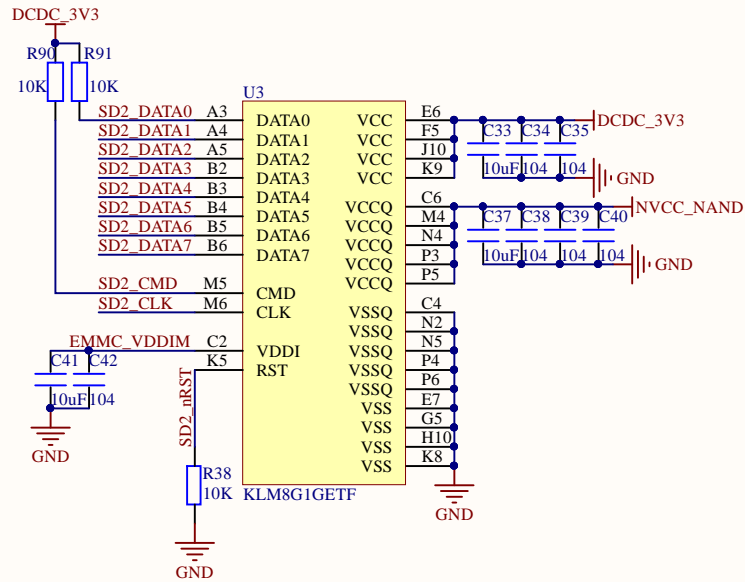


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Author: lycreturn@ALIENTEK	Size: A3	
Date: 2019-12-03	File: IMX6ULL_CORE_CONTROL.SchDoc	
Revision:		

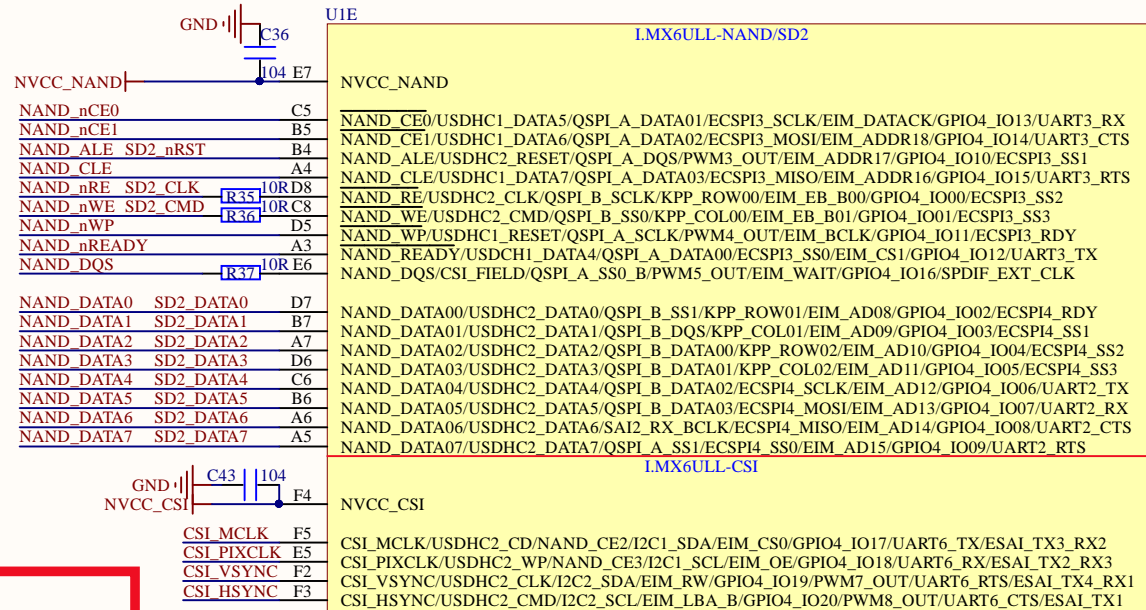


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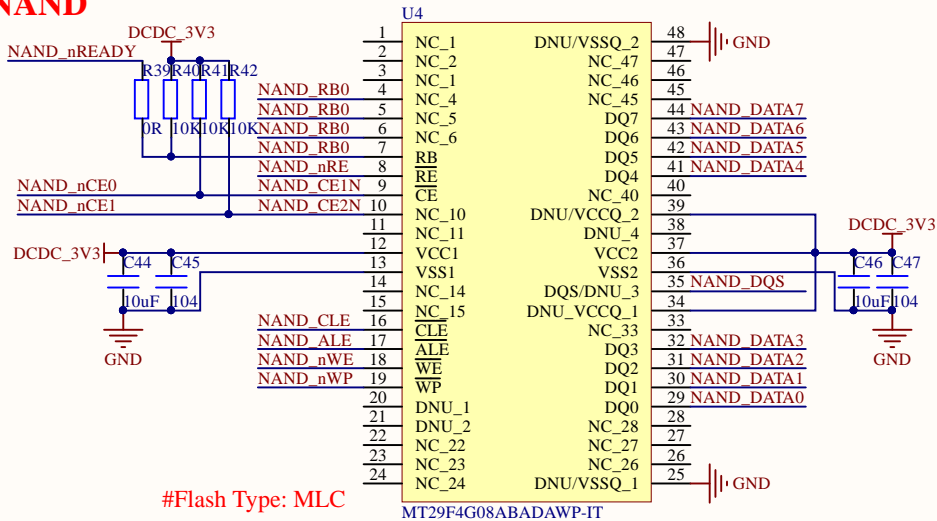
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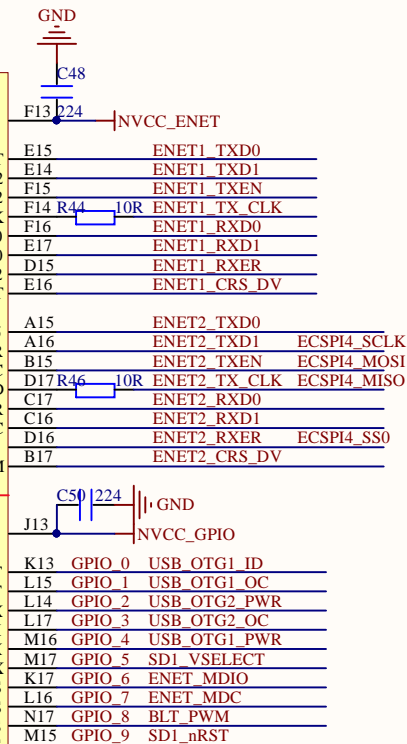
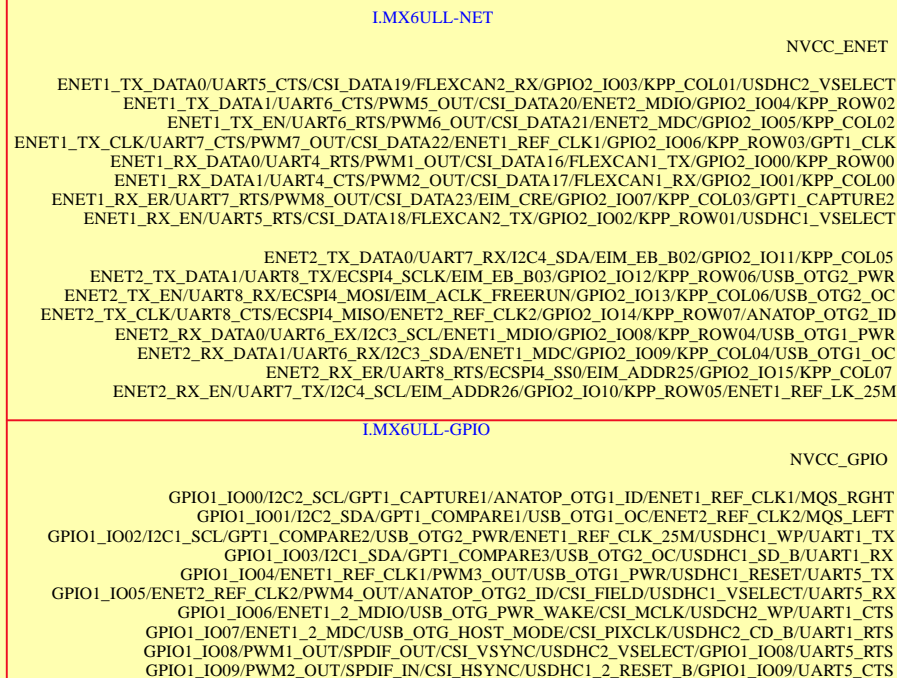
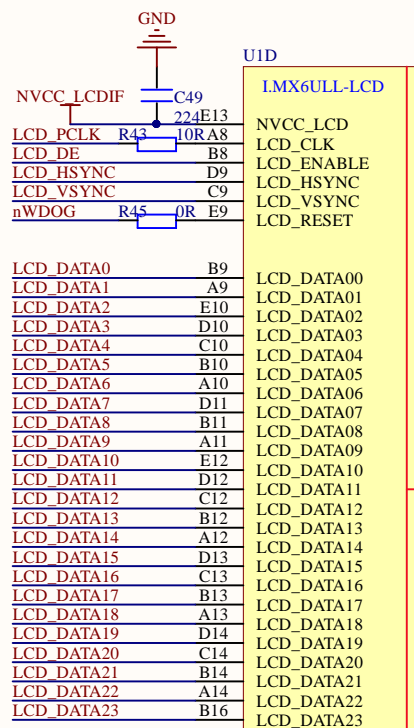
IMX6ULL_NAND



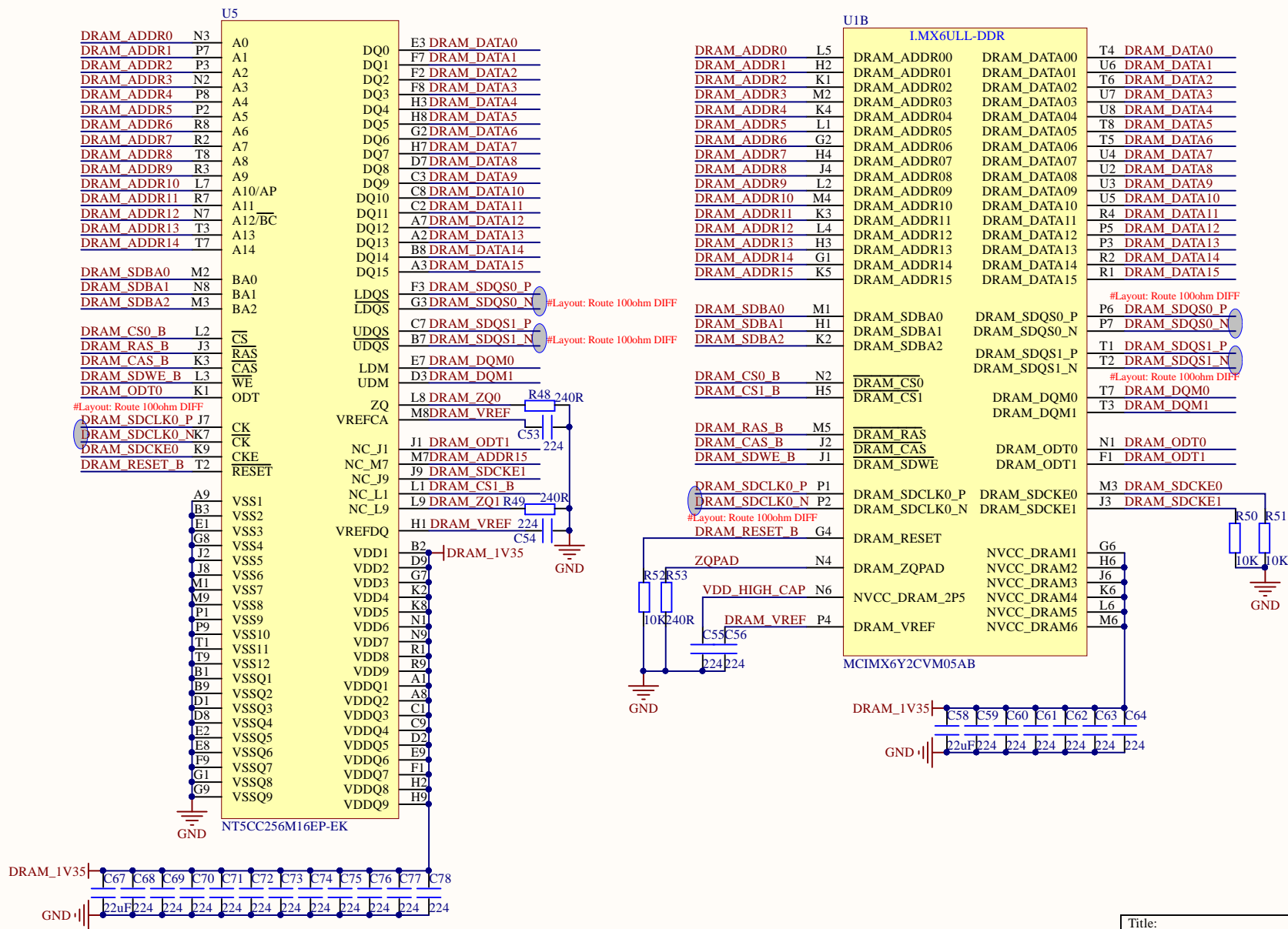
NAND



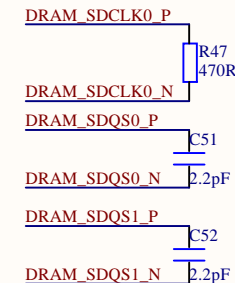
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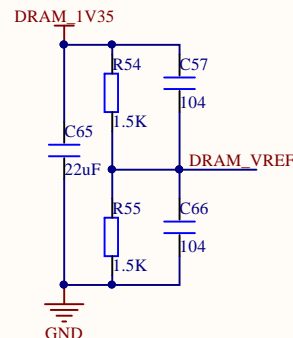
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Author: lycretun@ALIENTEK	Size: A4	
Date: 2019-12-03	File: IMX6ULL_CORE_LCDNET.SchDoc	
Revision:	Version: V1.0	



Note:
CLK termination: Place RXX close to U2



DDR3 VREF
#Note: 1K/1.5K are OK



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Date: 2019-12-03	File: IMX6ULL_CORE_LVDDR3.SchDoc	
Revision: *	Version: V1.0	

A

A

B

B

C

C

D

D



CSI_HSYNC	J1	1	60	CSI_VSYNC
CSI_MCLK	2	59	CSI_DATA3	
CSI_DATA2	3	58	CSI_DATA7	
CSI_DATA6	4	57	CSI_DATA1	
CSI_PIXCLK	5	56	CSI_DATA0	
CSI_DATA5	6	55	CSI_DATA4	
LCD_DATA0	7	54	SD1_CLK	
LCD_DATA1	8	53	SD1_CMD	
LCD_DATA2	9	52	SD1_DATA2	
LCD_DATA3	10	51	SD1_DATA3	
LCD_DATA4	11	50	SD1_DATA1	
LCD_DATA5	12	49	SD1_DATA0	
LCD_DATA6	13	48	SNVS_TAMPER9 LCD_DISP	
LCD_DATA7	14	47	GPIO_5 SD1_VSELECT	
LCD_DATA8	15	46	LCD_DE	
LCD_DATA9	16	45	LCD_PCLK	
LCD_DATA10	17	44	LCD_HSYNC	
LCD_DATA11	18	43	LCD_VSYNC	
LCD_DATA12	19	42		
LCD_DATA13	20	41	PMIC_ON_REQ	
LCD_DATA14	21	40	RESET	
LCD_DATA15	22	39	SNVS_TAMPER6 ENET2_INT	
LCD_DATA16	23	38	ENET2_RXD0	
LCD_DATA17	24	37	ENET2_RXD1	
LCD_DATA18	25	36	ENET2_TXD0	
LCD_DATA19	26	35	ENET2_TXD1	
LCD_DATA20	27	34	ENET2_RXER	
LCD_DATA21	28	33	ENET2_CRS_DV	
LCD_DATA22	29	32	ENET2_TXEN	
LCD_DATA23	30	31	ENET2_TX_CLK	

VDD_COIN_3V

3710M060046G3FT01

DC5V	J2	1	60	
DC5V	2	59	USB_OTG2_VBUS	GND
SNVS_TAMPER4	3	58	USB_OTG1_VBUS	GND
ONOFF	4	57	USB_OTG2_DP	
SNVS_TAMPER1 BEEP	5	56	USB_OTG2_DN	
SNVS_TAMPER0 9D_INT	6	55	USB_OTG1_DP	
BOOT_MODE0 SHIFT_SDI	7	54	USB_OTG1_DN	
BOOT_MODE1 SHIFT_SHCP	8	53	nUSB_OTG_CHD	
SNVS_TAMPER8 SHIFT_nOE	9	52	GPIO_0 USB_OTG1_ID	
SNVS_TAMPER7 SHIFT_STCP	10	51	UART1_TXD	
SNVS_TAMPER5 ENET1_INT	11	50	GPIO_1 KEY0	
SNVS_TAMPER2 PERI_PWREN	12	49	UART1_CTS KEY2	
GPIO_2 KEY1	13	48	GPIO_3 LED0	
GPIO_4 LED1	14	47	UART1_RXD	
GPIO_9 SD1_nRST	15	46	GPIO_7 MDC	
GPIO_8 BLT_PWM	16	45	GPIO_6 MDIO	
JTAG_TDI SAI2_TX_BCLK	17	44	UART1_RTS USDHC1_CD_B	
JTAG_TDO SAI2_TX_SYNC	18	43	UART2_TXD	
JTAG_TCK SAI2_RX_DATA	19	42	UART2_RXD	
JTAG_TMS SAI2_MCLK	20	41	UART2_RTS CAN2_RX	
JTAG_nTRST SAI2_TX_DATA	21	40	UART2_CTS CAN2_TX	
JTAG_MOD SPDIF_OUT	22	39	UART3_TXD	
ENET1_TXD0	23	38	UART3_RXD	
ENET1_RXD1	24	37	UART3_CTS CAN1_TX	
ENET1_CRS_DV	25	36	UART3_RTS CAN1_RX	
ENET1_RXD0	26	35	UART4_RXD I2C1_SDA	
ENET1_TXEN	27	34	UART4_TXD I2C1_SCL	
ENET1_TXD1	28	33	UART5_RXD I2C2_SDA	
ENET1_TX_CLK	29	32	UART5_TXD I2C2_SCL	
ENET1_RXER	30	31		

3710M060046G3FT01

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