A Report On

Assignment -2

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by

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FOR THE COURSE

ELP736

Physical Design Laboratory

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Problem Statement

Perform the following task in INNOVUS
1) Partitioning: breaks up a circuit into smaller sub-circuits or modules that can be designed or analyzed individually.
2) Floorplanning: determines the shapes and arrangement of sub-circuits or modules, as well as the locations of external ports and IP or macro-blocks
Task to be done in GENUS

Design Frequency Specifications:

wclk: 100MHz
rclk: 300MHz

Annexures:

a. Work area path:
/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2
b. GitHub ID:
https://github.com/DJ-dineshjoshi/async_fifo/tree/main/assignment2
c. The floorplan is located at below path. Also it has been uploaded onto github.
/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr/fifo_floorplan

1. Partitioning

The partitioning has been done with the below steps:

a. The design is loaded into innovus tool using File > Import Design > Load.
b. The already configured Default.globals file is picked. The Default.global contains the netlist path, the top module name, the lef file and the mmmc file information.

```
 1 ############################################################
 2 #  Generated by:      Cadence Innovus 16.26-s040_1
 3 #  OS:                Linux x86_64(Host ID hertz1)
 4 #  Generated on:      Tue Mar 15 23:17:56 2022
 5 #  Design:
 6 #  Command:           save_global Default.globals
 7 ############################################################
 8 #
 9 # Version 1.1
10 #
11
12 set ::TimeLib::tsgMarkCellLatchConstructFlag 1
13 set conf_qxconf_file {NULL}
14 set conf_qxlib_file {NULL}
15 set defHierChar {/}
16 set distributed_client_message_echo {1}
17 set distributed_mmmc_disable_reports_auto_redirection {0}
18 set eco_post_client_restore_command {update_timing ; write_eco_opt_db ;}
19 set init_gnd_net {VSS}
20 set init_lef_file {../synth/lef/tf/uk65lscllmvbbr_6m1t0f.lef ../synth/lef/uk65lscllmvbbr.lef}
21 set init_mmmc_file {Default.view}
22 set init_pwr_net {VDD}
23 set init_top_cell {fifo}
24 set init_verilog {../synth/netlist/fifo_post_opt.v}
25 set latch_time_borrow_mode max_borrow
26 set pegDefaultResScaleFactor 1
27 set pegDetailResScaleFactor 1
28 set report_inactive_arcs_format {from to when arc_type sense reason}
29 set tso_post_client_restore_command {update_timing ; write_eco_opt_db ;}
30
~
~
~
Default.globals [RO]
```

Fig: Default.globals file contents

c. The mmmc file is also created beforehand and indicated in figure below

```
1 # Version:1.0 MMMC View Definition File
2 # Do Not Remove Above Line
3 create_rc_corner -name Default_rc_corner -preRoute_res {1.0} -preRoute_cap {1.0} -preRoute_clkres {0.0} -p
  reRoute_clkcap {0.0} -postRoute_res {1.0} -postRoute_cap {1.0} -postRoute_xcap {1.0} -postRoute_clkres {0.
  0} -postRoute_clkcap {0.0} -cap_table {/afs/iitd.ac.in/user/e/ee/een202501/Music/counter_design_database_4
  5nm/captable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl}
4 create_library_set -name typ_time_library -timing {/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/
  libraries/UMC65LLSC/synopsys/ccs/uk65lscllmvbbr_100c25_tc_ccs.lib}
5 create_constraint_mode -name fifo_constraints -sdc_files {/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assig
  nments/assignment2/synth/sdc/fifo.sdc}
6 create_delay_corner -name typ_delay_corner -library_set {typ_time_library} -rc_corner {Default_rc_corner}
7 create_analysis_view -name typ_case -constraint_mode {fifo_constraints} -delay_corner {typ_delay_corner}
8 set_analysis_view -setup {typ_case} -hold {typ_case}
```

Fig: Default.view file contents (The MMMC file contents)

d. After loading the design, the layout viewer in the innovus tool shows the grids

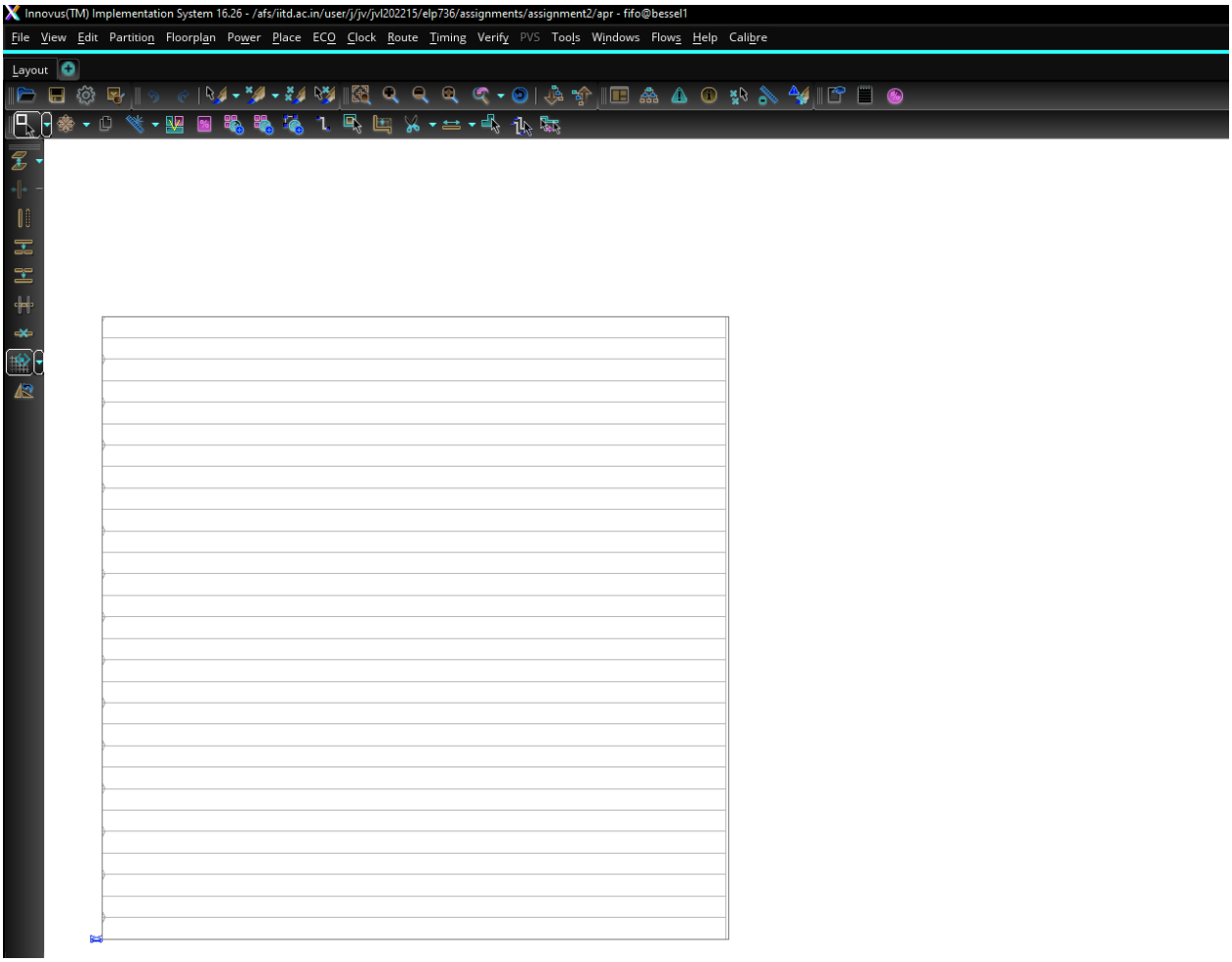

Figure: Cadence Layout Viewer window after design import

e. Next, for partitioning, go to Partition > Specify Partition. In the editor window, add any hierarchical instance name. Multiple instances can also be added. The equivalent command for script/nongui usage is:

definePartition -hinst fifomem -coreSpacing 0.0 0.0 0.0 0.0 -railWidth 0.0 -minPitchLeft 2 -minPitchRight 2 -minPitchTop 2 -minPitchBottom 2 -reservedLayer { 1 2 3 4 5 6 7} -pinLayerTop { 2 4 6} -pinLayerLeft { 3 5 7} -pinLayerBottom { 2 4 6} -pinLayerRight { 3 5 7} -placementHalo 0.0 0.0 0.0 0.0 -routingHalo 0.0 -routingHaloTopLayer 7 -routingHaloBottomLayer 1

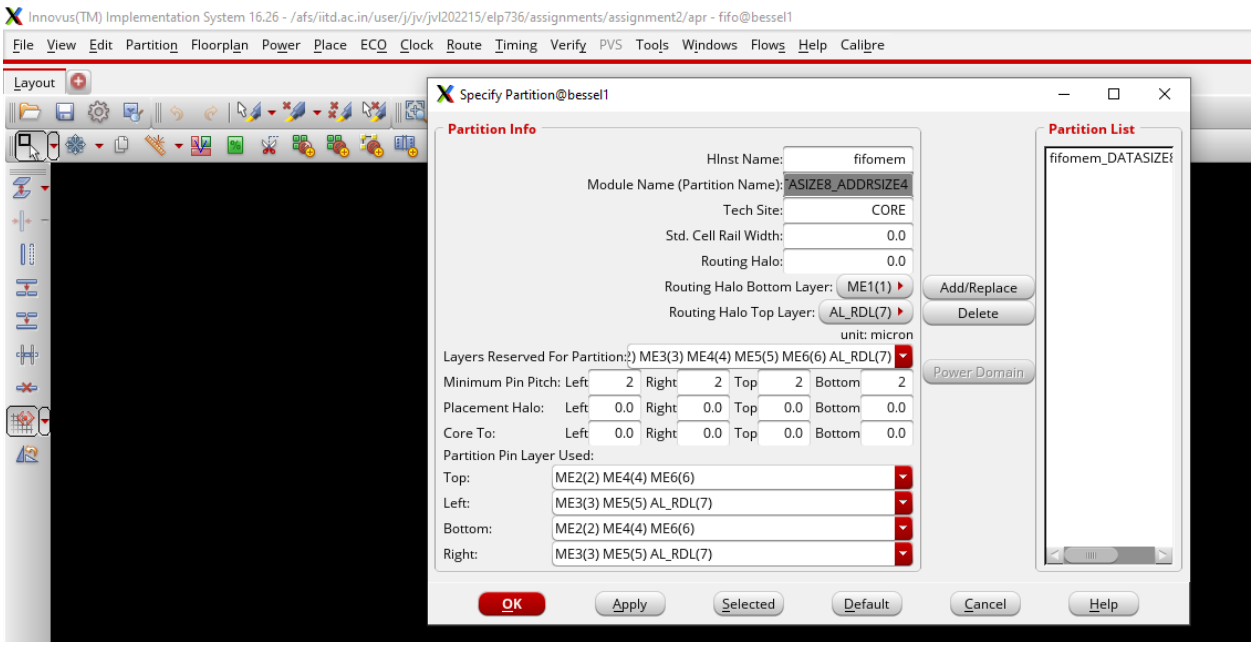

Figure: Adding partition by writing the instance name and clicking on Add/Replace

f. On clicking on OK, the partition becomes visible as a block adjacent.

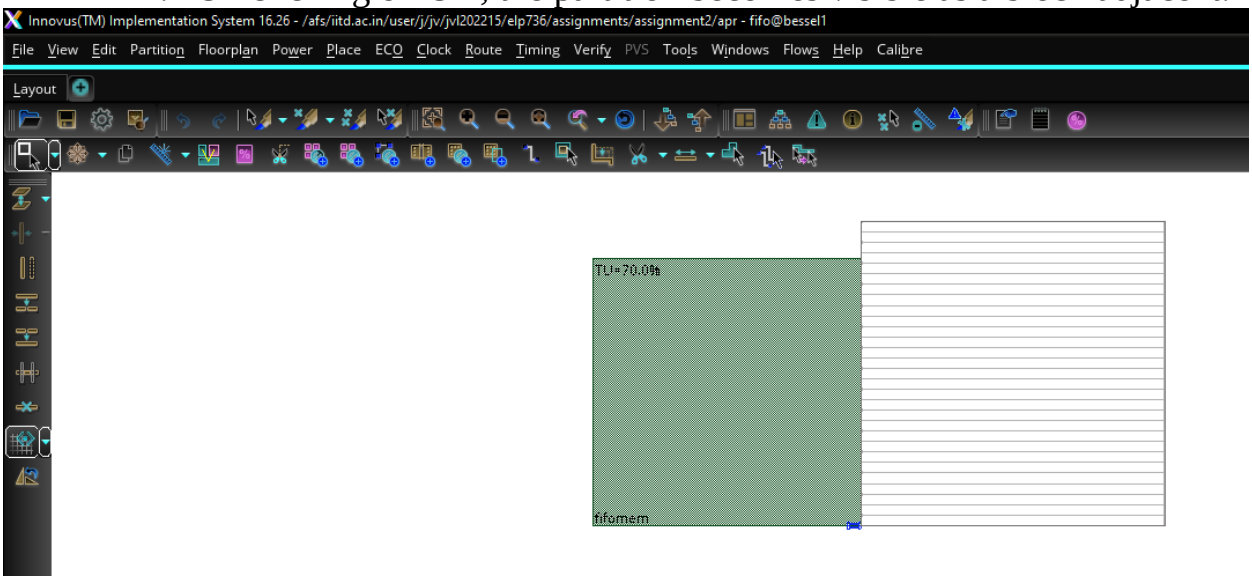

Figure: Selecting fifomem as the partition

g. Now, the standard cells should be placed. Go to Place > Place Standard Cell. Click on Run Full Placement and click on OK.

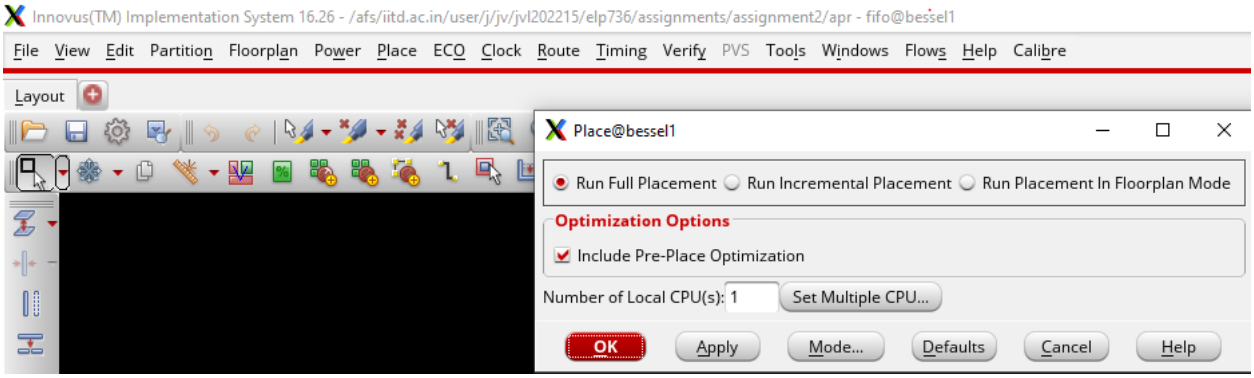

Figure: Selecting Standard Cell Placement

h. This shows a placed layout. To see the floorplan with partition indicated, go to Amoeba view.

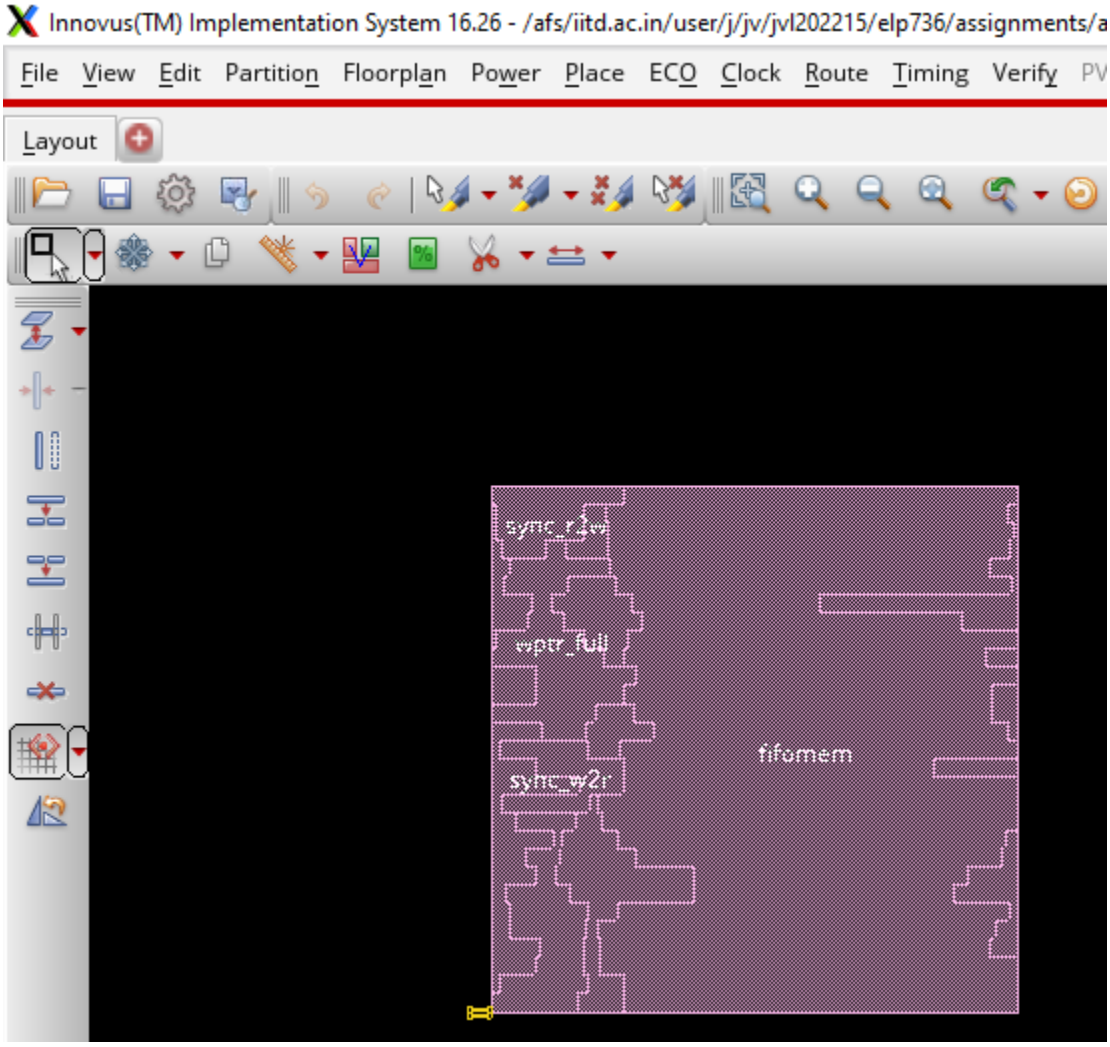

Figure: Partitioning view indicating fifomem partition

i. The layout can be seen in the physical view as indicated below

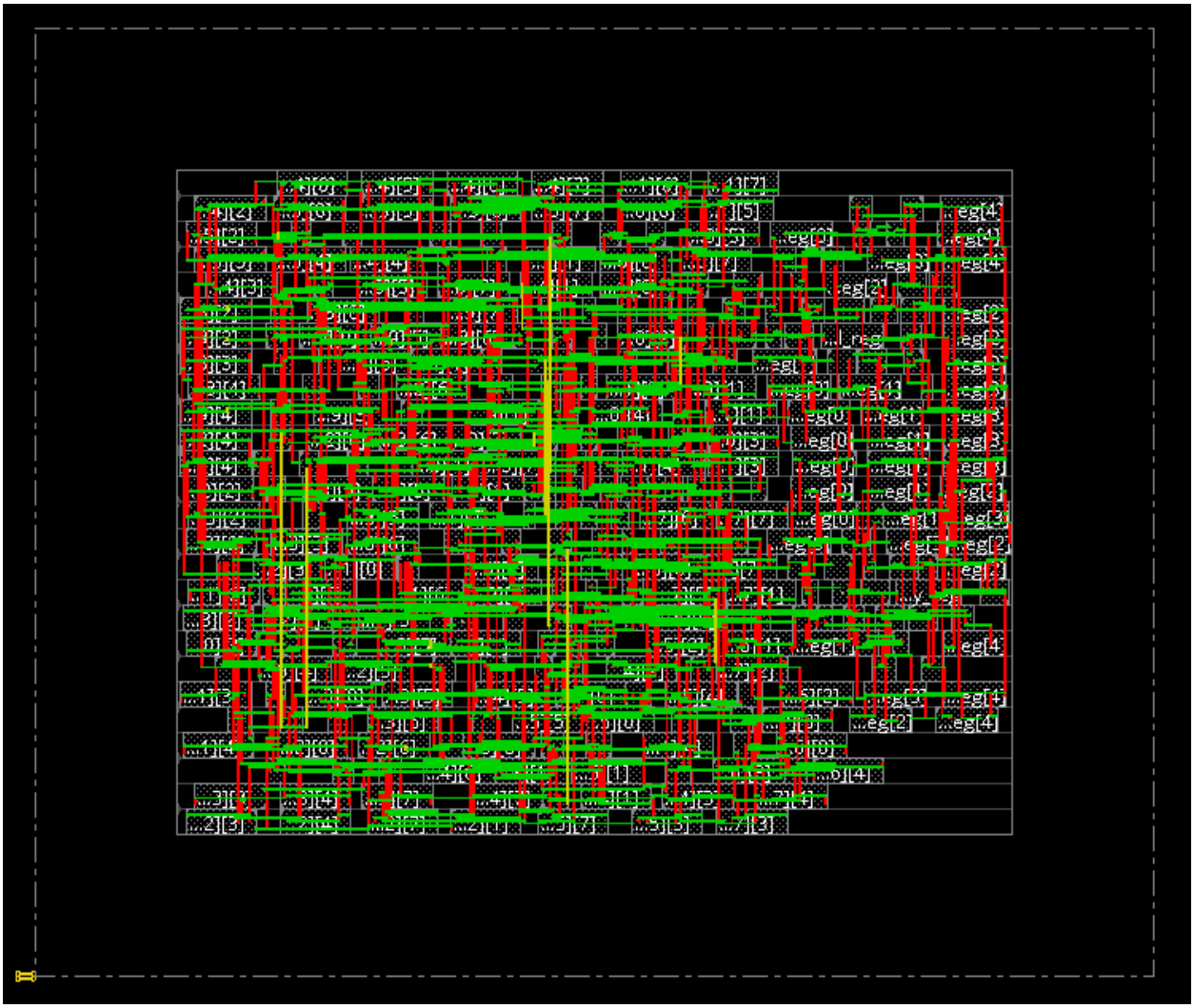

Figure: The physical view of layout

This completes the Partitioning part.

2. Floorplan

The floorplan has been built using the below steps:

a. Click on Floorplan > Specify Floorplan and select Core Size by Aspect Ratio.

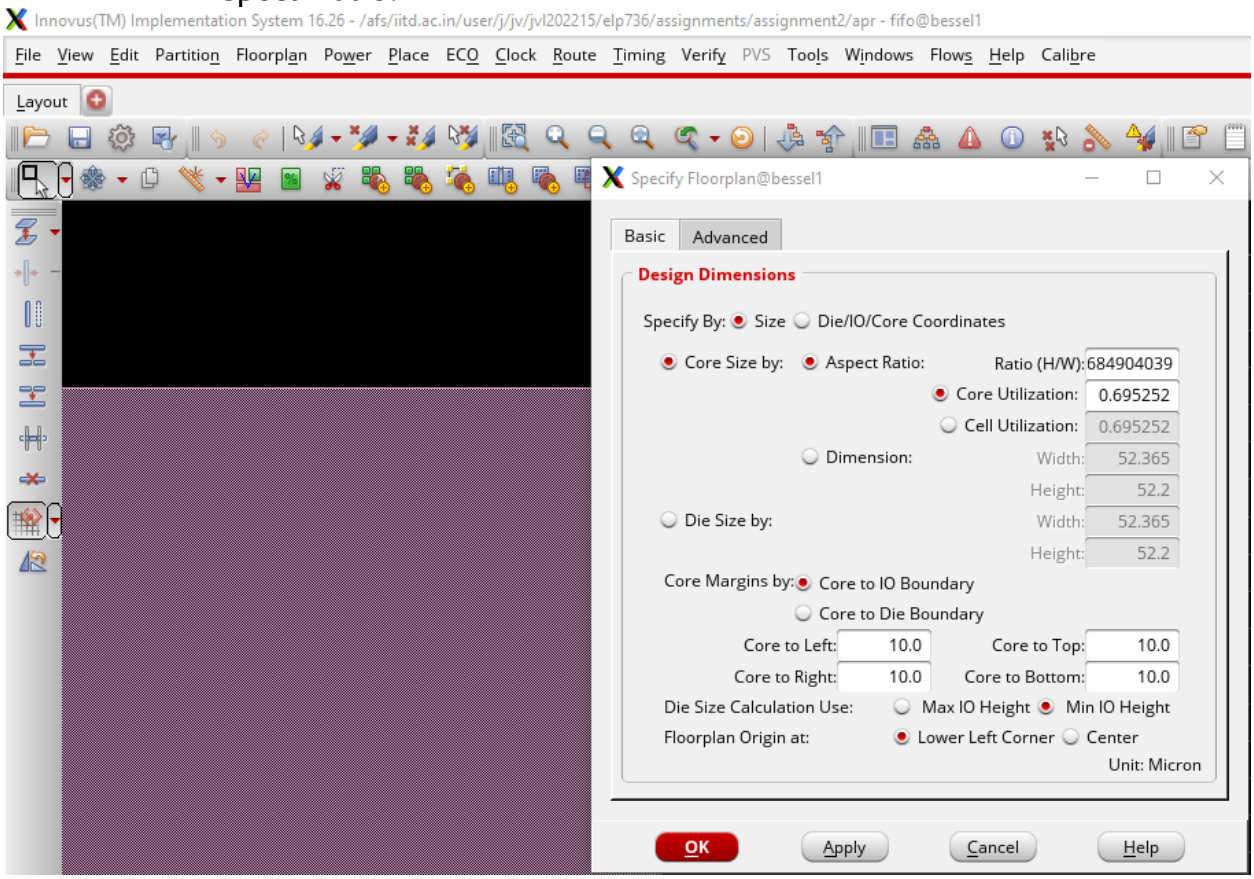

Figure: Updating the floorplan specifications.

b. Update the specifications. Add Core to IO boundary as 10. Click on OK. A box becomes available outside the core with the spacings as mentioned in Core to IO Boundary specifications in previous step.

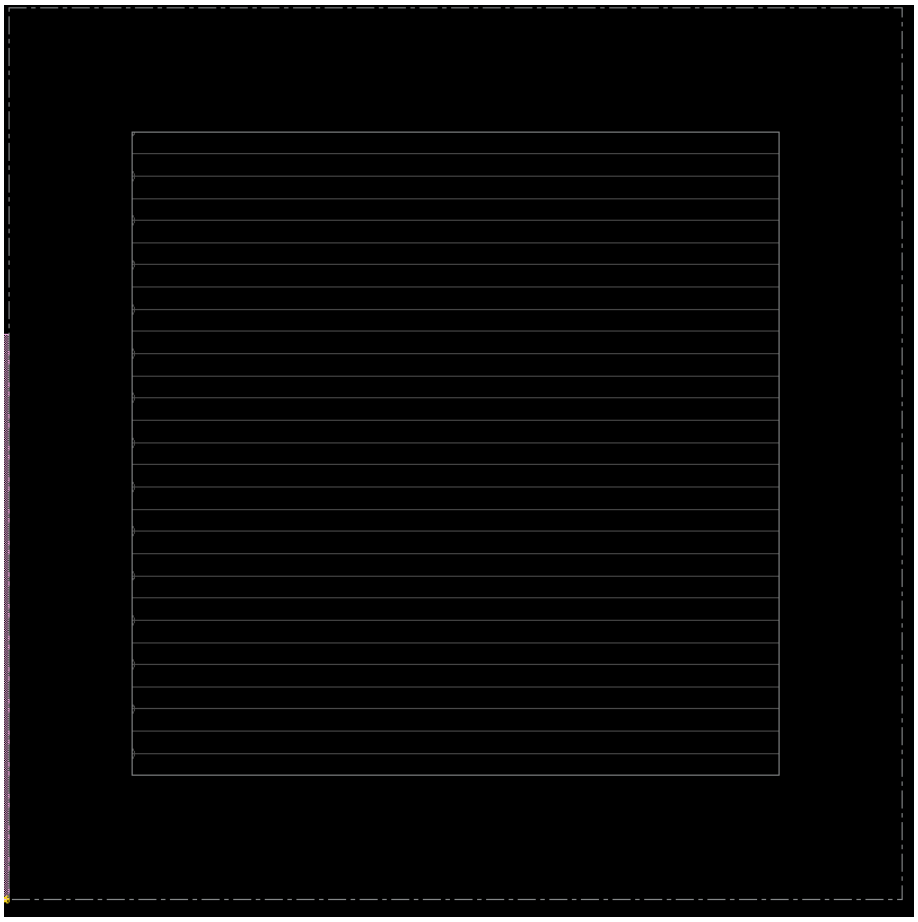

Figure: The Core to IO boundary specifications visible in the layout viewer

c. Now, edit the pin allocations by Edit > Pin Editor. After the pin editing, the floorplan appears as in figure below. The equivalent command for script/nongui users is:

setPinAssignMode -pinEditInBatch true
editPin -fixOverlap 1 -unit MICRON -spreadDirection clockwise -side Right -layer 1 -spreadType start -spacing 0.2 -start 0.0 0.0 -pin {{rdata[0]} {rdata[1]} {rdata[2]} {rdata[3]} {rdata[4]} {rdata[5]} {rdata[6]} {rdata[7]} wfull rempty}
setPinAssignMode -pinEditInBatch false

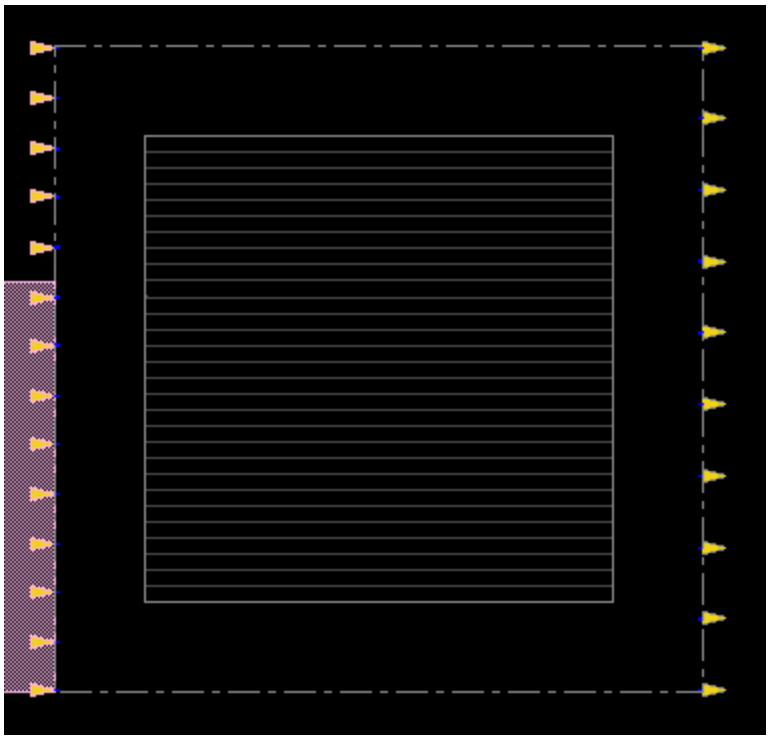

Figure: The pin allocations done

With this, we are done with the floorplanning, next we will proceed to power planning stage.