A Report On

Assignment -2

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by

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FOR THE COURSE

ELP736

Physical Design Laboratory

IIT Delhi

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1. Problem Statement

Read this paper. Then do PD(Physical Design) flow. Assume any clock frequency like (10MHz or 20MHz).

As the GENUS part is done in Assignment-I, use the generated gate-level Netlist and SDC file.

Submission:

Report containing the snapshots of each step of PD flow.

Mail your submission to: een202498@iitd.ac.in, een202501@iitd.ac.in, jvl202216@iitd.ac.in.

2. Working Directory

Annexures:

a. Work area path:
/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2
b. GitHub ID:
https://github.com/DJ-dineshjoshi/async_fifo/tree/main/assignment2
c. The floorplan is located at below path. Also it has been uploaded onto github.
/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr/fifo_floorplan

Frequencies used:

Read clock frequency: 30MHz.

Write clock frequency: 10MHz.

3. Steps for RTL to GDSII flow

a. Import design

a. Launch innovus using below commands:
   % load_module innovus20; load_module encounter
   % innovus &
b. Go to File > Design Import and add the Verilog file path, the lef file path and the power pins as per below figure

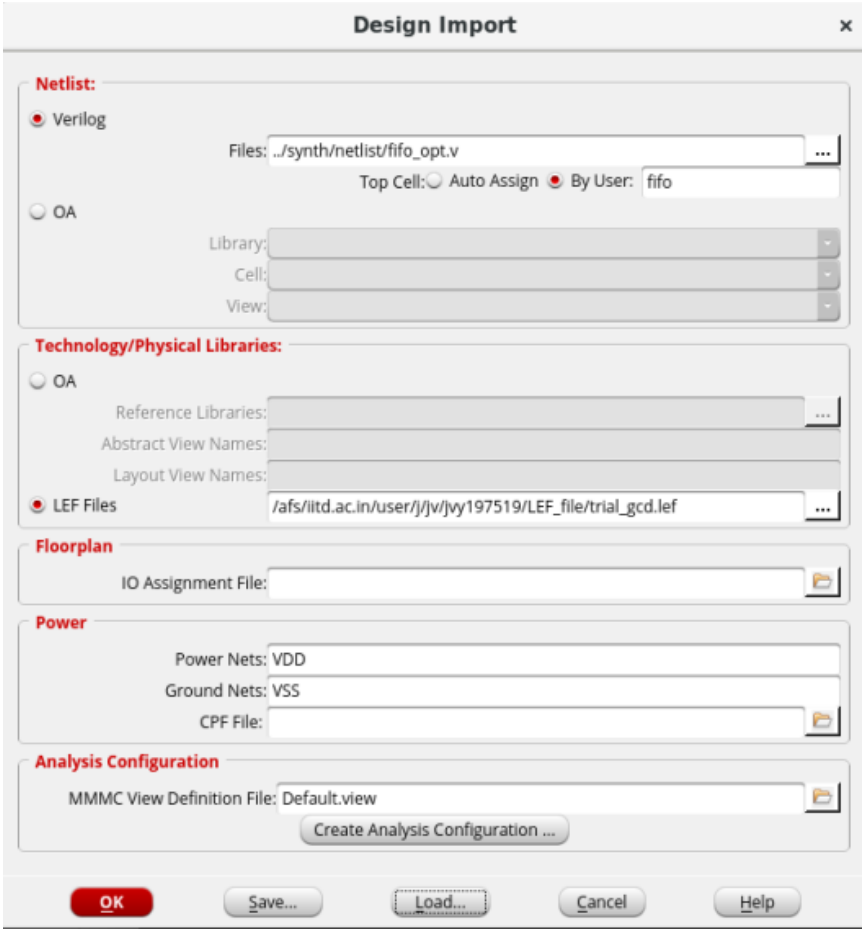

Figure: Loading Design into innovus

c. In the MMMC View Definition file, click on Create Analysis Configuration.
    i. In the MMMC Browser window, add the library sets for max and min timing libraries.
    Library sets -> Name: max_timing_library -> Add under Timing Library Files ->
    Add file
    /afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/uk65lscllmvbbr_090c125_wc_ccs.lib
    Library sets -> Name: min_timing_library -> Add under Timing Library Files ->
    Add file
    /afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/uk65lscllmvbbr_110c-40_bc_ccs.lib
    ii. Update the RC Corner
    RC Corner -> Name: Default_rc_corner -> QRC Tech file: Add
    /afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/process/UMK65FDKLLC00000OA_B11/RuleDecks/QRC/RCmin/qrcTechFile
    iii. Update the Delay corners for wcs and bcs
    Add Delay Corner -> Name: max_delay_corner -> RC Corner: Default_rc_corner -> Library set: max_timing _library
    Add Delay Corner -> Name: min_delay_corner -> RC Corner: Default_rc_corner -> Library set: min_timing _library

iv. Create constraint modes for worst_case and best_case corners
    Constraints Mode -> Name: fifo_constraints -> fifo.sdc
v. Create Analysis views
    Analysis View -> Name: worst_case -> Delay corner: max_delay
    Analysis View -> Name: best_case -> Delay corner: min_delay
    Setup Analysis -> Analysis view: worst_case
    Hold Analysis -> Analysis view: best_case
vi. Save&Close – Default.view
vii. Save the file as Default.globals for directly loading for further cases.

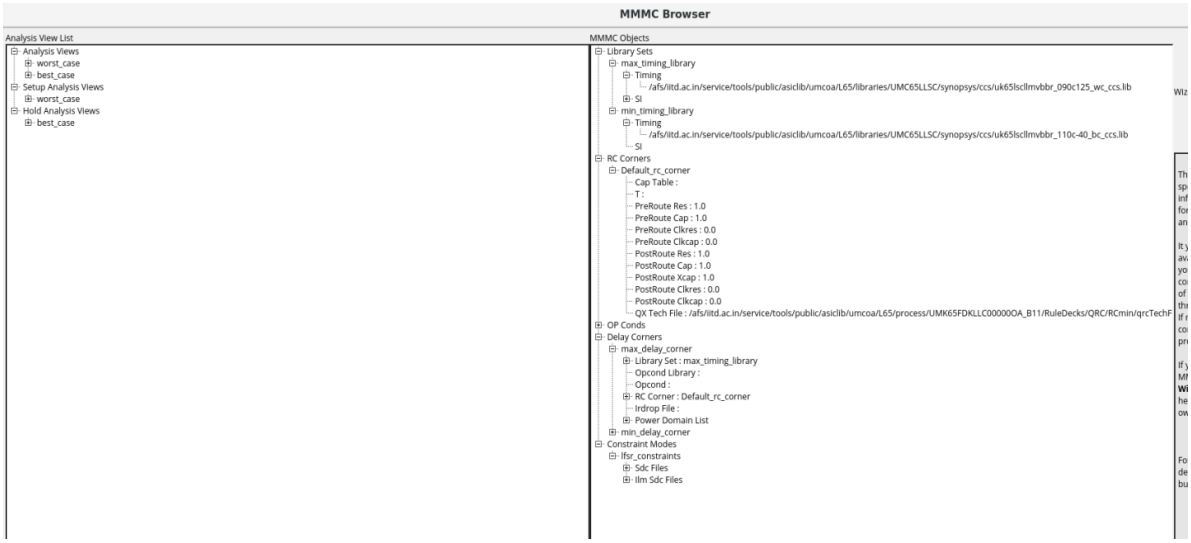

Figure: Providing the inputs to the lfsr.view file

b. Click on OK, the innovus terminal shows below message after design import:

```
*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPLF-200            1  Pin '%s' in macro '%s' has no ANTENNAGAT...
WARNING   IMPLF-108            1  There is no overlap layer defined in any...
WARNING   IMPVL-159         2154  Pin '%s' of cell '%s' is defined in LEF ...
WARNING   TECHLIB-302         20  No function defined for cell '%s'. The c...
WARNING   TECHLIB-436         20  Attribute '%s' on '%s' pin '%s' of cell ...
WARNING   TECHLIB-1365        20  The %s vector group for %s has a duplica...
*** Message Summary: 2216 warning(s), 0 error(s)

innovus 1>
```

Figure: Innovus messages after design import

c. Review the layout screen after design import. A box with rows will appear as below

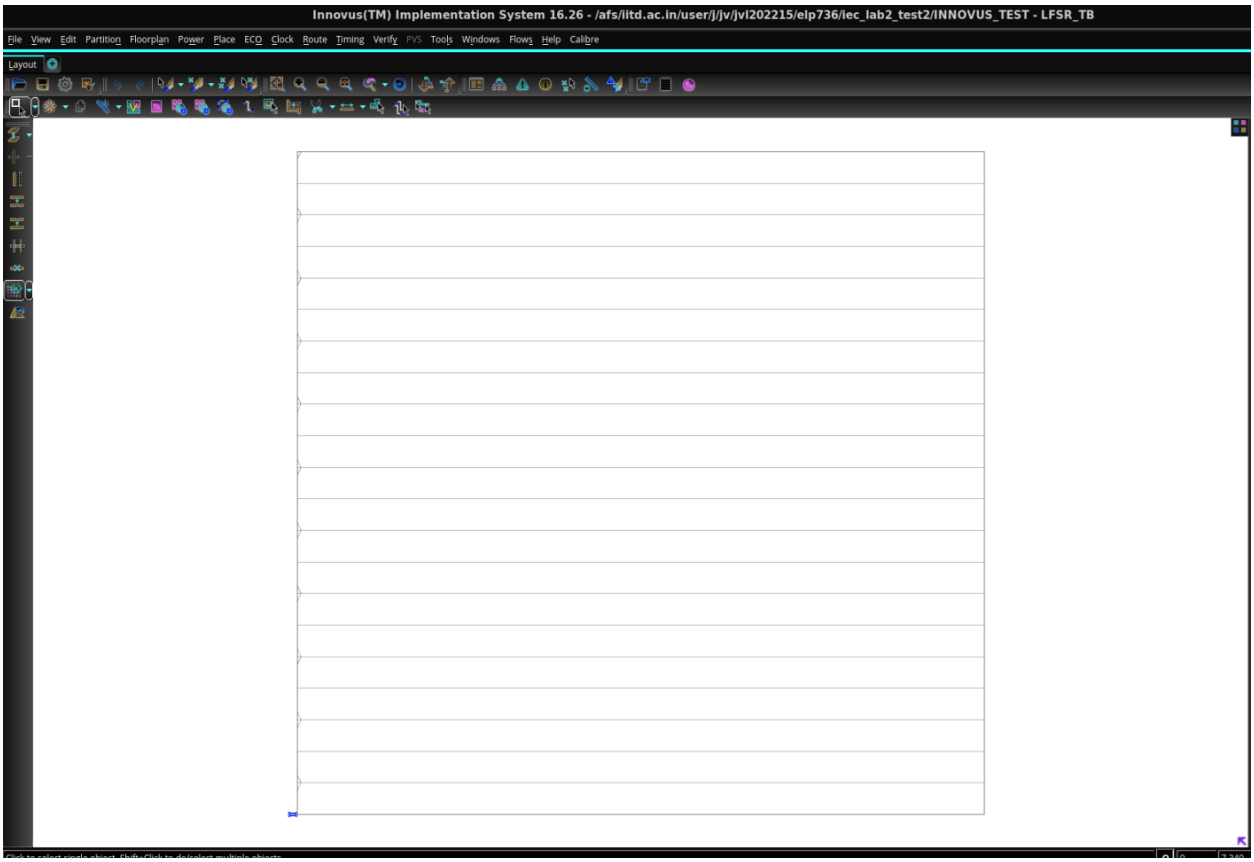

Figure: Layout after loading the files:

b. Partitioning

a. For partitioning, go to Partition > Specify Partition. In the editor window, add any hierarchical instance name. Multiple instances can also be added. The equivalent command for script/nongui usage is:

definePartition -hinst fifomem -coreSpacing 0.0 0.0 0.0 0.0 -railWidth 0.0 -minPitchLeft 2 -minPitchRight 2 -minPitchTop 2 -minPitchBottom 2 -reservedLayer { 1 2 3 4 5 6 7} -pinLayerTop { 2 4 6} -pinLayerLeft { 3 5 7} -pinLayerBottom { 2 4 6} -pinLayerRight { 3 5 7} -placementHalo 0.0 0.0 0.0 0.0 -routingHalo 0.0 -routingHaloTopLayer 7 -routingHaloBottomLayer 1

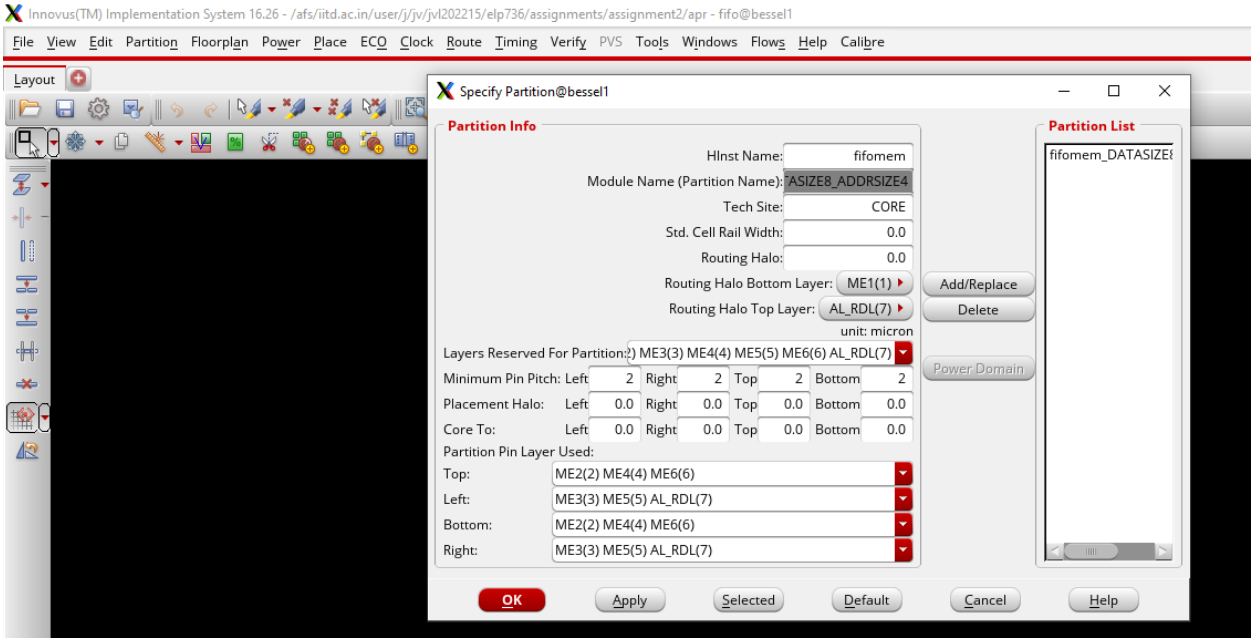

Figure: Adding partition by writing the instance name and clicking on Add/Replace

b. On clicking on OK, the partition becomes visible as a block adjacent.

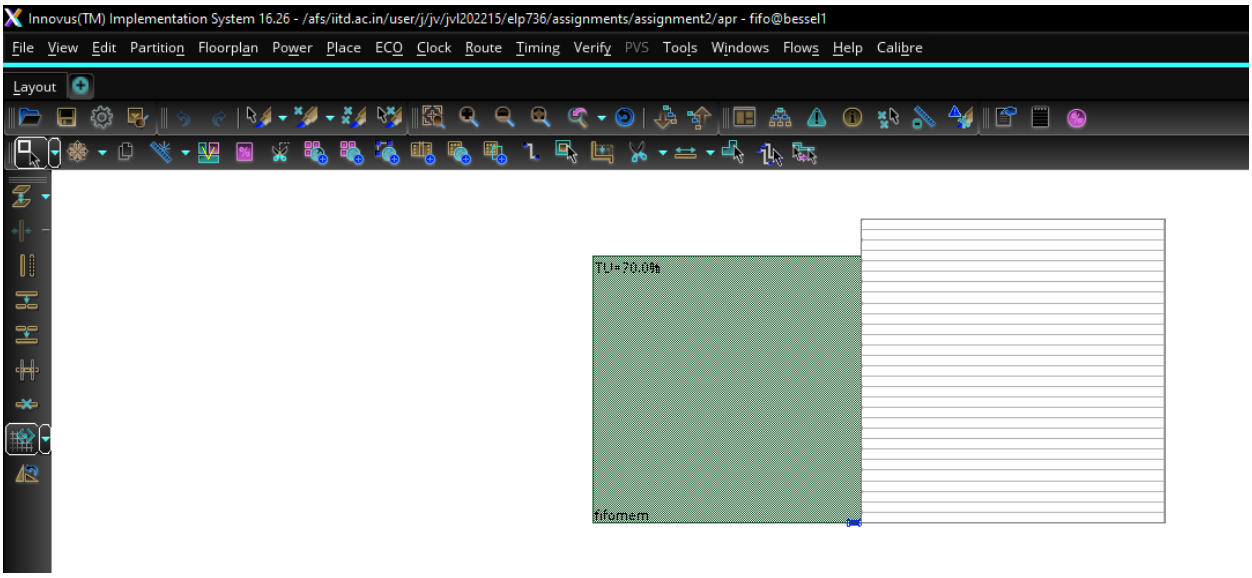

Figure: Selecting fifomem as the partition

c. This shows a placed layout. To see the floorplan with partition indicated, go to Amoeba view.

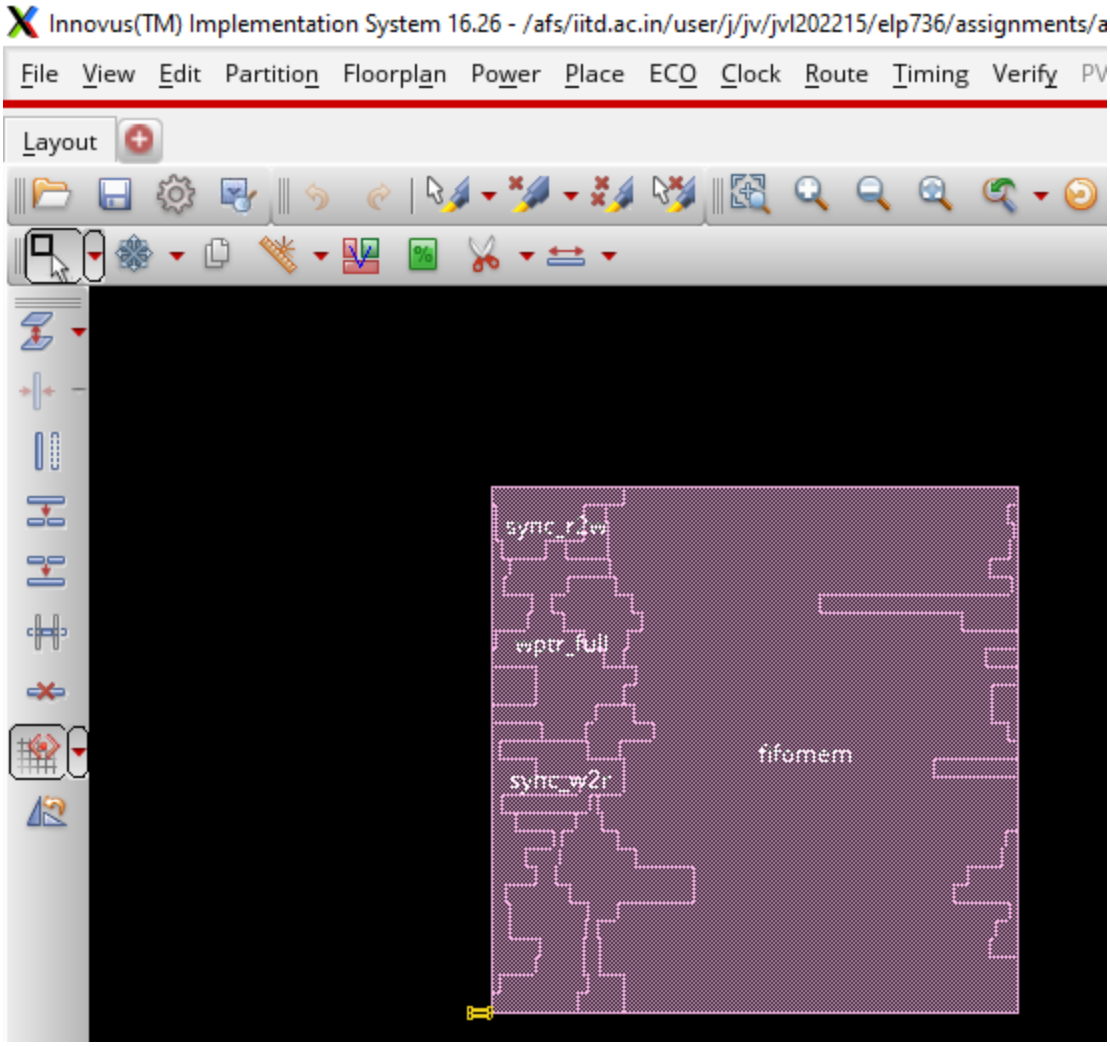

Figure: Partitioning view indicating fifomem partition

This completes the Partitioning part.

c. Floorplan Specification

d. Provide below settings for specifying floorplan:

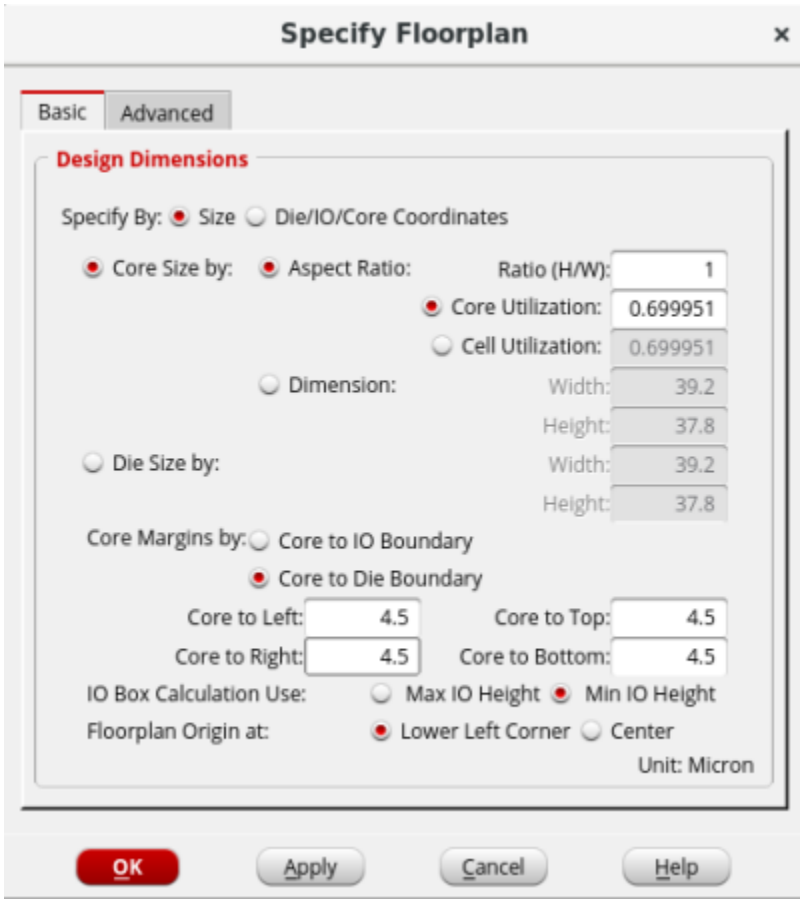

Figure: Floorplan specifications

e. Clicking on OK loads the layout with the floorplan with a box between the core and the die as shown in below figure.

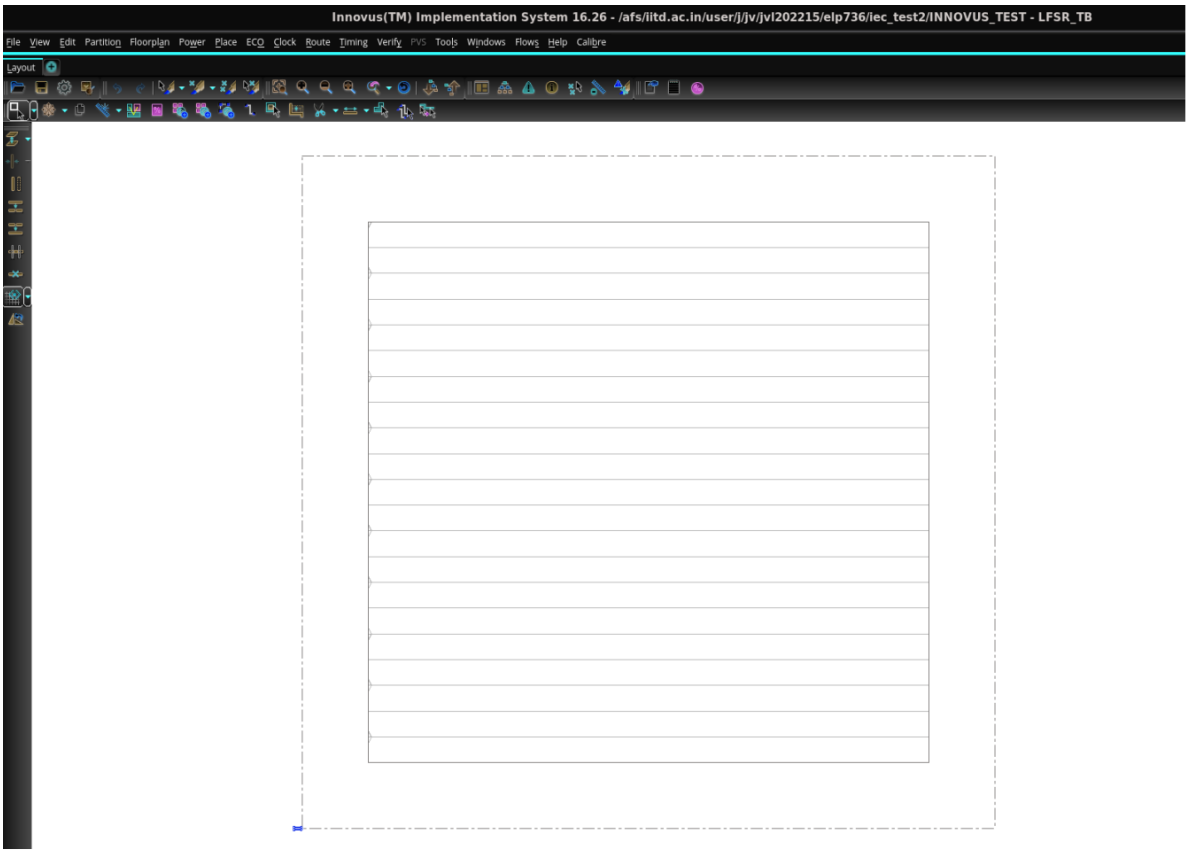

Figure: Floorplan layout

d. Power Planning:

f. Add VDD and VSS rings by going to

Figure: Adding power supply rings

g. Layout after adding rings appears as below

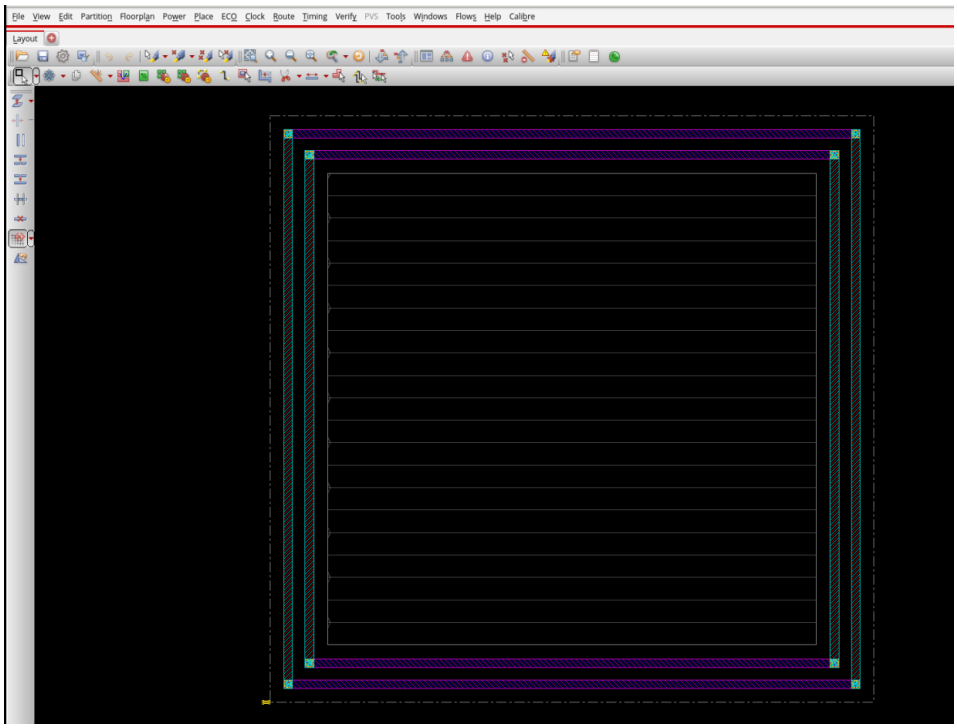

Figure: Layout after ring addition

h. Add stripes as per the below specifications

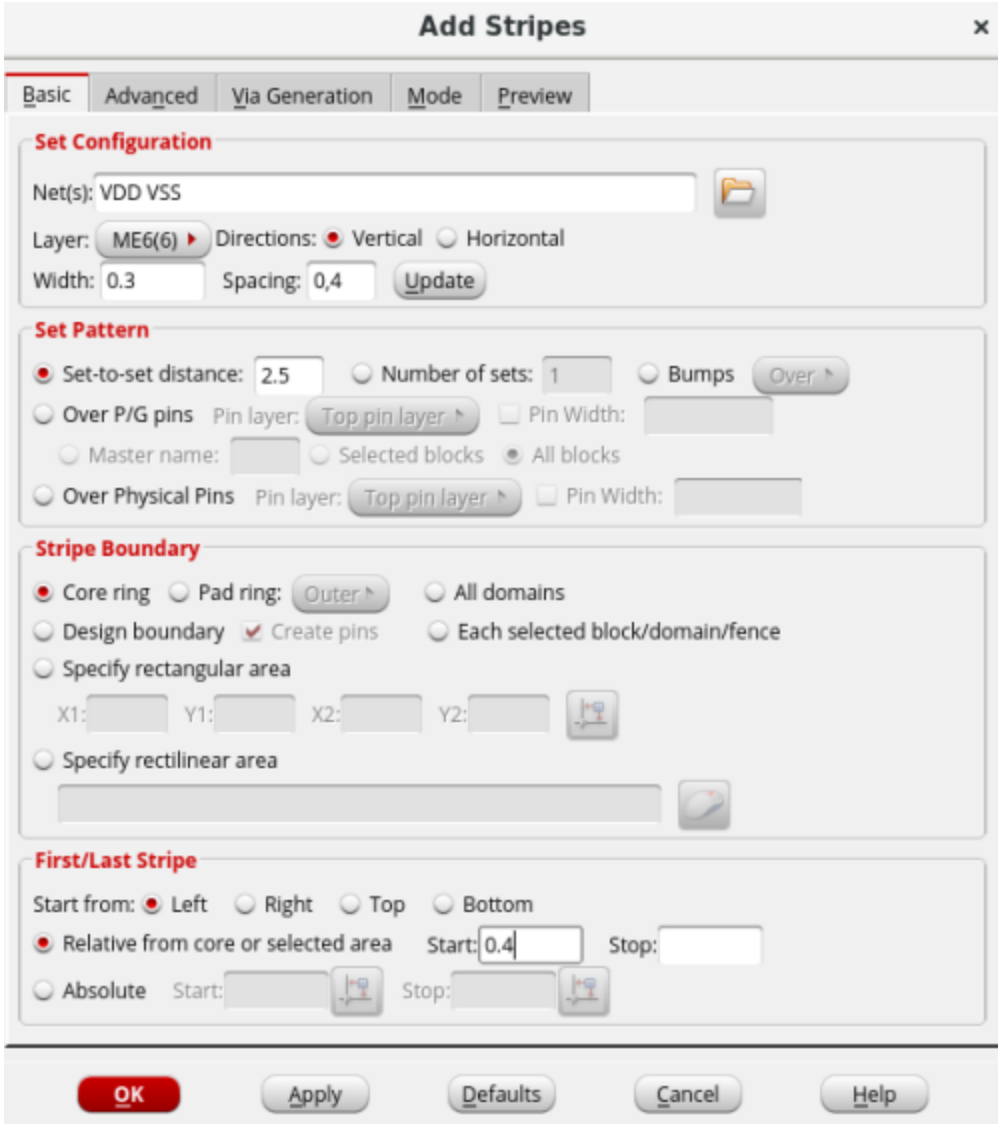

Figure: Stripes addition specifications

i. Layout after stripes addition appears as shown in next figure:

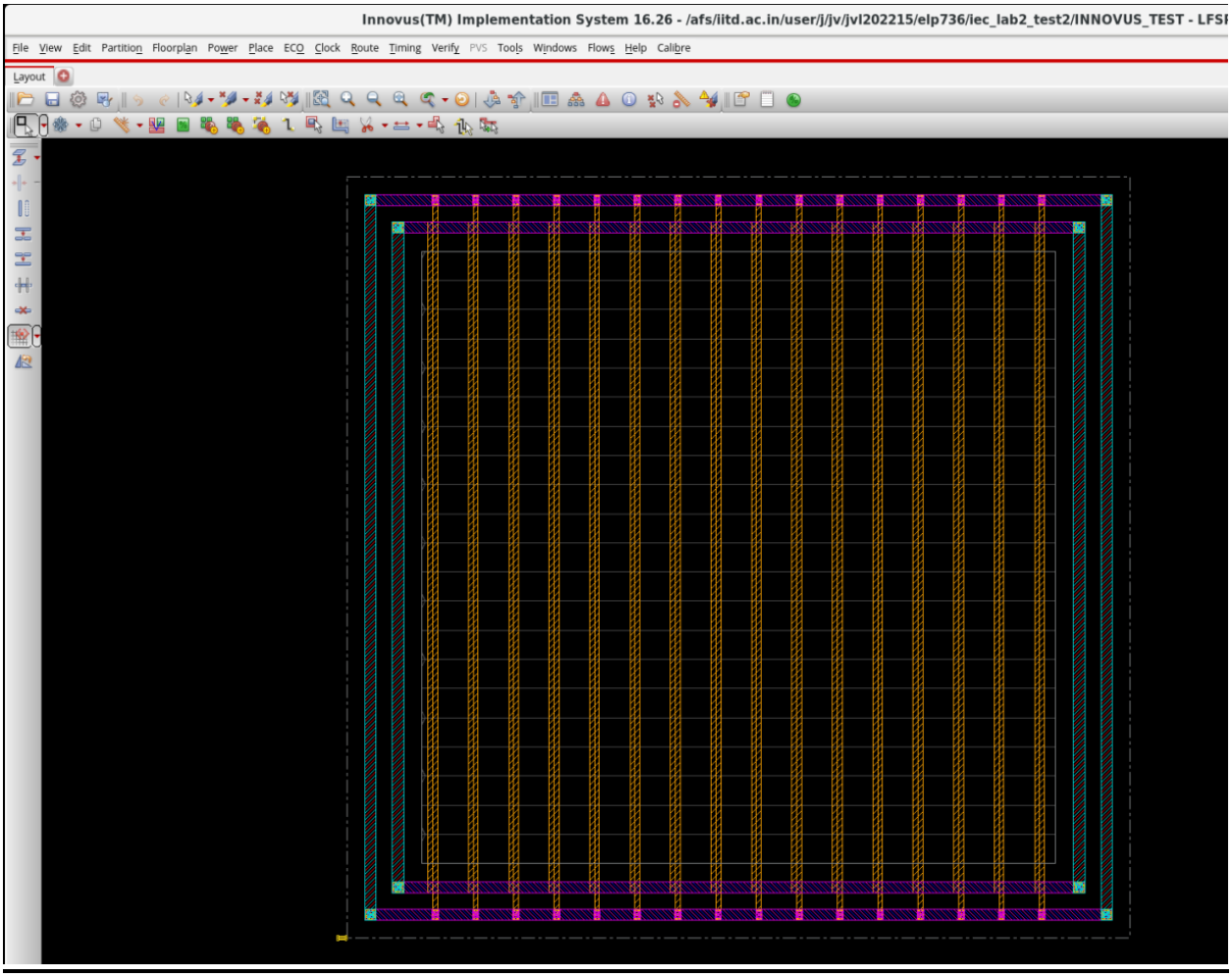

Figure: Layout after stripes addition

j. Add special routes as shown per below specifications:

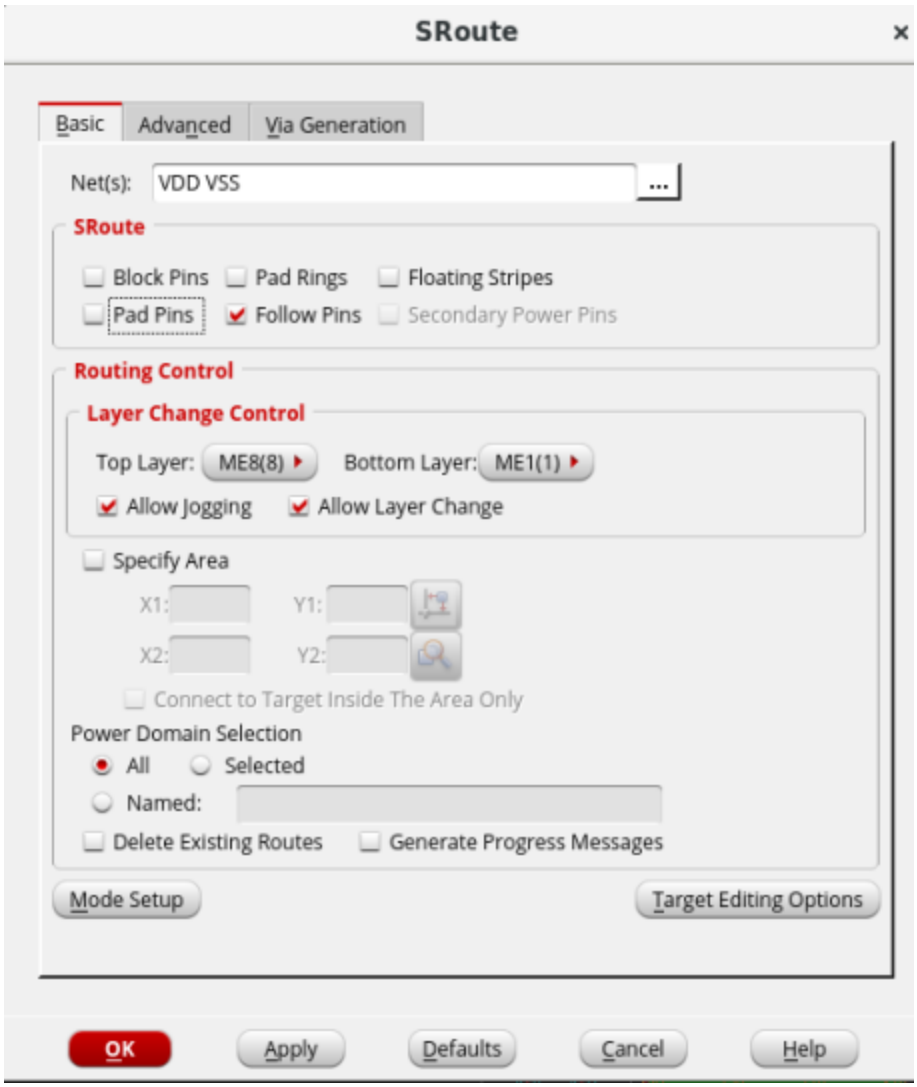

Figure: Special route addition

e. Allocating pin orientations:

a. Edit pin directions. First select all the input pins and then allocate them to the left on metal layer 3.

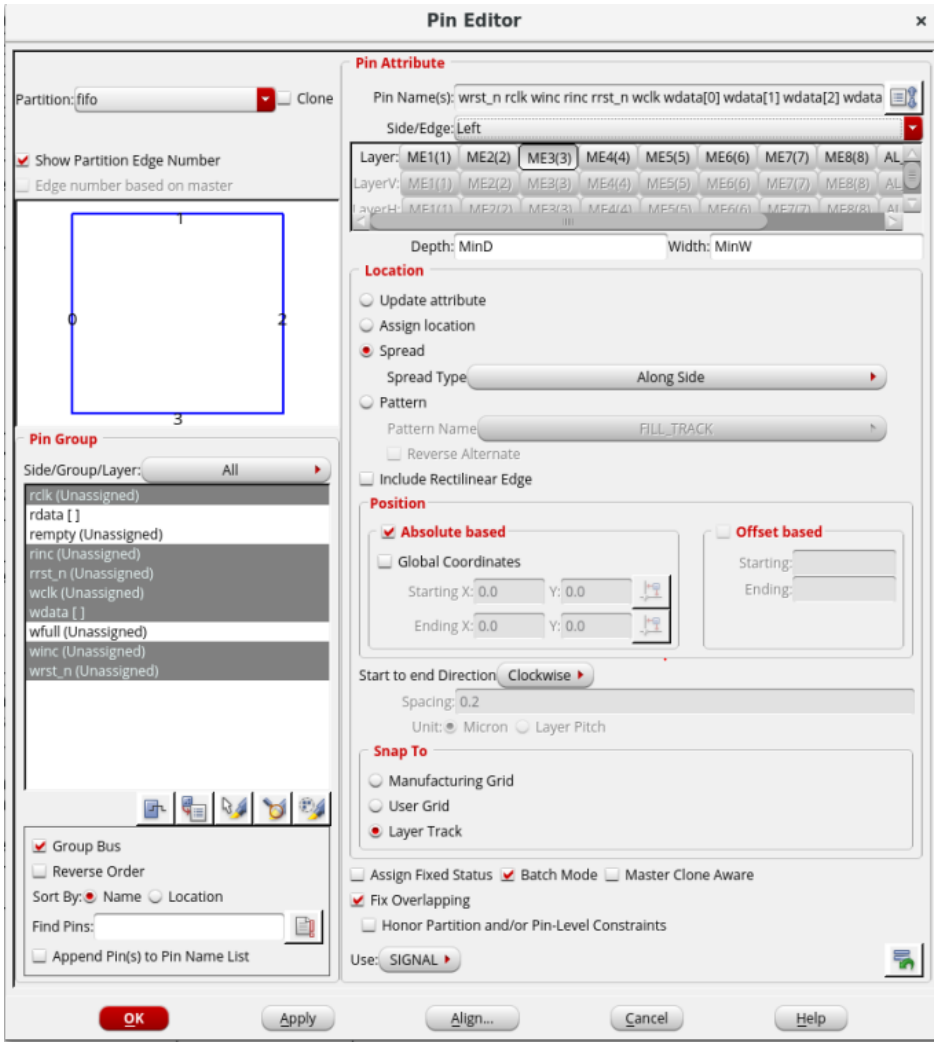

Figure: Editing input pin properties for pin orientation

b. Do the same for the output pins and allocate them to the right.

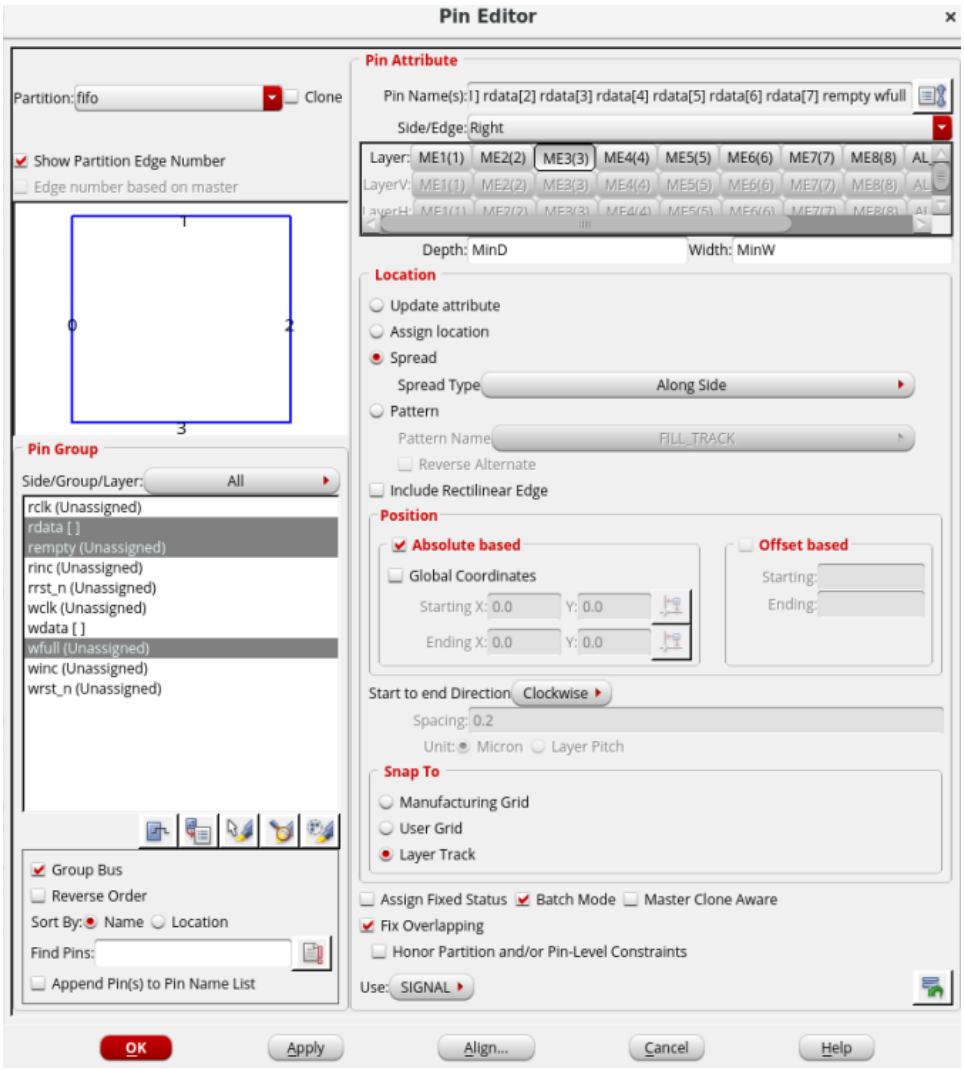

Figure: Editing output pin properties

c. Layout after edit pin directions allocation appears as shown in below figure

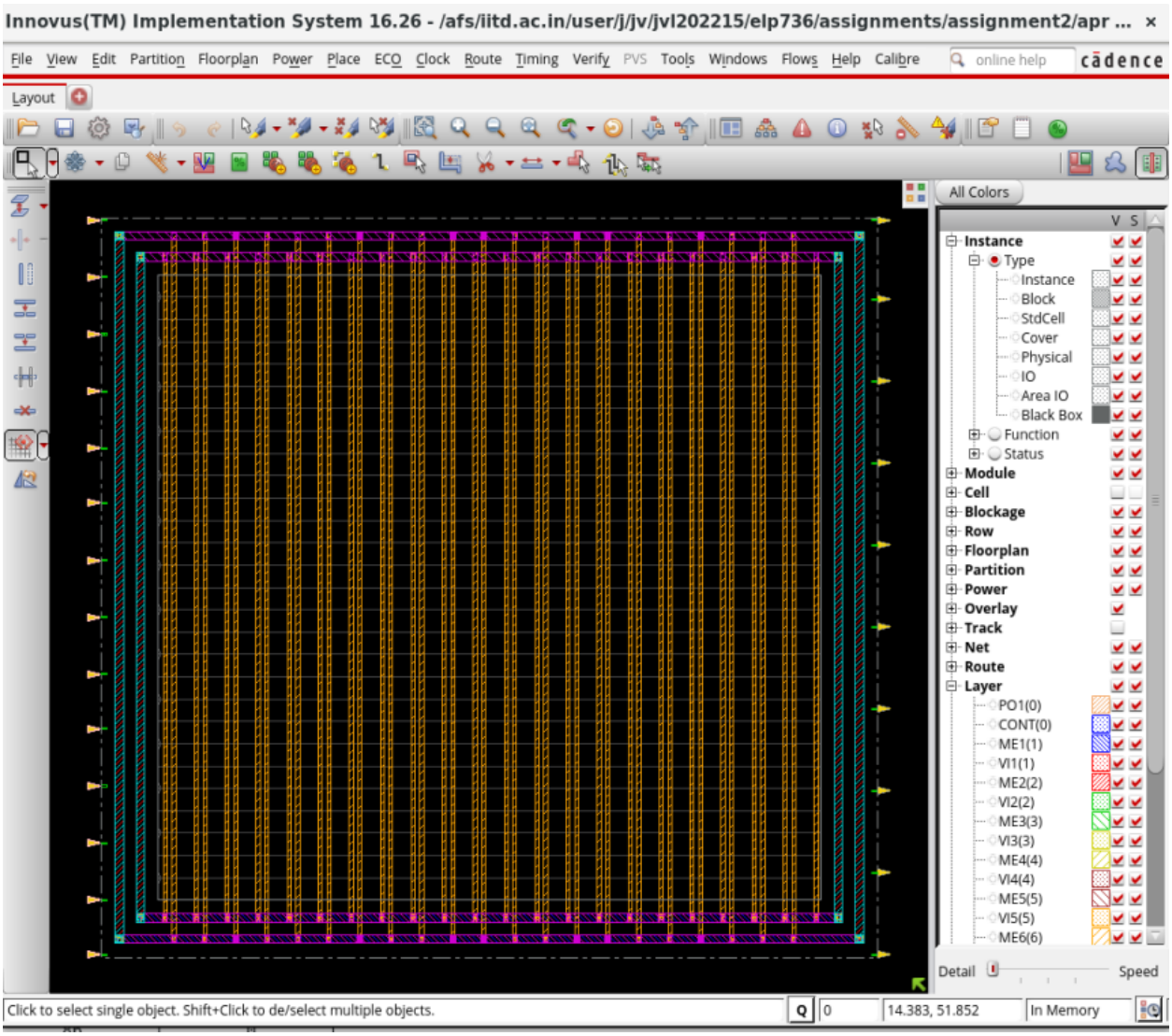

Figure: Layout after pin placment

f. Standard Cell placement:

a. Place standard cells. For this, go to Place > Place Standard Cells.
b. Click on Run Full Placement and include pre-place optimization.

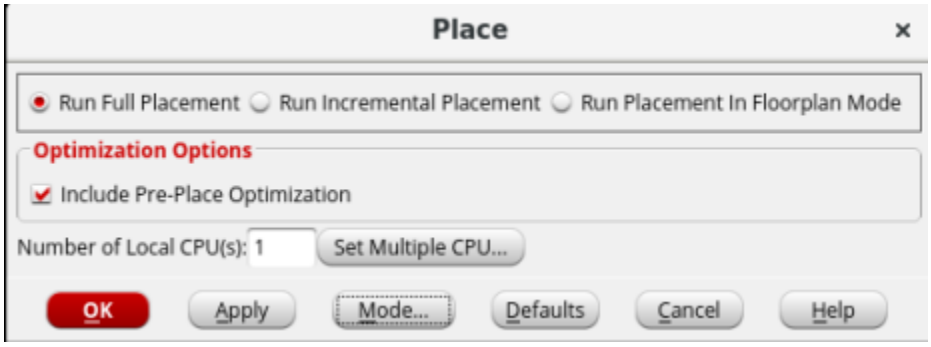

Figure: Specifications for standard cell placement

c. On clicking on OK, the layout appears as shown in next figure.

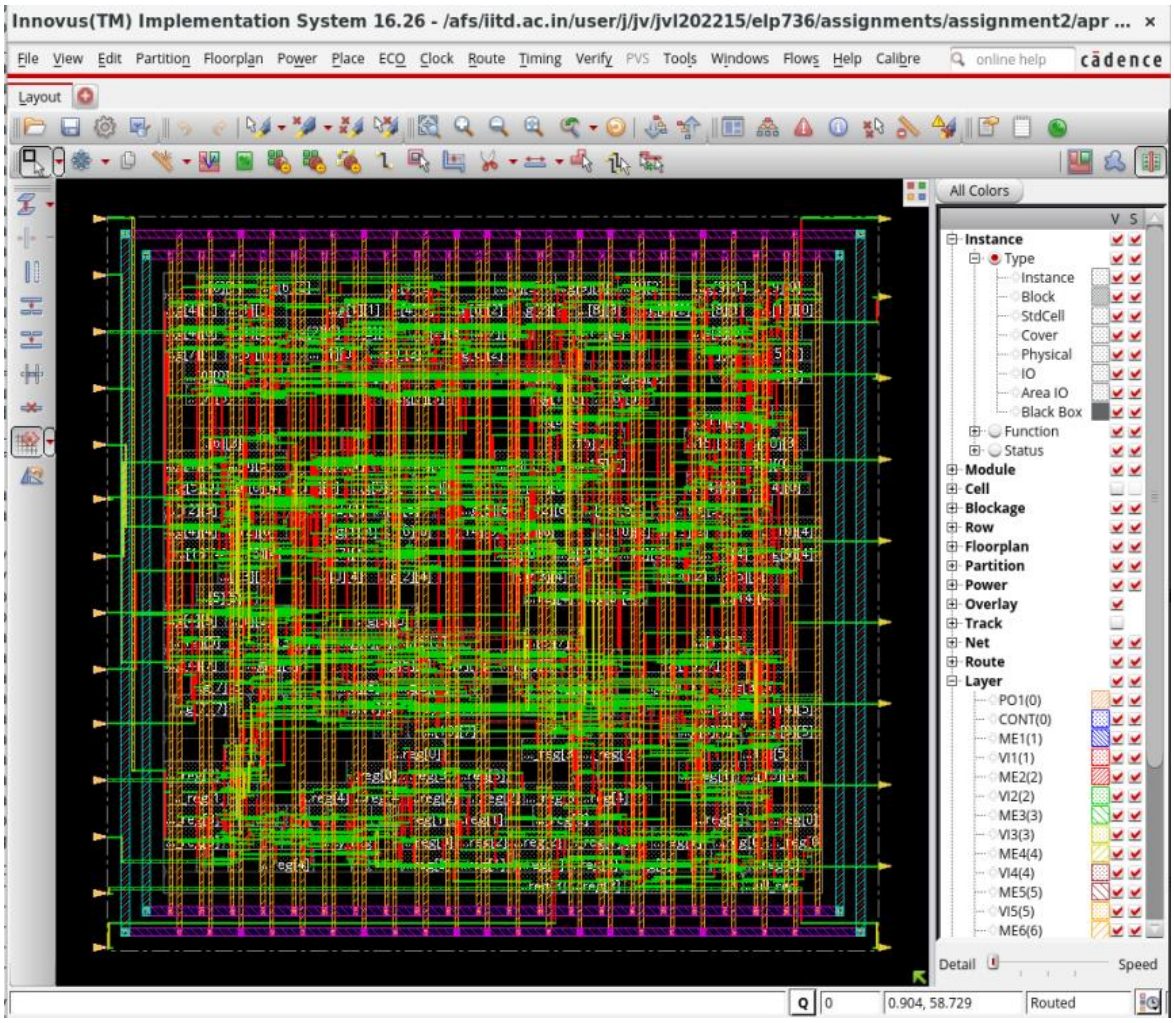

Figure: Layout after standard cell placement

d. Run placement optimization. Run below command in innovus terminal

   place_opt_design

e. The layout after placement optimization, appears as shown in next figure:

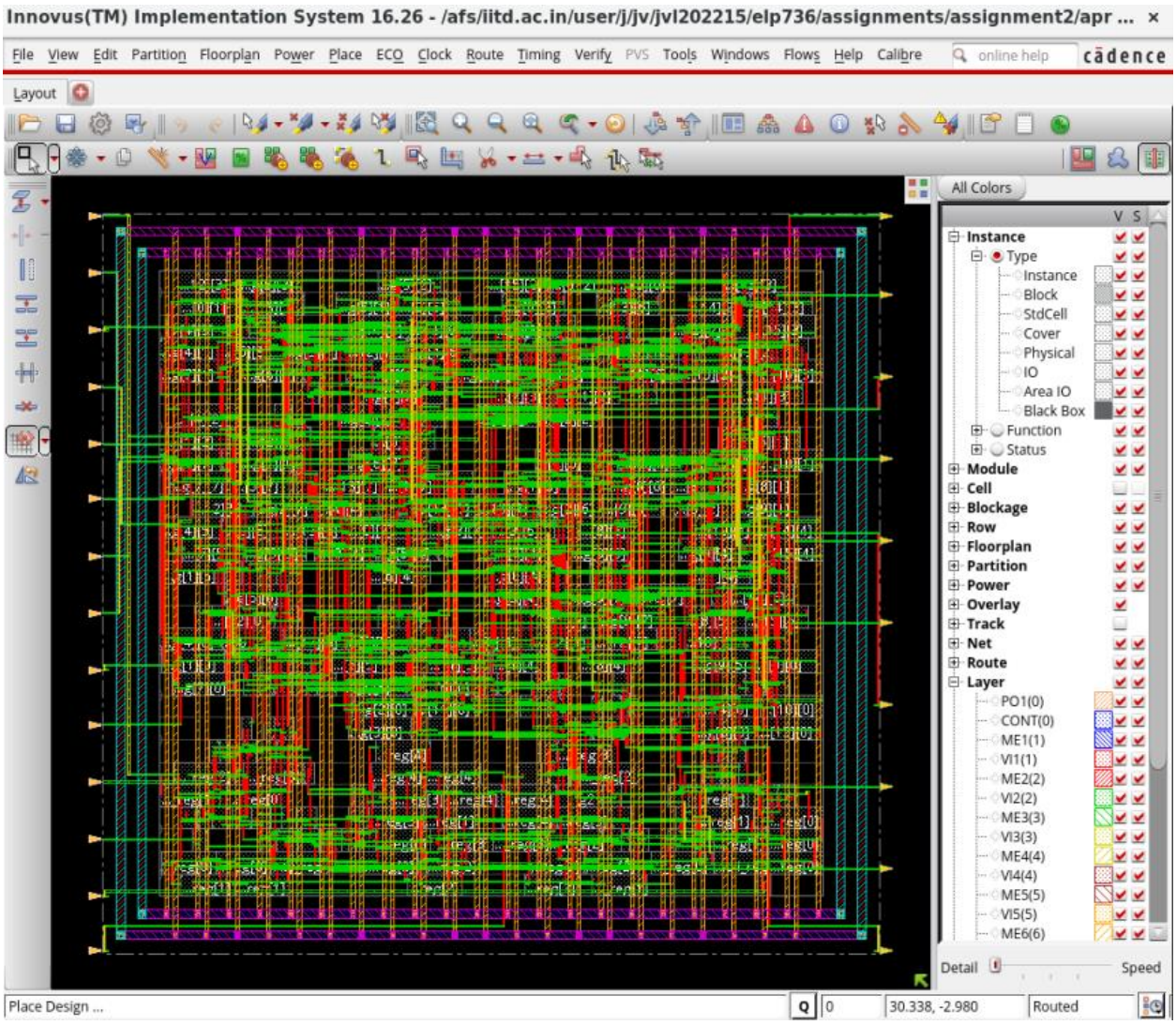

Figure: Layout after placement optimization

g. preCTS Timing Analysis:

Timing analysis:

a. PreCTS: Check preCTS timing analysis

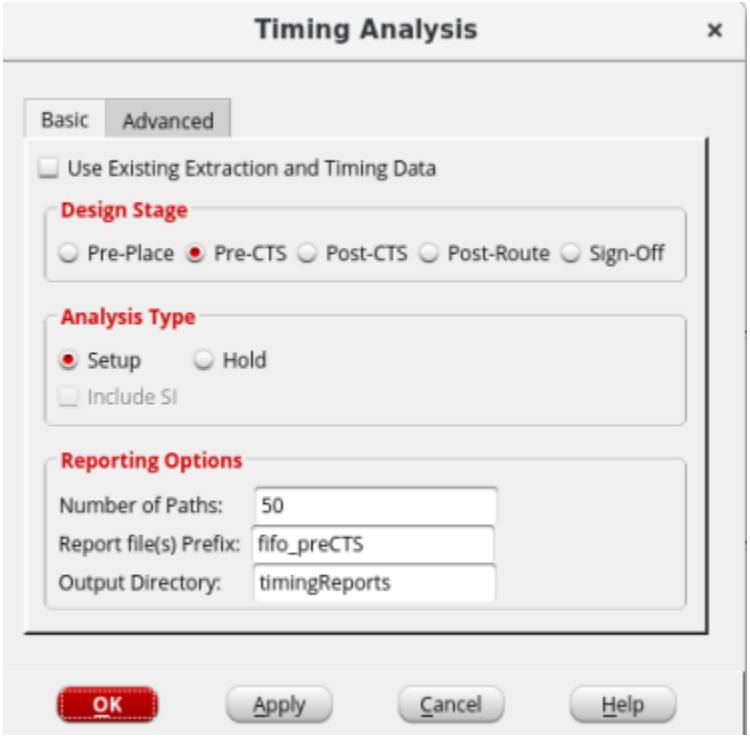

Figure: preCTS timing report generation

b. On clicking on OK, the terminal shows the timing report as shown below:

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 30.628  | 30.838  | 30.628  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 70.746%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.66 sec
Total Real time: 1.0 sec
Total Memory Usage: 2041.40625 Mbytes
innovus 3>
```

Figure: preCTS setup timing with no violation

c. Now, check hold analysis

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.163  |  0.079  | -0.163  |
|           TNS (ns):| -9.328  |  0.000  | -9.328  |
|    Violating Paths:|   169   |    0    |   169   |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

Density: 70.746%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.65 sec
Total Real time: 1.0 sec
Total Memory Usage: 2010.710938 Mbytes
innovus 3>
```

Figure: Hold analysis having 169 violations

h. CTS:

k. Run below commands for Clock Tree Synthesis on innovus terminal:

create_ccopt_clock_tree_spec

ccopt_design

l. These commands build the Clock Tre and the second one optimizes post CTS.

i. postCTS Timing Analysis:

m. PostCTS, first check timing report with same staep as done in preCTS.

n. The setup report is clean with 0 violations

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 30.803  | 30.902  | 30.803  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)   |
+----------------+------------------+------------+-------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)        |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)        |
|   max_fanout   |      0 (0)       |     0      |      0 (0)        |
|   max_length   |      0 (0)       |     0      |      0 (0)        |
+----------------+------------------+------------+-------------------+

Density: 71.602%
Routing Overflow: 2.20% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.28 sec
Total Real time: 0.0 sec
Total Memory Usage: 2087.445312 Mbytes
innovus 5>
```

Figure: postCTS setup timing report

o. Now, we go to hold summary report.

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.107  |  0.071  | -0.107  |
|           TNS (ns):| -4.017  |  0.000  | -4.017  |
|    Violating Paths:|   40    |    0    |   40    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

Density: 71.602%
Routing Overflow: 2.20% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.7 sec
Total Real time: 1.0 sec
Total Memory Usage: 2067.296875 Mbytes
innovus 5>
```

Figure: postCTS hold timing summary report

p. Since slack is -ve, we try optimization for hold. The post Optimization postCTS timing report indicates 0ns hold slack which indicates that hold is marginal after postCTS optimization.

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 worst_case
Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 30.803  | 30.902  | 30.803  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.000  |  0.071  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 71.803%
Routing Overflow: 2.20% H and 0.00% V
------------------------------------------------------------
**optDesign ... cpu = 0:00:12, real = 0:00:14, mem = 2145.9M, totSessionCpu=0:06:37 **
*** Finished optDesign ***
innovus 5>
```

Figure: Optimization after postCTS timing

j. **Route:**

q. Now we go for routing. Go to Route > NanoRoute:

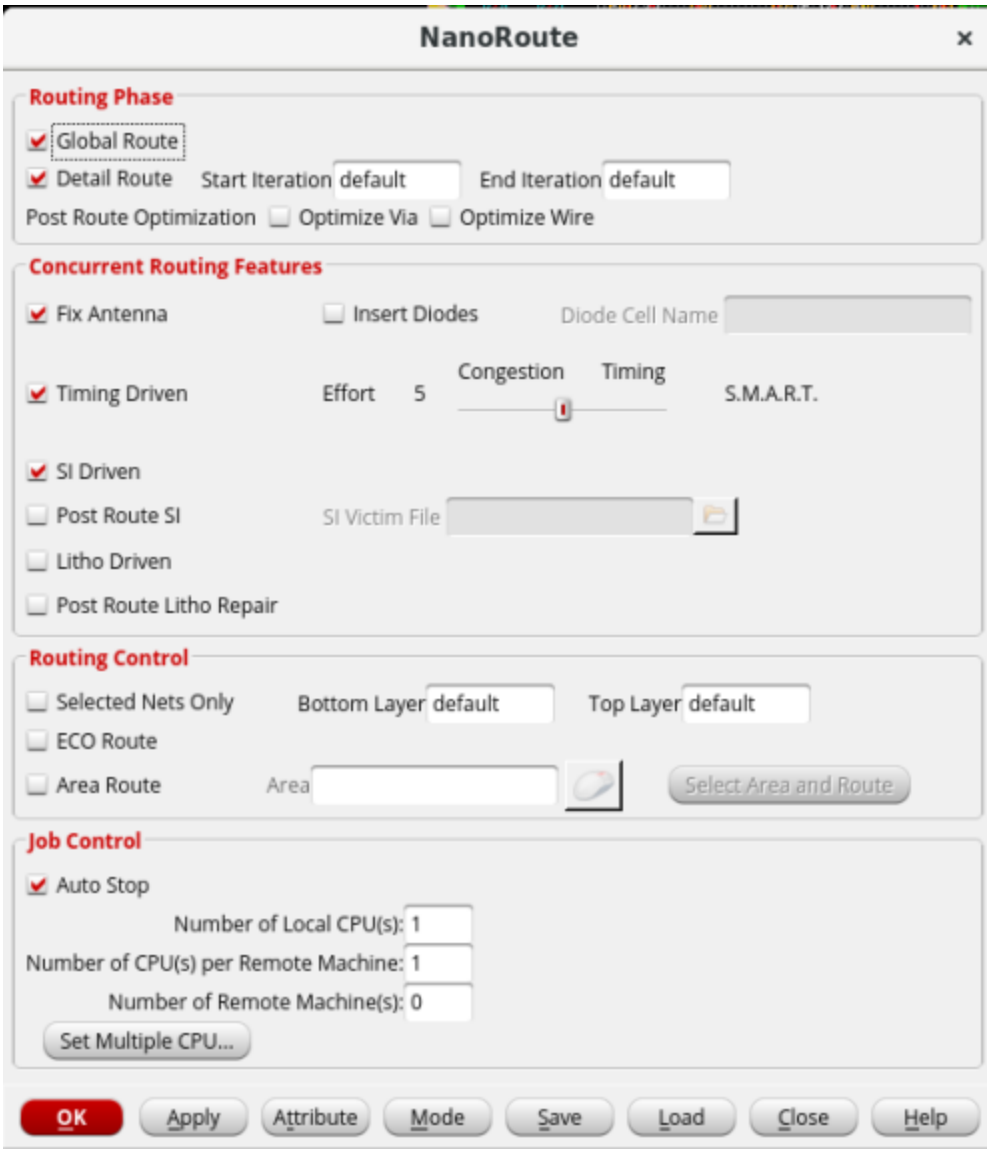

Figure: Specifications for NanoRoute

r. The layout post nanoroute appears as below:

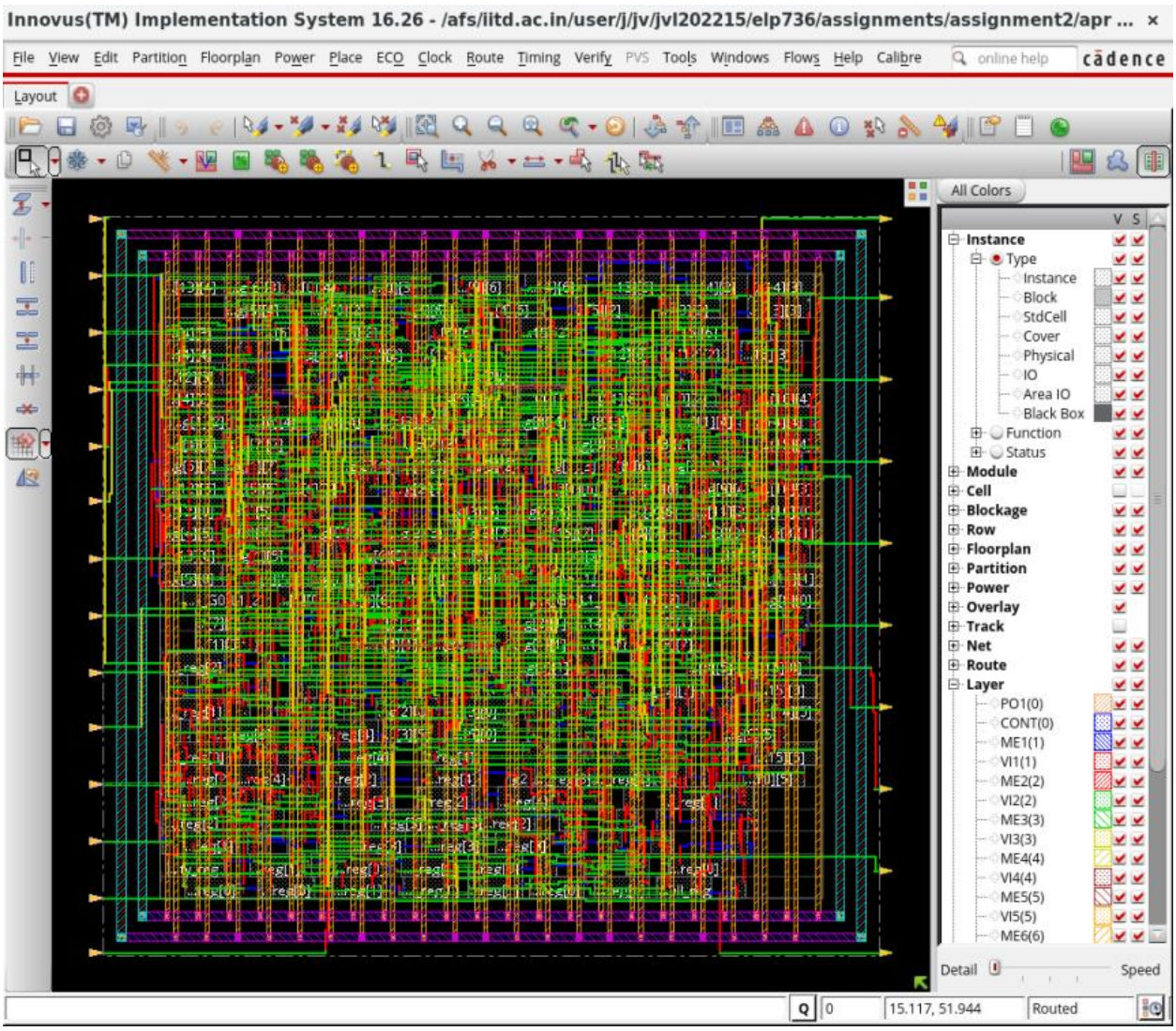

Figure: Layout after NanoRoute

k. postRoute Timing Analysis:

s. Before running post route timing analysis, we need to consider OCVs in our analysis, hence below command is required to be run.

setAnalysisMode -analysisType onChipVariation

t. Running timing report by Timing > Report Timing > postRoute we get report as below. There is no setup violation.

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 30.747  | 30.747  | 30.772  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      1 (21)      |   -0.024    |      1 (21)      |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 71.803%
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 28.59 sec
Total Real time: 33.0 sec
Total Memory Usage: 2111.65625 Mbytes
Reset AAE Options
innovus 6>
```

Figure: postRoute setup timing

u. Now, we go for hold analysis after postRoute

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.045  |  0.030  | -0.045  |
|           TNS (ns):| -3.507  |  0.000  | -3.507  |
|    Violating Paths:|   128   |    0    |   128   |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

Density: 71.803%
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 1.13 sec
Total Real time: 1.0 sec
Total Memory Usage: 2077.140625 Mbytes
Reset AAE Options
innovus 6>
```

Figure: hold analysis postRoute

v. Since still the slack is -ve, we try for postRoute optimization.

```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

Setup views included:
 worst_case
Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 30.747  | 30.747  | 30.773  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.011  |  0.030  |  0.011  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   464   |   286   |   326   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 73.301%
Total number of glitch violations: 0
------------------------------------------------------------
**optDesign ... cpu = 0:00:25, real = 0:00:28, mem = 2257.8M, totSessionCpu=0:09:08 **
 ReSet Options after AAE Based Opt flow
*** Finished optDesign ***
innovus 6>
```

Figure: Optimization over postRoute timing analysis

w. Now, the setup and hold both are clean with margins in WNS for both setup and hold.

l. Extracting RC:

x. Go to Timing > Extract RC and save the spef and spf files as shown in figure below.

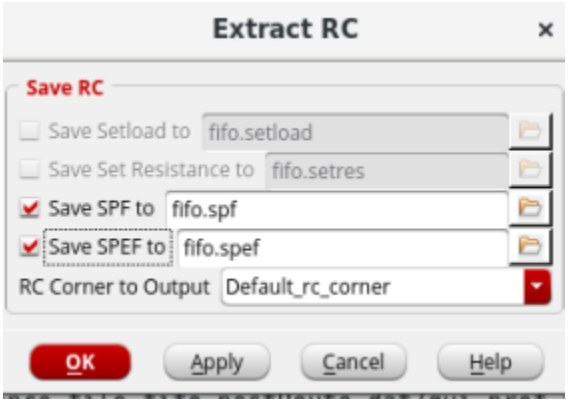

Figure: Extracting spef and spf files

m. Verify

a. Verify Geometry:

a. Click on Verify > Verify Geometry to report if any errors or not.
b. The logs indicate **0 violations**

```
innovus 6>  *** Starting Verify Geometry (MEM: 2440.9) ***

**WARN: (IMPVFG-257):   verifyGeometry command is replaced by verify_drc command.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 2880
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.4  MEM: 0.0M)

innovus 6>
```

Figure: Verify Geometry Logfile Snippet

b. **Verify DRC:**

a. Click on Verify > Verify DRC to report if any errors or not.
b. The logs indicate **0 violations**

```
innovus 6> #-report fifo.drc.rpt                    # string, default="", user setting
 *** Starting Verify DRC (MEM: 2440.9) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 62.600 59.600} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

Figure: Verify DRC Logfile Snippet

c. **Verify Connectivity:**

a. Click on Verify > Verify Connectivity to report if any errors or not.
b. The logs indicate **0 violations**

Verify Connectivity:

```
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Thu Apr  7 04:24:35 2022

Design Name: fifo
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (62.6000, 59.6000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Thu Apr  7 04:24:35 2022
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 6>
```

Figure: Verify Connectivity Logfile Snippet

d. **Verify LVS:** The Spectre tool license availability is an issue. Hence LVS cannot be checked.

4. **Final Layout:**

The final Layout appears as below:

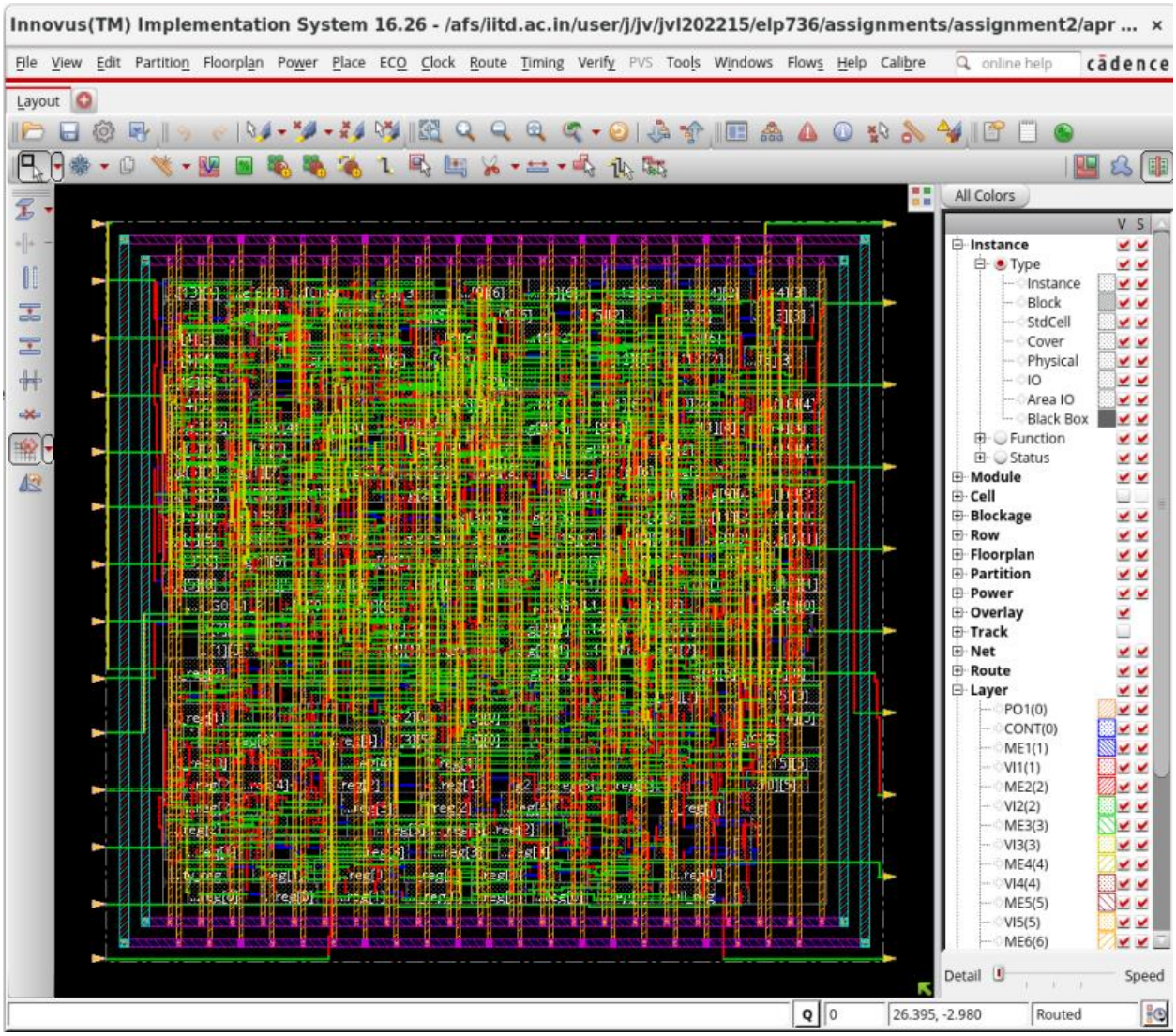

Figure : Final Layout

5. **Summary and Conclusion:**

a. The complete RTL to GDSII workflow till the final nano-route state has been performed.
b. All the timing violations have been cleaned up.
c. The DRC, Connectivity and Geometry checks have been performed and there is no violation therein.