A Report On

Assignment -2

by

Dinesh Joshi (JVL202215)

FOR THE COURSE

ELP736

Physical Design Laboratory

IIT Delhi

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Problem Statement

Perform the following task in INNOVUS
1) Partitioning: breaks up a circuit into smaller sub-circuits or modules that can be designed or analyzed individually.
2) Floorplanning: determines the shapes and arrangement of sub-circuits or modules, as well as the locations of external ports and IP or macro-blocks
Task to be done in GENUS

Design Frequency Specifications:

wclk: 100MHz
rclk: 300MHz

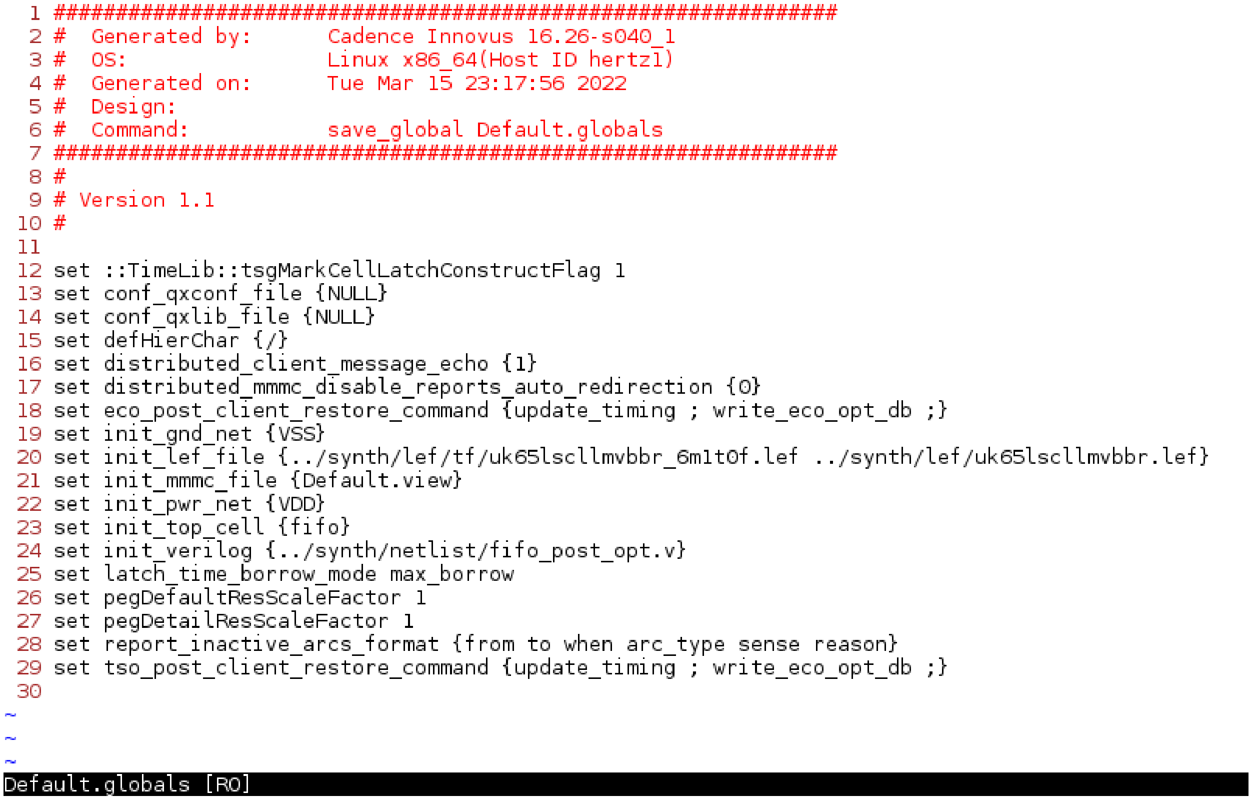
Annexures:

a. Work area path: **/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2**
b. GitHub ID: **https://github.com/DJ-dineshjoshi/async_fifo/tree/main/assignment2**
c. The floorplan is located at below path. Also it has been uploaded onto github. **/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr/fifo_floorplan**

1. Partitioning

The partitioning has been done with the below steps:

a. The design is loaded into innovus tool using File > Import Design > Load.
b. The already configured Default.globals file is picked. The Default.global contains the netlist path, the top module name, the lef file and the mmmc file information.



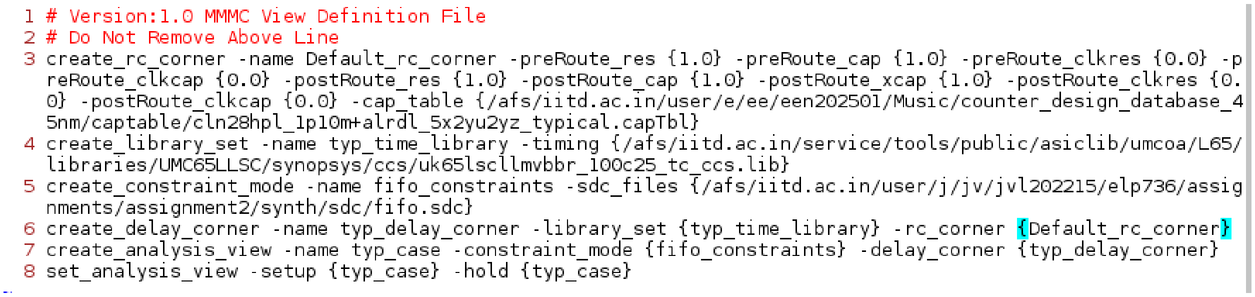
```
#################################################################
#  Generated by:      Cadence Innovus 16.26-s040_1
#  OS:                Linux x86_64(Host ID hertz1)
#  Generated on:      Tue Mar 15 23:17:56 2022
#  Design:
#  Command:           save_global Default.globals
#################################################################
#
# Version 1.1
#

set ::TimeLib::tsgMarkCellLatchConstructFlag 1
set conf_qxconf_file {NULL}
set conf_qxlib_file {NULL}
set defHierChar {/}
set distributed_client_message_echo {1}
set distributed_mmmc_disable_reports_auto_redirection {0}
set eco_post_client_restore_command {update_timing ; write_eco_opt_db ;}
set init_gnd_net {VSS}
set init_lef_file {../synth/lef/tf/uk65lscllmvbbr_6m1t0f.lef ../synth/lef/uk65lscllmvbbr.lef}
set init_mmmc_file {Default.view}
set init_pwr_net {VDD}
set init_top_cell {fifo}
set init_verilog {../synth/netlist/fifo_post_opt.v}
set latch_time_borrow_mode max_borrow
set pegDefaultResScaleFactor 1
set pegDetailResScaleFactor 1
set report_inactive_arcs_format {from to when arc_type sense reason}
set tso_post_client_restore_command {update_timing ; write_eco_opt_db ;}

~
~
~
Default.globals [RO]
```

Fig: Default.globals file contents

c. The mmmc file is also created beforehand and indicated in figure below



```
# Version:1.0 MMMC View Definition File
# Do Not Remove Above Line
create_rc_corner -name Default_rc_corner -preRoute_res {1.0} -preRoute_cap {1.0} -preRoute_clkres {0.0} -preRoute_clkcap {0.0} -postRoute_res {1.0} -postRoute_cap {1.0} -postRoute_xcap {1.0} -postRoute_clkres {0.0} -postRoute_clkcap {0.0} -cap_table {/afs/iitd.ac.in/user/e/ee/een202501/Music/counter_design_database_45nm/captable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl}
create_library_set -name typ_time_library -timing {/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs/uk65lscllmvbbr_100c25_tc_ccs.lib}
create_constraint_mode -name fifo_constraints -sdc_files {/afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/synth/sdc/fifo.sdc}
create_delay_corner -name typ_delay_corner -library_set {typ_time_library} -rc_corner {Default_rc_corner}
create_analysis_view -name typ_case -constraint_mode {fifo_constraints} -delay_corner {typ_delay_corner}
set_analysis_view -setup {typ_case} -hold {typ_case}
```

Fig: Default.view file contents (The MMMC file contents)

d. After loading the design, the layout viewer in the innovus tool shows the grids

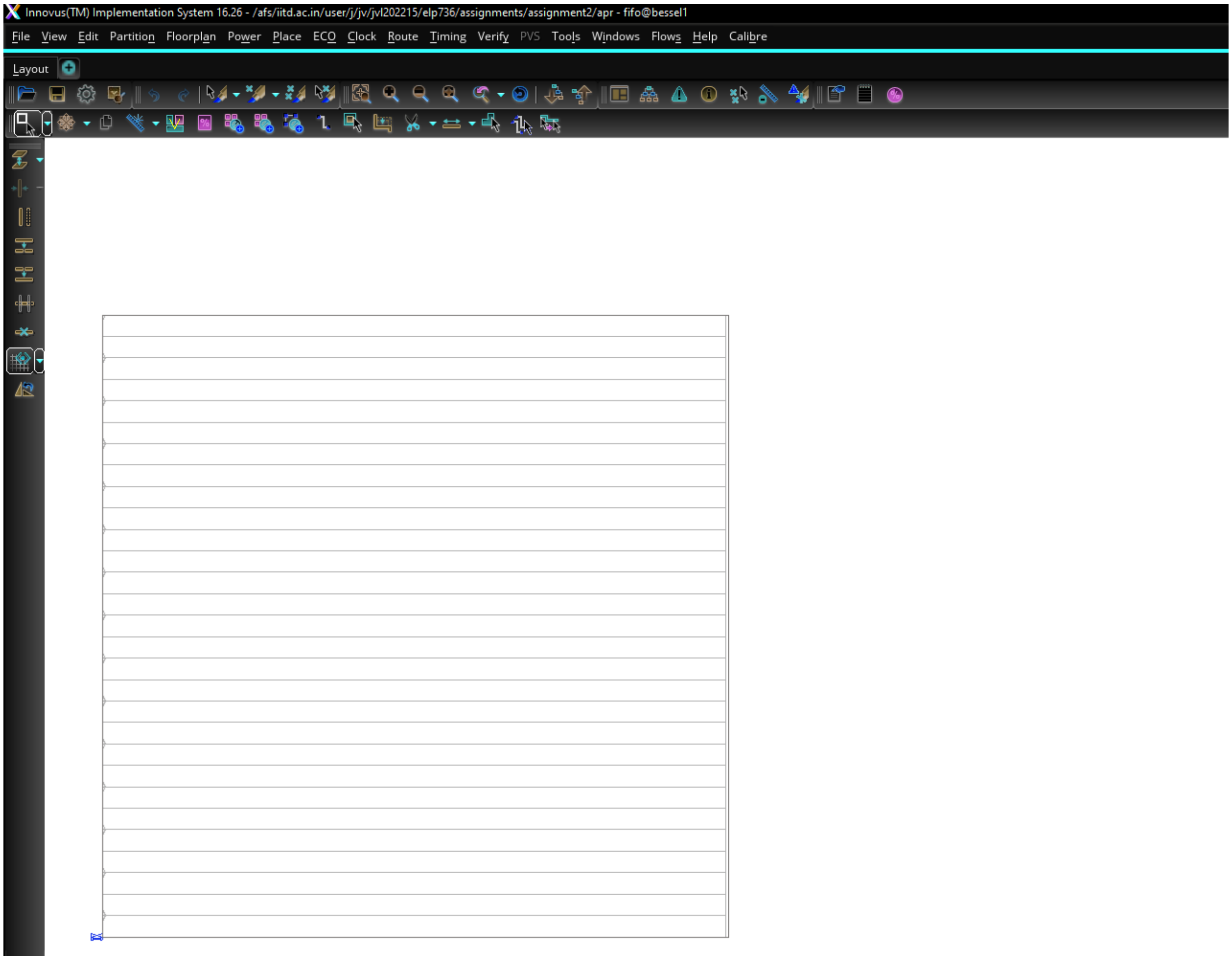
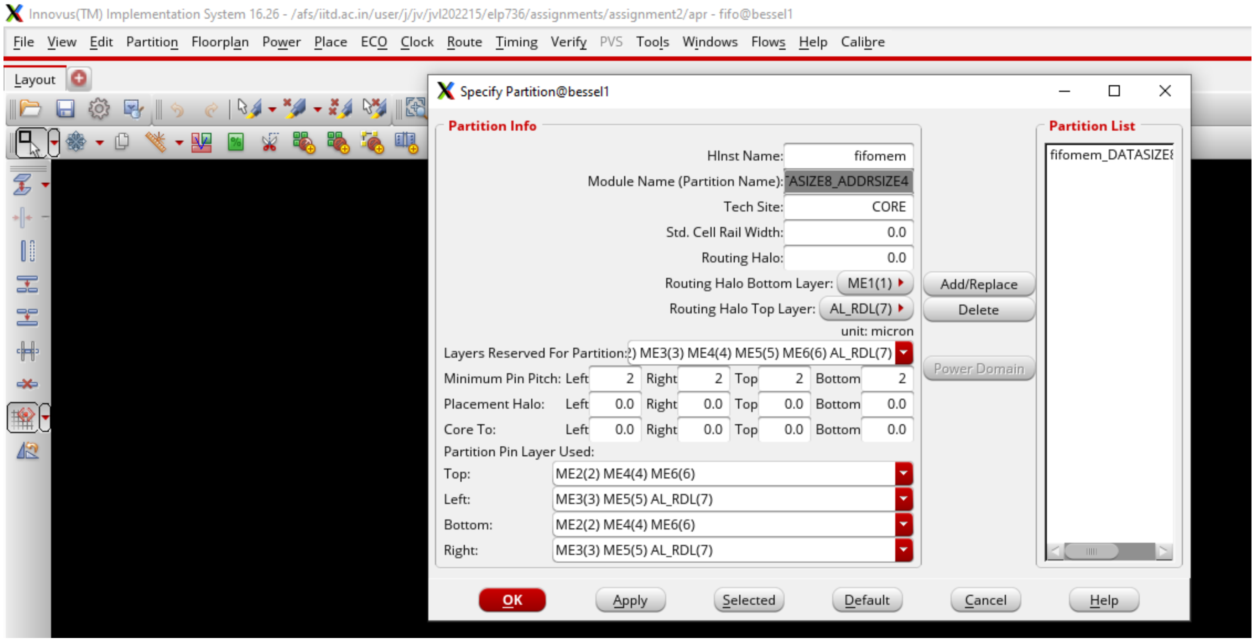

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Layout

Figure: Cadence Layout Viewer window after design import

e. Next, for partitioning, go to Partition > Specify Partition. In the editor window, add any hierarchical instance name. Multiple instances can also be added. The equivalent command for script/nongui usage is:

definePartition -hinst fifomem -coreSpacing 0.0 0.0 0.0 0.0 -railWidth 0.0 -minPitchLeft 2 -minPitchRight 2 -minPitchTop 2 -minPitchBottom 2 -reservedLayer { 1 2 3 4 5 6 7} -pinLayerTop { 2 4 6} -pinLayerLeft { 3 5 7} -pinLayerBottom { 2 4 6} -pinLayerRight { 3 5 7} -placementHalo 0.0 0.0 0.0 0.0 -routingHalo 0.0 -routingHaloTopLayer 7 -routingHaloBottomLayer 1


Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Layout
Specify Partition@bessel1
Add/Replace
Delete
Power Domain
OK
Apply
Selected
Default
Cancel
Help

Partition Info

HInst Name: fifomem

Module Name (Partition Name): ASIZE8_ADDRSIZE4

Tech Site: CORE

Std. Cell Rail Width: 0.0

Routing Halo: 0.0

Routing Halo Bottom Layer: ME1(1)

Routing Halo Top Layer: AL_RDL(7)

unit: micron

Layers Reserved For Partition: 2) ME3(3) ME4(4) ME5(5) ME6(6) AL_RDL(7)

Minimum Pin Pitch: Left 2 Right 2 Top 2 Bottom 2

Placement Halo: Left 0.0 Right 0.0 Top 0.0 Bottom 0.0

Core To: Left 0.0 Right 0.0 Top 0.0 Bottom 0.0

Partition Pin Layer Used:

Top: ME2(2) ME4(4) ME6(6)

Left: ME3(3) ME5(5) AL_RDL(7)

Bottom: ME2(2) ME4(4) ME6(6)

Right: ME3(3) ME5(5) AL_RDL(7)

Partition List

fifomem_DATASIZE8

Figure: Adding partition by writing the instance name and clicking on Add/Replace

f. On clicking on OK, the partition becomes visible as a block adjacent.

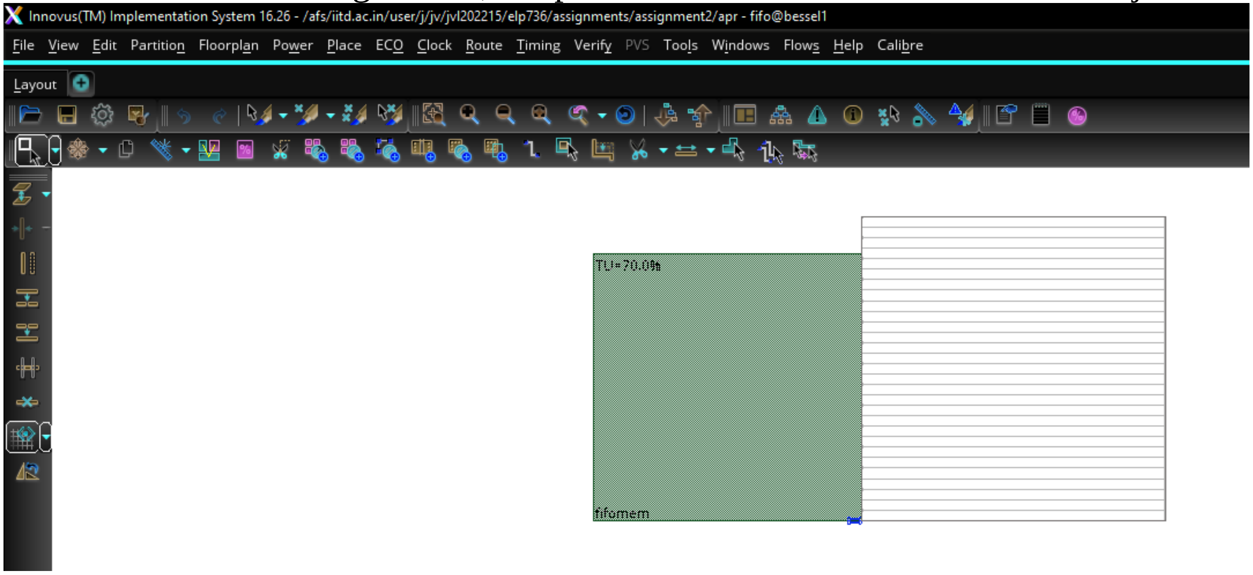
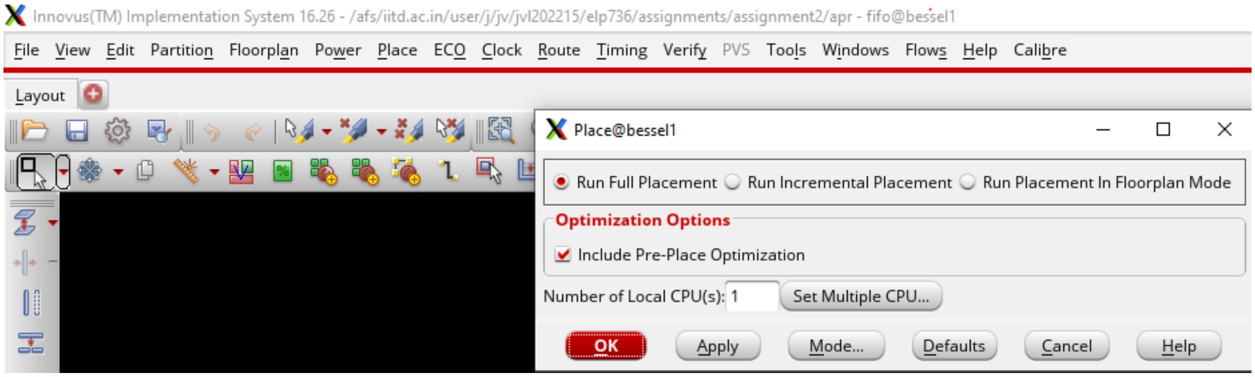

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Layout
TU=70.0%
fifomem

Figure: Selecting fifomem as the partition

g. Now, the standard cells should be placed. Go to Place > Place Standard Cell. Click on Run Full Placement and click on OK.


Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Layout
Place@bessel1
OK
Apply
Mode...
Defaults
Cancel
Help
Set Multiple CPU...

● Run Full Placement ○ Run Incremental Placement ○ Run Placement In Floorplan Mode

Optimization Options

☑ Include Pre-Place Optimization

Number of Local CPU(s): 1

Figure: Selecting Standard Cell Placement

h. This shows a placed layout. To see the floorplan with partition indicated, go to Amoeba view.

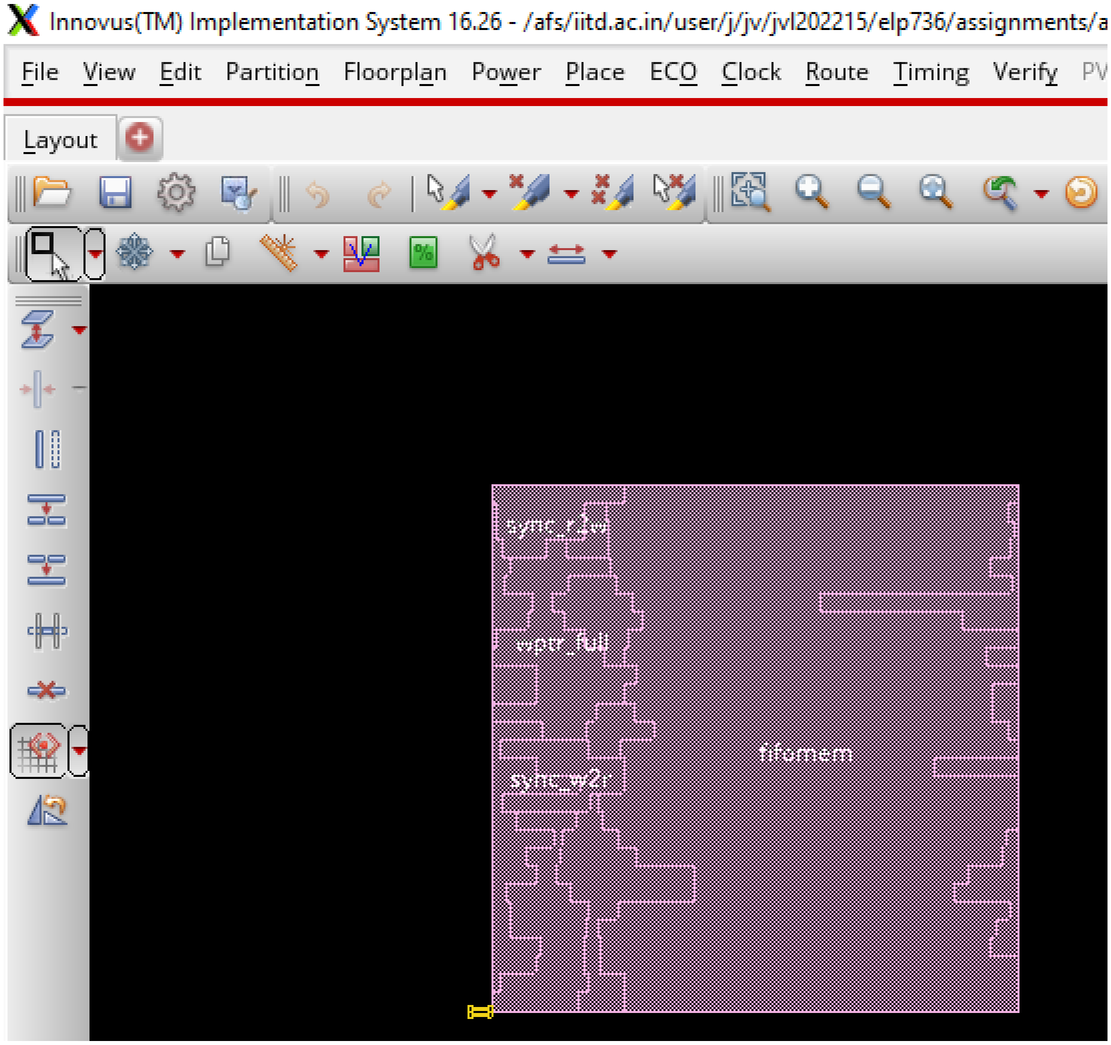

Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/a
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PV
Layout
sync_r2w
wptr_full
fifomem
sync_w2r

Figure: Partitioning view indicating fifomem partition

i. The layout can be seen in the physical view as indicated below

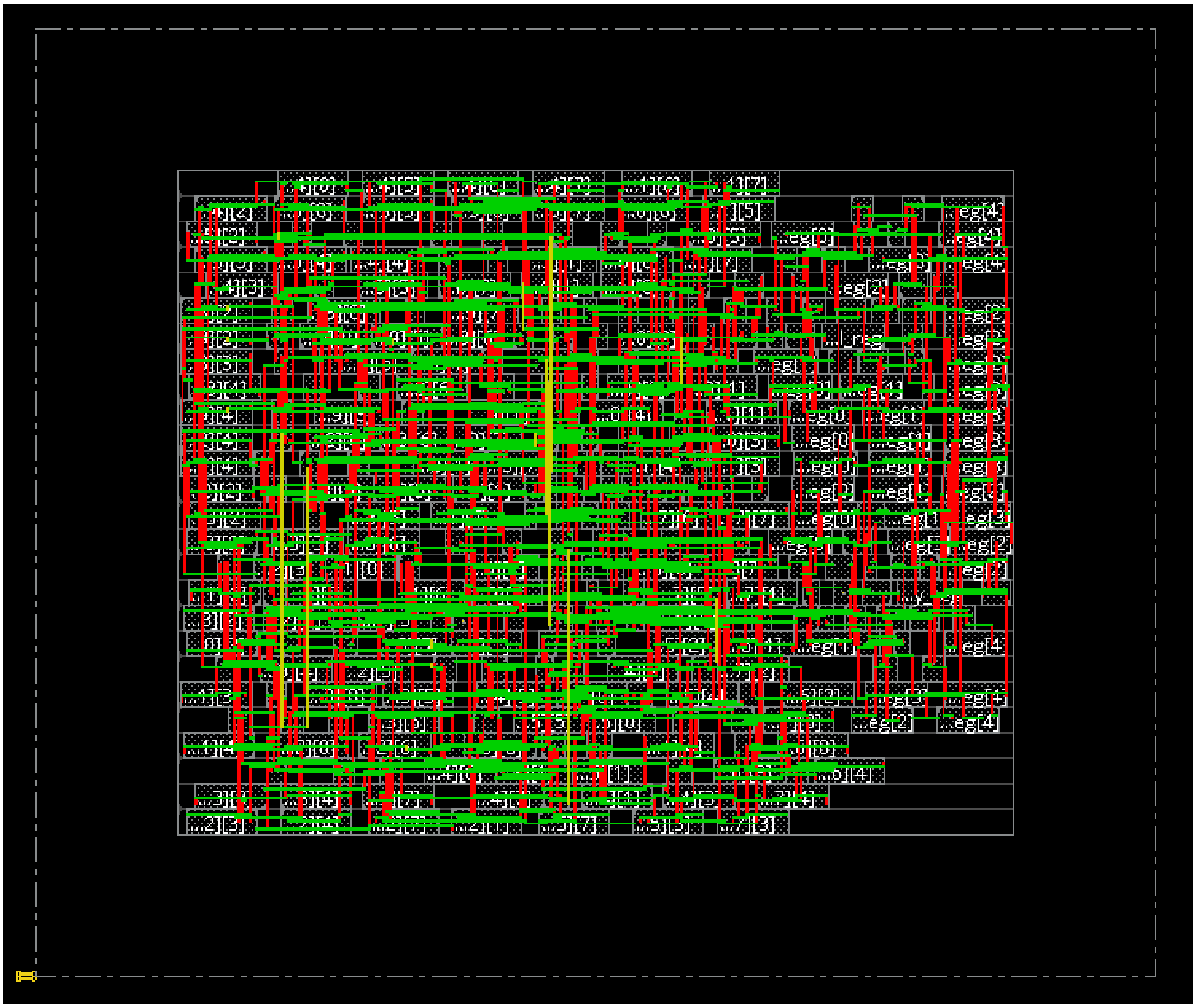


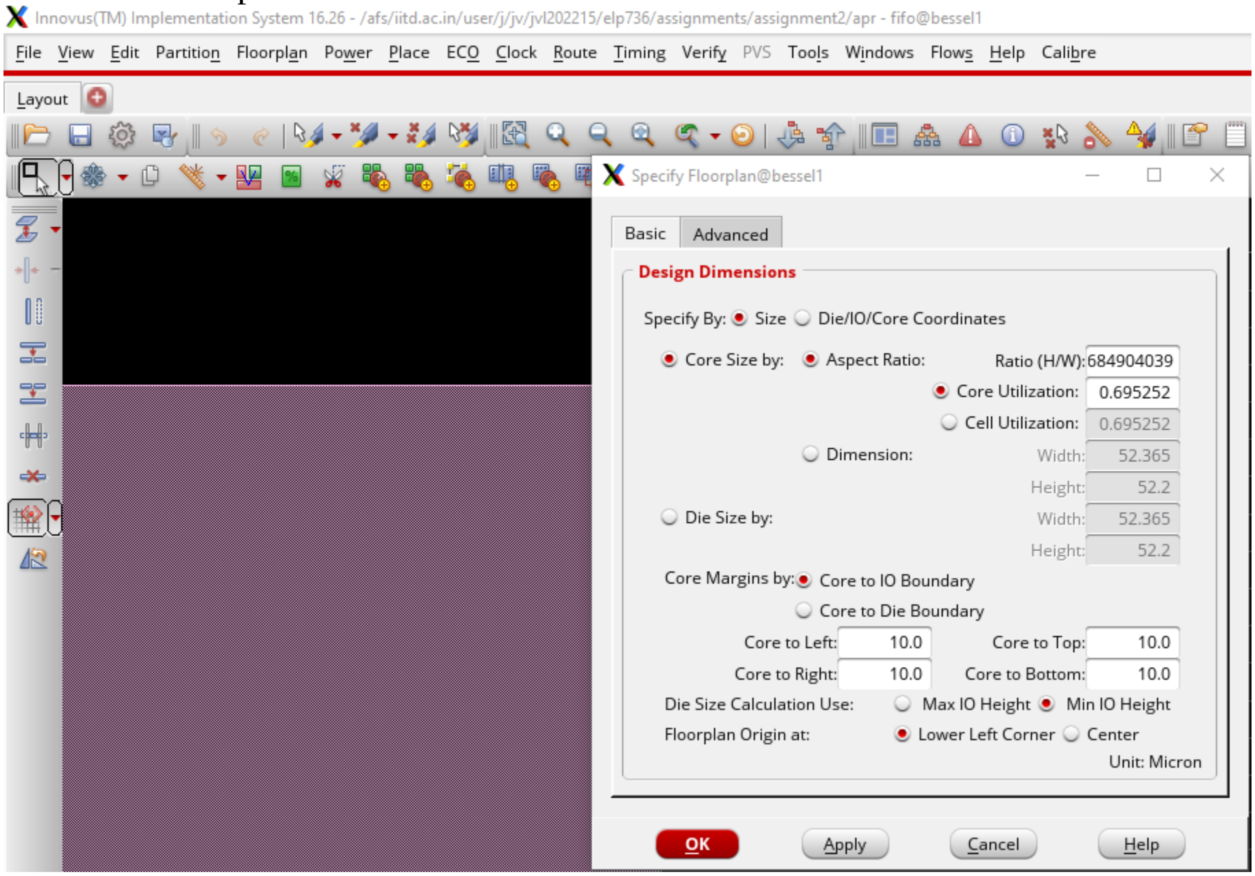
Figure: The physical view of layout

This completes the Partitioning part.

2. Floorplan

The floorplan has been built using the below steps:

a. Click on Floorplan > Specify Floorplan and select Core Size by Aspect Ratio.


Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help Calibre
Layout
Specify Floorplan@bessel1
Basic Advanced
OK Apply Cancel Help

Design Dimensions

Specify By: ● Size ○ Die/IO/Core Coordinates

● Core Size by: ● Aspect Ratio: Ratio (H/W): 684904039

● Core Utilization: 0.695252

○ Cell Utilization: 0.695252

○ Dimension: Width: 52.365 Height: 52.2

○ Die Size by: Width: 52.365 Height: 52.2

Core Margins by: ● Core to IO Boundary ○ Core to Die Boundary

Core to Left: 10.0 Core to Top: 10.0

Core to Right: 10.0 Core to Bottom: 10.0

Die Size Calculation Use: ○ Max IO Height ● Min IO Height

Floorplan Origin at: ● Lower Left Corner ○ Center

Unit: Micron

Figure: Updating the floorplan specifications.

b. Update the specifications. Add Core to IO boundary as 10. Click on OK. A box becomes available outside the core with the spacings as mentioned in Core to IO Boundary specifications in previous step.

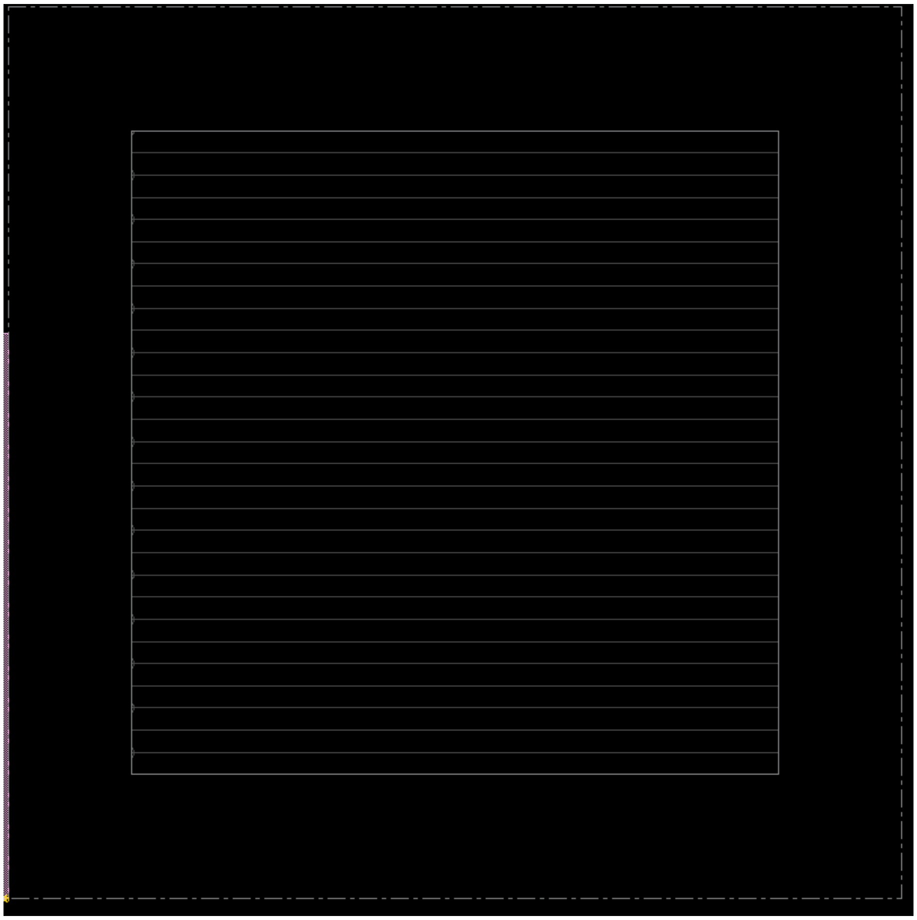


Figure: The Core to IO boundary specifications visible in the layout viewer

c. Now, edit the pin allocations by Edit > Pin Editor. After the pin editing, the floorplan appears as in figure below. The equivalent command for script/nongui users is:

```
setPinAssignMode -pinEditInBatch true
editPin -fixOverlap 1 -unit MICRON -spreadDirection clockwise -
side Right -layer 1 -spreadType start -spacing 0.2 -start 0.0 0.0 -pin
{{rdata[0]} {rdata[1]} {rdata[2]} {rdata[3]} {rdata[4]} {rdata[5]}
{rdata[6]} {rdata[7]} wfull rempty}
setPinAssignMode -pinEditInBatch false
```

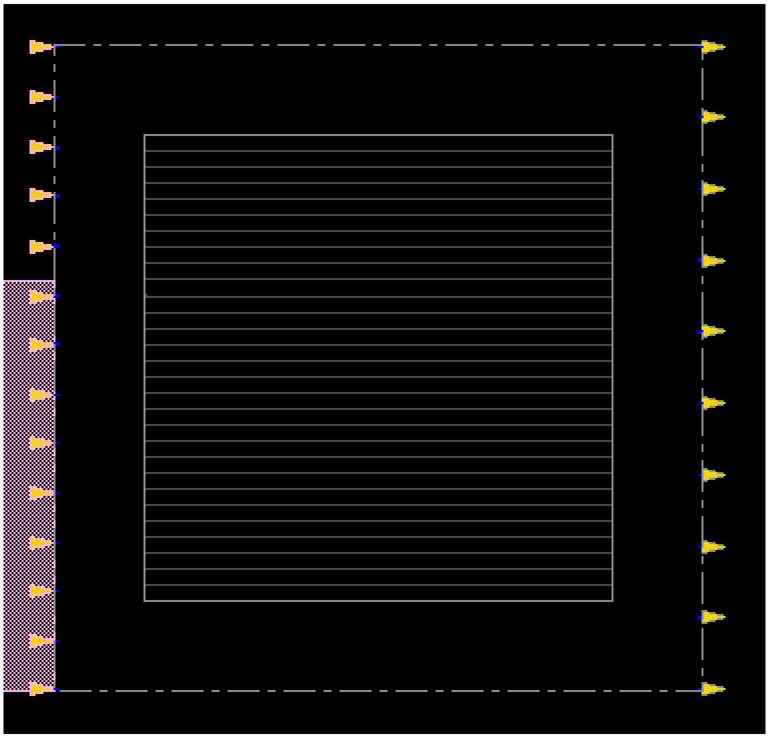


Figure: The pin allocations done

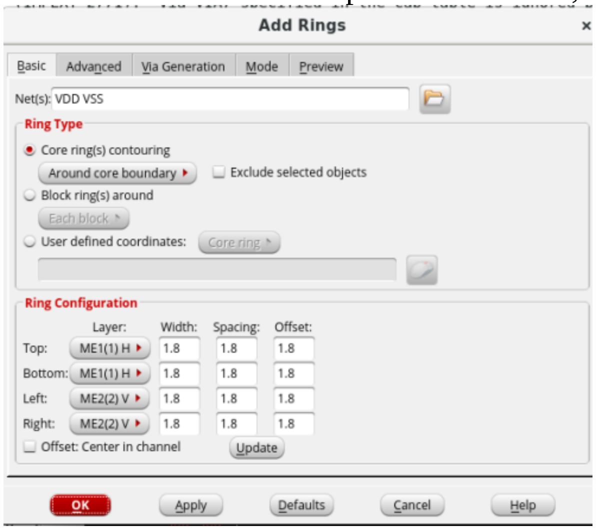
With this, we are done with the floorplanning, next we will proceed to power planning stage.

3. Powerplan

For power planning, following steps should be followed:

a. Go to Power > Power Planning > Add Rings

b. Select VDD and VSS as the nets and provide the width, spacing and offsets.



Add Rings

Basic | Advanced | Via Generation | Mode | Preview

Net(s): VDD VSS

Ring Type

● Core ring(s) contouring

Around core boundary ▸ □ Exclude selected objects

○ Block ring(s) around

Each block ▸

○ User defined coordinates: Core ring ▸

Ring Configuration

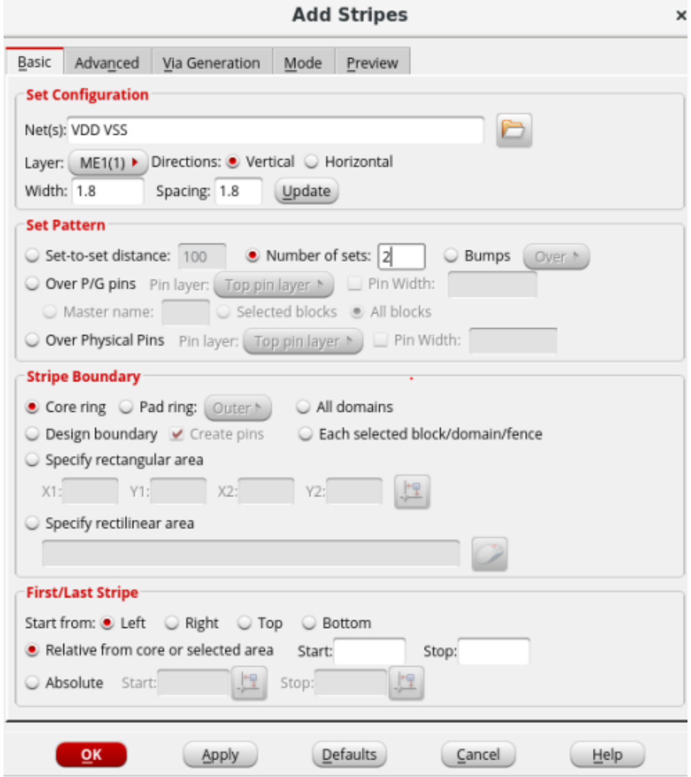
	Layer:	Width:	Spacing:	Offset:
Top:	ME1(1) H ▸	1.8	1.8	1.8
Bottom:	ME1(1) H ▸	1.8	1.8	1.8
Left:	ME2(2) V ▸	1.8	1.8	1.8
Right:	ME2(2) V ▸	1.8	1.8	1.8

□ Offset: Center in channel Update

OK Apply Defaults Cancel Help

Figure: The rings being added on VDD and VSS

c. Now go to Power > Power Planning > Add stripes and add required set of stripes to VDD and VSS. We have added 2 sets.



Add Stripes

Basic | Advanced | Via Generation | Mode | Preview

Set Configuration

Net(s): VDD VSS

Layer: ME1(1) ▸ Directions: ● Vertical ○ Horizontal

Width: 1.8 Spacing: 1.8 Update

Set Pattern

○ Set-to-set distance: 100 ● Number of sets: 2 ○ Bumps Over ▸

○ Over P/G pins Pin layer: Top pin layer ▸ □ Pin Width:

○ Master name: ○ Selected blocks ● All blocks

○ Over Physical Pins Pin layer: Top pin layer ▸ □ Pin Width:

Stripe Boundary

● Core ring ○ Pad ring: Outer ▸ ○ All domains

○ Design boundary ☑ Create pins ○ Each selected block/domain/fence

○ Specify rectangular area

X1: Y1: X2: Y2:

○ Specify rectilinear area

First/Last Stripe

Start from: ● Left ○ Right ○ Top ○ Bottom

● Relative from core or selected area Start: Stop:

○ Absolute Start: Stop:

OK Apply Defaults Cancel Help

Figure: Stripes being added on VDD and VSS

d. This completes the power planning stage. The layout appears as indicated in the figure below:

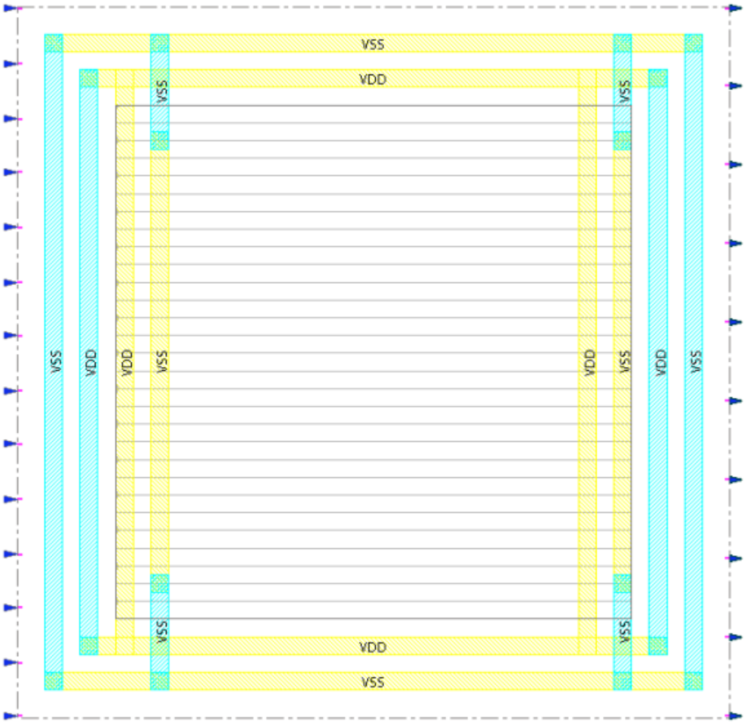
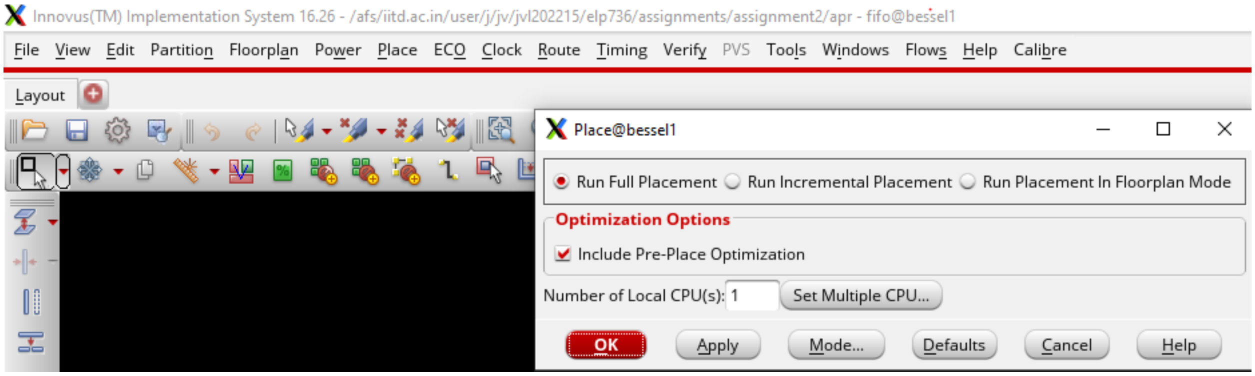


Figure: Layout post Power planning

4. Placement

The steps followed for placement are as follows:

a. The standard cells are placed. Go to Place > Place Standard Cell. Click on Run Full Placement and click on OK.



Innovus(TM) Implementation System 16.26 - /afs/iitd.ac.in/user/j/jv/jvl202215/elp736/assignments/assignment2/apr - fifo@bessel1

Place@bessel1

● Run Full Placement ○ Run Incremental Placement ○ Run Placement In Floorplan Mode

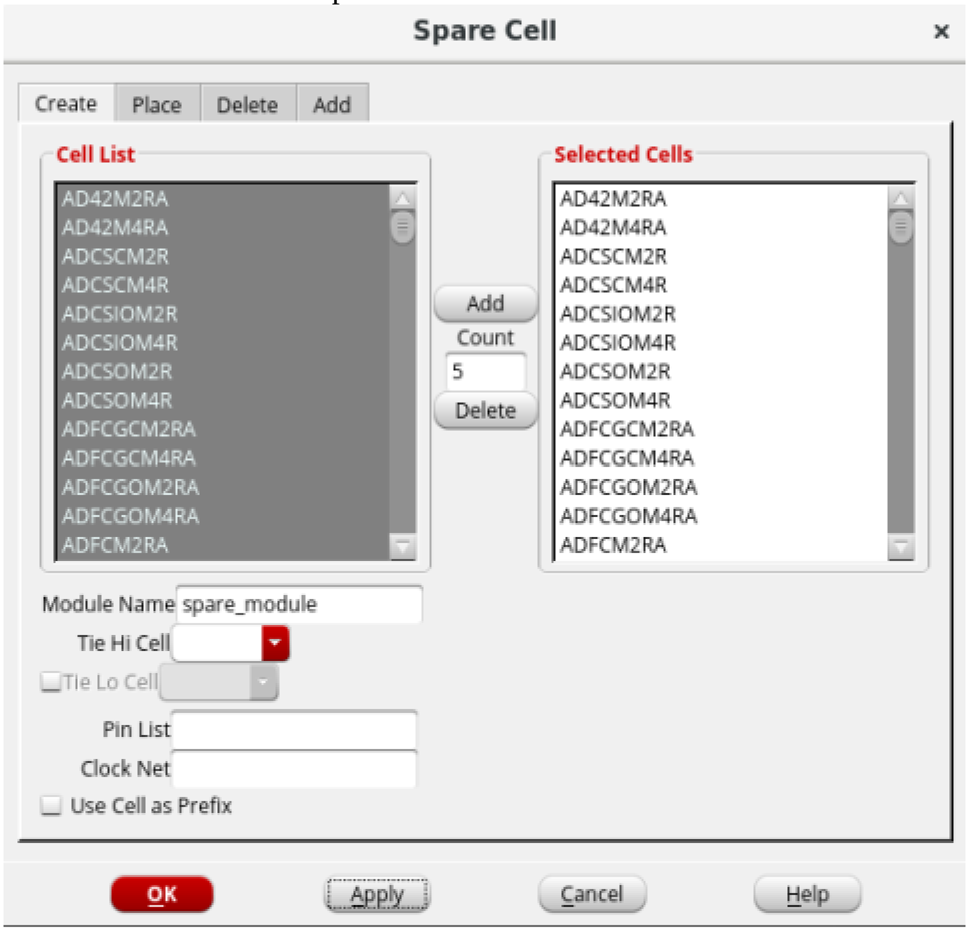
Optimization Options

☑ Include Pre-Place Optimization

Number of Local CPU(s): 1

Figure: Selecting Standard Cell Placement

b. Go to Place > Place Spare Cells. Add 5 instances of all modules.



Spare Cell

Cell List

AD42M2RA
AD42M4RA
ADCSCM2R
ADCSCM4R
ADCSIOM2R
ADCSIOM4R
ADCSOM2R
ADCSOM4R
ADFCGCM2RA
ADFCGCM4RA
ADFCGOM2RA
ADFCGOM4RA
ADFCM2RA

Selected Cells

AD42M2RA
AD42M4RA
ADCSCM2R
ADCSCM4R
ADCSIOM2R
ADCSIOM4R
ADCSOM2R
ADCSOM4R
ADFCGCM2RA
ADFCGCM4RA
ADFCGOM2RA
ADFCGOM4RA
ADFCM2RA

Count 5

Module Name spare_module

Tie Hi Cell

□ Tie Lo Cell

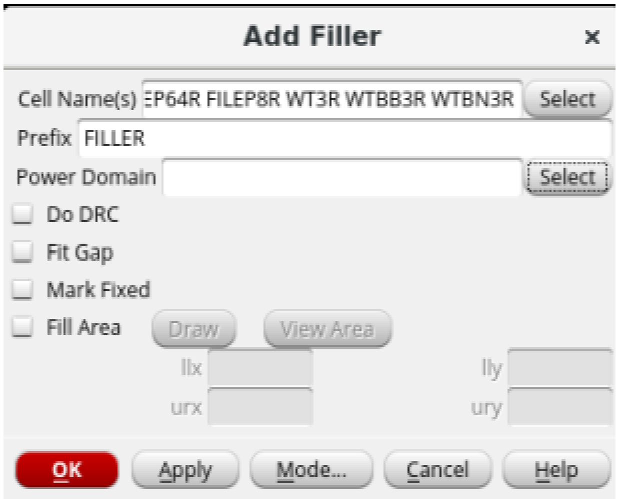
Pin List

Clock Net

□ Use Cell as Prefix

Figure: Selecting Spare Cell Placement

c. Now we can proceed to Filler cell placement. Go to Place > Physical Cell > Add Filler



Add Filler

Cell Name(s) :P64R FILEP8R WT3R WTBB3R WTBN3R

Prefix FILLER

Power Domain

□ Do DRC

□ Fit Gap

□ Mark Fixed

□ Fill Area

Figure: Filler addition

d. Now we have the standard cells, the spare cells and the filler cells, all are added. This completes the placement part. The post placement layout appears as below.

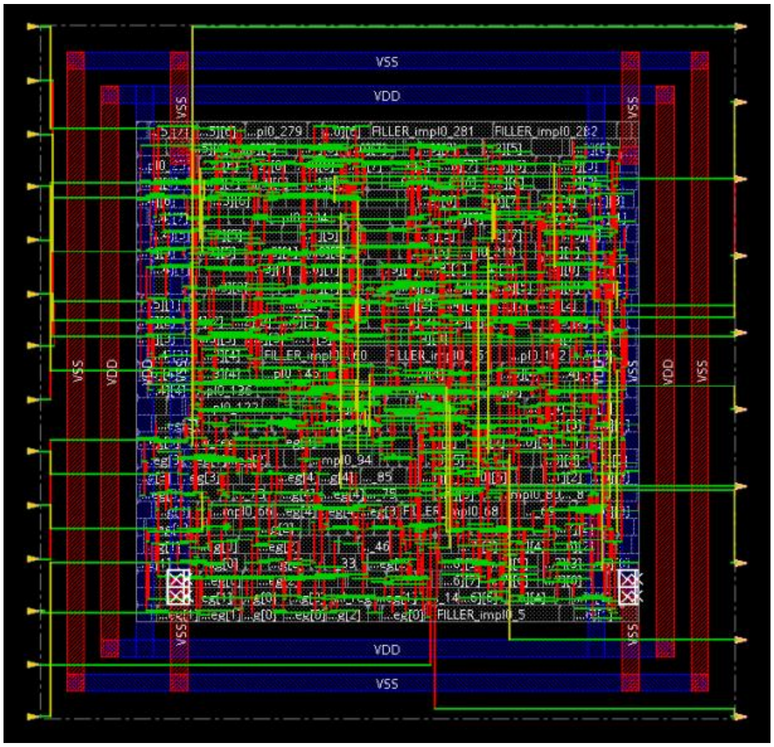


Figure: Layout after placement