SiFive FE310-G000 Preliminary Datasheet
1.0.4

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Proprietary Notice

Release Information

Version	Date	Changes
1.0.4	August 28, 2017	Correct AON_PSD_LFALTCLK name on datasheet.
1.0.3	August 4, 2017	Add OTP information
1.0.2	August 3, 2017	Correct dimensions of recommended footprint
1.0.1	July 24, 2017	Correct DWAKEUP_N and AON_PMU_OUT_0 pin assignments
1.0.0	July 6, 2017	Preliminary Datasheet Release

Contents

Chapter 1

FE310-G000 Description

1.1 Features

- SiFive E31 Coreplex up to 320MHz.
- Flexible clocking options including internal PLL, free-running ring oscillator and external 16MHz crystal.
- 1.61 DMIPs/MHz, 2.73 Coremark/MHz
- RV32IMAC
- 8kB OTP Program Memory
- 8kB Mask ROM
- 16kB Instruction Cache
- 16kB Data SRAM
- 3 Independent PWM Controllers
- External RESET pin
- JTAG, SPI and UART interfaces.
- QSPI Flash interface.
- Requires 1.8V and 3.3V supplies.
- Hardware Multiply and Divide

1.2 Description

The FE310-G000 is the first Freedom E300 SoC, and is the industrys first commercially available RISC-V SoC. The FE310-G000 is built around the E31 Coreplex instantiated in the Freedom E300 platform.

The *Freedom E300 Platform and FE310-G000* manuals should be read together with this datasheet. This datasheet provides electrical specifications and an overview of the FE310-G000.

The FE310-G000 is offered as engineering samples only, with limited factory testing. A fully qualified revision of this part in the same package and with a similar pinout will be available in production quantities. Please consult with SiFive marketing for schedule and specification.

The FE310-G000 comes in a convenient, industry standard 6x6mm 48-lead QFN package (0.4mm pad pitch).

Chapter 2

FE310-G000 Pins

2.1 FE310-G000 Pinout

The FE310-G000 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) should be connected directly to the ground plane.

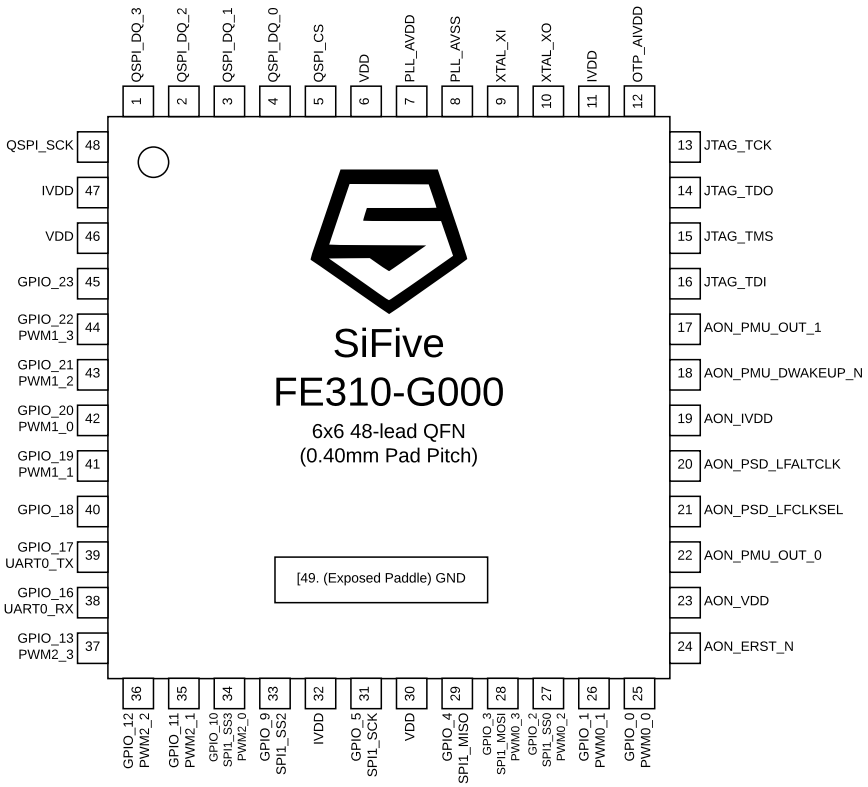

Figure 2.1: FE310-G000 Pinout

2.2 Pin Descriptions

2.3 Power Pins

VDD (6, 30, 46) : Core supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

IVDD (11, 32, 47) : I/O supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.

AON_VDD (23) : AON supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

AON_IVDD (19) : AON I/O supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

OTP_AIVDD (12) : OTP supply voltage. 3.3V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All IVDD pins must be connected externally.
n **PLL_AVDD (7) :** PLL supply voltage. 1.8V +/- 10%. Recommended 1uF ceramic bypass capacitor to GND plane mounted close to the device. All VDD pins must be connected externally.

PLL_AVSS (8) : Isolated PLL supply bypass. Connect through a 1uF ceramic capacitor to PLL_AVDD. This pin is not to be connected directly to GND.

GND (49) : Exposed paddle is a ground return and should be connected directly to the ground plane.

2.4 Crystal Drivers

XTAL_XI (9) : 16MHz Crystal Input
XTAL_XO (10) : 16MHz Crystal Output

An external 16MHz crystal may be connected between the two XTAL pins. The crystal should have a capacitive load of 12 pF and an ESR 80 Ohms. An external oscillator may also be used to drive the FE310-G000 through the XTAL_XI input, in which case the XTAL_XO pin should be left floating. The external oscillator should operate between GND and the 1.8V VDD supply.

2.5 JTAG

JTAG_TCK (13) : JTAG TCK Input
JTAG_TDO (14) : JTAG TDO Output
JTAG_TMS (15) : JTAG TMS Input
JTAG_TDI (16) : JTAG TDI Input

Please refer to the *E300 Platform Reference Manual* for information on the JTAG and debug facilities.

2.6 QSPI

QSPI_DQ_3 (1) : Bidirectional Quad SPI Data Line
QSPI_DQ_2 (2) : Bidirectional Quad SPI Data Line
QSPI_DQ_1 (3) : Bidirectional Quad SPI Data Line
QSPI_DQ_0 (4) : Bidirectional Quad SPI Data Line

QSPI_CS (5) : Quad SPI Chip Select OUTPUT, Active Low.
QSPI_SCK (48) : Quad SPI Clock OUTPUT

Please refer to the *E300 Platform Reference Manual* for information on the SPI FLASH interface and to the Applications Notes and Errata section of this datasheet for information in the SPI implementation.

2.7 GPIO Multiplexed Outputs

The General Purpose Input/Output pins are multiplexed with PWM, SPI and UART functions as described in Table 2.1. GPIO pins may be configured as inputs or outputs, with a weak pull-up, and with two drive strengths. In addition, PWM, SPI and UART functions may be multiplexed on the pins through the GPIO control register. Please refer to the *E300 Platform Reference Manual* for information on GPIO capabilities.

Name	Pin	GPIO	PWM	SPI	UART
GPIO_0	25	0 I/O	PWM0_0 O		
GPIO_1	26	1 I/O	PWM0_1 O		
GPIO_2	27	2 I/O	PWM0_2 O	SPI1_SS0	
GPIO_3	28	3 I/O	PWM0_3 O	SPI1_MOSI	
GPIO_4	29	4 I/O		SPI1_MISO	
GPIO_5	31	5 I/O		SPI1_SCK	
GPIO_9	33	9 I/O		SPI1_SS2	
GPIO_10	34	10 I/O	PWM2_0 O	SPI1_SS3	
GPIO_11	35	11 I/O	PWM2_1 O		
GPIO_12	36	12 I/O	PWM2_2 O		
GPIO_13	37	13 I/O	PWM2_3 O		
GPIO_16	38	16 I/O			UART0_RX I
GPIO_17	39	17 I/O			UART0_TX O
GPIO_18	40	18 I/O			
GPIO_19	41	19 I/O	PWM1_0 O		
GPIO_20	42	20 I/O	PWM1_1 O		
GPIO_21	43	21 I/O	PWM1_2 O		
GPIO_22	44	22 I/O	PWM1_3 O		
GPIO_23	45	23 I/O			

Table 2.1: GPIO pin assignments.

2.8 AON Block Interface Pins

The following pins interface to the Always-ON (AON) block. AON Block I/O pins are 1.8V only.

AON_PMU_OUT_0 (22) : Programmable SLEEP control OUTPUT, 1.8V levels.
AON_PMU_OUT_1 (17) : Programmable SLEEP control OUTPUT, 1.8V levels.
AON_PMU_DWAKEUP_N (18) : Digital Wake-From-Sleep INPUT, active LOW. 1.8V levels.
AON_ERST_N (24) : External System Reset INPUT, active LOW. 1.8V levels.
AON_PSD_LFALTCLK (20) : Optional 32kHz Clock Input. 1.8V levels.
AON_PS_LFCLKSEL (21) : 32kHz Clock Source Selector. 1.8V levels. When driven low, AON PSD LFALTCLK input is used as the 32 kHz low-frequency clock source. When left unconnected or driven high, the internal LFROSC source is used.

Chapter 3

Configuration and Block Diagram

3.1 Block Diagram

Figure 3.1 shows the overall block diagram of FE310-G000ḞE310-G000 contains an E31-based Coreplex, a selection of flexible I/O peripherals, a dedicated off-chip Quad-SPI flash controller for execute-in-place, 8 KiB of in-circuit programmable OTP memory, 8 KiB of mask ROM, clock generation, and an always-on (AON) block including a programmable power-management unit (PMU).

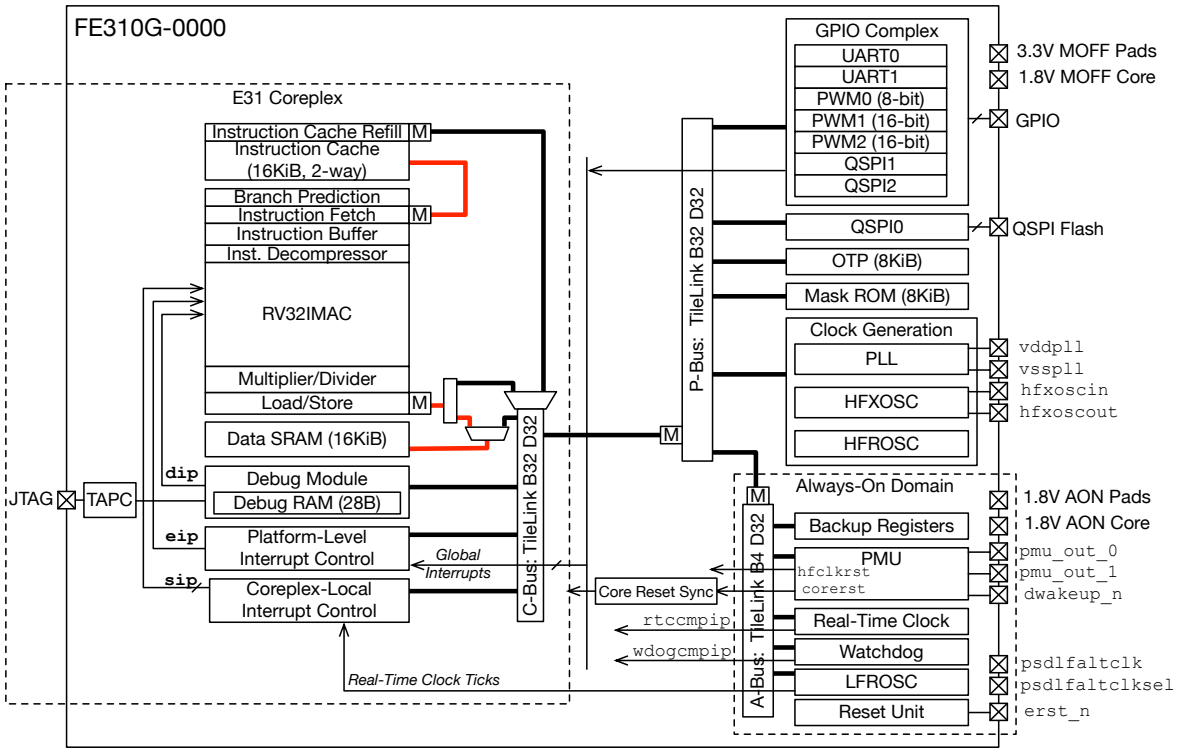

Figure 3.1: FE310-G000 top-level block diagram.

3.2 E31 Coreplex Configuration

The core is configured to support the RV32IMAC ISA options.

The branch predictor configuration has 40 branch-target buffer (BTB) entries, 128 branch-history (BHT) entries, and a two-entry return-address stack (RAS).

The integer multiplier completes 8 bits per cycle, so takes up to four clock cycles for a single 32×32 multiply operation.

The integer divider completes one bit per clock cycle, with an early out.

The instruction cache is a 16 KiB two-way set associative with 32-byte lines.

The data SRAM is 16 KiB.

The system mask ROM is 8 KiB in size and contains simple boot code. The system ROM also holds the platform configuration string and debug ROM routines.

3.3 CLINT

The Coreplex-Local Interrupt Controller (CLINT) supports the standard timer and software interrupts.

3.4 PLIC

The platform-level interrupt controller (PLIC) receives interrupt signals from the peripheral devices and prioritizes these for service by the core. The PLIC supports 7 programmable priority levels. Please refer to the chapter "FE310-G000 Interrupts" in the *SiFive FE310-G000 Manual* for more information on the PLIC implementation.

3.5 JTAG Connections

A four-wire 1149.1 JTAG connection is used to connect the external debugger to the internal debug module.

3.6 Debug Module

The debug module is accessed over JTAG, and has support for two programmable hardware breakpoints. The debug RAM has 28 bytes of storage.

3.7 Quad-SPI Flash

A dedicated quad-SPI (QSPI) flash interface is provided to hold code and data for the system. The QSPI interface supports burst reads of 32 bytes over TileLink to accelerate instruction cache refills. The QSPI can be programmed to support eXecute-In-Place modes to reduce SPI command overhead on instruction cache refills. The QSPI interface also supports single-word data reads over the primary TileLink interface, as well as programming operations using memory-mapped control registers.

3.8 GPIO Complex

The GPIO complex manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. FE310-G000

has two additional QSPI controllers in the GPIO block, one with four chip selects and one with one. FE310-G000 also has two UARTs. FE310-G000 has three PWM controllers, two with 16-bit precision and one with 8-bit precision.

3.9 Always-On (AON) Block

The AON block contains the reset logic for the chip, an on-chip low-frequency oscillator, a watchdog timer, connections for an off-chip low-frequency clock source, the real-time clock, a programmable power-management unit, and 16×32-bit backup registers that retain state while the rest of the chip is powered down.

The AON can be instructed to put the system to sleep. The AON can be programmed to exit sleep mode on a real-time clock interrupt or when the external digital wakeup pin, `dwakeup_n`, is pulled low. The `dwakeup_n` input supports wired-OR connections of multiple wakeup sources.

3.10 Power Supply

FE310-G000 requires two dedicated power rails providing 1.8 V power to the always-on block and core logic, and 3.3 V to the I/O pads.

Chapter 4

FE310-G000 Typical Electrical Specifications

Note: These electrical specifications are TYPICAL ONLY, and are not thoroughly tested in engineering sample parts. Production versions of the devices will be provided with a complete electrical specification. Except where otherwise noted, the typical electrical parameters are specified under the following conditions: Ambient Temperature 27C, VDD Supply Voltage 1.8V, IVDD Supply Voltage 3.3V, Processor Clock 16MHz crystal. ***These are preliminary specifications and are subject to change without notice based on characterization.***

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IIVDD	IVDD Supply Current	ACTIVE, 16MHz		8		mA
		ACTIVE, 250MHz		16		mA
IVDD	VDD Supply Current	ACTIVE, 16MHz		8		mA
		ACTIVE, 250MHz		150		mA

Table 4.1: FE310-G000 Supply Voltage and Current Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	Input Voltage LOW Threshold	GPIO		0.9		V
VIH	Input Voltage HIGH Threshold	GPIO		0.9		V
VOL	Output Voltage LOW	GPIO, DS=0, 1mA DC Load		20		mV
		GPIO, DS=1, 1mA DC Load		16		mV
		GPIO, DS=0, 20mA DC Load		380		mV
		GPIO, DS=1, 20mA DC Load		280		mV
VOH	Output Voltage HIGH, with respect to VDDIO	GPIO, DS=0, 1mA DC Load		-18		mV
		GPIO, DS=1, 1mA DC Load		-14		mV
		GPIO, DS=0, 20mA DC Load		-400		mV
		GPIO, DS=1, 20mA DC Load		-290		mV
IOL	Output Current LOW	GPIO, DS=0, VGPIO=0.3V		16		mA
		GPIO, DS=1, VGPIO=0.3V		21		mA
IOH	Output Current HIGH	GPIO, DS=0, VGPIO=3.0V		-15		mA
		GPIO, DS=1, VGPIO=3.0V		-21		mA
IPUL	Output Pull-Up Current	GPIO, VGPIO=0V		-85		uA
	(PUE=1)	GPIO, VGPIO=2V		-75		uA
ILKH	Input Leakage, HIGH	GPIO, VGPIO=3.3V		200		pA
ILKL	Input Leakage, LOW	GPIO, VGPIO=0V		-100		pA

Table 4.2: FE310-G000 Input/Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FLFRO	Low Frequency Ring Oscillator Center Frequency			40		kHz
FHFRO	High Frequency Ring Oscillator Center Frequency			72		MHz
FMAX	Maximum Tested Operating Frequency			320		MHz

Table 4.3: FE310-G000 AC Characteristics

Chapter 5

FE310-G000 Application Notes and Errata

5.1 Boot Code

The FE310-G000 boots by jumping to the beginning of the OTP memory and executing code found there. As shipped, the OTP memory at the boot location is preprogrammed to jump immediately to the end of the OTP memory, which contains the following code to jump to the beginning of the SPI-Flash at `0x2000_0000`:

```
fence 0,0
li t0, 0x20000000
jr t0
```

`fence 0,0` is encoded as `0x0000_000F`, and the instruction may be modified by burning additional bits to transform it into a JAL instruction (opcode `0x6F`) to execute arbitrary code rather than jumping directly to the beginning of the SPI-Flash.

Please refer to the OTP Memory section of this datasheet for more information on programming the OTP.

5.2 Trimmed Values

As shipped the OTP memory contains the following information:

Item	**OTP Address**	**Factory Value**	**Description**
BOOT	0	0x7f50_106f	Code to jump to LAST FENCE
LIFECYCLE	2044	0x1	OTP Lifecycle Counter
HFROSC TRIM	2043	Varies	HFROSC trim value
STAMP	2041	Varies	Device ID Stamp, not guaranteed unique.
LAST FENCE	2045	0x0000_000F 0x2000_02b7 0x0002_8067	Code to jump to SPI-FLASH.

Table 5.1: FE310-G000 OTP Contents as Shipped

5.3 Errata

[AON-1] Core Power Shutdown

Issue: The core power supply cannot be shut down without resetting the device.

Symptoms: Device resets when core power is shut down.

Workaround: Do not shut down core power.

[SPI-1] SPI-Flash Interface DQ[3]

Issue: The output enable signal for DQ[3] is not driven properly.

Symptoms: Address and write data using DQ[3] for transmission will not function properly. Reads using DQ[3] are unaffected.

Workaround: Do not use opcode 0xEB in the Extended SPI protocol. In some devices, this command is also referred to as QUAD INPUT/OUTPUT FAST READ. Do not use the Native Quad SPI Protocol. In some devices, this command is also referred to as FAST READ.

[SPI-2] SPI-Flash Interface Frame Lengths

Issue: Certain frame lengths do not work properly.

Symptoms: Certain frame lengths do not work, and will result in the master sending one extra clock pulse. The slave device may then become out of sync.

Workaround: The following frame lengths are supported and can be used. Do not use other frame lengths.
Serial: 0, 2, 4, 6, 8
Dual: 0, 1, 3, 5, 7, 8
Quad: 0, 1, 2, 3, 5, 6, 7, 8

[TRAP-1] Compressed ebreak Instruction

Issue: Calling compressed `ebreak` can cause illegal instruction exception instead of breakpoint exception.

Symptoms: Calling `c.ebreak` causes illegal instruction exception instead of breakpoint exception.

Workaround: Do not use compressed `c.ebreak` instruction. Use `ebreak`.

Chapter 6

FE310-G000 OTP Application Notes

6.1 OTP Programming Warnings

Warning: Improper use of the One Time Programmable (OTP) memory may result in a nonfunctional device and/or unreliable operation.

- OTP Memory must be programmed following the procedure outlined below *exactly*.
- OTP Memory is designed to be programmed or accessed only while the system clock is running between 1MHz and 37MHz.
- OTP Memory must be programmed **only** while the power supply voltages remain within specification.

6.2 OTP Programming Procedure

1. LOCK the otp:
   (a) Writing 0x1 to `otp_lock`
   (b) **Check that 0x1 is read back from** `otp_lock`.
   (c) Repeat this step until 0x1 is read successfully.
2. SET the programming voltages by writing the following values:

   ```
   otp_mrr=0x4
   otp_mpp=0x0
   otp_vppen=0x0
   ```

3. WAIT 20us for the programming voltages to stabilize
4. ADDRESS the memory by setting `otp_a`
5. WRITE **one bit at a time**:
   (a) set **only** the bit you want to write high in `otp_d`
   (b) Bring `otp_ck` HIGH for 50us

   (c) Bring `otp_ck` LOW.

   Note that this means **only** one bit of `otp_d` should be high at any time.

6. VERIFY the written bits setting `otp_mrr=0x9` for read margin.
7. SOAK any verification failures by repeating steps 2-5 using 400us pulses.
8. REVERIFY the rewritten bits setting `otp_mrr=0xF`. Steps `7,8` may be repeated up to 10 times before failing the part.
9. UNLOCK the otp by writing `0x0` to `otp_lock`.

Chapter 7

FE310-G000 Package Information

7.1 Package Outline Drawing - 48QFN

The FE310-G000 is offered in a convenient 48-lead 6x6 QFN package (0.4mm lead pitch). The exposed paddle (Pin 49) should be connected directly to the ground plane.

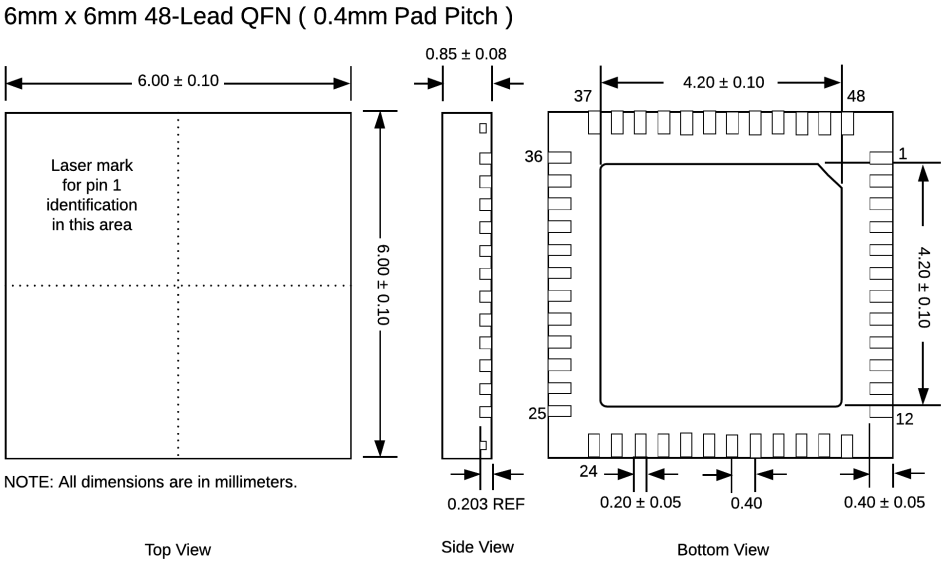

Figure 7.1: 48QFN Package Outline Drawing (0.4mm pitch)

7.2 Recommended PCB Footprint - 48QFN

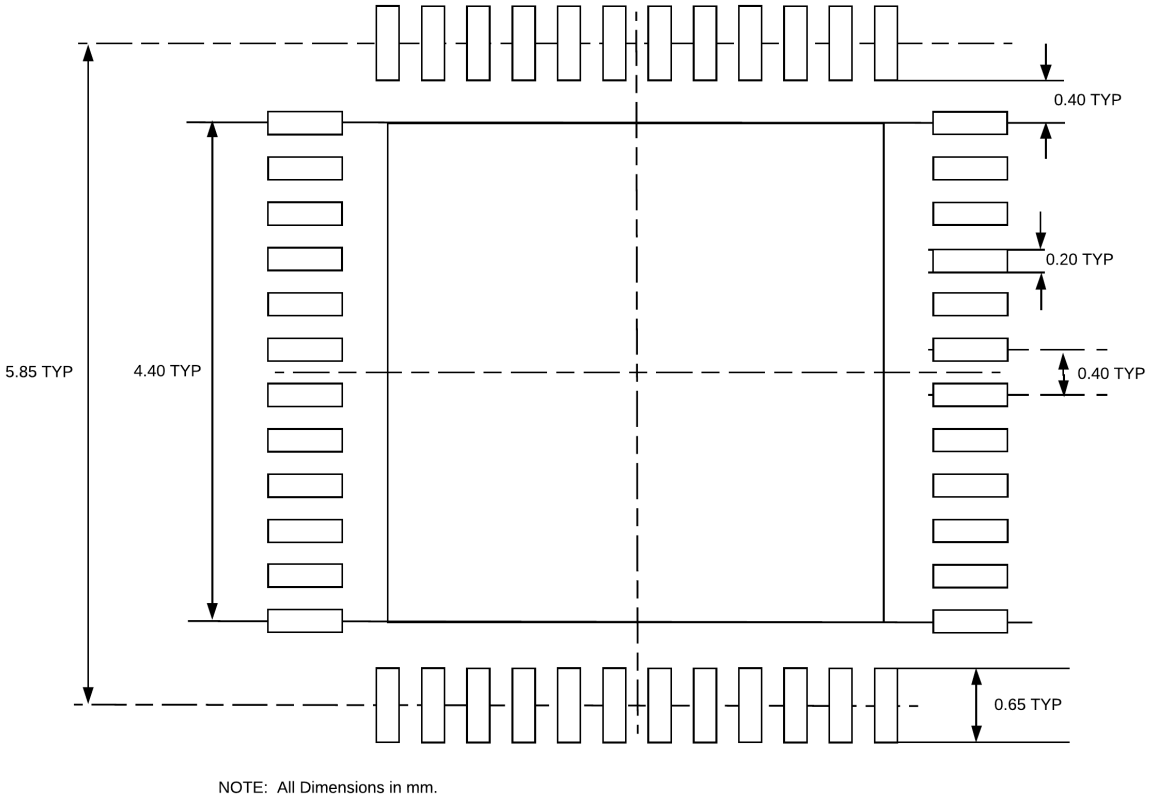

Figure 7.2: 48QFN PCB Footprint Drawing (0.4mm pitch)