
STM32
CubeMX

1. Description

1.1. Project

Project Name	Point
Board Name	custom
Generated with:	STM32CubeMX 6.1.0
Date	12/30/2020

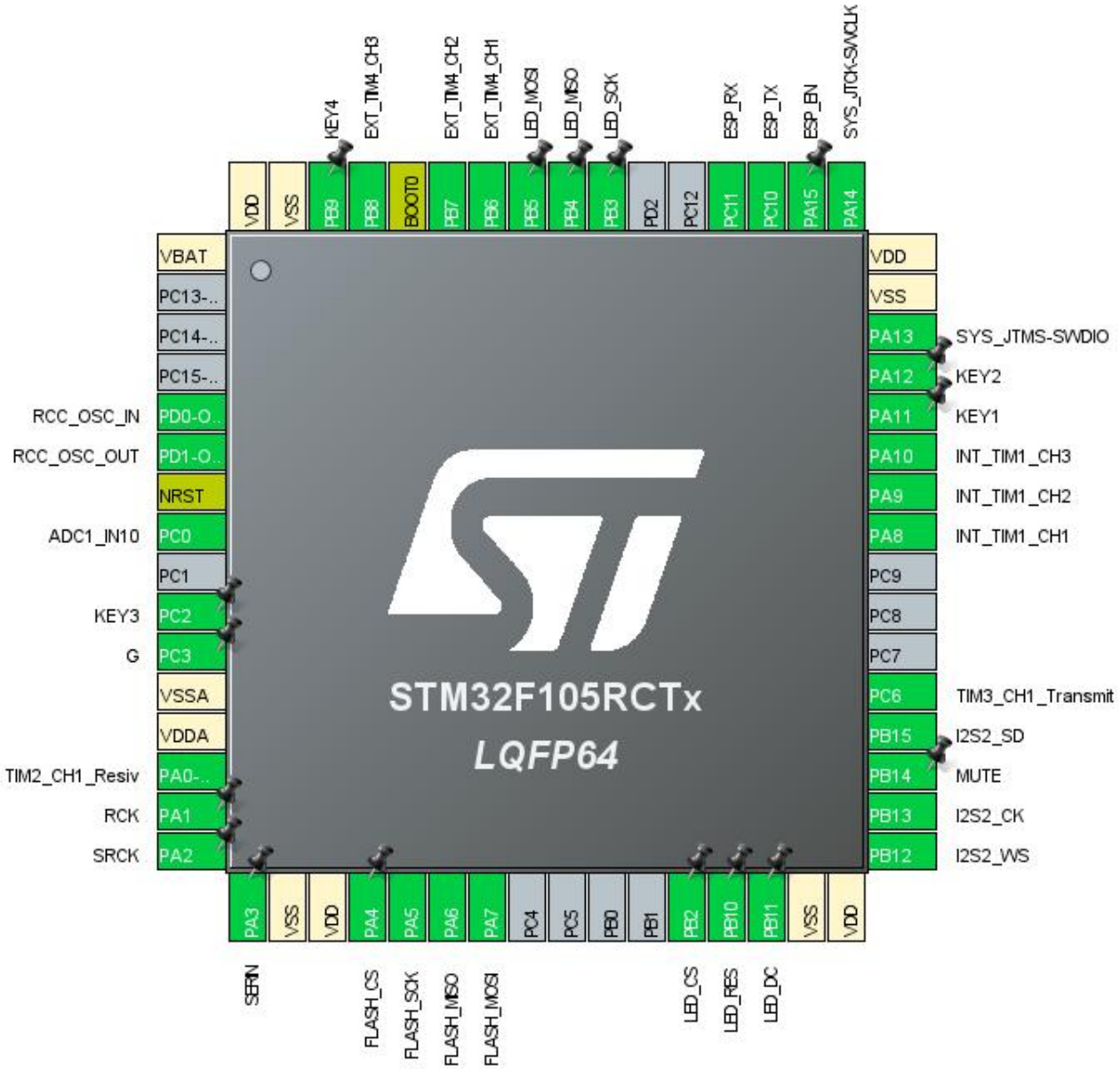
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F105/107
MCU name	STM32F105RCTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration



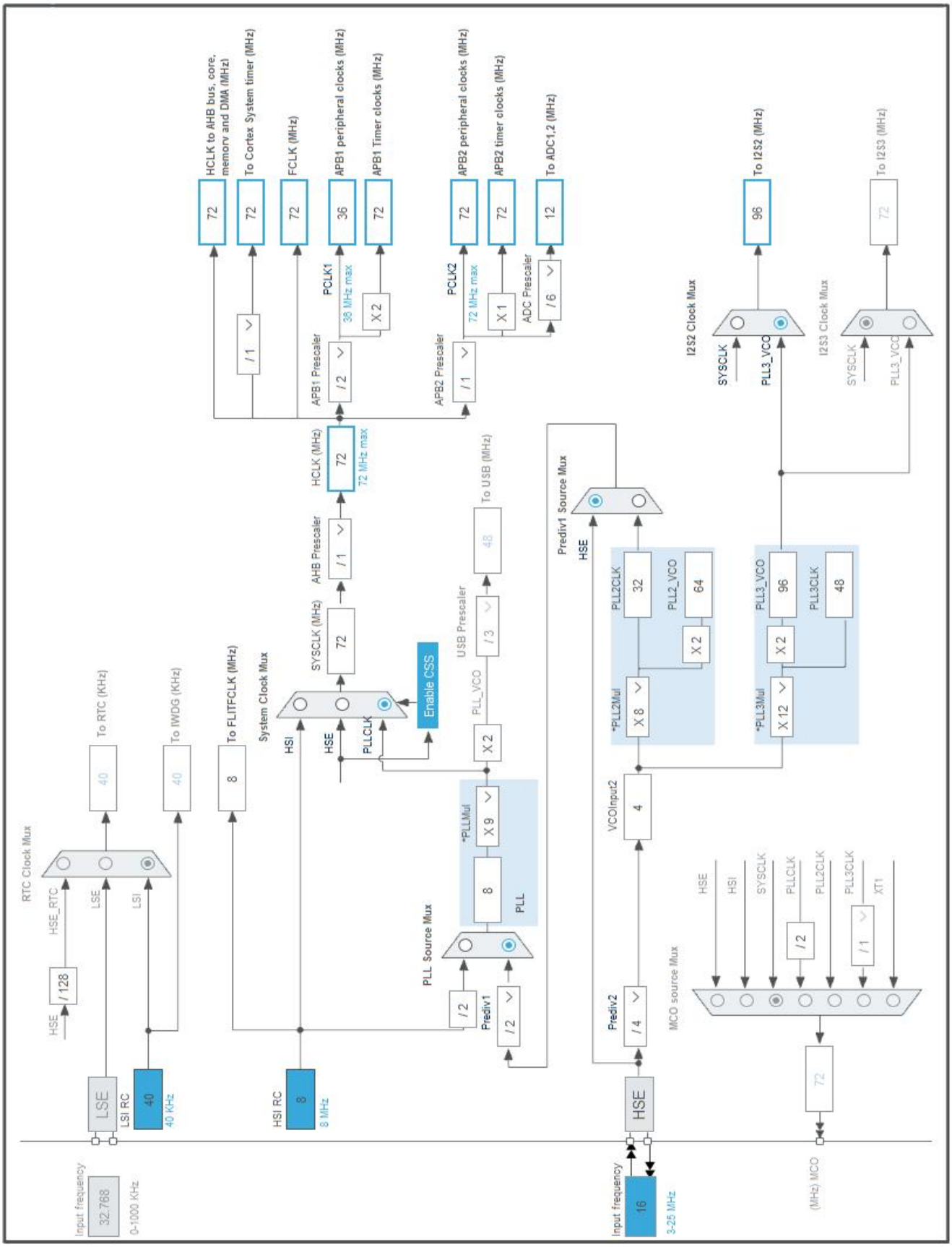
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	
10	PC2 *	I/O	GPIO_Input	KEY3
11	PC3 *	I/O	GPIO_Output	G
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM2_CH1	TIM2_CH1_Resiv
15	PA1 *	I/O	GPIO_Output	RCK
16	PA2 *	I/O	GPIO_Output	SRCK
17	PA3 *	I/O	GPIO_Output	SERIN
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	FLASH_CS
21	PA5	I/O	SPI1_SCK	FLASH_SCK
22	PA6	I/O	SPI1_MISO	FLASH_MISO
23	PA7	I/O	SPI1_MOSI	FLASH_MOSI
28	PB2 *	I/O	GPIO_Output	LED_CS
29	PB10 *	I/O	GPIO_Output	LED_RES
30	PB11 *	I/O	GPIO_Output	LED_DC
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	I2S2_WS	
34	PB13	I/O	I2S2_CK	
35	PB14 *	I/O	GPIO_Output	MUTE
36	PB15	I/O	I2S2_SD	
37	PC6	I/O	TIM3_CH1	TIM3_CH1_Transmit
41	PA8	I/O	TIM1_CH1	INT_TIM1_CH1
42	PA9	I/O	TIM1_CH2	INT_TIM1_CH2
43	PA10	I/O	TIM1_CH3	INT_TIM1_CH3
44	PA11 *	I/O	GPIO_Input	KEY1
45	PA12 *	I/O	GPIO_Input	KEY2
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	ESP_EN
51	PC10	I/O	UART4_TX	ESP_TX
52	PC11	I/O	UART4_RX	ESP_RX
55	PB3	I/O	SPI3_SCK	LED_SCK
56	PB4	I/O	SPI3_MISO	LED_MISO
57	PB5	I/O	SPI3_MOSI	LED_MOSI
58	PB6	I/O	TIM4_CH1	EXT_TIM4_CH1
59	PB7	I/O	TIM4_CH2	EXT_TIM4_CH2
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	EXT_TIM4_CH3
62	PB9 *	I/O	GPIO_Input	KEY4
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Point
Project Folder	C:\LW\Point\Firmware\FW\Point
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x0
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_I2S2_Init	I2S2
5	MX_SPI1_Init	SPI1
6	MX_SPI3_Init	SPI3
7	MX_TIM2_Init	TIM2
8	MX_ADC1_Init	ADC1
9	MX_TIM3_Init	TIM3
10	MX_TIM5_Init	TIM5
11	MX_TIM1_Init	TIM1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM4_Init	TIM4
13	MX_UART4_Init	UART4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F105/107
MCU	STM32F105RCTx
Datasheet	DS6014_Rev10

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

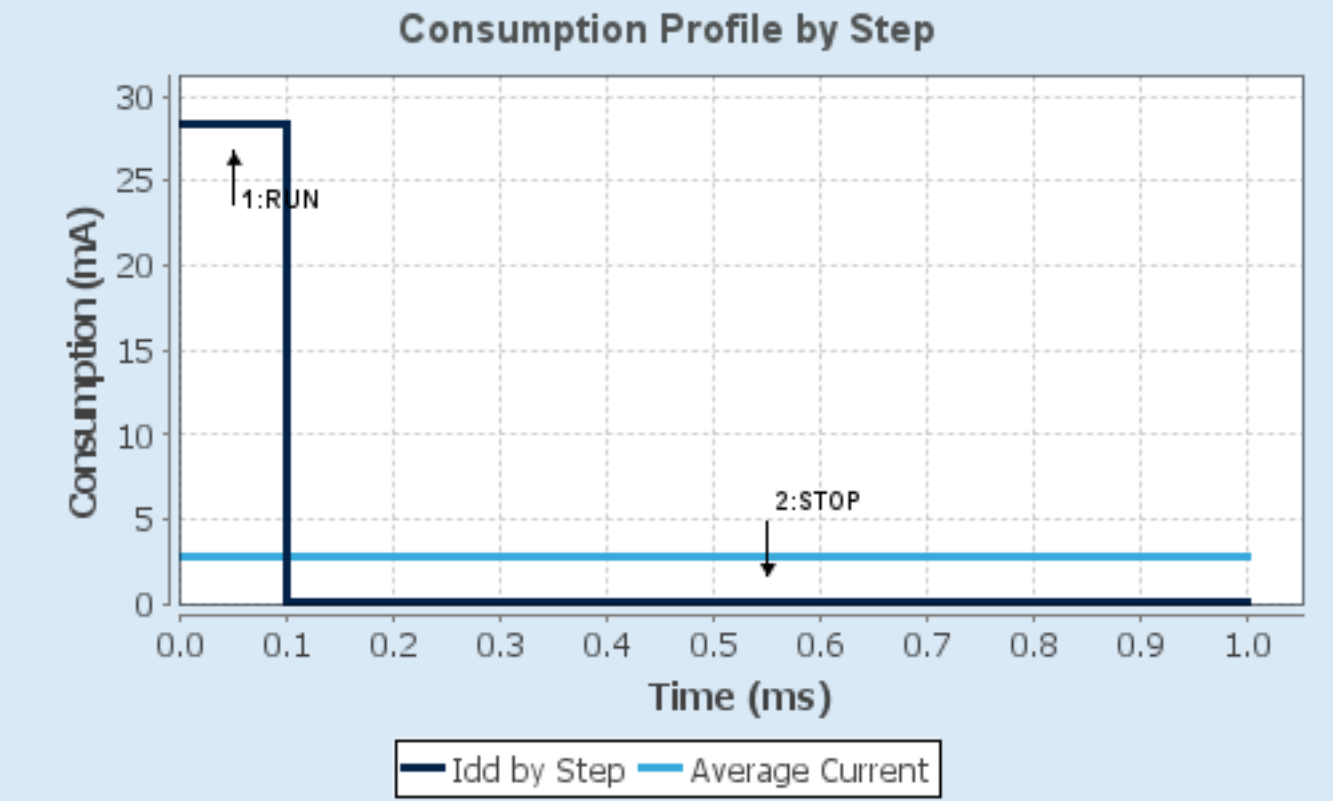
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	28.3 mA	26 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.8	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.85 mA
Battery Life	1 month, 19 days, 4 hours	Average DMIPS	61.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN10

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	**Disable ***

ADC_Injected_ConversionMode:

Enable Injected Conversions	**Enable ***
Number Of Conversions	**1 ***
External Trigger Source	External Trigger on injected channels are disabled (Auto-injection mode selected)
Injected Conversion Mode	**Auto Injected Mode ***
Rank	1
Channel	Channel 10
Sampling Time	**239.5 Cycles ***
Injected Offset	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. I2S2

Mode: Half-Duplex Transmit Only Master

7.2.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	16 Bits Data on 16 Bits Frame
Selected Audio Frequency	**44 KHz ***
Real Audio Frequency	**44.117 KHz ***

Error between Selected and Real	**0.26 % ***

Clock Parameters:

Clock Polarity	Low

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SPI3

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.7. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.8. TIM2

Channel1: Input Capture direct mode

Channel2: Input Capture indirect mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Indirect
Prescaler Division Ratio	No division

7.9. TIM3

Slave Mode: Gated Mode

Trigger Source: ITR2

Channel1: PWM Generation CH1

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Gated Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM4

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. TIM5

Channel2: Output Compare No Output

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Output Compare (OC1REF) ***

Output Compare No Output Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High

7.12. UART4

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	**1000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. FREERTOS

Interface: CMSIS_V2

7.13.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	2.00

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	**64 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	**Disabled ***
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	**Enabled ***

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**32768 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	**Enabled ***
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	**Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	128

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.13.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	**Disabled ***
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	**Enabled ***
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.13.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	n/a	n/a	
I2S2	PB12	I2S2_WS	Alternate Function Push Pull	n/a	Low	
	PB13	I2S2_CK	Alternate Function Push Pull	n/a	Low	
	PB15	I2S2_SD	Alternate Function Push Pull	n/a	Low	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	**High ***	FLASH_SCK
	PA6	SPI1_MISO	Input mode	No pull-up and no pull-down	**n/a**	FLASH_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	**High ***	FLASH_MOSI
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	n/a	**High ***	LED_SCK
	PB4	SPI3_MISO	Input mode	No pull-up and no pull-down	**n/a**	LED_MISO
	PB5	SPI3_MOSI	Alternate Function Push Pull	n/a	**High ***	LED_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	INT_TIM1_CH1
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	INT_TIM1_CH2
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	INT_TIM1_CH3
TIM2	PA0-WKUP	TIM2_CH1	Input mode	No pull-up and no pull-down	n/a	TIM2_CH1_Resiv
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	n/a	Low	TIM3_CH1_Transmit
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	n/a	Low	EXT_TIM4_CH1
	PB7	TIM4_CH2	Alternate Function Push Pull	n/a	Low	EXT_TIM4_CH2
	PB8	TIM4_CH3	Alternate Function Push Pull	n/a	Low	EXT_TIM4_CH3
UART4	PC10	UART4_TX	Alternate Function Push Pull	n/a	**High ***	ESP_TX
	PC11	UART4_RX	Input mode	No pull-up and no pull-down	**n/a**	ESP_RX
GPIO	PC2	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY3
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	G
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	RCK
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SRCK
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SERIN
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	FLASH_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_CS
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RES
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_DC
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MUTE
	PA11	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY1
	PA12	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY2
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ESP_EN
	PB9	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA1_Channel3	Memory To Peripheral	Low
SPI2_TX	DMA1_Channel5	Memory To Peripheral	**Very High ***
SPI1_RX	DMA1_Channel2	Peripheral To Memory	Low
SPI3_TX	DMA2_Channel2	Memory To Peripheral	Low
UART4_RX	DMA2_Channel3	Peripheral To Memory	**Medium ***
UART4_TX	DMA2_Channel5	Memory To Peripheral	Low
TIM4_UP	DMA1_Channel7	Peripheral To Memory	Low
TIM5_CH2	DMA2_Channel4	Peripheral To Memory	**Very High ***
SPI3_RX	DMA2_Channel1	Peripheral To Memory	Low

SPI1_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_TX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***

SPI1_RX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI3_TX: DMA2_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_RX: DMA2_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA2_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

TIM4_UP: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM5_CH2: DMA2_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI3_RX: DMA2_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel2 global interrupt	true	5	0
DMA1 channel3 global interrupt	true	5	0
DMA1 channel5 global interrupt	true	5	0
DMA1 channel7 global interrupt	true	5	0
TIM7 global interrupt	true	0	0
DMA2 channel1 global interrupt	true	5	0
DMA2 channel2 global interrupt	true	5	0
DMA2 channel3 global interrupt	true	5	0
DMA2 channel4 global interrupt	true	5	0
DMA2 channel5 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
UART4 global interrupt	unused		

8.3.2. NVIC Code generation

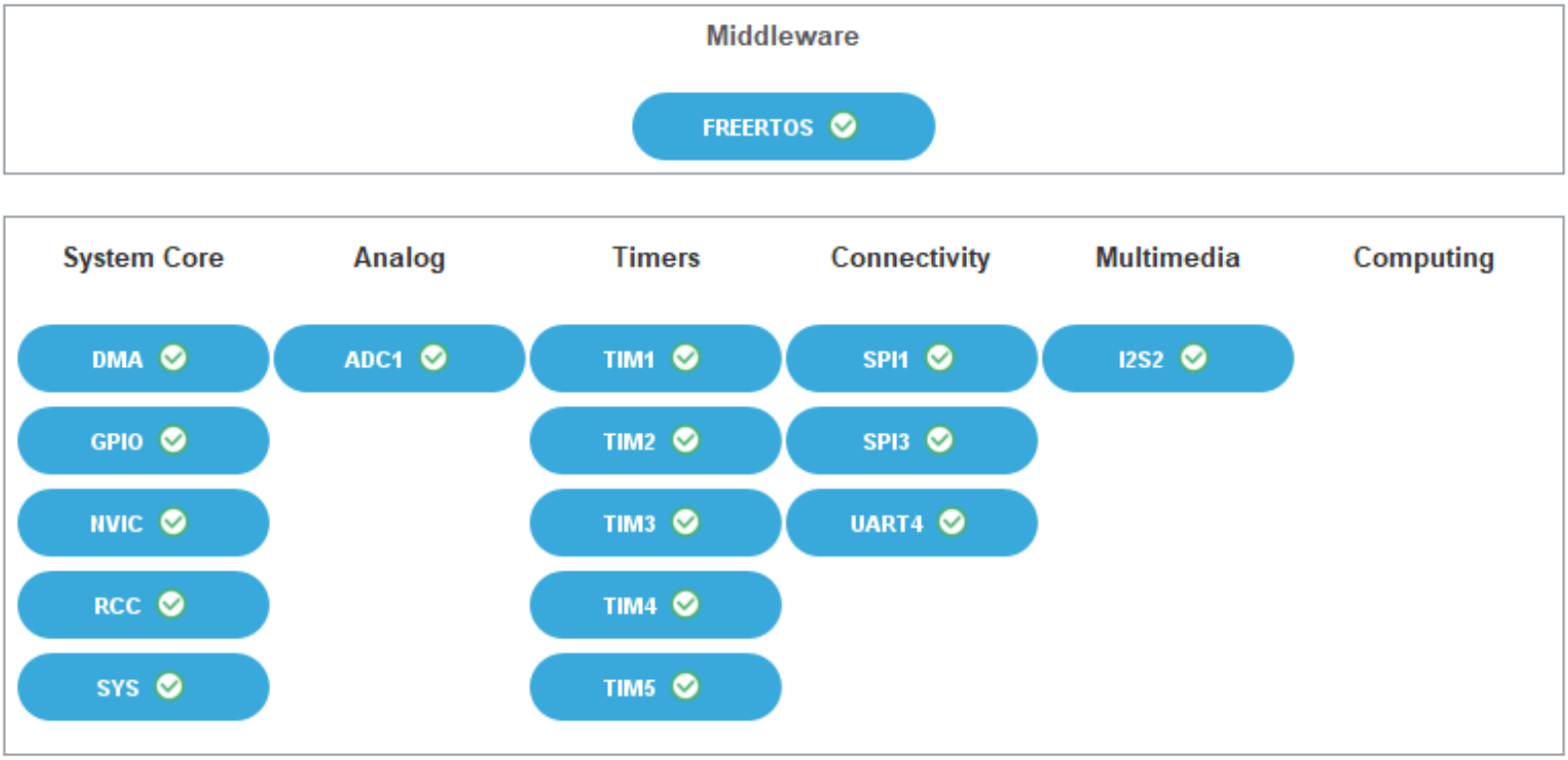
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
DMA1 channel7 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
DMA2 channel1 global interrupt	false	true	true
DMA2 channel2 global interrupt	false	true	true
DMA2 channel3 global interrupt	false	true	true
DMA2 channel4 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/CD00220364.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/CD00171190.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00228163.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00283419.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/CD00238166.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00164185.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00032987.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033267.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033344.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00052530.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
Application note	http://www.st.com/resource/en/application_note/DM00209695.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf