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Seat No.	
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**[5559]-193**

**S.E. (Computer) (Second Semester) EXAMINATION, 2019**

**MICROPROCESSOR**

**(2015 PATTERN)**

**Time : 2 Hours**

**Maximum Marks : 50**

*Instructions to the candidates:*

- Answer Question No. 1 OR 2, 3 OR 4, 5 OR 6 and 7 OR 8.
- Neat diagram must be drawn whenever necessary.
- Figures to the right indicate full marks.
- Assume suitable data, if necessary.

- List fundamental data types of 80386. [02]
  - Describe following different flags defined in 80386 Processor - [04]  
a) DF      b) VM      c) NT      d) RF
  - Explain shift and rotate instructions of 80386. [06]

OR
- Draw and explain the format of a selector. [02]
  - List and explain control registers of 80386. [04]
  - With help of diagram explain the 80386 mechanism to translate logical address to linear address. [06]
- List aspects of protection related to pages. [02]
  - With appropriate diagram explain the concept of privilege levels in 80386. [04]
  - How Call gate descriptor is used to locate the procedure in another code segment? How protection is provided? [06]

OR
- Define "Faults". [02]
  - Explain "How 80386 identifies interrupts?" [04]
  - By which two ways, 80386 allows input/output to be performed? Explain each in details. [06]

P.T.O.

- 5) a) Explain features of "Virtual 8086 mode". [03]  
b) Explain 80386 processor state after RESET. [04]  
c) What all initializations required to start processor in protected mode after reset? [06]

OR

- 6) a) Write a short note on "Switching to protected mode". [02]  
b) List the features of 80386 architecture that supports debugging. [05]  
c) With the necessary diagrams explain entering and leaving V86 mode? [06]
- 7) a) Draw and explain read cycle with non-pipelined address timing. [08]  
b) Which data types are supported by 80387? [05]

OR

- 8) a) Draw and explain write cycle with pipelined address timing. [08]  
b) The 80387 instructions are divided into which functional groups? Explain with one example of each. [05]