Sandisk Flash101 Management

Western Digital Confidential

2023.06.23

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Contents

1. NAND Flash Technology

1. NAND Flash Technology

- **Flash Memory**

  비휘발성 전자식 저장 장치

  [종류]

  -NAND flash

  -NOR flash

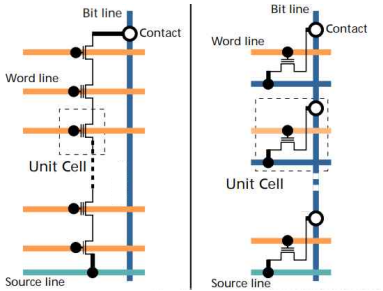
  [사용처]

  digital cameras, mobile phones, computers, digital audio players, USB drive, etc.

출처:https://www.usbmemorydirect.com/blog/what-is-flash-memory/, https://stylezineblog.com/4478

1. NAND Flash Technology

- **NAND Flash vs NOR Flash**



Characteristic	NAND Flash	NOR Flash
connection method	connect in series	connect in parallel
Cost per bit	Lower	Higher
Random read speed	Slower	Faster
Write speed	Faster	Slower
Erase speed	Faster	Slower

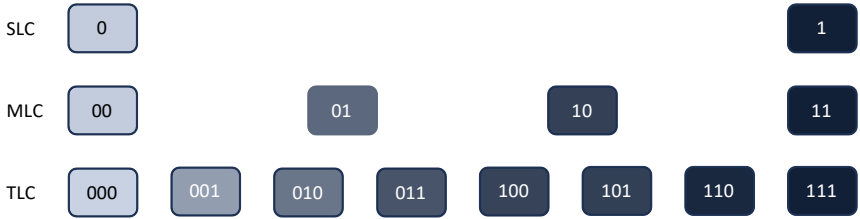
A comparison of the characteristics

출처:https://blog.csdn.net/LUOHUATINGYUSHENG/article/details/88953659

2. NAND Flash Cell

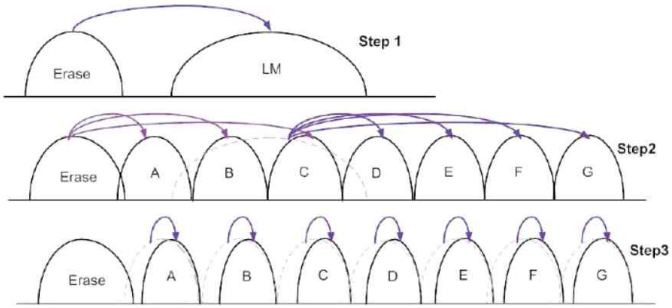
2. NAND Flash Cell

- **NAND flash types**
  - **Floating gate의 전자량으로 신호 구분**



2. NAND Flash Cell

- **MLC, TLC로 갈수록 쓰기 속도가 느린 이유**
  - 쓰기를 위한 컨트롤 게이트 전압이 한번에 구현되지 않는다

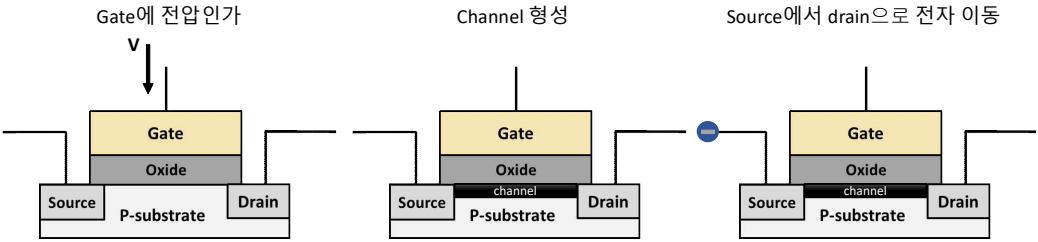


출처: https://gamma0burst.tistory.com/593

3. NAND Flash Architecture

3. NAND Flash Architecture

- **MOS structure**



3. NAND Flash Architecture

- **Flash Memory - write**

Word Line과 Bit Line에 전압 인가

↓

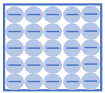
Channel 형성

↓

Channel 전자 tunneling

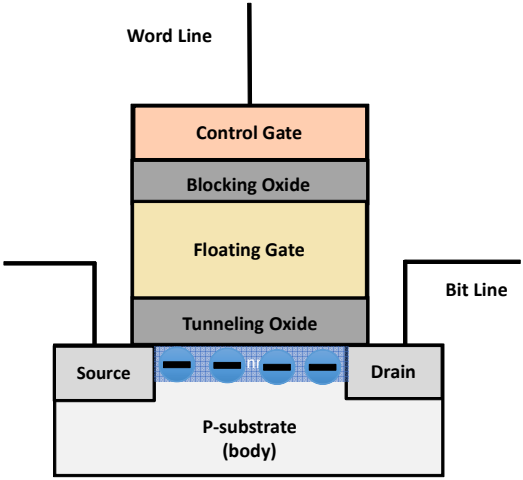
↓

Floating gate에 전자 trap



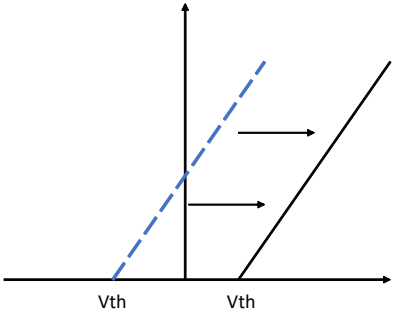
전자 있는 cell = 0
write

전자 없는 cell =1
reset

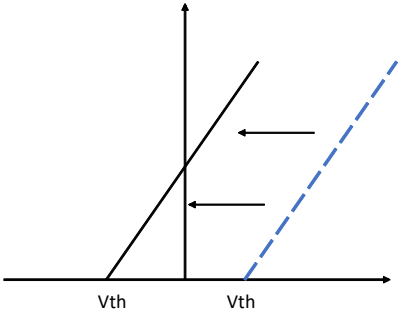


3. NAND Flash Architecture

- **Threshold voltage**



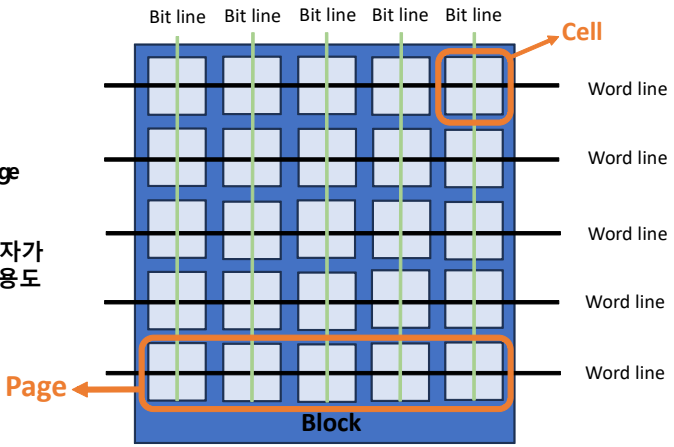
Floating Gate에 전자 들어왔을때
Vth 상승



Floating Gate에 전자 빠져나갈때
Vth 하강

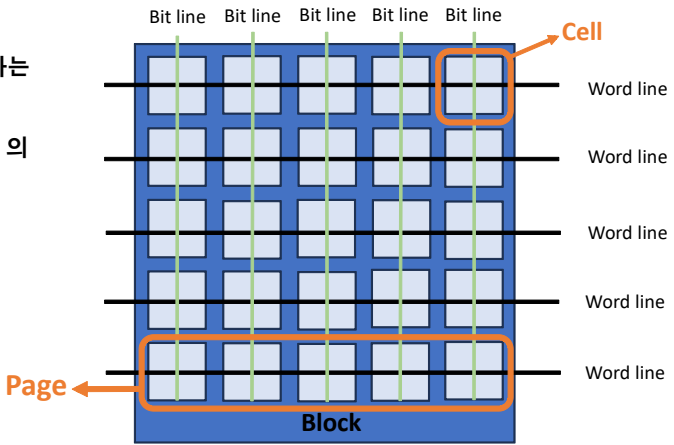
3. NAND Flash Architecture

- **Word Line & Bit Line**
  - X축으로 Word Line 공유
  - Y축으로 Bit Line 공유
  - Word Line은 읽으려는 page 선택하는 용도
  - Bit Line은 전류를 흘려 전자가 있는지 없는지 확인하는 용도



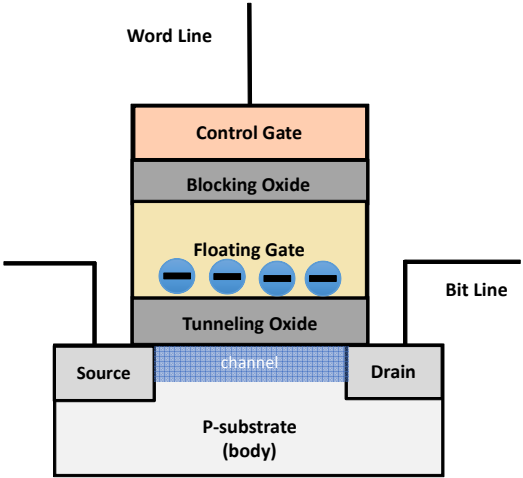
3. NAND Flash Architecture

- **Page & Block**
  - **Page: Word Line 을 공유하는 cell들의 집합**
  - **Block: page들의 집합, cell 의 body를 공유**



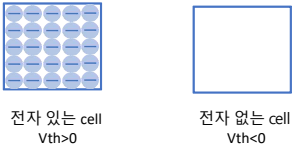
3. NAND Flash Architecture

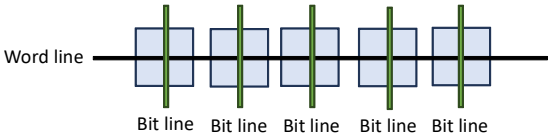
- **Flash Memory – erase**
  - Body와 Bit Line에 강한 전압 인가
  - Floating gate의 전자를 body쪽으로 끌어냄
  - 각각의 block은 동일한 body를 공유
    -> block 단위로 지워야함



3. NAND Flash Architecture

- **Read**
  - 모든 bit line과 word line에 전압인가
  - 읽으려는 page의 word line만 0V 인가
  - 선택된 page에서 write된 cell은 channel이 형성되지 않아 전류 흐르지 않음
    -> 0으로 인식
  - 아닌 cell은 1로 인식





3. NAND Flash Architecture

- **Life**
  - **Write/Erase과정에서 Tunneling oxide 손상 (hot carrier effect)**
  - **SLC > MLC > TLC로 갈수록 더 정밀하게 전자의 수 조절해야함**

    -> TLC 수명 매우 짧음
  - **공정 미세화로 channel 길이 짧아짐 -> 수명 줄어듬**

4. Inherent Challenges

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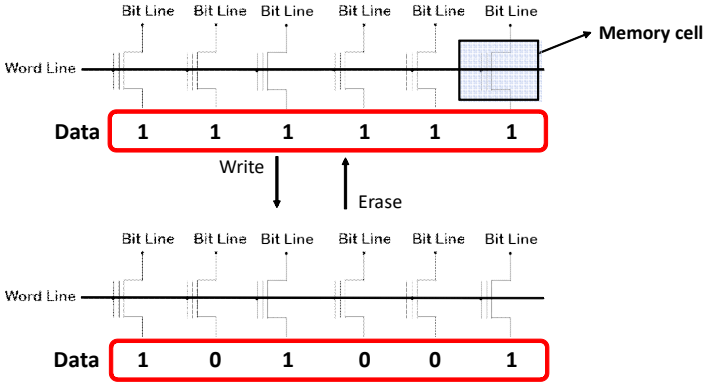
- **Inherent NAND Flash Challenge**

1. **Need to Erase before writing**
2. **Wear out mechanism that limits service life**
3. **Data errors caused by write and read disturb**
4. **Data retension errors**
5. **Initial and runtime bad blocks**

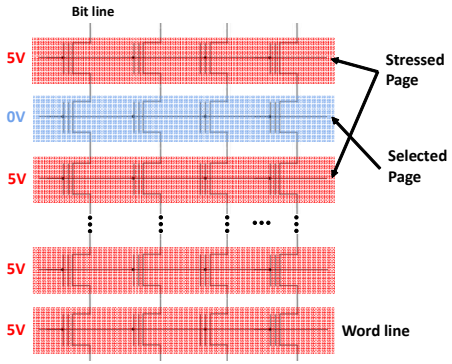
4. Inherent Challenges

- **Need to Erase before writing**

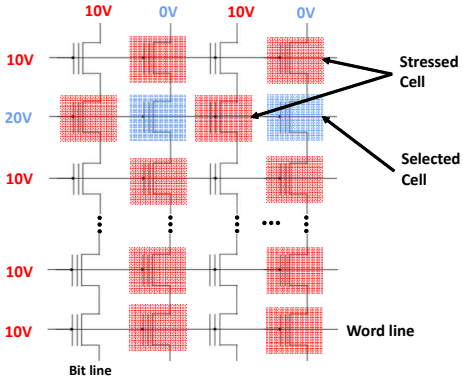


4. Inherent Challenges

- **Data errors caused by write and read disturb**



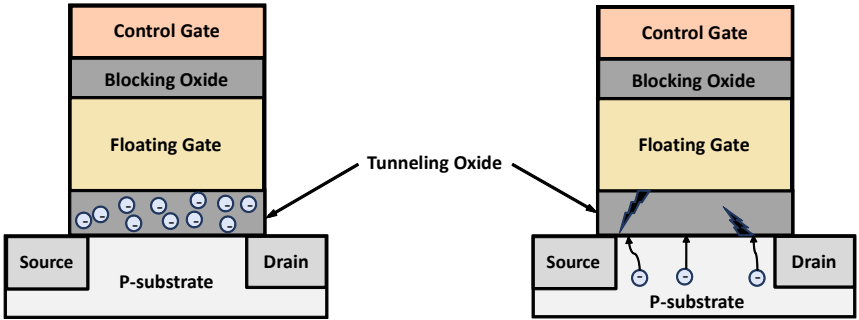
Read Disturb



Write Disturb

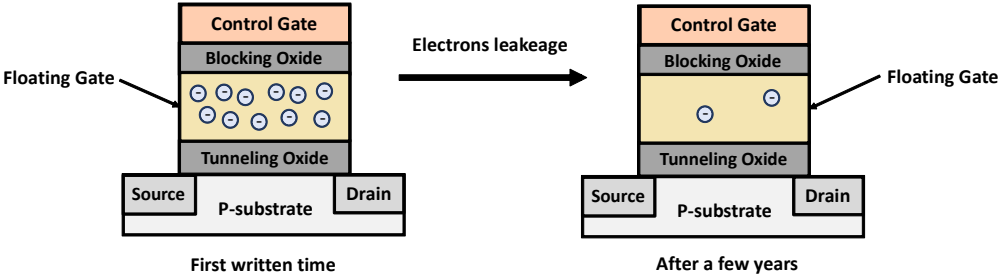
4. Inherent Challenges

- **Wear out mechanism that limits service life**



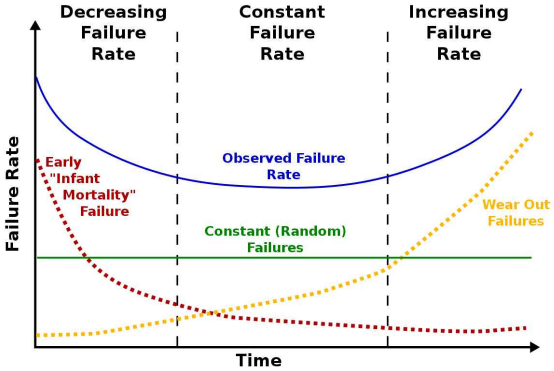
4. Inherent Challenges

- **Data retension errors**



4. Inherent Challenges

- **Initial and runtime bad blocks**



출처: https://www.architecting.it/blog/avoiding-the-storage-performance-bathtub-curve/

5. Flash Management System

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- **Flash Management System**

1. Wear Leveling

2. Exception Management

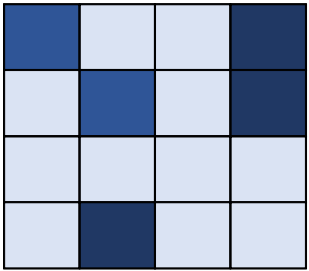
2.1. NAND Failure Management

2.2. Unstable Power Supply

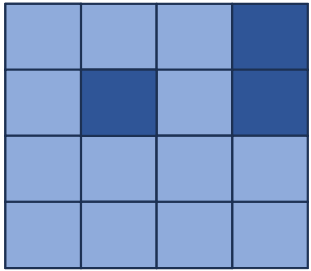
3. Error Detection and Correction

5. Flash Management System

- **Wear Leveling**



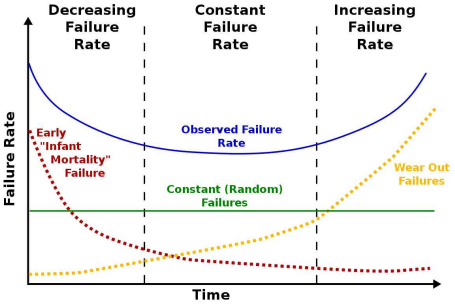
Without Wear Leveling



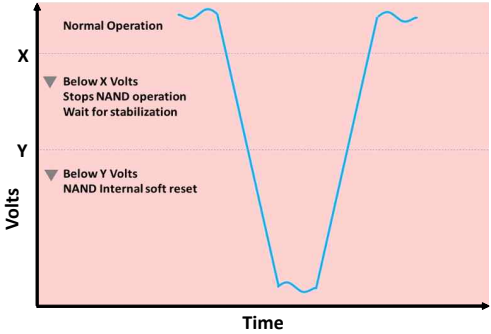
With Wear Leveling

5. Flash Management System

- **Exception Management**



NAND Failure Management



Unstable Power Supply Management

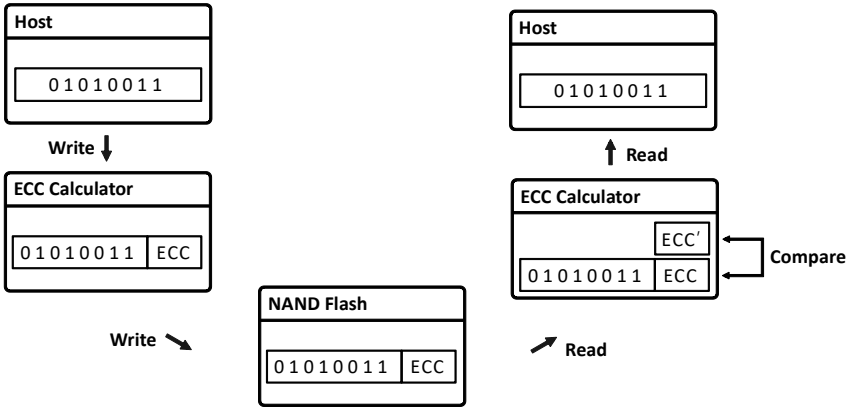
5. Flash Management System

▪ Error Detection and Correction

- 플래시 메모리의 사용 시간이 늘어감에 따라 셀들이 마모된다.
- 마모된 셀들에 데이터를 쓰거나 읽는 상황이 발생한다.
- 올바른 데이터를 쓰거나 읽지 못하는 오류가 생긴다.
- 이러한 오류를 파악하고 수정하기위해 ECC(Error Correction Code) 메커니즘을 사용한다.
- ECC를 사용함으로서 플래시 메모리의 전반적인 안정성이 향상된다.
- 대표적 예시: BCH(Bose, Ray-Chauduri, Hocquenghem), LDPC(Low Density Parity Code)

5. Flash Management System

- **Error Detection and Correction**



6. System Optimization Techniques

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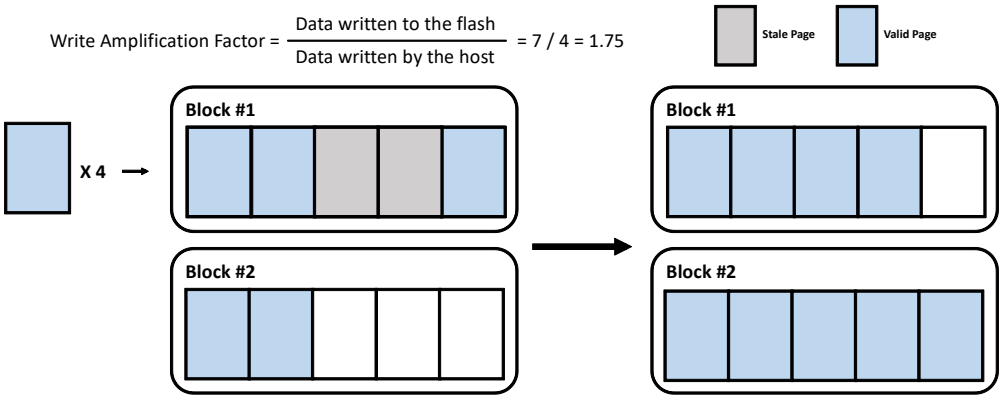
- **Write Amplification**

$$\text{Write Amplification Factor} = \frac{\text{Data written to the flash}}{\text{Data written by the host}} = 7 / 4 = 1.75$$



6. System Optimization Techniques

- **Understand and Optimize System**

  1. Understand the workload requirements

  2. Understand system's WA factor

  3. Optimize system's write pattern

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Thank you!
Q & A ?

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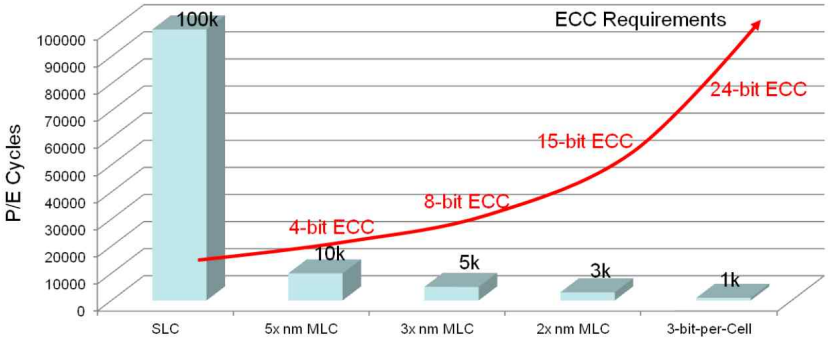
5. Flash Management System

- **Error Detection and Correction**



출처: Y. Cai et al., Error Patterns in MLC NAND Flash Memory: Measurement, Characterization, and Analysis, DATE, 2012