Design Tradeoffs for SSD Reliability

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FAST' 19

2024. 07. 24

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Contents

Introduction

- The reliability of flash memory, the basic storage medium for SSDs, is gradually decreasing
  - Flash memories for high storage densities suffer from high error rates for a variety of reasons
    - Wear-and-tear
    - Gradual charge leakage
    - Data disturbance ..
- Several reliability improvement technologies have caused performance degradation in SSDs
  - Data re-read, Data scrubbing, Error correction code, Redundancy scheme, Threshold voltage tuning ..
- Proposal of an holistic reliability management that selectively applies appropriate technologies

Background

- Reliability Enhancement Techniques

Table 1: Comparison of SSD reliability enhancement techniques.

Techniques	Impact on average performance	Impact on tail performance	Write amplification	Management overhead	Related work
ECC (hard-decision)	Negligible	None	Negligible	None	BCH, LDPC [35]
ECC (soft-decision)	None	High	Negligible	Negligible	LDPC [18, 35]
Threshold voltage tuning	None	High	None	Voltage levels	Read retry [12] Voltage prediction [14, 38]
Intra-SSD redundancy	High for small stripes; low for large stripes	Low for small stripes; high for large stripes	High	Stripe group information	Dynamic striping [31, 33] Intra-block striping [46] Parity reduction [25, 34]
Background data scrubbing	Depends	Depends	Depends	Block metadata such as erase count or read count	Read reclaim [22] Read refresh [37]

Background

$$
\begin{aligned}
&RBER(cycles, time, reads) \\
&= \varepsilon + \alpha \cdot cycles^{k} && \text{(wear)} \\
&\quad + \beta \cdot cycles^{m} \cdot time^{n} && \text{(retention)} \\
&\quad + \gamma \cdot cycles^{p} \cdot reads^{q} && \text{(disturbance)}
\end{aligned}
$$

- Errors in Flash Memory
  - Wear
    - Repeated programs and erases (P/E cycling) wear out the flash memory cells that store electrons (data)
  - Retention loss
    - Electrons stored in flash memory cells gradually leak over time, making it difficult to correctly read the data
    - Errors caused by retention loss increase as cells wear
  - Disturbance
    - Reading a wordline in a block weakly programs other wordlines in the block, unintentionally inserting more electrons into their memory cells

Background

- Raw Bit Error Rate (RBER)

$$
\begin{aligned}
&RBER(cycles, time, reads) \\
&= \varepsilon + \alpha \cdot cycles^{k} && \text{(wear)} \\
&\quad + \beta \cdot cycles^{m} \cdot time^{n} && \text{(retention)} \\
&\quad + \gamma \cdot cycles^{p} \cdot reads^{q} && \text{(disturbance)}
\end{aligned}
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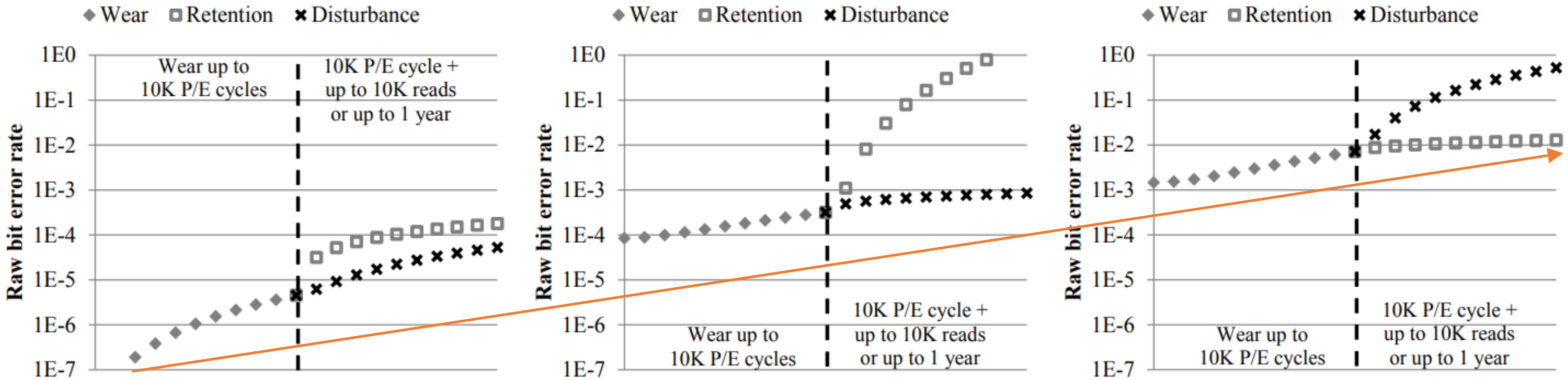
Table 2: RBER model parameters. Parameters ε, α, β, γ, k, m, n, p, and q describe the RBER model in Equation 1. R^2 represents the goodness of fit and is computed using the log values of the data and model, and N is the sample size.

Flash memory	Year	ε	α	β	γ	k	m	n	p	q	R^2	N
3x-nm MLC [52]	2011	5.06E-08	1.05E-14	9.31E-14	4.17E-15	2.16	1.80	0.80	1.07	1.45	0.984	98
2y-nm MLC [13, 14]	2015	8.34E-05	3.30E-11	5.56E-19	6.26E-13	1.71	2.49	3.33	1.76	0.47	0.988	173
72-layer TLC	2018	1.48E-03	3.90E-10	6.28E-05	3.73E-09	2.05	0.14	0.54	0.33	1.71	0.969	54



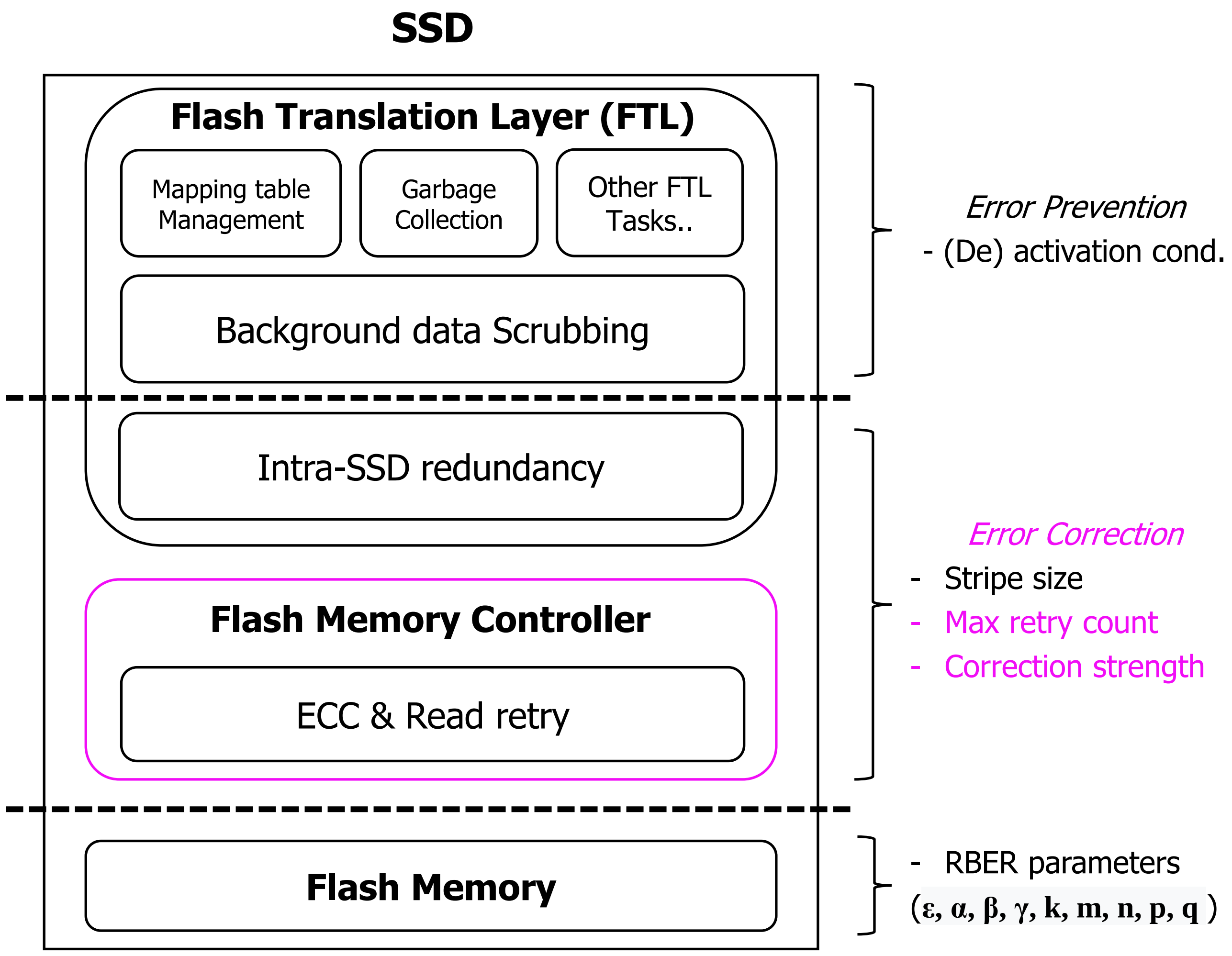
(a) 3x-nm MLC. (b) 2y-nm MLC. (c) 72-layer TLC.

Figure 3: Projected RBER graphs based on model parameters in Table 2. Each graph shows the error rate caused by the three mechanisms: wear, retention loss, and disturbance. In the first half of the x-axis, RBER increases due to repeated programs and erases (up to 10K cycles). In the second half, the cells are kept at 10K P/E cycle, but the data are repeatedly read (up to 10K reads) to induce disturbance errors or are left unaccessed (up to 1 year) for retention errors.

Design Tradeoffs for SSD Reliability

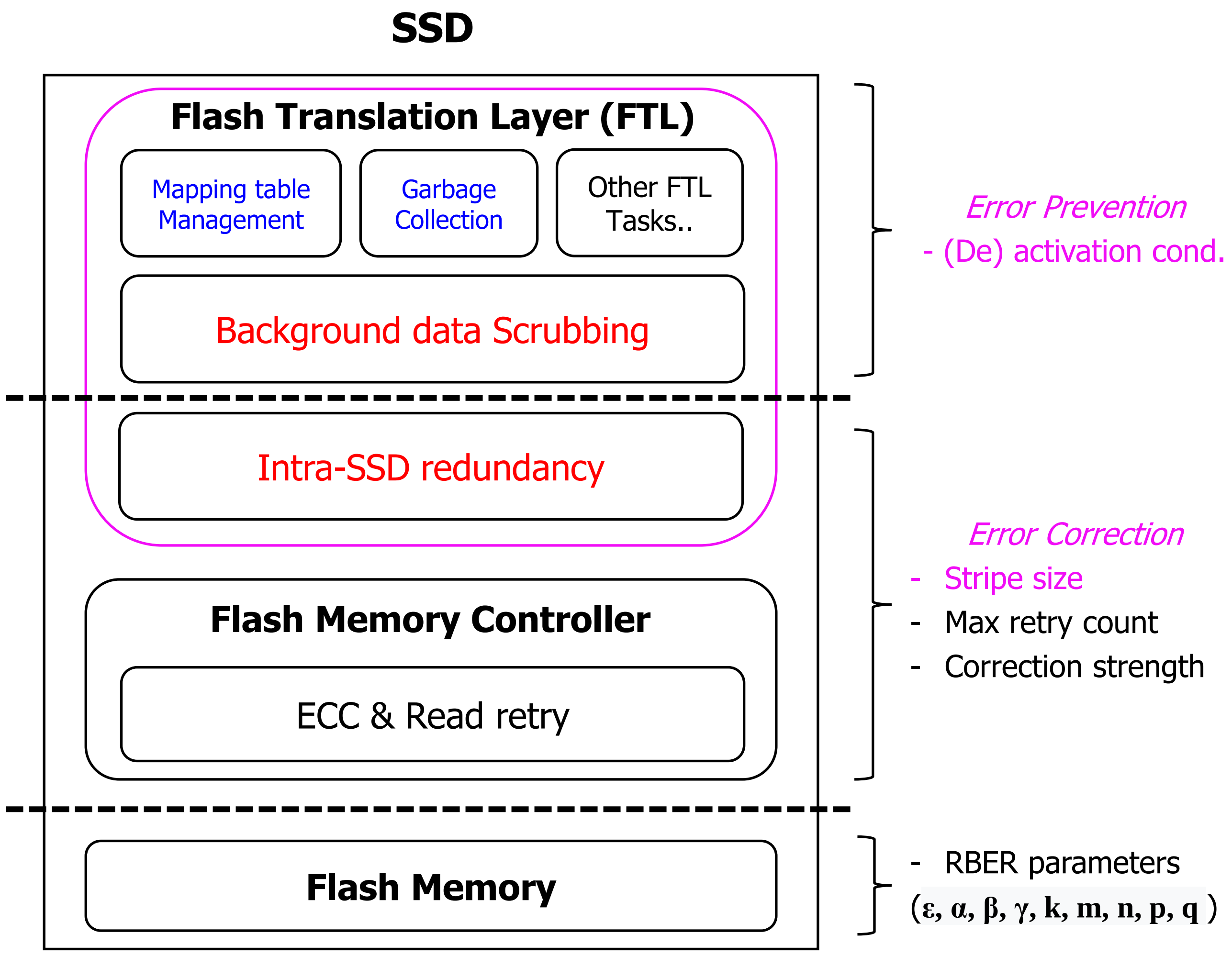
- Flash Memory Controller
  - Hard-decision ECC
  - Soft-decision ECC
  - Threshold voltage tuning (Read retry)

Soft-decision ECC and Threshold voltage tuning: Data re-read



Design Tradeoffs for SSD Reliability

- Flash Translation Layer (FTL)
  - Mapping Table Management
  - Garbage Collection
  - Intra-SSD redundancy
  - Data Scrubbing



Design Tradeoffs for SSD Reliability

- Flash Translation Layer (FTL)
  - Intra-SSD redundancy
    - Reconstruct data when ECC (both hard-decision and data re-read) fails
    - Increased frequency of writing parity data reduces the number of reads to reconstruct the data
  - Data Scrubbing
    - Prevent errors from accumulating by relocating them in the background
    - Proactive relocation of data prevents the ECC in the controller from failing

→ These firmware-oriented reliability pay a cost in the <u>present</u> to reduce the penalty in the <u>future</u>

→ Increase the write amplification and accelerate wear, not only reducing the lifetime of the SSD

Evaluation of SSD Reliability

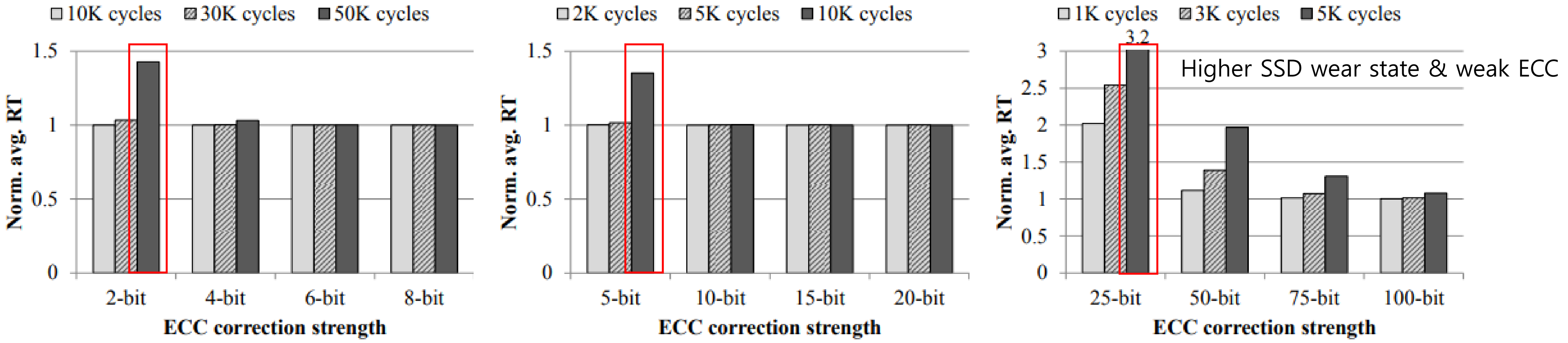
- Evaluation of SSD Reliability
  - Error Correction Code
  - Intra-SSD Redundancy
  - Background Scrubbing
  - Retention Test

Table 3: System configuration.

Parameter	Value	Parameter	Value
# of channels	8	Read latency	50μs
# of chips/channel	4	Program latency	500μs
# of planes/chip	2	Erase latency	5ms
# of blocks/plane	1024	Data transfer rate	667MB/s
# of pages/block	256	Physical capacity	256GiB
Page size	16KiB	Logical capacity	200GiB

Evaluation of SSD Reliability

- Error Correction Code
  - Performance degrades not only when the SSD is more worn out but also with weaker ECC correction strength
  - In the higher SSD wear states, errors are more frequent, and weaker ECC induces more data re-reads



(a) 3x-nm MLC. (b) 2y-nm MLC. (c) 72-layer TLC.

Figure 4: Average read response time for the three SSDs at various wear states. For each graph, the x-axis shows the correction strength for the ECC, and the performance is normalized to that with ∞ error correction strength. The response time increases not only when the SSD is more worn out, but also when weaker ECC is used.

Evaluation of SSD Reliability

- Error Correction Code
  - ∞-bit ECC: No data re-reads
  - n-bit ECC: n↓ → ECC becomes weaker, the error increases and more re-reads
  - Increasing the ECC strength has diminishing returns

    → This necessitates SSD internal redundancy and data scrubbing for data reconstruction

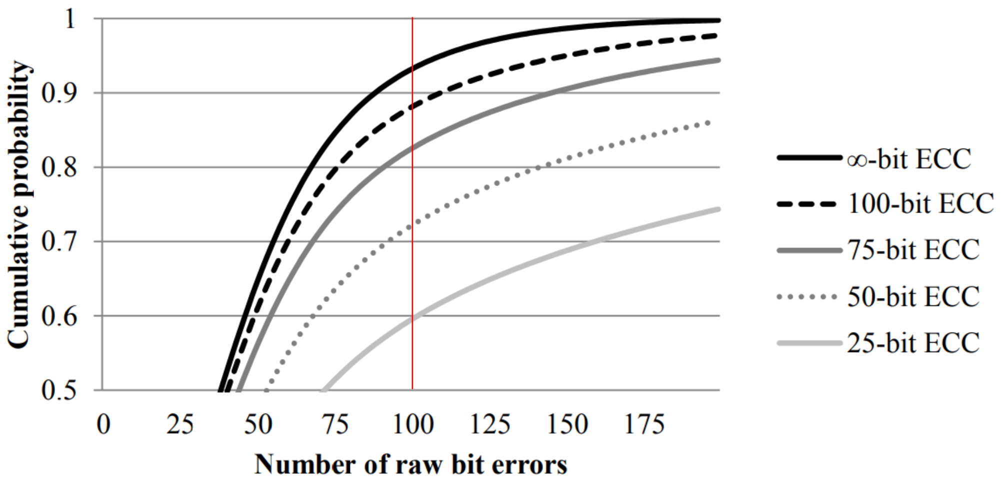
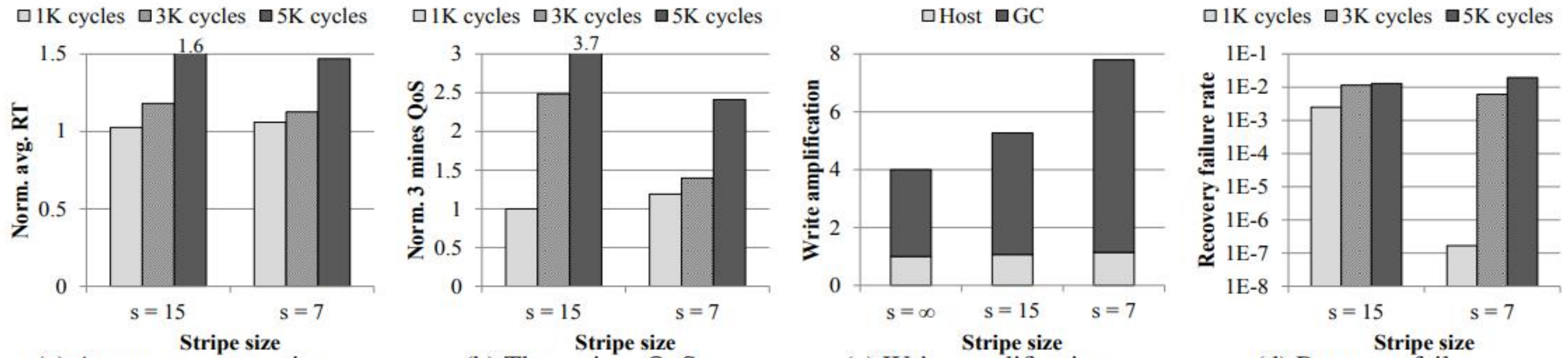


Figure 5: CDF of raw bit errors with varying ECC correction strength for the 72-layer TLC SSD of 5K initial wear state.

Evaluation of SSD Reliability

- Intra-SSD Redundancy
  - **max retry count = 1**
  - Frequent data reconstruction degrades perf. especially in terms of long-tail latency because of increased internal traffic
  - Accessing other pages in the stripe group can be uncorrectable through ECC, causing data recovery to fail
  - Setting the max retry count to one reveals more weakness of intra-SSD redundancy than its strength



(a) Average response time. (b) Three nines QoS. (c) Write amplification. (d) Recovery failure.

Figure 6: Performance, write amplification, and reliability for the 72-layer TLC SSD when `max retry count` is *one*. The performances in Figure 6a and Figure 6b are normalized to a system with ∞ correction strength. Using intra-SSD redundancy increases write amplification (Figure 6c), but moreover does not warrant full data recovery (Figure 6d).

Evaluation of SSD Reliability

- Intra-SSD Redundancy
  - **max retry count = 3**
  - In this scenario, the performance changes are due to the increase in traffic for writing parity data
  - Most data recovery attempts succeed, but still does not warrant full data reconstruction (Except in high wear state)
  - Further increasing the max retry count suppresses the use of data reconstruction through redundancy
    - Benefits of using redundancy scheme are eliminated while the penalty of accelerated wear and increased WAF remain

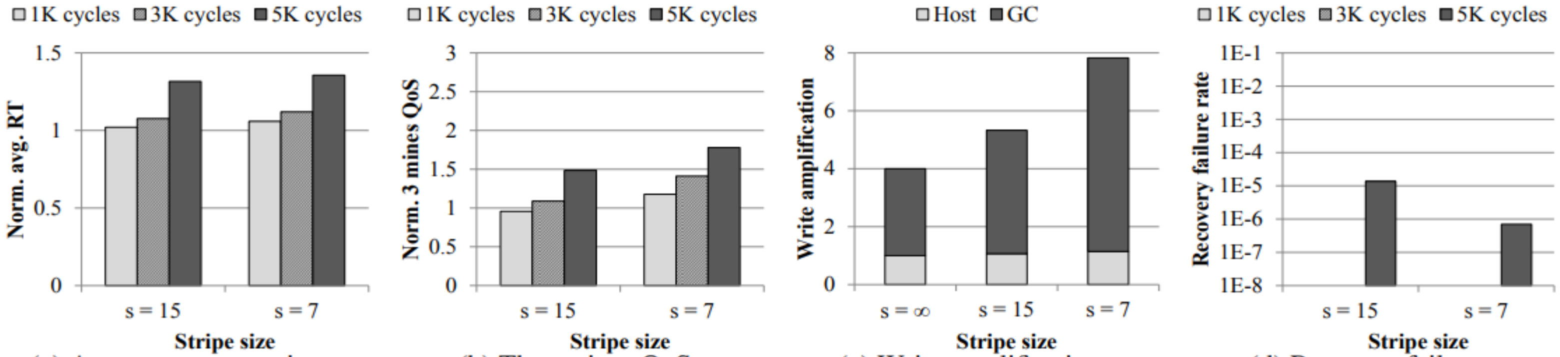
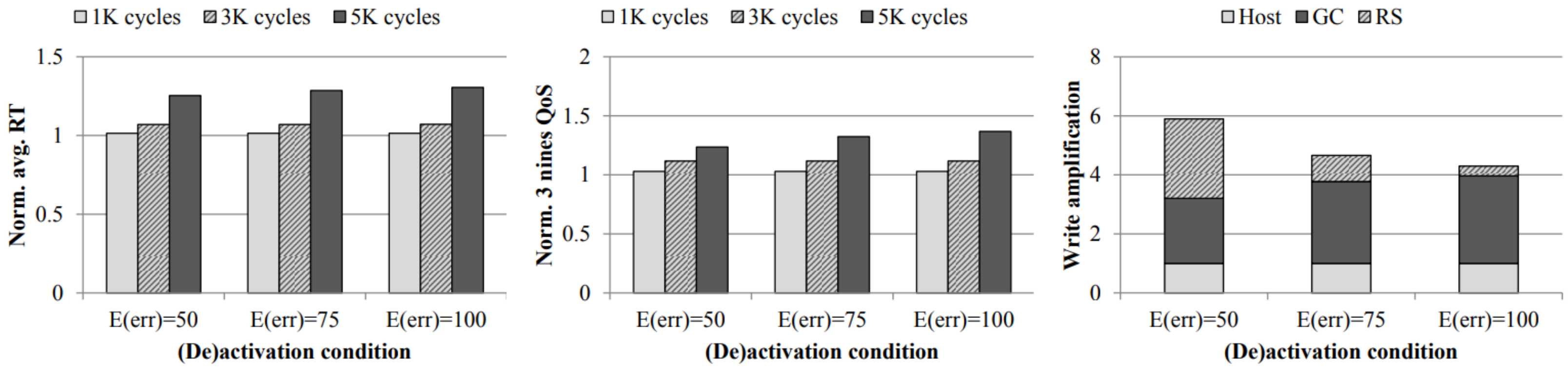


Figure 7: Performance, write amplification, and reliability for the 72-layer TLC SSD when `max retry count` is *three*. The performance degradation is not as severe as shown in Figure 6, but the write amplification (Figure 7c) remains similar. Reliability improves, but not all data can be reconstructed fully in the 5K wear state (Figure 7d).

Evaluation of SSD Reliability

- Background Scrubbing
  - Oracle data scrubber: SSD can be tracked to compute the RBER at any given point in time (not feasible in practice)
  - E(err)=50 relocates data most aggressively, while E(err)=100 does so lazily
  - Scrubbing is not a panacea, but it is more suitable than intra-SSD redundancy for complementing the underlying ECC
    - Scrubber's perf. overhead is less than the redundancy, and the increase in WAF only occurs the end-of-life phase

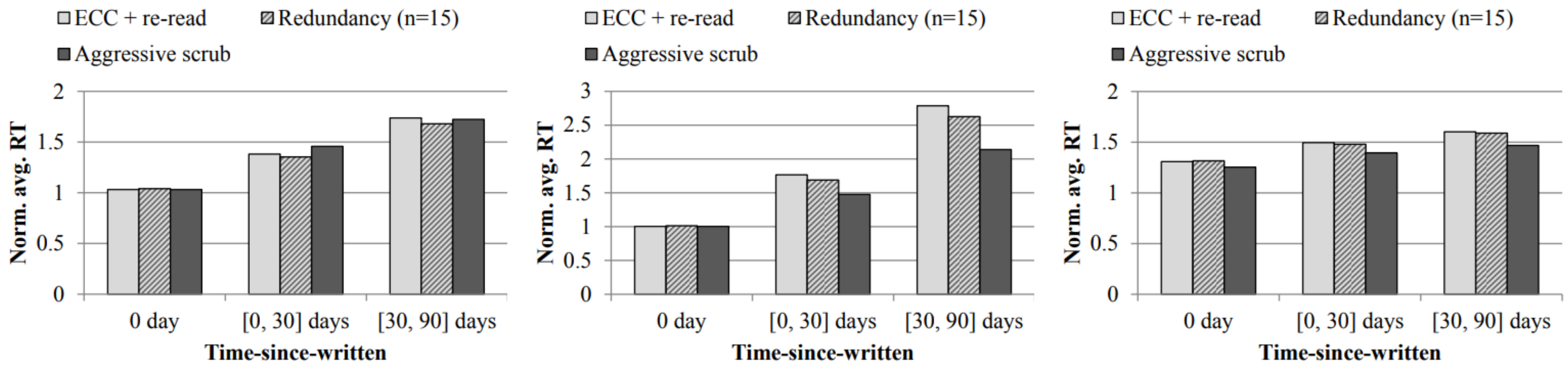


(a) Average response time. (b) Three nines QoS. (c) Write amplification at the 5K wear state.

Figure 8: Performance and write amplification for the 72-layer TLC SSD using oracle scrubbing. The performances are normalized to an SSD with ∞ ECC strength. The oracle scrubber's (de)activation condition uses the expected number of errors per block. The ECC engine corrects up to 75-bit errors, so the E(err)=50 represents an aggressive scrubber.

Evaluation of SSD Reliability

- Retention Test
  - Effects of data loss due to charge leakage by initializing a non-zero time-since-written value for each data
  - Performance difference between the background scrub approach and others becomes more noticeable
  - Compared to the scheme that relies on data re-reads, the aggressive scrubber reduces the perf. degradation by 23% for the [30,90] days setting



(a) 3x-nm MLC at the 50K wear state. (b) 2y-nm MLC at the 10K wear state. (c) 72-layer TLC at the 5K wear state.

Figure 9: Average read response time for the three SSDs (all at end-of-life wear state) with various initial time-since-written states. For 0 days, all blocks starts with no retention loss penalty. For [0,30] days, each block starts with an initial time-since-written between 0 and 30 days. Similarly, [30,90] days initializes blocks with values between 30 and 90 days. Performance is normalized to ∞-bit ECC.

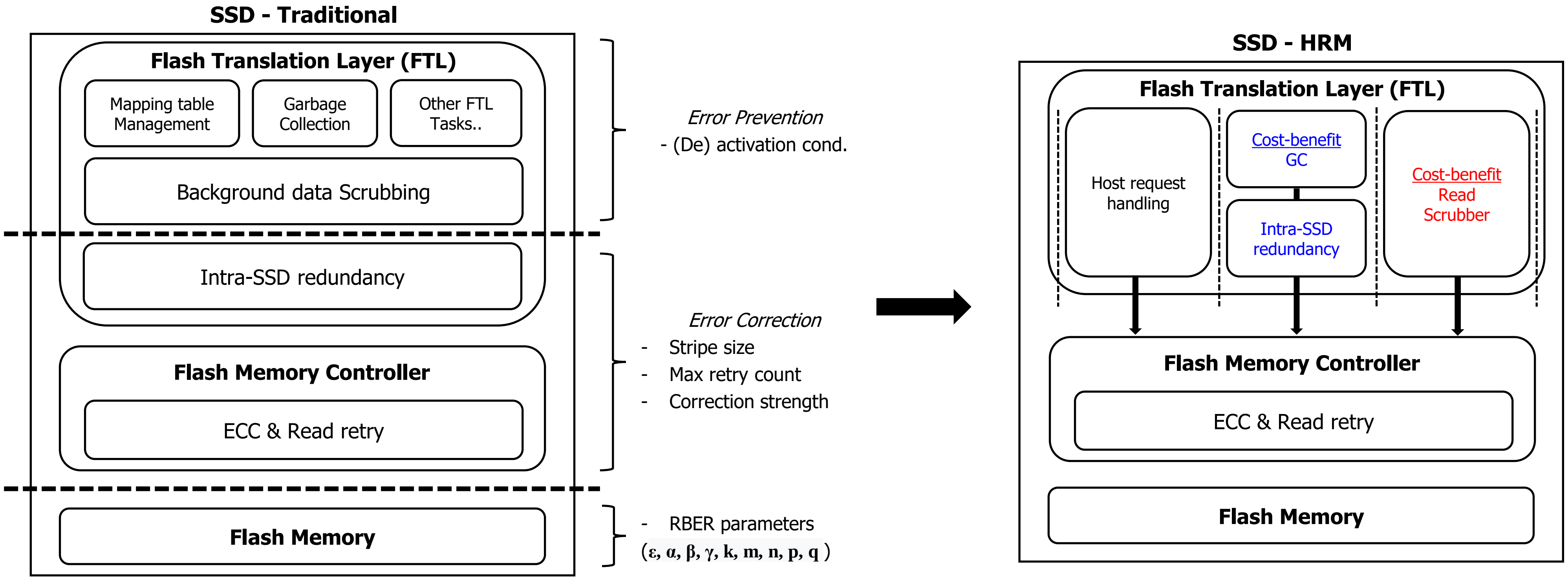
Discussion

- In the high wear states, data re-reads severely degrade the performance
  - Data re-read further increases the bit error rate, cause subsequent accesses to perform more data re-reads
- Intra-SSD redundancy is the only mechanism to recover data when a random chip and wordline fail
  - There are more cons than pros in terms of performance, write amplification, and reliability
- Background Scrubbing is more robust, reducing the perf decrease at the end-of-life states
  - The effectiveness of scrubbing depends on the accuracy of error prediction and internal traffic management

→ There is no one size fits all solution

Proposal

- Holistic Reliability Management (HRM)
  - Selectively applies appropriate technologies depending on data characteristics
- Apply redundancy to infrequently accessed data and apply scrubbing to frequently read data
  - The Read scrubber(RS) is read hot, while the leftover data selected by the GC is cold

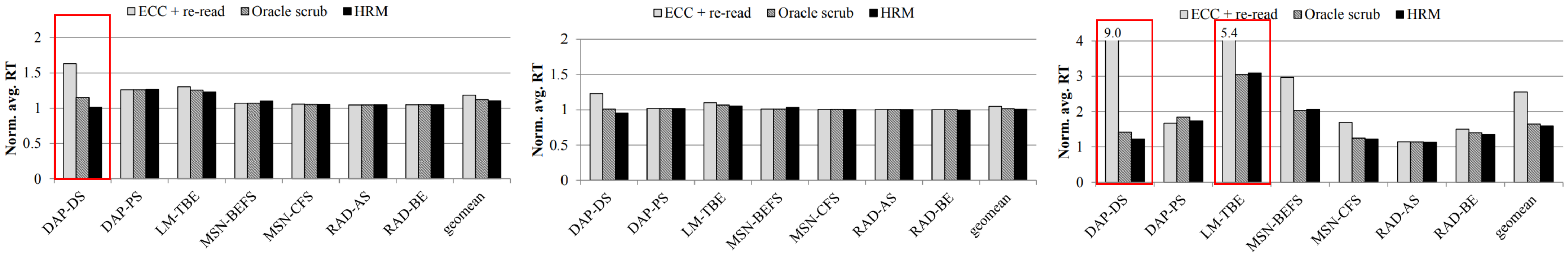


Experiment

- Real-world I/O traces from Microsoft production servers
  - Normalized to the performance of ∞-bit ECC on the three SSDs
  - End-of-life phase of SSDs
  - 200 GiB range
  - 4KiB boundaries

Table 4: Trace workload characteristics. `Access footprint` is the size of the logical address space accessed, and `Data accessed` is the total amount of data transferred. `Hotness` is the percentage of data transferred in the top 20% of the frequently accessed address.

Workload	Application description	Duration (hrs)	Access footprint (GiB)		Data accessed (GiB)		Hotness (%)	
			Write	Read	Write	Read	Write	Read
DAP-DS	Advertisement caching tier	23.5	0.2	3.5	1.0	40.5	77.8	35.3
DAP-PS	Advertisement payload	23.5	35.1	35.1	42.9	35.2	34.6	20.3
LM-TBE	Map service backend	23.0	192.7	195.5	543.7	1760.0	34.4	45.1
MSN-BEFS	Storage backend file	5.9	30.8	45.8	102.3	193.7	56.9	58.7
MSN-CFS	Storage metadata	5.9	5.7	14.6	14.0	27.0	58.5	56.6
RAD-AS	Remote access authentication	15.3	4.8	1.2	18.7	2.4	63.3	53.1
RAD-BE	Remote access backend	17.0	14.7	8.3	53.3	97.0	49.0	32.7



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Conclusion & Limitation

- Examine the design tradeoffs of the existing reliability enhancement techniques in SSDs across multiple dimensions such as performance, write amplification, and reliability.

- Existing solutions exhibit both strengths and weaknesses, and propose a reliability management scheme that selectively applies appropriate techniques to different data.

- Necessity to integrate the SSD-level design framework (FTL and flash controller) and memory cell-level models that accurately describe electron distributions

Q&A

Thank you

Paper Review

- 논문에서 좋았던 부분
  - 논문에서 제안하는 Holistic Reliability Management (HRM)를 설명하기 위해 선행 기술들에 대한 연구(Chapter 3, 4)가 상세히 진행되어 있어 HRM을 이해하는데 어렵지 않았으며, 글을 읽기가 수월했습니다.
  - 다른 논문들과 다르게 Experiment (HRM) 부분이 적었지만, 이를 제안하기 위한 Evaluation 부분에 중점을 둔 것 같았습니다.
  - 논문의 중간중간에 실험 또는 제안의 한계를 명시하는 것이 인상깊었습니다.

Table 2: RBER model parameters. Parameters ε, α, β, γ, k, m, n, p, and q describe the RBER model in Equation 1. R^2 represents the goodness of fit and is computed using the log values of the data and model, and N is the sample size.

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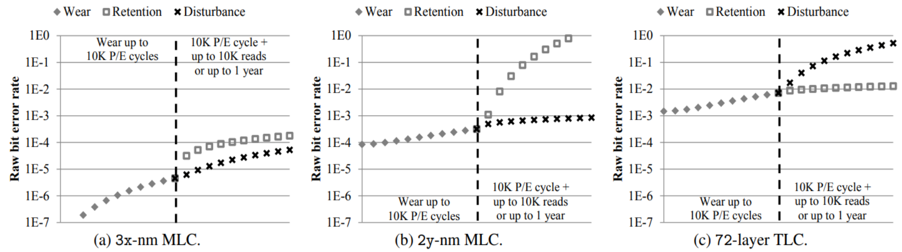

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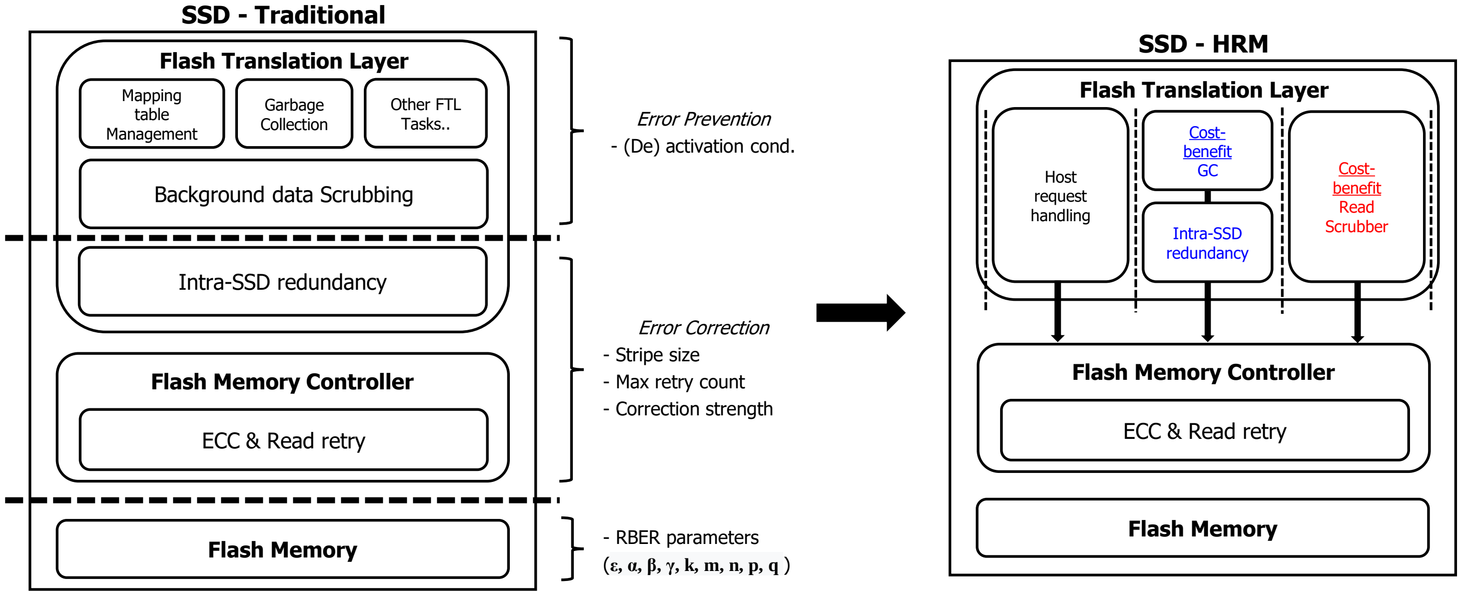

Paper Review

- Q: 왜 Wear leveling을 사용하여 Cell을 균등하게 사용하는가? (왜 하나의 Cell을 집중적으로 사용하지 않는가?)

  - Cell lifetime: 플래시 메모리는 P/E 사이클을 반복할수록 셀의 수명이 짧아지는데, 특정 셀만 집중적으로 사용하면 해당 셀이 빨리 마모되어 전체 디바이스의 수명을 단축시킨다.

    → 웨어 레벨링은 모든 셀에 균등한 P/E를 보장함으로써 특정 셀이 집중적으로 마모되지 않도록 한다.

  - Error rate: 플래시 메모리는 사용 시간이 길어질수록 오류율이 증가하는데, 특정 셀이 집중적으로 사용되면 해당 셀에서 발생하는 오류가 더 많이 축적된다.

    → 웨어 레벨링을 통해 셀 사용을 균등하게 하여 전체적인 오류율을 낮출 수 있다.

  - Data integrity: 특정 셀에 대한 지나친 의존은 데이터가 손상되거나 손실될 위험을 증가시킨다.

    → 웨어 레벨링은 데이터를 균등하게 분배하여 저장함으로써 데이터의 무결성을 유지한다.

  - System performance: 셀의 마모 상태가 고르지 않으면 특정 블록이 자주 GC를 필요로 하여 성능 저하를 발생시킬 수 있다.

    → 웨어 레벨링은 이러한 문제를 완화하여 SSD의 전반적인 성능을 유지시킨다.