OKI semiconductor

MSM5218

ADPCM SPEECH ANALYSIS/SYNTHESIS IC

GENERAL DESCRIPTION

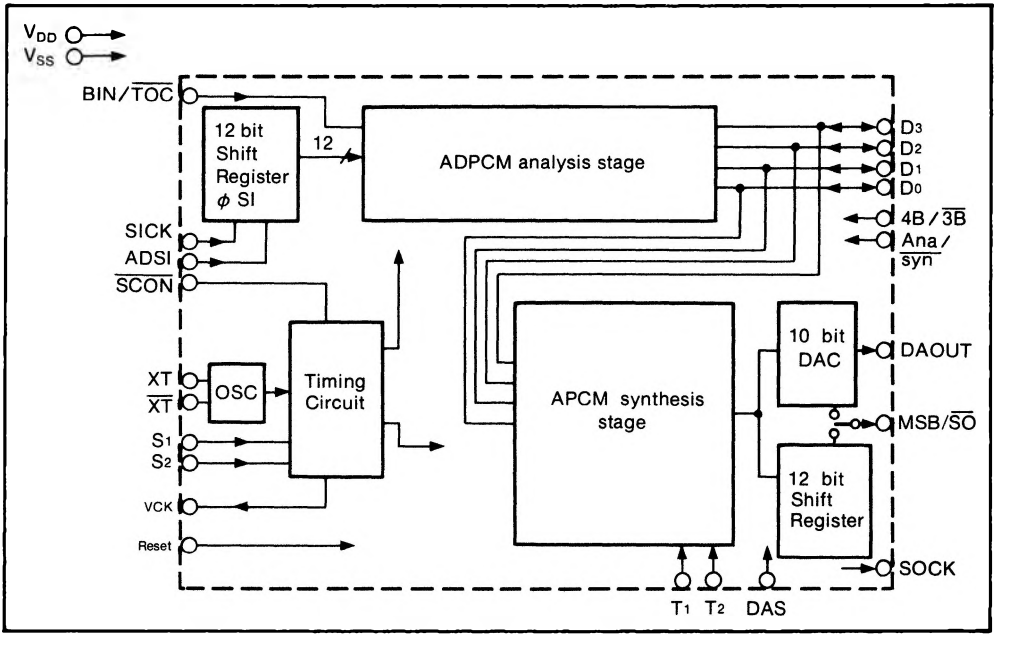
The MSM5218 is a complete speech analysis/synthesis LSI featuring the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression. The MSM5218 contains an analysis stage where serial PCM data is compressed to 3- or 4-bit parallel ADPCM data. In addition, a synthesis stage synthesizes PCM data from ADPCM data. This PCM data can be output directly or routed to the internal 10-bit DAC for analog signal output.

In addition to simplifying speech analysis and simulation, this circuit enables users to develop their own speech analysis and synthesis systems.

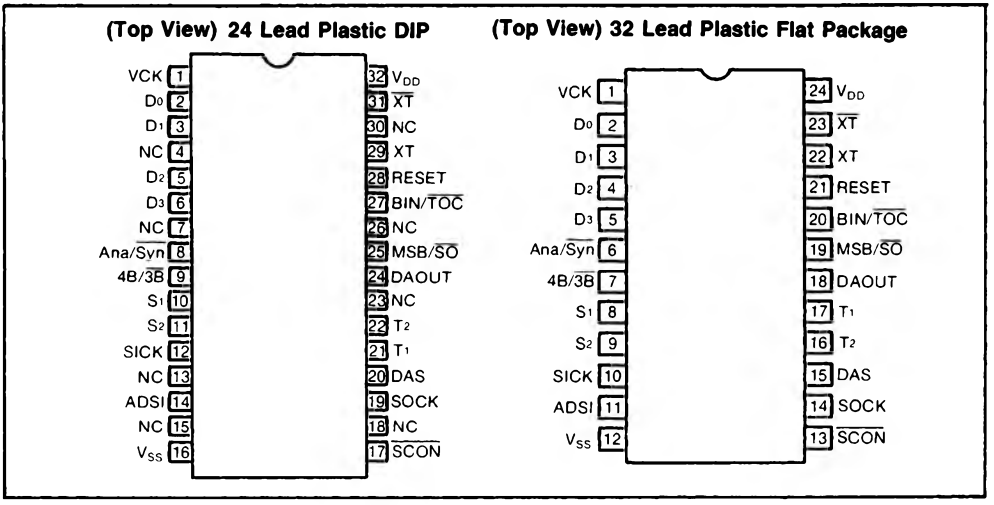
FEATURES

- One-chip speech analyzer/synthesizer
- 3- or 4-bit ADPCM system
- ADPCM data compatible with Oki's synthesis LSI MSM5205RS
- Single power supply
- Variable sampling frequency (4 kHz, 6 kHz, 8 kHz)
- Low power consumption CMOS process (15 mW typical)
- Built-in 10-bit D/A converted for analog output
- Handshaking signals provided for synchronous operation with an external A/D converter.
- 24 pin plastic DIP, 32 pin plastic flat.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	Ta = 25°C	-0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	-0.3 to V_{DD}	V
Power dissipation	P_D	Ta = 25°C	200 max	mW
Storage temperature	Tstg	—	-55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may after device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	—	+3 to +6	V
Operating temperature	Top	—	-30 to +70	°C

D.C./A.C. CHARACTERISTICS

(V_{DD} = 5V ± 5%, Ta = −30°C to +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All input except T_1, T_2	4.2	—	—	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	—	—	0.8	V
Input High Current(1)	I_{IH}	$V_{IN} = V_{DD}$	—	—	1	μA
Input Low Current	I_{IL}	V_{IN} = 0V	—	—	-1	μA
Output High Current	I_{OH}	$\overline{SCON}$, VCK, SOCK, MSB/$\overline{SO}$, D0~D3 Vo = 4.2V	-50	—	—	μA
Output Low Current	I_{OL}	$\overline{SCON}$, VCK SOCK, MSB/$\overline{SO}$, D0 ~ D3 Vo = 0.4V	50	—	—	μA
Oscillator Frequency	f_{OSC}	Specified Oscillator	—	384	768	kHz
Operating Current Operating Current	I_{DD} I_{DD}	f_{VCK} = 8 kHz f_{VCK} = 16 kHz	— —	3 6	6 12	mA mA
DA. OUT Output Impedance	V_{OR}		100	—	kΩ	
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale V_{DD} = +5V	—	±4	—	LSB
SICK Clock Frequency	f_{SICK}		—	—	500	kHz
Input High current (2)	I_{IH2}	$V_{IN} = V_{DD}$ Note 1	20	—	400	μA

Note1: Applicable for Reset

PIN DESCRIPTION

Pin Name	Terminal Number		I/O
	24 DIP	32 FLT	
V_{CK}	1	1	O

This pin outputs a signal whose frequency is equal to the sampling frequency selected by S1, S2 inputs.

D_0	2	2	I/O
D_1	3	3	I/O
D_2	4	5	I/O
D_3	5	6	I/O

Data I/O port for the ADPCM data. For 3-bit ADPCM data, D_0 input is not used.

ANA/$\overline{SYN}$	6	8	I/O

Analyze/synthesize function selector. Controls data I/O port direction. When high, data I/O are outputs and simultaneous analysis and synthesis occur. When low, data I/O are inputs and no analysis occurs.

4B/$\overline{3B}$	7	9	O

Specifies whether 3-bit or 4-bit ADPCM data is to be used. High = 4-bit.

S_1	8	10	I
S_2	9	11	I

These inputs select the sampling frequency according to figure 1.

SICK	10	12	I

Clock input for clocking in serial PCM data from an external ADC into the internal 12-bit shift resister.

ADSI	11	14	I

Serial PCM data input.

V_{SS}	12	16	I

Ground (0V)

$\overline{SCON}$	13	17	O

Output which signals the start of conversion.

SOCK	14	19	O

When serial PCM data output mode is selected (DAS = H), this pin provides a 192 kHz signal which is synchronized with the output of the serial PCM data through the MSB/$\overline{SO}$ pin. Each bit of the 12-bit PCM data will be valid before the positive edge of this 192 kHz signal.

DAS	15	20	O

Selector for analog signal output (DAS = L), or serial PCM data output (DAS = H).

Pin Name	Terminal Number		I/O
	24 DPI	32 FLT	
T1	17	21	I
T2	16	22	I

IC test pins used at factory for testing purposes only. During normal operation, T1 is grounded and T2 is left open.

DAOUT	18	24	O

Analog signal output pin.

MSB/$\overline{SO}$	19	25	O

MSB/serial data output pin — MSB of the data in the internal 10-bit DAC will appear at this pin if analog signal output mode (DAS = L) is selected. When serial PCM data output mode is selected (DAS = H), serial PCM data can be clocked out of this pin.

BIN/$\overline{TOC}$	20	27	I

Specifies whether the input serial PCM data is in binary or 2's complement form.

RESET	21	28	I

An active high input which initializes the MSM5218RS internal circuitry. To be effective, must be held true for at least one VCK time.

XT	22	29	I
$\overline{XT}$	23	31	I

Oscillator inputs for a 384 kHz crystal or ceramic resonator (Figure 2).

V_{DD}	24	32	I

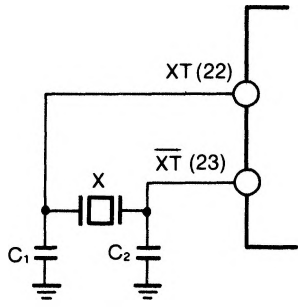
Power supply pin. (typical +5V)

S1	S2	Sampling Frequency
L	L	4 kHz (384 kHz/96)
L	H	6 kHz (384 kHz/64)
H	L	8 kHz (384 kHz/48)
H	H	Prohibited

Note: The 384 kHz oscillator must be used whether 4 kHz, 6 kHz, 8 kHz.

With 384 kHz oscillator. Other oscillator frequencies are possible and will proportionately modity the sample rate.

Figure 1



X-384 KHz

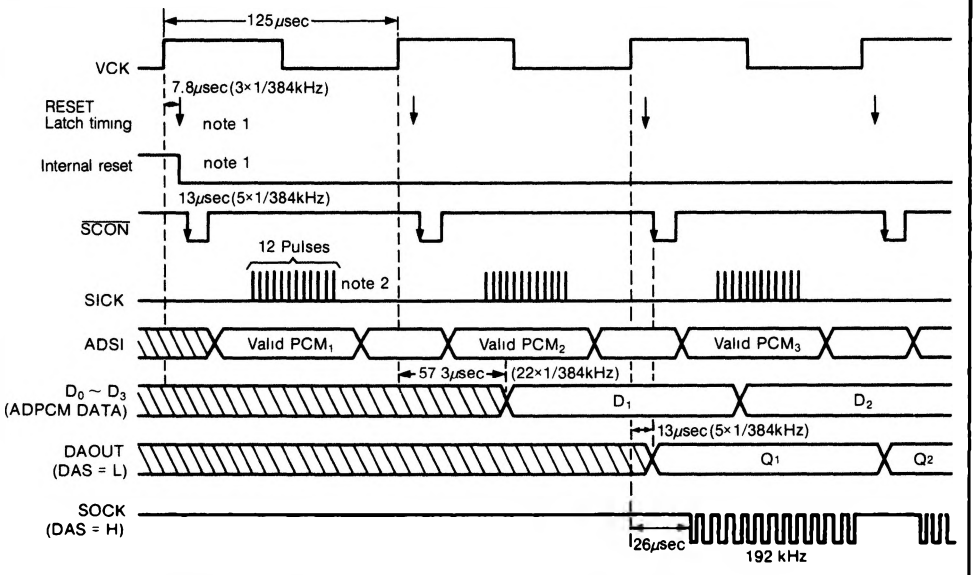
C_1-220pF
C_2-220pF

Murata Corporation
CSB 384P
Or as required to match crystal or ceramic resonator load specifications.

XT and $\overline{XT}$ (Oscillator connector pins)

Figure 2

ANALYSIS WITH SIMULTANEOUS SYNTHESIS (f_{SAMPLE} = 8kHz)

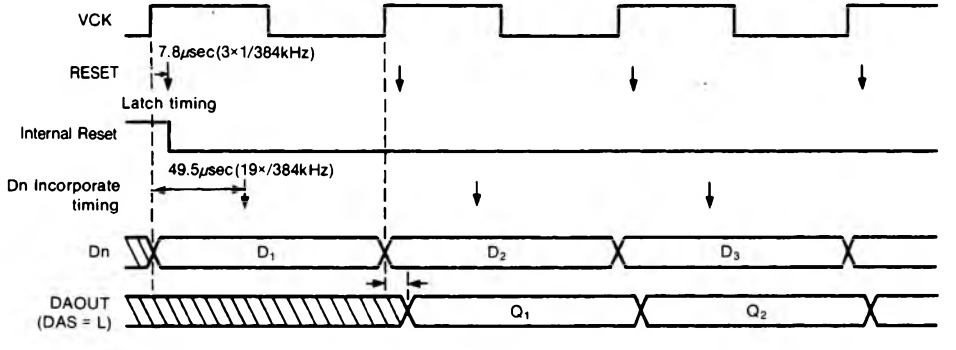


Note 1: The state of the RESET input is strobed into the internal reset latch by the reset latch timing pulse. Analysis begins on the H to L transition of internal reset

Note 2: Up to 12 bits of PCM data may be strobed into the device by SICK. If more than 12 SICK pulses occur in a given VCK cycle, only the last 12 are regarded as valid. The cycle of SICK pulses must be completed before the next SCON- pulse.

PCMn: nth input PCM data (12 bits)

SYNTHESIS ONLY (f_{SAMPLE} = 8kHz)



Dn: nth ADPCM data.

Qn: Analog output corresponding to input nth ADPCM data.

Figure 3

BLOCK DIAGRAM - ANALYZER

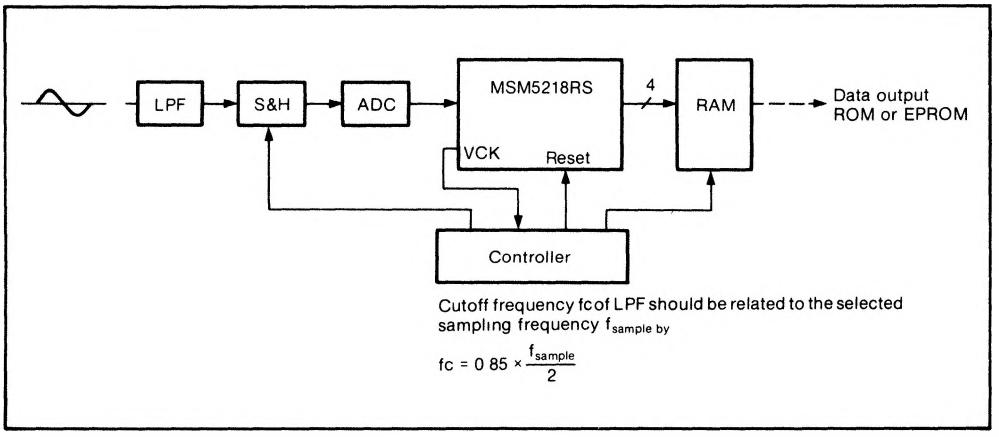


Figure 4

BLOCK DIAGRAM - SYNTHESIZER

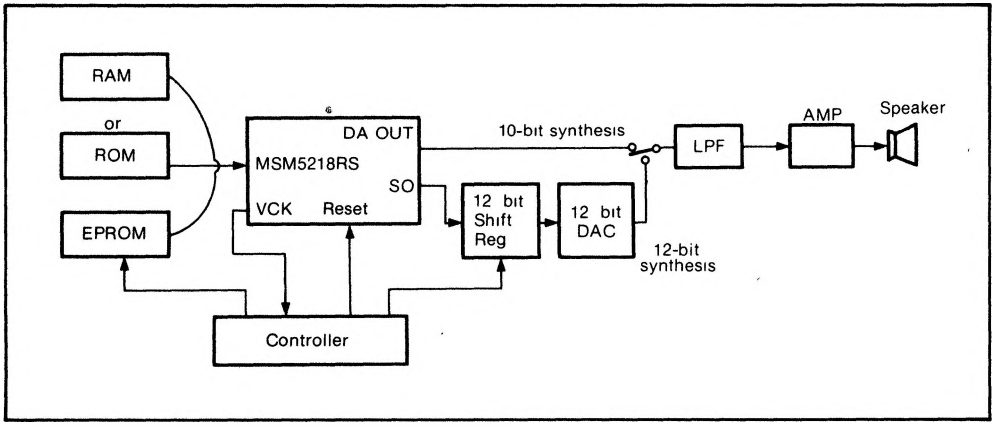


Figure 5

DISTINCTION BETWEEN MSM5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method. However, with the exception that MSM5218 is equipped with an overflow protection.
In other words, when all 12 PCM bits become '1' any further exceeding analog input would cause a data overflow which is catched and re-routed as the MSB in case of MSM5218.
MSM5205 returns to 'all bits zero' when a data overflow sets in.
Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the A to D converter should be limited to 80% of the converters maximum input range. The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

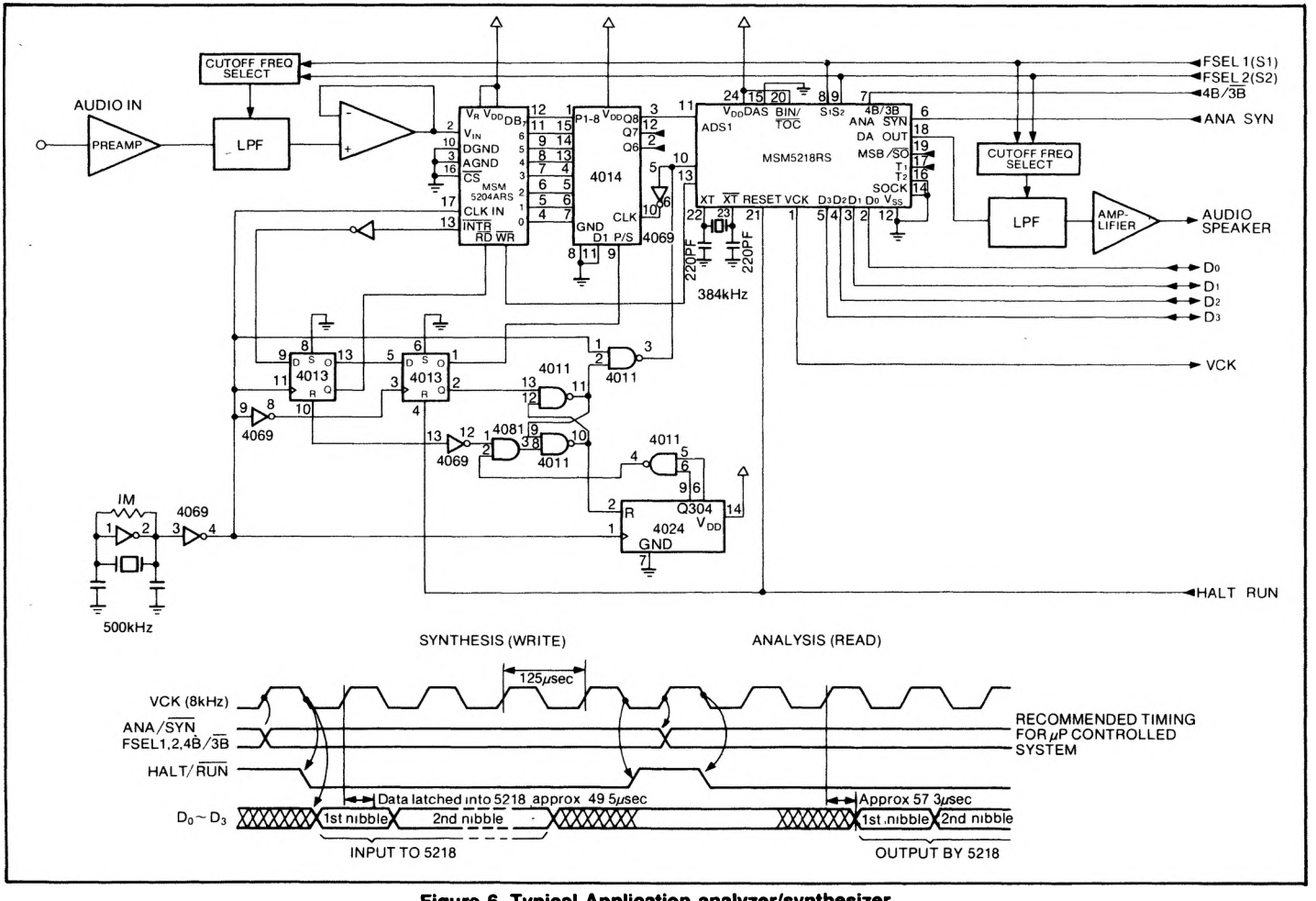


Figure 6 Typical Application analyzer/synthesizer