PRODUCT: 8245 **REV:** 0 **DATE:** 1/20/78

The 8245 is a general purpose graphics display device that operates in conjunction with raster scan type displays. Its primary purpose is to provide a means for generating and moving objects on a TV screen for use in the customer game market. However, its generality and flexibility makes it suitable for use also in teaching machines, animation displays, simulation trainers, and etc.

This device is a peripheral that communicates over the data and address bus of the 8048/8748. Although other microprocessors may be used with it, these particular devices provide the greatest capability for the low system cost.

FEATURES

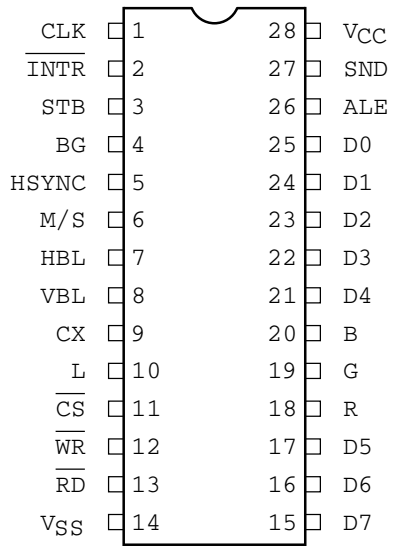
- Single 5V supply
- 28 pin CerDip or plastic DIP package.
- 8048/8748/8085 Compatible.
- Partial color TV sync generator, CCIR standards.
- Provides shapes that are mask programmable in internal ROM.
- Accommodate up to 32 object locations on the display simultaneously.
- Devices may be multiplexed to provide greater than 32 object locations on the display.
- All movement of objects displayed is under software control in the microprocessor.
- Display objects that collide return status and location information to the microprocessor.
- Provides Red, Green, Blue, Luminance, and Sound outputs.

* Note: Signals that are asserted when the variable is low voltage are designated by a $\overline{\ }$, eg. $\overline{CS}$ is active low.

SYMBOL	I/O	
D0-D7	I/O	Data/Address lines to/from 8048/8749.
$\overline{CS}$	I	Chip Select enables writing to or reading from the addressed Functional block within the device.
ALE	I	Address Latch Enable allows the contents of the multiplexed address/data bus to be interpreted as an address.
$\overline{WR}$	I	Write Strobe causes the bus data to be written into the previously selected memory element.
$\overline{RD}$	I	Read Strobe allows status and counter information to be read from the device.
$\overline{IRQ}$	I	Interrupt request to the microprocessor, set Low for request and cleared when the status register is read.
HSYNC	O	Horizontal sync.
VBL	I/O	Vertical blanking identifies the period during which the display is blank while the CRT beam is in vertical retrace.
HBL	O	Horizontal blanking identifies the period during which the display is blank while the CRT beam is in horizontal retrace.
M/S	I	Master/Slave designates a device to be either a master or a slave unit. A master, so designated, feeds VBL and HBL to itself from its internal sync generator and also sends VBL and HBL out to the slave device if one exists. A slave, so designated receives VBL and HBL for its internal synchronization.

CLK	I	The clock input operates at a fixed frequency of 3.54 MHz. The duty cycle shall be 50% with 5% deviation.
R	O	The Red output is a chroma signal representing objects that are to be displayed in a read color.
G	O	The Green output is a chroma signal representing objects that are to be displayed in a green color.
B	O	The Blue output is a chroma signal representing objects that are to be displayed in a read color.
L	O	The Luminance output represents the ORed result of active patterns in the minor system, the major system, and the grid (if set grid bright is active)
BG	O	The Burst Gate defines the duration of the 4.43 MHz color reference signal required for generation of the composite color signal in external analog circuitry.
SND	O	The Sound output provides an audio driving signal to the external sound modulator.
STB	I	The position strobe input.
CX	I	Chip Expander. If there are 2 8245's in a system, LUM #2 is connected to CX #1 and LUM #1 is connected to CX #2. This allows status or overlaps between objects on different chips to be read by the CPU.
VCC	I	+5V supply.
VSS	I	Gnd.

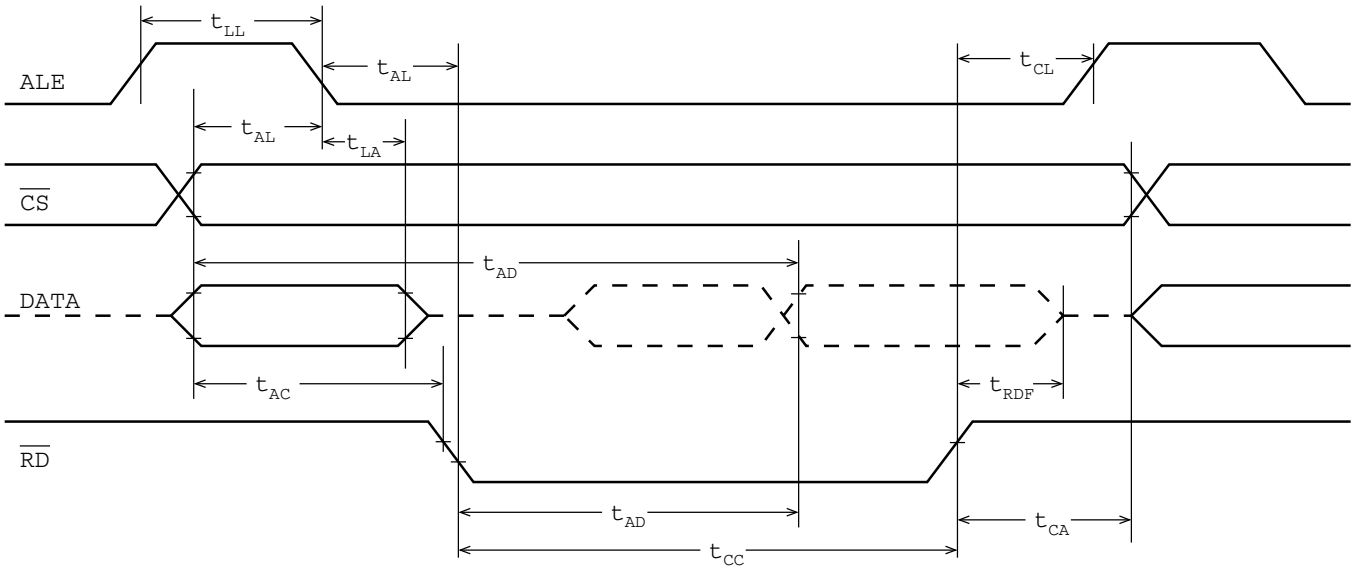
8245 PINOUT



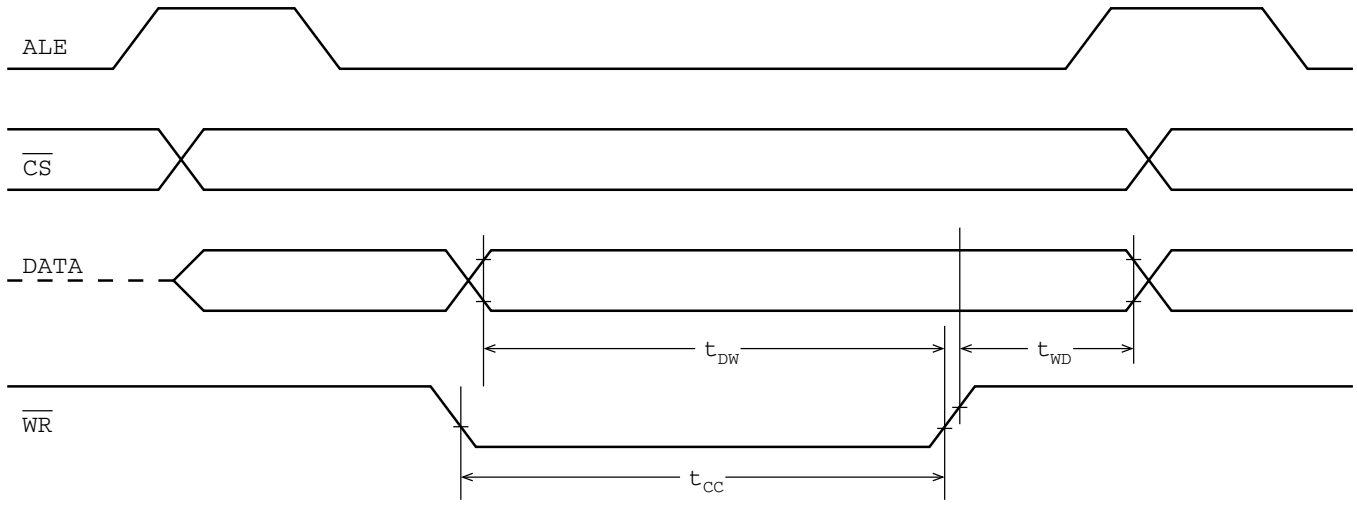
SUMMARY

The 8085 timings are more restrictive than the 8048 timings. Although the initial game product will match an 8245 with an 8048, it is desirable to design the 8245 to work with both the 8048 and the 8085. This will allow upwards compatibility with the more powerful CPU and very probably will extend the product life of the 8245. The following timings should allow the 8245 to work in either system.

READ CYCLE:



WRITE CYCLE:



References: “Standard Peripheral Timing for 8085 Bus”, April 20, 1976; 8048/8748/8035 <cropped> datasheet, September 1976

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tAL	Address valid before T.E. of ALE	50		NSEC
tLA	Address hold time after ALE	100		NSEC
tLL	ALE width	100		NSEC
tAC	Address valid to L.E. of control	150		NSEC
tLC	T.E. of ALE to L.E. of control	100		NSEC
tAD	Address valid to valid data out		400	NSEC
tRD	Data out delay from RD		150	NSEC
tRDF	Data bus float after RD	10	75	NSEC
tCC	Width of control	250		NSEC
tDW	Data in valid to T.E. of WR	150		NSEC
tWD	Data valid after T.E. of WR	0		NSEC
tCL	T.E. of control to L.E. of ALE	20		NSEC
tRV	T.E. of control to L.E. of next control	300		NSEC
tCA	Address hold after control	0		NSEC

NOTE: The 8245 will ignore the information on the data lines except for the cycles when $\overline{RD}$ or $\overline{WR}$ are active.

8245 ELECTRICAL SPECIFICATION

D.C. CHARACTERISTICS

T_A = 0ºC to 70ºC; V_{CC} = +5V ±5%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{IL}*	Input low voltage	V_{SS}-0.5		0.8	V	
V_{IH}*	Input high voltage	2.0		V_{CC}	V	
V_{OL}	Output low voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output high voltage	2.4			V	I_{OH} = -200µA
I_{IL} ≤	Input leakage			± 20	µA	(V_{SS} + 0.45) ≤ V_{IN} ≤ V_{CC}
I_{CC}	V_{CC} current drain			200	mA	

A.C. CHARACTERISTICS

T_A = 0ºC to 70ºC; V_{CC} = +5V ±5%; V_{SS} = 0V

Timing measurements are made at the following reference voltages unless otherwise noted:

Input "1" = 2.0V, "0" = 0.8V
Output "1" = 2.0V, "0" = 0.8V

Output loading consists of one TTL load and 50pF total external capacitance except the system bus which is loaded by one TTL load and 100pF.

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* Except CLK input which has V_{IL} = 0.5 MAX V_{IH} = 4.0 MIN and rise/fall time Rise and fall times will be 200 NSEC or less. Rise and fall times will be measured from 0.8V to 2.0V. RGB outputs occur within 25 nsec, of each other, luminance output will occur 0 to 150 nsec, after RGB.

FUNCTIONAL SPECIFICATION

The 8245 is organized as a group of subfunction blocks that communicate via an internal bus with the I/O port. Most of the subfunctions are individually addressable for the transfer of information with the controlling microprocessor. These blocks may be categorized functionally as follows:

1. Major display system
2. Minor display system
3. Grid display system
4. Sound system
5. Status and control circuits
6. Sync generator

The use of both major and minor display systems provides hardware parallelism to circumvent the problem of concurrent objects. In general, the single major system is used to display fixed objects, while the plurality of minor systems similarly handles moving objects. In exceptional cases nonstrategic moving objects may be placed in the major system but this should be avoided where accommodation is provided by the minor systems. All objects in the major system are composed of 8 X 7 bit arrays,* while all objects in the minor system are composed of 8 X 8 bit arrays. Larger objects are produced by concatenation of the basic arrays. All major system objects start on even lines.

The grid display system places a segment programmable grid in the background of the display. Any grid segment may be either inserted or deleted programmatically to produce a variety of arrays such as checkerboards, racetracks, mazes, and etc. An additional feature allows vertical segments to be expanded horizontally and thus provide illuminated square and rectangular areas.

The sound system contains both a random noise generator as well as a programmed sound section. The resulting signals may be combined digitally to produce special effects such as gun shot sounds.

The status and control circuits provide a message transfer mechanism between the 8245 and the microprocessor. Control messages sent from the microprocessor are utilized within the control circuits. These messages determine the types of status messages to be returned and also define certain key conditions associated with the displayed objects. The status messages returned to the microprocessor from the 8245 provide information relative to the display that is used by the microprocessor for input to the program.

* An 8 X 7 array is composed of 8 horizontal dots and (7 X 2) horizontal lines.

- missing -

The first group uses four CAM locations to provide starting points for multiple objects. Each group CAM location contains an additional 2-bit counter and thereby is able to point to four LSS* locations. Thus, the first group controls the placement and selection of 16 objects. If the fourth pattern is truncated all four objects will be truncated to the height of the fourth.

The second group within the major system provides for the placement of game obstacles that are either fixed in location or may be movable within certain restrictions. As movable objects, they should not be utilized as strategic elements such as balls, bullets, race cars, etc. However, they do provide slow moving obstacles such as covered wagons or other vehicles. In addition, these objects, when moving, should be prevented from overlapping any other objects in the major system as no means for identification by the microprocessor is available. This nonoverlapping function is achieved by proper programming. Within this group there is a one to one correspondence between a CAM location and a single displayed object. Since there are 12 CAM locations in the second group, there are also 12 objects that may be placed.

The portion of the total CAM array that constitutes the major system points to a total of 28 storage locations in the LSS. The information stored in the LSS represents the location address of the associated pattern in the pattern ROM. Rather than store the starting address of the desired pattern in the LSS, a two's complement displacement is stored. This expedient allows a simple hardware mechanism for sequencing through the consecutive addresses of ROM patterns as they are encountered. The displacement represents the difference between the starting address of the object pattern in ROM and the scanning line number in the raster display. This may be simply stated as follows:

$$LSS_N = \text{ROM object Address} - \left[\frac{(\text{VertiCam Data})_N}{2}\right]$$

N = Object Number

A single 9 bit adder is sufficient for accommodating all address sequencing for the major system. The LSS must be able to store 9 bit displacements. The sequence of events that takes place for the placement of an object pattern is as follows: As a match occurs between the contents of the beam location counter and the address stored in any particular CAM cell, a pointer enables an output from the particular associated line number, obtained from the line counter, and results in the address of the desired row of the object pattern in ROM. If the full 8 X 7 pattern is desired, then the first match of the CAM causes the above described procedure to produce the starting address of the object pattern in ROM. As horizontal matches occur on successive scan lines, a consequential incrementation of the ROM address occurs. An end of pattern address is detected on every eighth address and terminates the presentation of each particular object. There is no restriction as to whether a full 8 X 7 or any portion of the pattern in the vertical dimension may be presented as a displayed object. This flexibility allows the programmer to use fractions of object patterns if it is desired to do so.

*LSS = Linear Select Store

In addition to the 9 bit displacement in each location in the LSS, there is provision for the storage of 3 color bits. These bits designate the primary colors red, green, and blue. By the activation of more than one color bit simultaneously, various hues are also produced.

The following table presents a summary of the specifications for the major system:

Group	No. of CAM Loc.	No. of Bits in Vert. CAM	No. of Bits in Hor. CAM	No. of Simul Objects CAM loc.	No. of Simul Objects Group	No. of Selectable Objects *	Disp. Bits in LSS	Attribute Bits in LSS	Object Size
1	4	7	8	4	16	64	9	3	8 dots wide 14 lines high
2	12	7	8	1	12	64	9	3	8 dots wide 14 lines high

* There are 64 objects total, any of which can be selected by either Group.

MINOR DISPLAY SYSTEM

As a first order objective all strategic objects are selected and displayed by the minor display system. In some games it may be useful to put fixed objects in the minor system and there is no restriction that prevents this. There are four replicated blocks within the minor system. Each block is autonomous in function and provides for the placement of a single object. Each of these objects may collide with each other or with objects in the major system. In either event, the minor object is readily identifiable by the microprocessor so that immediate responsive action may be taken.

Minor system objects are locatable by a portion of the overall CAM array, just as in the major system. However, the similarity of the two systems ends in the signal path beyond the CAM array. Each of the four CAM locations in the minor system is dedicated and points to a singular block of object pattern bits located in RAM storage. In contrast, the CAM locations in the major system can point to any of the 64 objects stored in the pattern ROM. In addition, the mechanism for sequencing through the rows of the pattern RAM's is different than that used in the major system.
In place of a singular adder as used in the major system, each minor system contains its individual three bit counter. This counter is updated at the beginning of each horizontal scan line. The decoding of the counter points to the proper location in the pattern RAM. Thus, each dot row in an object is presented as the RAM locations are sequenced. The RAM locations are loadable from the internal bus by a Write operation of the microprocessor. The RAM has the capacity to store eight bytes for each object thereby allowing an 8 X 8 object presentation. Associated with each minor system is an Attribute Register whose contents are arranged as follows:

7	6	5	4	3	2	1	0
X	X	B	G	R	D	S	X_9

The Bits in this register are defined as follows:

Bit 0 - X_9 is the ninth Bit in the horizontal address of the beam location. This bit allows the beam location to be resolved to 140ns increments.

Bit 1 - The S or smoothing Bit allows a displacement of either the odd or even count horizontal sweep lines in order to provide an improved appearance of objects that visually rotate on the screen.

Bit 2 - The D or duration Bit determines whether an object will be presented in normal size or if its x and y dimensions will be increased by a factor of two.

Bit 3 - The R Bit specifies whether the object contains a red component of color display.

Bit 4 - The G Bit specifies whether the object contains a green component of color display.

Bit 5 - The B Bit specifies whether the object contains a blue component of color display.

Bits 6 and 7 - These bits are unspecified and exert no control.

The definition of the delay of dot rows within an object depends on Bits 0, 1, and 2 as shown in the following table:

Bit 2 D	Bit 1 S	Bit 0 X_9	Even Line Delay (ns)	Odd Line Delay (ns)
0	0	0	0	0
0	0	1	140	140
0	1	0	140	0
0	1	1	0	140
1	0	0	0	0
1	0	1	280	280
1	1	0	280	0
1	1	1	0	280

GRID DISPLAY SYSTEM

The grid display consists of an array of nine enclosed areas horizontally and eight areas vertically. Each line segment between the nodes of the array is individually controllable so that it may be presented or be inhibited.

A full array, consisting of all segments present, is created by combining nine complete horizontal display bars with ten complete vertical display bars. Each horizontal bar consists of nine concatenated bar segments, while a vertical bar consists of eight concatenated bar segments. Each horizontal bar on the TV screen is composed of three consecutive horizontal scan lines, while adjacent bars are spaced by 21 horizontal scan lines. A vertical bar is made up of a column of dot groups. Each dot group is programmable to consist of either two or sixteen clock intervals (3.54Mhz) in width*. A conventional grid utilizes two clock intervals while large area clock arrays, such as checkerboards, utilize sixteen clock intervals. The spacing between adjacent vertical bars is fourteen clock intervals. Thus, wide vertical bar segments that are adjacent, appear to be continuous displayed areas. The grid is centered vertically on the TV screen by allowing the first or top horizontal bar to start on the 24th horizontal scan line relative to the end of vertical blanking (VBL). Similarly, horizontal centering is accomplished by allowing the first or left-most vertical bar to start on the 10th clock cycle from the end of horizontal blanking (HBL).

A programmable feature allows the grid to be augmented by the addition of a dot matrix. In this case the dots appear at a physical placement on the TV screen, where otherwise the intersection of the horizontal and vertical bars would appear. The dots are composed of three horizontal scan line segments that have a width equivalent to two clock cycles. Since, a full array of dots is always presented, no segment programming requirement exists for dot arrays, although segments and dots can simultaneously be displayed.

An additional programmable feature allows the grid display, or any of its previously described subsets, to be either presented or inhibited on the TV screen.

The upper left hand corner of the grid has program coordinates (Y,X) = (13H,0BH). The observed position on the screen will be (Y,X) = (18H,18H).

* Horizontal displacement on the TV screen is directly proportional to time.

SOUND SYSTEM

The sound system generates a duty cycle modulated square wave from which an audio signal is extracted by means of an external low pass filter. The control of the duty cycle is effected by information that is transferred from the microprocessor to the 8245. This information consists of triple byte groups that determine the audio frequency and an accompanying 4 bits that determine volume.

The triple byte groups are loaded into three-eight bit shift registers located on the 8245. Each byte in the group is loaded sequentially into its respective register during a load interval. All three bytes are loaded in between consecutive shift clock pulses. The concatenation of the three registers results in a 24 bit string that is shifted out by this shift clock. The resulting serial pattern of ones and zeroes contains a fundamental band of frequency components that lie in the audio range. This particular signal is further "chopped" by a higher frequency that is a multiple of the shift clock. By duty cycle modulation of this "chopping" signal, the amplitude of the audio component is varied. There are four control bits that are used to control the audio level. These bits are loaded into a four bit down counter that is shifted by the high frequency shift clock. The resulting output is ANDED with the output from the three concatenated shift registers to produce the composite audio output. In addition to the four volume control bits, three other control bits are used to augment the overall operation of the sound system. A noise enable bit enables a feedback path in the output eight bit shift register, in the 25 bit shift path to produce the noise component. Simultaneously, the noise is added to the audio component that is progressing down the shift register.

The shift frequency for the register may be varied between two values by another control bit. This expedient allows low audio frequencies to be produced with fewer refresh cycles from the microprocessor than for high frequencies thus, reducing the load on the processor.

For the reproduction of certain audio tones that are subharmonically related to the shift clock, the need for microprocessor refresh is totally eliminated by recirculation of the 24 bit shift path.

The format of the sound control word is described below:

7	6	5	4	3	2	1	0
EN	X	S	N	V_3	V_2	V_1	V_0

Bits 0 - 3 - Volume Bits, collectively as a 4 bit word, these bits define the output audio level.

Bit - 4 - Noise Enable; controls noise generation and mixing with the audio signal. Bit 4 = 1, noise on; Bit = 0, noise off.

SOUND SYSTEM

Bit 5 - Shift Frequency; determines frequency of shift clock.
Bit 5 = 1, f = 3933Hz. Bit 5 = 0, f = 983Hz.

$$(3933\text{Hz} = \frac{H}{4} = \frac{15{,}734}{4}\ ;\ 983\text{Hz} = \frac{H}{16} = \frac{15{,}734}{16})$$

Bit 7 - Enable sound; 0 = No sound, 1 = sound.

For those modes of operation requiring sound refresh data from the microprocessor, an interrupt is generated each time that the 24 sound bits have been shifted through the three eight bit shift registers. A 5 bit counter set to module 24 counts shift clocks and determines when the interrupt should occur.

The sound shift registers, volume counter and sound control word register are all individually addressed by the microprocessor for the purpose of loading data. The address of these elements is shown under the topic of “Address Structure”.

CONTROL AND STATUS

The control over various operational parameters on the chip is effected by the bits in the control word that is written into the control register by the microprocessor. The bits in the control word are defined as follows:

Bit 0 – Enable Horizontal Interrupt, generates an interrupt 20 µs in advance of the occurrence of horizontal blanking. This advance notice to the microprocessor allows a sufficient interval for the reading of the status information so that appropriate control can be exerted during the horizontal blanking interval.

Bit 1* - Forced Position Strobe, allows the freezing of the beam location information in the X-Y position registers so that the microprocessor can locate the beam at any time. Bit 1 = 1 strobes beam location to X-Y registers. Bit 1 = 0 disables strobe internal, but external strobe through position strobe Pin can still take place.

Bit 2 – Enable Sound Interrupt, allows an interrupt to be generated whenever the sound register needs new data. Bit 2 = 1 enables sound interrupt, Bit 2 = 0 disables sound interrupt.

Bit 3 – Enable Grid, allows two luminance levels of the grid. If the bit is a 0, the luminance signal is inhibited during grid information intervals. If the Bit is a 1, the luminance signal is active during grid information intervals.

Bit 4 – Enable External Overlap Interrupt, allows an interrupt upon detection of an overlap, when more than one 8245 exists in a system.

Bit 5 – Enable Display, allows objects to be displayed. Bit 5 = 1 enables display; Bit 5 = 0 disables objects. The purpose of this bit is to allow the µP to write new data to the 8245 when the display is part way through a display field. It is the responsibility of the software to disable the display only when there are no active patterns being displayed.

Bit 6 – Dot Enable, allows the presentation of a dot array in addition to the grid array. The dots appear at the intersection of the horizontal and vertical lines in the grid format. Bit 6 = 1 enables dots; bit 6 = 0 enables normal grid.

Bit 7 – Grid Segment Width, allows the selection of narrow or wide vertical segments in the grid. Bit 7 = 1 enables wide segments; bit 7 = 0 enables narrow grid.

The color of the grid and background is determined by the data stored in the Color Latch. Also by setting the Enable Grid bit to '0' the grid can be turned off and the grid RAM can be used for other data storage. The bits in the Color Latch are defined as follows:

*The “or” of STB and Force Position Strobe will cause X-Y reg to follow the BLC. A falling edge on the OR output will freeze the BLC. The reg will remain frozen until after the x-register is read. This strobe will not cause false data to be loaded into latch (synchronized on 0 edge, when BLC is not changing).

Bit 0 - Grid Color Blue
Bit 1 - Grid Color Green
Bit 2 - Grid Color Red
Bit 3 - Background Color Blue
Bit 4 - Background Color Green
Bit 5 - Background Color Red
Bit 6 - Set Grid Bright

CONTROL AND STATUS

The Enable Overlap register allows for selectable masking of overlaps. When a bit in the Enable Overlap register is a '0' the overlap of that object with any other object will not set the bits for the other objects in the Overlap Status register. The bit pattern is as follows:

Bit 0 - Minor System 0
Bit 1 - Minor System 1
Bit 2 - Minor System 2
Bit 3 - Minor System 3
Bit 4 - Vertical Grid
Bit 5 - Horizontal Grid and dots
Bit 6 - External Chip
Bit 7 - Major System

The Overlap Status register stores the coincidences as they occur on the screen. Whenever two or more objects are simultaneously displayed the bits for both objects are set unless the Enable Overlap register has those bits masked. The External Chip overlap corresponds to the Signal on the 'CX' Pin. The bit pattern is the same as that of the Enable Overlap Register above. This register is reset when read.

The Control Status Word is used to determine the chip status and interrupt sources. The bit pattern is as follows:

Bit 0 - Horizontal Status - Starts 20 µs before Horizontal blank starts. Ends 5 µs before Horizontal blank ends.

Bit 1 - Position Strobe Status - Status of X-Y Register strobe '1' = Follow Beam Location Ctr, '0' = latched. (See note on page 14)

Bit 2 - Sound Needs Service - Sound register empty

Bit 3 - Vertical Status = Vertical Blanking

Bit 4 - N/C

Bit 5 - N/C

Bit 6 - External Chip Overlap Interrupt - Set when an overlap occurs with signal on 'CX' Pin.

Bit 7 - Major System Overlap - Set when the chip attempts to load major system shift register if shift register already has one. The status register bits 2, 6 and the interrupt flip flop are cleared by reading the status reg. The overlap status register is cleared when read.

SYNC GENERATOR

The sync generator operates as a non-addressable autonomous circuit block within the 8245. As such, it provides a source for synchronizing signals both for internal use by the 8245 circuitry and for transmission to external circuitry. Externally the signal becomes processed with the color, luminance, and sound signals and ultimately results in synchronization of the associated TV receiver.

The manner in which the signals are utilized is determined by the mode in which the 8245 operates in a particular configuration. In a small system, utilizing a single 8245, it is operated in the Master Mode. The signals from the sync generator
drive both the display circuitry on the 8245 and also exit the chip, via appropriate pins, to drive the external circuitry. The external logic and the 8245 sync logic together generate sync signals compatible with CCI standards.

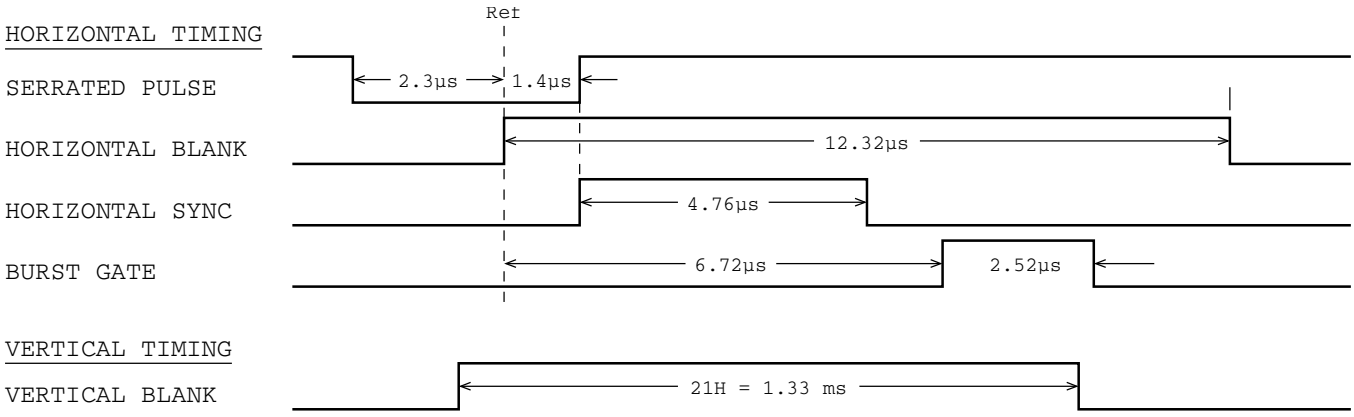
In larger system configurations, where the need for more than one 8245 exists, a single 8245 is designated the Master, as previously described. In addition, one or more 8244's are used as Slave Mode devices by connecting their M/S pins to Vss. The sync generator on a Slave Mode device is free to run but the output is not utilized outside the chip.

In Master Mode operation the sync generator signals used internally by the 8245 are horizontal blanking (HBL) and vertical blanking (VBL). Correspondingly, these two signals provide outputs along with horizontal sync (HSYNC) and color burst gate (BG). In Slave Mode operation the 8244 received only HBL and VBL from a Master Mode 8245.

The sync generator in conjunction with external logic provides non-interlaced synchronizing signals. It operates from a frequency of 3.54 Mhz. This clocking signal is divided by a factor of 227.0 in order to obtain the horizontal line frequency of 15,625 Hz.

In conjunction with external circuitry the horizontal line frequency is divided by a factor of 313 or 312 to produce the vertical sync frequency of 49.92 Hz. In the following timing diagrams, those signals shown under Horizontal Timing are reproduced at the 15,625 Hz rate, while the signals shown under Vertical Timing are reproduced at the 49.92 Hz or 50.08 Hz rate. Horizontal Blanking Burst Gate, and Horizontal Sync are generated during all portions of the vertical timing sequence. Vertical Interrupts are not generated within the 8245, although the vertical status bit is set during Vertical Blanking.

SYNC GENERATOR



ADDRESS STRUCTURE

The subfunction blocks within the 8244 may be individually addressed for the writing and in some cases, the reading of data. The addressing structure of these blocks is shown below:

CAM AND LINEAR SELECT STORE

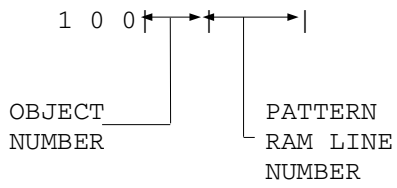
ADDRESS			SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0			
0	Object Number	0 0	LINE CAM (Y CAM)
0		0 1	DOT CAM (X CAM)
0		1 0	LSS BITS 0-7
0		1 1	LSS BITS 8-11

Note: For the Minor System LSS Bits 0-7 are attribute bits stored in the Attribute register.

ADDRESS STRUCTURE

MINOR SYSTEM PATTERN RAM

ADDRESS	SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0	PATTERN RAM



MISCELLANEOUS REGISTERS

ADDRESS		SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0		
1 0 1 X 0 0 0 0		CONTROL
	0 0 0 1	CONTROL STATUS
	0 0 1 0	OVERLAP STATUS AND OVERLAP ENABLE
	0 0 1 1	COLOR LATCH
	0 1 0 0	Y REGISTER
	0 1 0 1	X REGISTER
	0 1 1 0	NA
	0 1 1 1	SOUND 0
	1 0 0 0	SOUND 1
	1 0 0 1	SOUND 2
	1 0 1 0	SOUND STATUS

GRID

ADDRESS		SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0		
1 1 0 0	column number	HORIZONTAL SEGMENTS 0 to 7,
1 1 0 1		HORIZONTAL SEGMENTS 8
1 1 1 0		VERTICAL SEGMENTS

READ AND WRITE CAPABILITY:

READ/WRITE: ALL CAM
ALL LINEAR STORE EXCEPT MINOR SYSTEM
GRID RAM
MINOR SYSTEM PATTERN RAM
CONTROL REG.
SOUND STATUS REG.

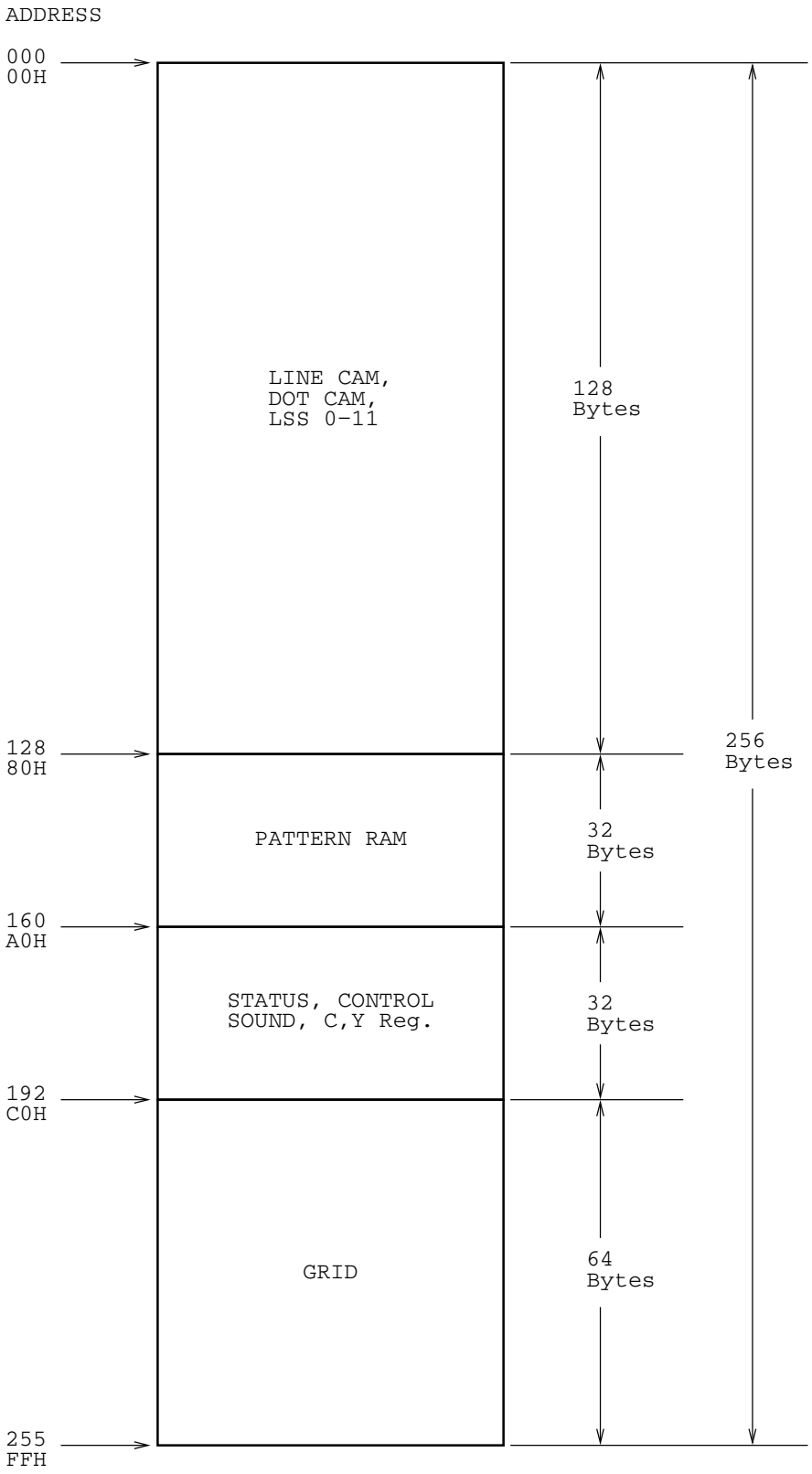
ADDRESS STRUCTURE

READ ONLY: X-REG
Y-REG
OVERLAP STATUS REG
CONTROL STATUS REG

WRITE ONLY: MINOR SYSTEM LINEAR STORE (ATTRIBUTE REG)
COLOR LATCH
ENABLE OVERLAP
SOUND REGS 0, 1, 2

ADDRESS STRUCTURE

The addressable function block structure may be shown by means of an overview address map as follows:



REGISTER ADDRESS

		CONTROL	CONTROL STATUS	OVERLAP STATUS ENABLE OVERLAP	Y REGISTER	X REGISTER
		A0	A1	A2	A4	A5
	7	Grid Width 1 = Wide	Major with Major	Major with minor or grid	MSB	MSB
BITS	6	Dot Enable	Ext. Chip Overlap*	External Chip		
	5	Enable Display	————	Horiz Grid		
	4	Enable Ext. Overlap	————	Vert Grid		
	3	Enable Grid	Vert. Status (V.B)	Minor Sys 3		
ENABLE	2	Enable Sound Int.	Sound Needs Service*	Minor Sys 2		
GRID	1	Forced Pos. Strobe*	Position Strobe Status*	Minor Sys 1		
	0	Enable Horiz. Int.	Horiz. Status*	Minor Sys 0	LSB	LSB

* Explained Below

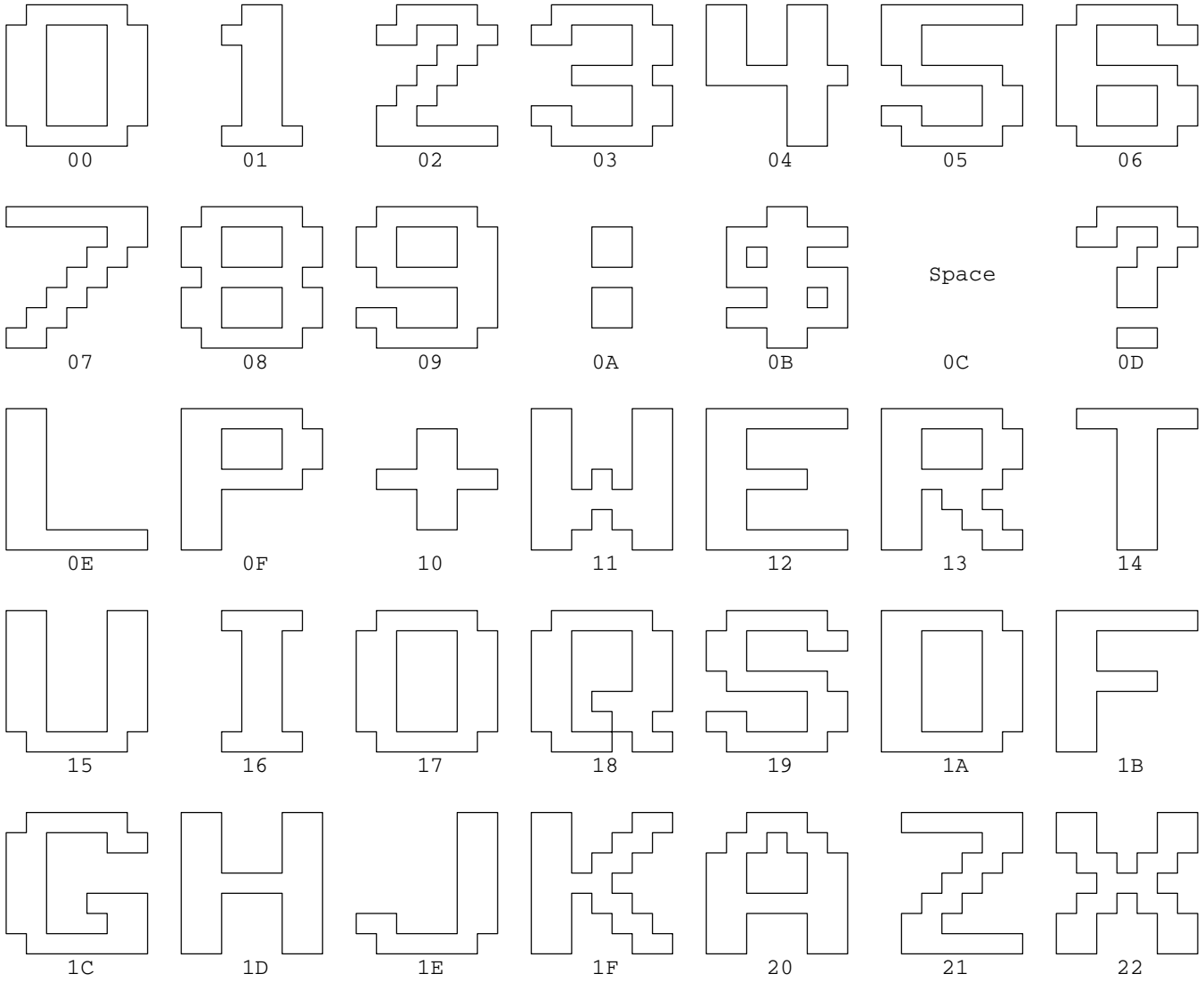
Forces Position Strobe: Bit = 1 Strobes beam location to X - Y registers. Bit = 0 Disables strobe.

External Chip Overlap: Set when an overlap occurs with signal on CX Pin.

Sound Needs Service: Sound register has been shifted out.

Position Strobe Status: Ored of strobe and Forced position strobe.

Horizontal Status: Starts 20 usec. before leading edge of horizontal blanking and ends 5 usec before lagging edge of Horizontal blanking.



Rom Character Set Final Version

10/13/7?

- missing -