

STD X – Trade Theory Electronics

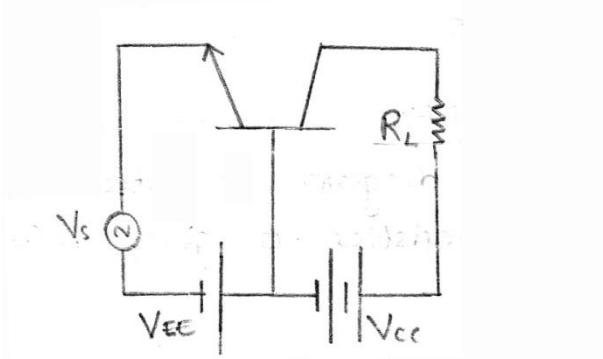
Module - 1

Transistor Configurations

A transistor can be used as an amplifier when biased to operate in the active region. An amplifier needs four terminals for its operation two for applying input and two for taking output. But a transistor has only three terminals. Therefore, to work as an amplifier, one terminal has to be made common for both input and output. Accordingly, there can be three transistor configurations or connections namely.

- 1) Common base (CB) configuration.
- 2) Common Emitter (CE) configuration.
- 3) Common collector (CC) configuration.

CB Configuration



In this configuration, input terminal is emitter and output terminal is collector.

input current - I_E

input voltage - V_{EB}

output voltage - I_C

output voltage - V_{CB}

Current relation in CB configuration

Current relation equation in CB configuration is given by,

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

Here, α_{dc} is dc current gain in CB configuration. I_{CBO} is reverse leakage current in CB configuration. I_{CBO} is very small and can be neglected.

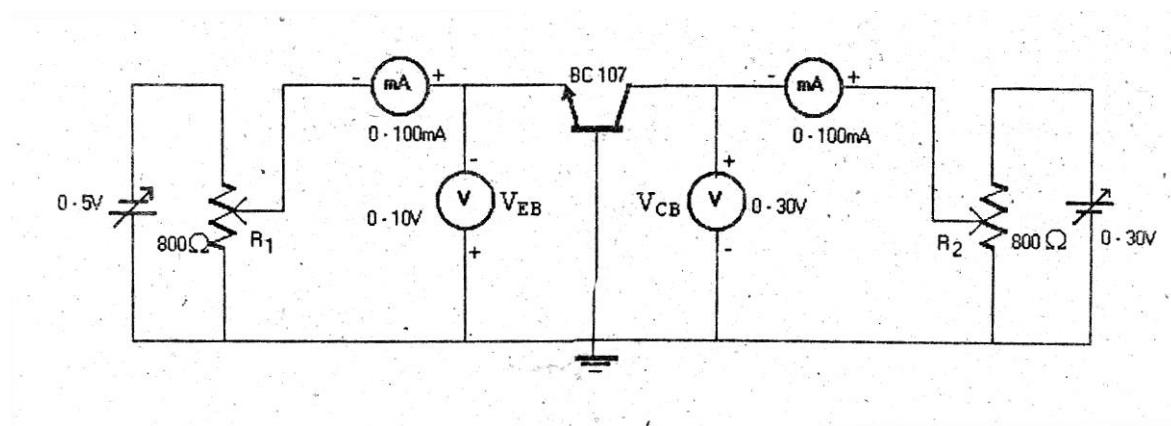
Then equation becomes,

$$I_C \approx \alpha_{dc} I_E$$

$$\text{Then } \alpha_{dc} = \frac{I_C}{I_E}$$

CB Characteristics

The circuit diagram to obtain common base characteristics is give below.

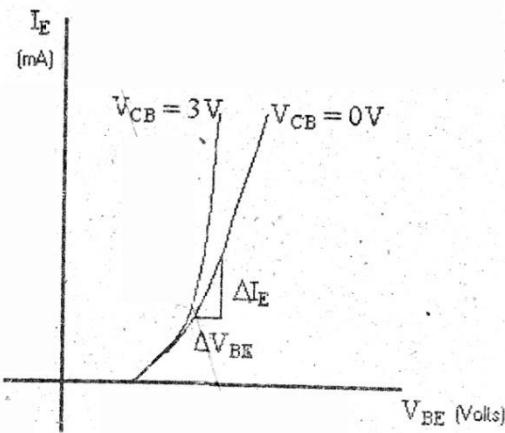


There are two types of characteristics for a transistor in CB configuration. They are:

- 1) Input characteristics
- 2) Output characteristics

Input characteristics

Input characteristics is a graph between input voltage V_{EB} and input current I_E for constant values of output voltage V_{CB} .



- There exist a cut in value of V_{EB} above which the value of emitter current increases rapidly.
- If we increase the value of V_{CB} , keeping V_{EB} constant, the value of I_E slightly increases.

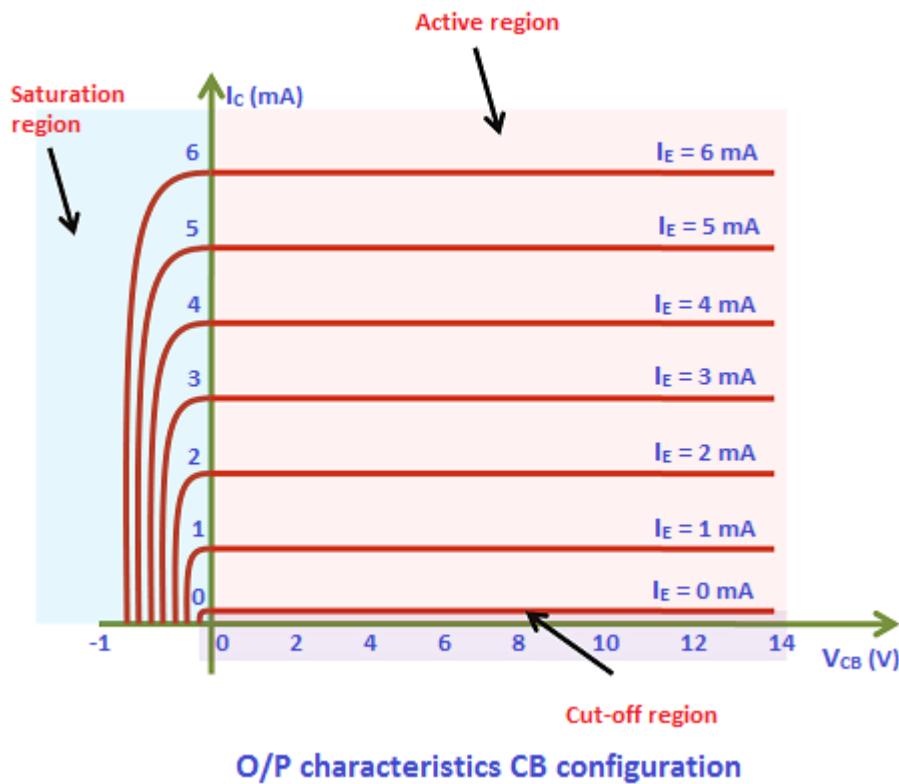
Dynamic or ac Input Resistance

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} / V_{CB} = \text{constant}$$

Dynamic input resistance (r_i) is given by the ratio of change in emitter – base voltage to the corresponding change in emitter current at constant collector – base voltage. Its value is very low and ranges from 20Ω to 100Ω .

Output characteristics

Output characteristics of a transistor in CB configuration is a graph between output voltage (V_{CB}) and output current (I_C) for constant values of input current (I_E).



The output characteristics may be divided into three distinct regions. They are :

- 1) Active region
- 2) Cut-off region
- 3) Saturation region

Active region

The region right side to the Y-axis and above $I_E=0$ characteristic curve where emitter-base junction is forward biased and collector-base junction is reverse biased is called active region.

In this region, the output current I_C remains almost constant but slightly increases with increase in V_{CB} . ie , Here transistor acts as a constant current source. In this region, output current I_C depends on input current I_E and transistor works as an amplifier.

Cut – off region

The region right side to the Y-axis and below $I_E=0$ characteristics curve where both emitter and collector junctions are reverse biased is called cut-off region.

In this region, collector current has a very small value called I_{CBO} . Transistor acts as an electronic switch in OFF condition.

Saturation region

The region left side to the Y-axis where both the emitter and collector junctions are forward biased is called saturation region.

In this region, if V_{CB} is made slightly negative, the value of I_c decreases sharply. If V_{CB} is made equal to the cut-in voltage value, the current I_c increases in the negative direction. Here, I_c does not depends upon I_E . In this region, transistor acts as an electronic switch in ON condition.

Dynamic output resistance (r_o)

$$r_o = \frac{\Delta V_{CB}}{\Delta I_c} / I_E = \text{constant}$$

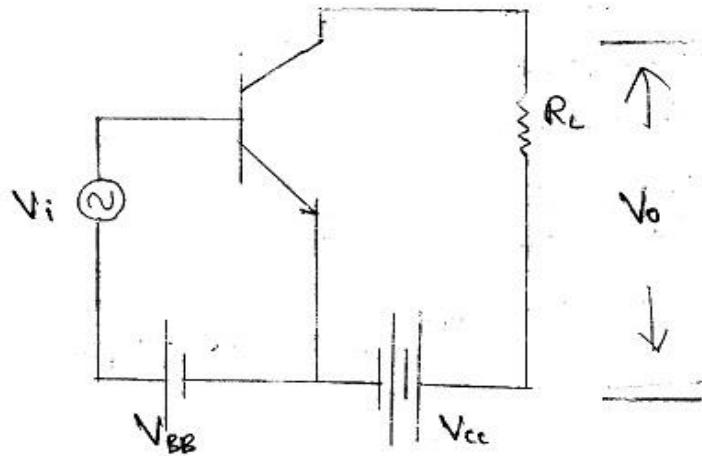
The value of r_o is very high. Its value is about $500 \text{ k}\Omega$.

AC current gain (α)

$$\alpha = \frac{\Delta I_c}{\Delta I_E} / V_{CB} = \text{constant}$$

The value of α is about 0.99

CE configuration



Here, input terminal is base and output terminal is collector.

input current – I_B

input voltage – V_{CB}

output current – I_C

output voltage - V_{CE}

Current relation in CE configuration

We know, for a transistor,

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad \longrightarrow \quad (1)$$

$$I_E = I_C + I_B \quad \longrightarrow \quad (2)$$

substituting equation(2) in equation(1)

$$I_C = \alpha_{dc} (I_C + I_B) + I_{CBO}$$

$$I_C = \alpha_{dc} I_C + \alpha_{dc} I_B + I_{CBO}$$

$$\text{ie, } I_C - \alpha_{dc} I_C = \alpha_{dc} I_B + I_{CBO}$$

$$I_C (1 - \alpha_{dc}) = \alpha_{dc} I_B + I_{CBO}$$

$$\text{Therefore } I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}} \quad \longrightarrow \quad (3)$$

The above equation may be simplified by defining,

$$\frac{\alpha_{dc}}{1-\alpha_{dc}} = \beta dc$$

and

$$\frac{I_{CBO}}{1-\alpha_{dc}} = I_{CEO}$$

Then equation (3) becomes,

$$I_C = \beta_{dc} I_B + I_{CEO} \quad \longrightarrow (4)$$

Here, β_{dc} is dc current gain in CE configuration and I_{CEO} is reverse leakage current in CE configuration.

Equation (4) can be written as

$$I_C \approx \beta_{dc} I_B \quad (I_{CEO} \text{ being a small quantity, can be neglected}).$$

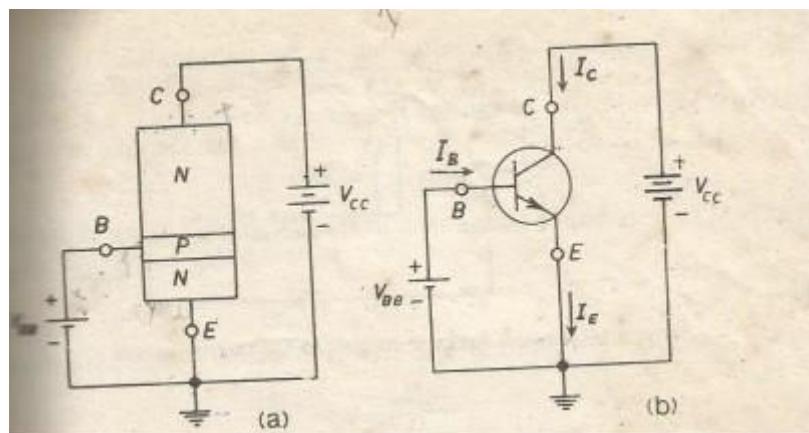
$$\text{Then } \beta_{dc} = \frac{I_C}{I_B}$$

AC current gain (β)

$$\beta = \frac{\Delta I_C}{\Delta I_B} / V_{CE} = \text{constant}$$

The value of β is high and ranges from 20 to 300

Common Emitter Biasing Arrangement



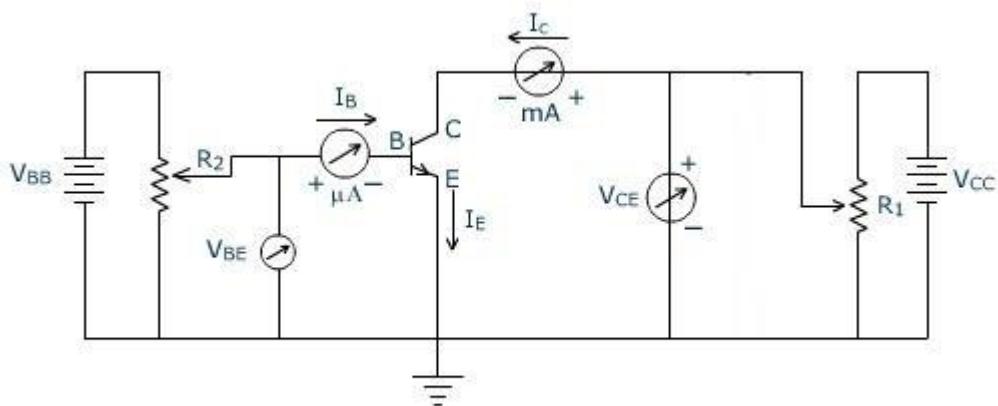
Here, emitter – base junction is forward biased by the battery potential V_{BB} and collector- base junction is reverse biased by the potential $V_{CC} - V_{BB}$

That is, in this configuration,

$$V_{CB} = V_{CE} - V_{BE}$$

CE characteristics

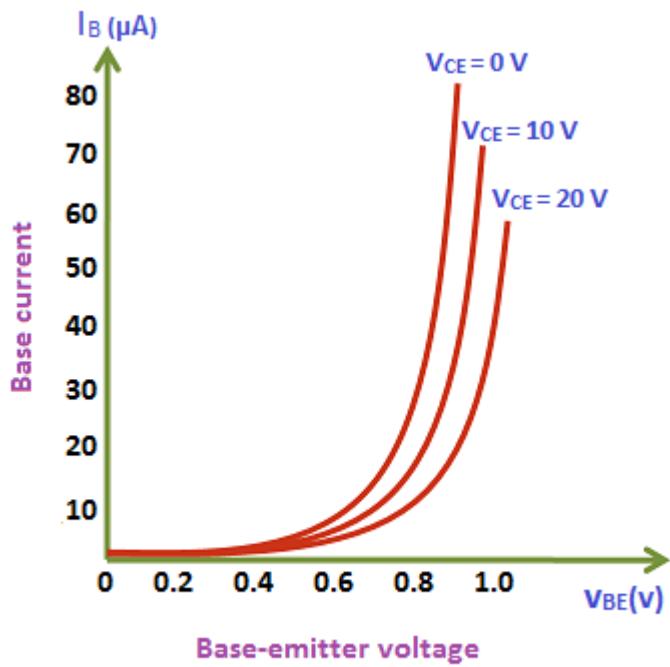
The circuit diagram to obtain CE input and output characteristics is given below.



Circuit for obtaining the characteristics of a npn transistor

Input Characteristics

Input characteristics in CE configuration is a graph between V_{BE} and I_B for constant values of V_{CE}



I/P characteristics CE configuration

- There exist a cut-in value of V_{BE} above which I_B increases rapidly. But here, as compared to CB configuration, I_B increases less rapidly with V_{BE} .
- If we increase the value of V_{CE} keeping V_{BE} constant, I_B decreases. (if V_{CE} increased, the width of depletion region at the collector-base junction increases. This decreases the effective width of base region. Hence the number of recombinations and base current decreases.

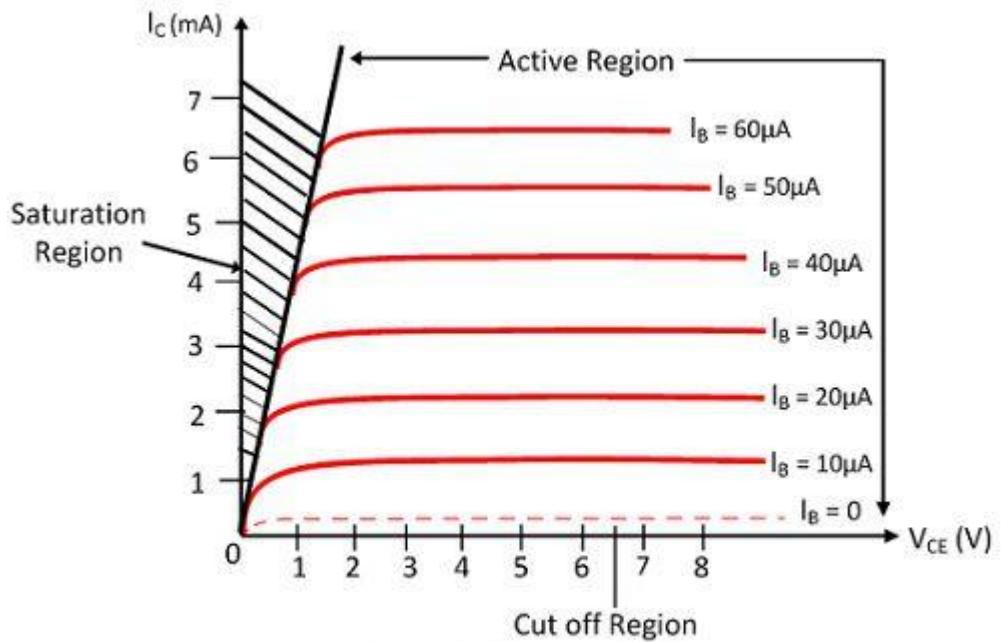
Dynamic input resistance (r_i)

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} / V_{CE} = \text{constant}$$

The value of r_i is low and ranges from 750Ω to $3 K \Omega$

Output characteristics

Output characteristics of transistor in CE configuration is a graph between V_{CE} and I_C for constant values of I_B .



Output Characteristic Curve

Circuit Globe

Output characteristics can be divided into three regions, namely,

- 4) Active region
- 5) Cut-off region
- 6) Saturation region

Active region

The region right side to the line $V_{CE} = \text{a few tenths of a volt}$ and above I_B characteristic curve where emitter-base junction is forward biased and collector – base junction is reverse biased is called active region.

In this region, the output current I_C remains almost constant but slightly increases with increase in V_{CE} . That is, in this region transistor acts like a constant current source. Here output current I_C depends on input current I_B . In this region, transistor works act as an amplifier.

Cut – off region

The region right side to the Y-axis and below $I_B=0$ characteristics curve where both emitter and collector junctions are reverse biased is called cut-off region.

In this region I_C has a small value equal to I_{CEO} . In this region, transistor act as an electronic switch in OFF condition.

Saturation region

The region left side to the V_{CE} a few tenths of volt and right side to the Y-axis where both the emitter and collector junctions are forward biased is called saturation region.

In this region I_C does not depends on I_B . In this region, transistor works as an electronic switch in ON condition.

Dynamic output resistance (r_o)

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} / I_B = \text{constant}$$

The value of r_o is high and typical value is $50 \text{ K } \Omega$

CC configuration

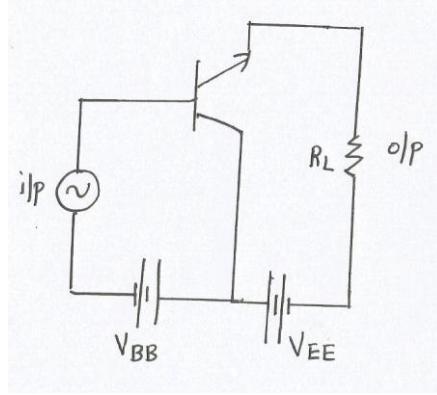
In this configuration, input terminal is base and output terminal is emitter.

input current – I_B

input voltage – $-V_{BC}$

output current - I_E

output voltage - V_{EC}



NPN transistor connected in CC configuration

Current relation in CC configuration

We know, for a transistor

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad \longrightarrow \quad (1)$$

$$I_E = I_C + I_B \quad \dots \quad (2)$$

$$\text{ie, } I_C = I_E - I_B$$

Using this relation in equal (1), we get

$$I_E - I_B = \alpha_{dc} I_E + I_{CBO}$$

$$\text{ie, } I_E - \alpha_{dc} I_E = I_B + I_{CBO}$$

$$I_E (1 - \alpha_{dc}) = I_B + I_{CBO}$$

$$\text{ie, } I_E = \frac{I_B}{1 - \alpha_{dc}} + \frac{I_{CBO}}{1 - \alpha_{dc}}$$

$$\text{ie } I_E = \frac{1}{1 - \alpha_{dc}} I_B + \frac{I_{CBO}}{1 - \alpha_{dc}}$$

The above equation may be simplified by defining $\frac{1}{1 - \alpha_{dc}} = \gamma_{dc}$ and $\frac{I_{CBO}}{1 - \alpha_{dc}} = I_{CEO}$

Then equation becomes,

$$I_E = \gamma_{dc} I_B + I_{CEO}$$

Here, γ_{dc} is dc current gain in CC configuration and I_{CEO} is leakage current in CC configuration.

$$\gamma_{dc} = \frac{I_E}{I_B}$$

The value of γ_{dc} is very high and ranges from 20 to 300.

Relation between γ_{dc} and β_{dc}

$$\beta_{dc} + 1 = \frac{\alpha_{dc}}{1 - \alpha_{dc}} + 1$$

$$= \frac{\alpha_{dc} + 1 - \alpha_{dc}}{1 - \alpha_{dc}}$$

$$= \frac{1}{1 - \alpha_{dc}} = \gamma_{dc}$$

$$\text{i.e., } \gamma_{dc} = \beta_{dc} + 1$$

α_{dc} in terms of β_{dc}

We know,

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

$$\text{i.e., } \beta_{dc} (1 - \alpha_{dc}) = \alpha_{dc}$$

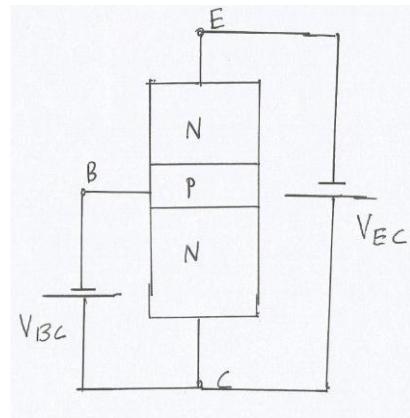
$$\beta_{dc} - \beta_{dc} \alpha_{dc} = \alpha_{dc}$$

$$\text{i.e., } \beta_{dc} = \alpha_{dc} + \beta_{dc} \alpha_{dc}$$

$$\beta_{dc} = \alpha_{dc} (1 + \beta_{dc})$$

$$\text{i.e., } \alpha_{dc} = \beta_{dc} / (1 + \beta_{dc})$$

Common Collector Biasing Arrangement

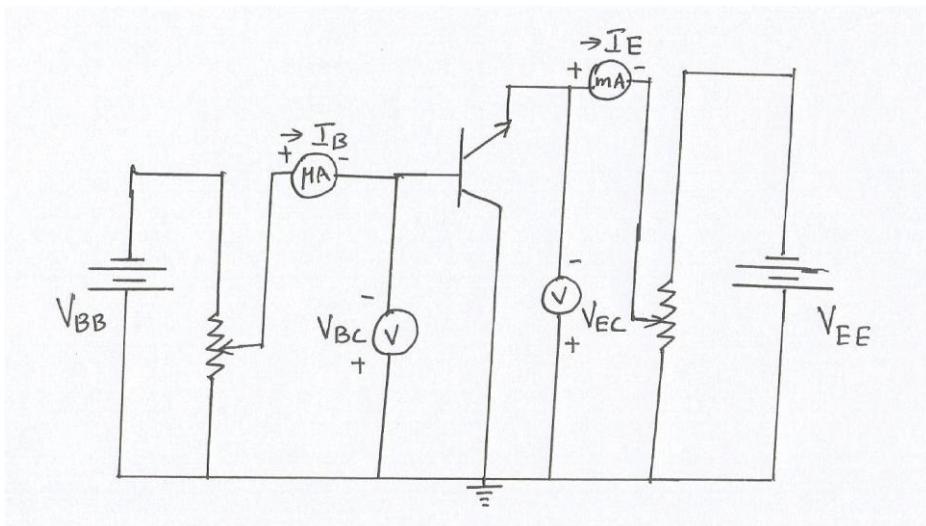


In this configuration, the input side (base –collector side) is reverse biased by the potential V_{BC} and the emitter – base junction is forward biased by the potential.

$$V_{EB} = V_{EC} - V_{BC}$$

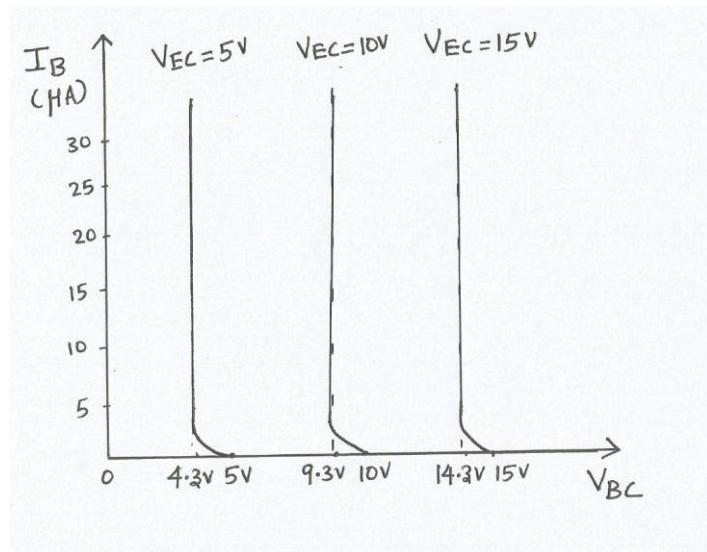
Common collector characteristics

Circuit diagram to obtain CC characteristics is given below.



Input characteristics

Input characteristics in CC configuration is a graph between V_{BC} and I_B for constant values of V_{EC} .



The o/p current I_B depends on the voltage V_{EB} . For I_B to be a large value, V_{EB} should be in the range from 0.5v to 0.7 v.

V_{EB} can be calculated by using the equation.

$$V_{EB} = V_{EC} - V_{BC}$$

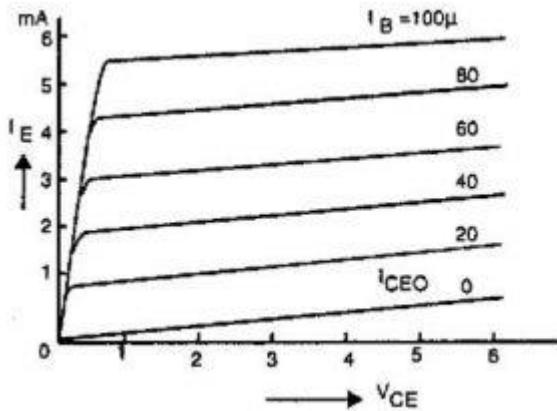
Consider the characteristic curve for $V_{EC} = 5v$. Here, if we increase the value of V_{BC} to a value more than 4.3v, the value of V_{EB} decreased below 0.7v and due to which I_B decreases. Finally, if V_{BC} and hence I_B becomes 0.

In CC configuration, the i/p side (base-collector junction) is reverse biased. Therefore, the input resistance r_i will be very high. Typical value is $750 \text{ K } \Omega$.

Output characteristics

Output characteristics in CC configuration is a graph between V_{EC} and I_E for constant values of I_B .

Compared to CE configuration, the only difference here is that I_E is shown along Y-axis instead of I_C . But we know, for a transistor, I_E approximately equals I_C . Therefore the output characteristics in CC configuration will be very similar to that in CE configuration.



In CC configuration, the output side is forward biased. Therefore, output resistance is very low. Typical value is 50Ω .

Comparison of three transistor configuration

No.	Parameters	CB	CE	CC
1.	Input resistance	Very low ($20-100 \Omega$)	Low ($750 \Omega - 3 K\Omega$)	Very high (about $750 K\Omega$)
2.	Output resistance	Very high (about $500K\Omega$)	High ($50K\Omega$)	Very low (about 50Ω)
3.	Current gain	Very low (α is less than unity)	High (β Ranges from 20-300)	Very high (γ Ranges from 20-300). $\gamma = \beta + 1$
4.	Voltage gain	High (about 150)	Very high (about 500)	Very low (less than unity)
5.	Leakage current	Very low (Typical value of $I_{CBO} = 1 \mu A$)	low (Typical value of $I_{CEO} = 100 \mu A$)	low (Typical value of $I_{CEO} = 100 \mu A$)
6.	Application	For high frequency application	For audio frequency application	As buffer amplifier

Reason for low voltage gain in CC configuration

In CC configuration, negative feedback occurs. Due to the effect of negative feedback, voltage gain will be very low. The phenomenon of reducing input voltage due to the effect of output voltage is called negative feedback.

Reason for the popular usage of CE configuration in amplifier

CE configuration is commonly used in amplifier. Reason are :

- High current gain
- High voltage gain
- High power gain
- Moderate output to impedance ratio- Output impedance to input impedance is moderate (about 50). This makes the circuit arrangement an ideal one for coupling between various transistor amplifier stages.

1. For a transistor $I_E = 10\mu A$. Find the values of I_C , α , β and γ .

Ans: $I_E = 10\mu A$

$$I_E = 10\mu A = 0.1MA$$

$$I_E = I_C + I_B$$

$$\text{Therefore, } I_C = I_E - I_B = 10 - 0.1$$

$$9.9 MA$$

$$\alpha = \frac{I_C}{I_E}$$

$$= \frac{9.9}{10} = .99$$

$$\beta = \frac{I_C}{I_B}$$

$$= = \frac{9.9}{0.1}$$

$$= 99$$

$$\gamma = \beta + 1 =$$

$$99 + 1 = 100$$

Buffer amplifier

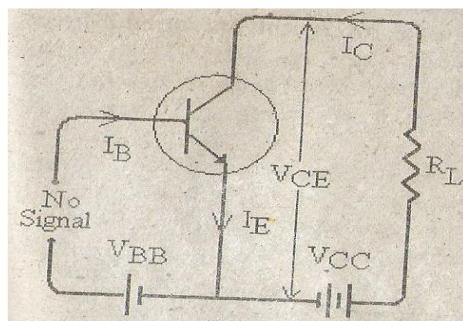
Buffer amplifier is connected in between two power amplifier stages to achieve impedance matching. So that maximum power can be transferred from the output of one power amplifier to the input of next power amplifier.

Need for biasing

- To fix the operating point at the centre of active region.
- To stabilize the operating point against temperature variations.
- To stabilize the operating point against transistors parameter variations.

Operating point : Zero signal values of collector current (I_C) and collector voltage (V_{CE}) for a transistor is called operating point or quiescent point (Q point)

DC load line



A biasing circuit to set the operating point within the active region is shown above.

Applying KVL to the output side, we get

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\text{ie, } V_{CE} = V_{CC} - I_C R_C$$

The above equation is a first degree equation and can be drawn as a straight line on the output characteristics. To draw the straight line, we have to find out two end points.

Let, $I_C = 0$

Then, $V_{CE} = V_{CC}$

Therefore one end point is $(V_{CC}, 0)$ on the x – axis.

To find the other end point,

let, $V_{CE} = 0$

Then, $0 = V_{CC} - I_C R_C$

Therefore the other end point is $(0, \frac{V_{CC}}{R_C})$ on the y-axis.

The straight line joining these two end points $(V_{CC}, 0)$ and $(0, \frac{V_{CC}}{R_C})$ on the characteristics is called dc load line.

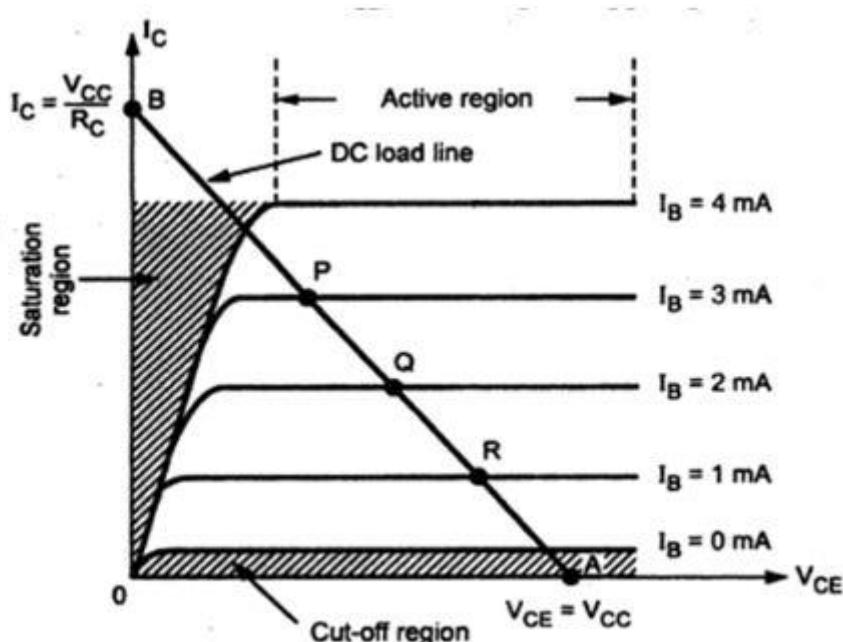


Fig 3.5: Common emitter output characteristics with d.c. load line

The operating point will always lie on DC load line. The exact position of operating point will be at the intersection of dc load line and the collector curve corresponding to a particular have current .

When an AC signal is applied, the position of operating point will shift along the load line.

If the operating point is fixed at the centre of dc load line (point Q), the operating point will always lie with the active region during the entire cycle of input signal. Then faithfull amplification can be achieved.

If operating point is fixed near to saturation point (point P), the transistor may go into saturation region during the positive peak of input signal. These distortion will occur. Then positive half cycle will be clipped .

If the operating point is fixed near to cut-off point(point R), the transistor may go into cut-off region during the negative peak of input signal. Then also distortion will occur- ie , negative half of output may be clipped. ie, For faithful amplification, mid-point biasing (operating point at the centre of dc load line) is preferred.

Stabilization

The process of making operating point independent of temperature variations or transistors parameter variations is known as stabilization.

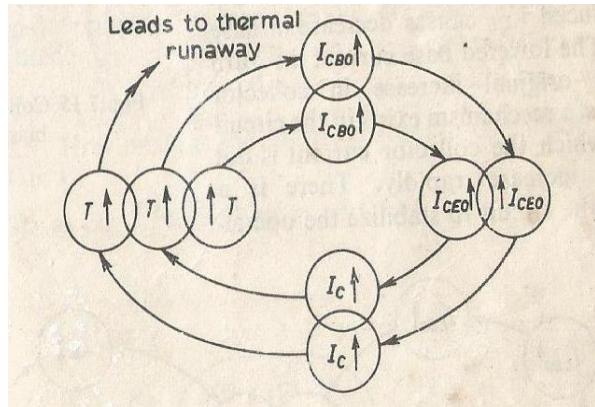
Need for stabilization

Stabilization of operating point is necessary due to the following reasons :

- Temperature dependence of I_C - the collector current I_C is given by $I_C = \beta I_B + I_{CEO}$. When temperature increase, the leakage currents I_{CBO} I_{CEO} increases . Then collector current I_C increases. Thus the position of operating point changes.
- Transistor parameter variations – The values of transistor parameters such as β and V_{BE} are not exactly the same for any two transistors even of the same type.

When a transistor is replaced by another of the same type, these variations change the operating point.

- Thermal runaway – The self destruction of an unstabilized transistor is known as thermal runaway.



Stability factor

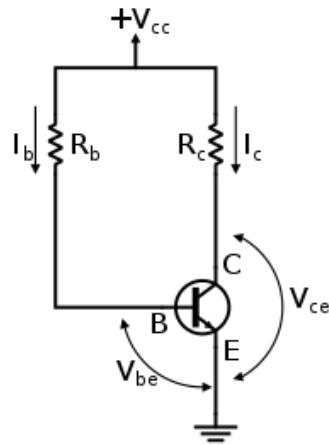
The rate of change of collector current I_C with respect to the collector leakage current I_{CO} at constant β and I_B is called stability factor.

i.e, stability factor, $s = \frac{dI_C}{dI_{CO}}$ at constant β and I_B

In order to achieve greater thermal stability, it is desirable to have a low stability factor as possible.

Different Biasing circuits

- 1) *Fixed bias circuit (base resistor method)*



In this circuit, a high value resistor R_B is connected between base and +ve end of supply and a low value resistor R_C is connected between collector and +ve end of supply. By this connection, the emitter-base junction is forward biased and collector-base junction is reverse biased. The required value of zero signal base current I_B and hence I_C can be made to flow by fixing a proper value of base resistor R_B .

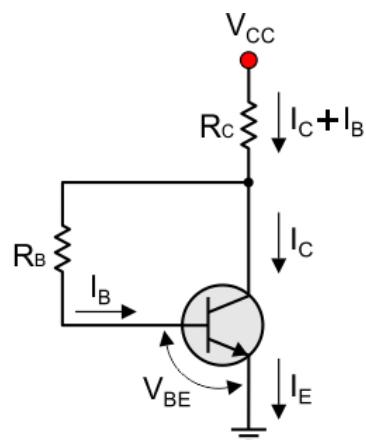
Advantages

- The biasing circuit is very simple .
- The circuit is compact and has low cost.
- Biasing conditions can be easily set.

Disadvantages

- The circuit provides no stabilization.
- Stability factor is very high. Therefore, there are strong chances of thermal runaway.

2) Collector to base feedback biasing circuit



In this circuit, the base resistor R_B is connected to the collector instead of connecting it to the positive end of supply V_{CC} .

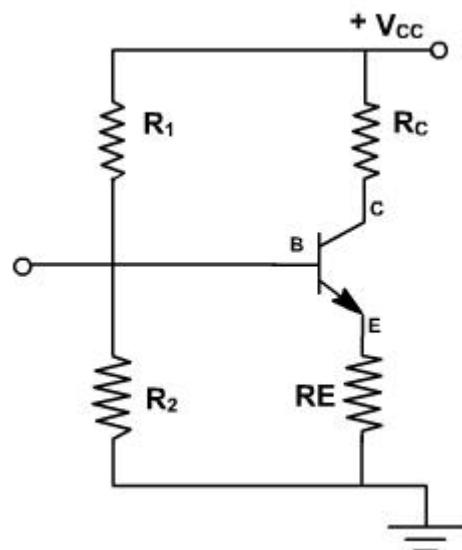
Advantages

- The biasing circuit is very simple.
- The circuit is compact and has low cost.
- Biasing conditions can be easily set.
- Circuit provides some stabilization of operating point.

Disadvantages

- The circuit does not provide good stabilization especially against transistor parameter variations.
- The circuit provides negative feedback and due to which gain will be low when used in amplifier.

3) Voltage divider biasing circuit



In this circuit, two resistors R_1 and R_2 are connected across the supply voltage V_{CC} and provide biasing. The name voltage divider comes from the voltage divider network formed by R_1 and R_2 forward biases the base-emitter junction. This causes the base current and hence collector current to flow in the circuit.

Circuit analysis

Suppose that the current flowing through resistance R_1 is I_2 . As base current. I_B is very small, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1

$$\text{The current } I_1 = \frac{V_{CC} -}{R_1 + R_2}$$

therefore voltage drop across resistor R_2

$$V_2 = I_1 \cdot R_2$$

$$= \frac{V_{CC} -}{R_1 + R_2} \cdot R_2$$

Applying KVL to the base circuit we get

$$V_2 - V_{BE} - I_E R_E = 0$$

Therefore

$$I_E R_E = V_2 - V_{BE}$$

Therefore

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \approx I_C$

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$

Here V_{BE} is very small quantity and if it is neglected, equation becomes

$$I_C \approx \frac{V_2 -}{R_E}$$

From the above equation, it is clear that I_C does not at all depend upon β . Though I_C depends upon V_{BE} , in practice since V_B is very small compared to V_2 , I_C is practically independent of V_{BE} . Thus I_C in this circuit almost independent of transistor parameters and hence good stabilization is ensured.

Applying KVL to the output side

$$\begin{aligned} V_{CC} &= I_C R_C + V_{CE} + I_E R_E \\ &= V_{CE} + I_C R_C + I_C R_E \quad (\text{therefore } I_E \approx I_C) \\ &= V_{CE} + I_C (R_C + R_E) \end{aligned}$$

$$\text{Therefore } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilization in this circuit

Consider the equation

$$V_2 = V_{BE} + I_E R_E$$

$$V_2 = V_{BE} + I_C R_E \quad (\text{since } I_E \approx I_C)$$

Suppose that collector current I_C increases due to the rise in temperature. This will cause the voltage drop across emitter resistor R_E to increase. Since V_2 is a constant, the value of V_{BE} decreases. This causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Advantages

- We can easily fix the operating point at the centre of active region.
- Circuit provides very good stabilization against temperature and transistor parameter variations.
- Stability factor is very low.

Disadvantages

- If capacitor is not connected in parallel with R_E , due to negative feedback voltage gain will be low.

Voltage Amplifier Using Transistor

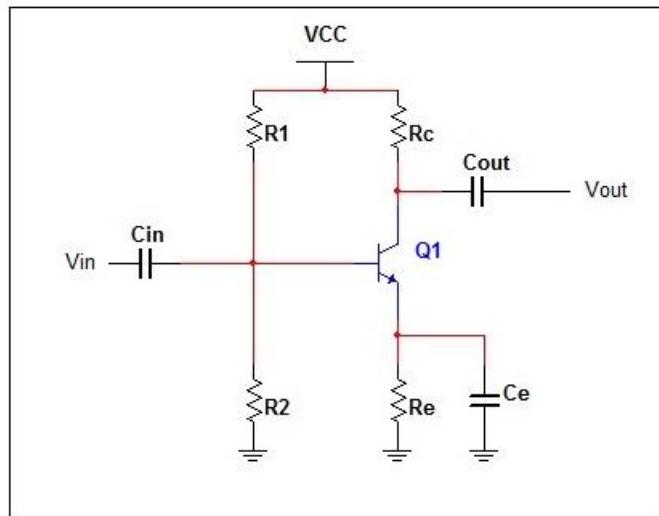


Fig 15 voltage amplifier

The various circuit element and their functions are given below:-

Voltage divide biasing Circuit

Voltage divide biasing circuit is used to fix the operating point at the centre of active region and to provide good stabilization.

1. Input Capacitor (Cin)

Cin is used to couple AC input signal to the base of the transistor. It allows only AC signals to flow and blocks DC component. If it is not used, the signal source resistance Rs will come across R2 and thus change the bias.

2. Emitter bypass Capacitor.

Cin is used in parallel with RE to provide a low reactance path to the amplified AC signal. If it is not used, then the amplifier AC signal flowing through RE will cause a voltage drop across it, thereby reducing the output voltage (ie AC negative feedback will occur).

3. Coupling capacitor

Coupling capacitor is used to couple AC signal from one stage of amplification to the next stage. If it is not used, Rc will come in parallel with R1 of the next stage, thereby altering the biasing condition of the next stage, ie the coupling capacitor Cc isolates dc of one stage from the next stage, but allows the passage of ac signal.

Working Of The Voltage Amplifier

Transistor is biased to operate in the active region by using voltage divider biasing circuit. It also provides stabilization to the operating point.

The signal to be amplified is connected to the base circuit. Then the base - emitter voltage V_{BE} varies with time. As a result , the input current I_B also varies with time. In the active region I_C depends on input current I_B . Therefore a similar variation occurs in the collector current. This varying collector current passes through the resistor R_C and varying voltage is developed across it. This varying voltage is the output voltage V_o . The output voltage V_o is many times greater then input voltage V_s . The amplification can be illustrated as given below.

Assume that input signal voltage is 20mV. Let the collector current variation is 0.5mA.

Then the output voltage is

$$V_o = I_C R_C \text{ if } R_C = 5k\Omega \text{ then}$$

$$V_o = 0.5 \text{ mA} \times 5k\Omega = 2.5 \text{ V}.$$

Then voltage gain

$$A_v = \frac{V_o}{V_i} = \frac{2.5 \text{ V}}{20 \text{ mV}} = 125$$

Phase reversal in CE Single stage Voltage Amplifier

In common emitter connection, when the input signal voltage increases in the positive direction, the output voltage increases in the negative direction and vice versa. In other words, there is a phase difference of 180° between the input and output voltage in CE connection.

The phase difference of 180° between the signal voltage and output voltage in a common emitter single stage amplifier is known as phase reversal.

The value of V_{CE} is given by

$$V_{CE} = V_{CC} - I_C R_C$$

When the input signal voltage increases in the positive half cycle, the base current also increase. The result is that collector current and hence voltage drop $I_C R_C$ increases . As V_{CC} is constant, therefore output voltage V_{CE} decreases. In other words, as the signal voltage is increasing in the positive half cycle the out put voltage is increasing in the negative direction. ie output is 180° out of phase with the input.

Classification of Amplifiers

1. According to use- According to usage, amplifiers can be classified basically into voltage amplifier and power amplifier.
2. According to frequency range used - According to frequency range, amplifiers can be classified as audio amplifier and radio amplifier. Audio amplifier used to amplify signal within the range of 20Hz to 20KHz.
3. According coupling methods – depending upon the coupling device used, the amplifiers are classified as RC coupled amplifiers, transformer coupled amplifiers and direct coupled amplifiers.
4. According to the mode of operation- According to the mode of operation ,there are four types of amplifiers, They are Class A, Class B, Class AB, and class C amplifiers

Multistage transistor amplifier.

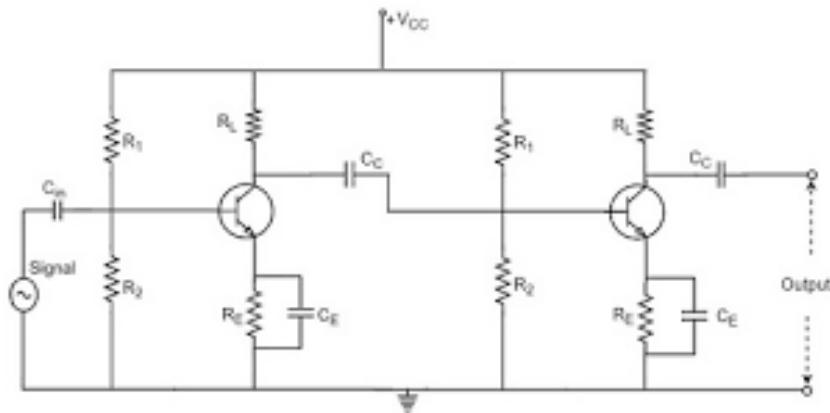
A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier.

In a multistage amplifier, a number of single amplifiers are connected in cascade arrangement ie, output of first stage to the input of the second stage through a suitable coupling device and so on.

- The purpose of coupling device is to transfer ac output of one stage to the input of the next stage.
- To isolate the dc conditions of the one stage from the next stage.

Types of multistage amplifiers

1. RC Coupled amplifier



Gain

The ratio of output electrical quantity to the input of the amplifier is called its gain.

The gain of multistage amplifier is equal to the product of gains of individual stages. For example if G_1 , G_2 and G_3 are the individual voltage gains of a three stage amplifier, then total voltage gain

$$G = G_1 \times G_2 \times G_3$$

Frequency response

The graph between voltage gain and signal frequency of an amplifier is known as frequency response.

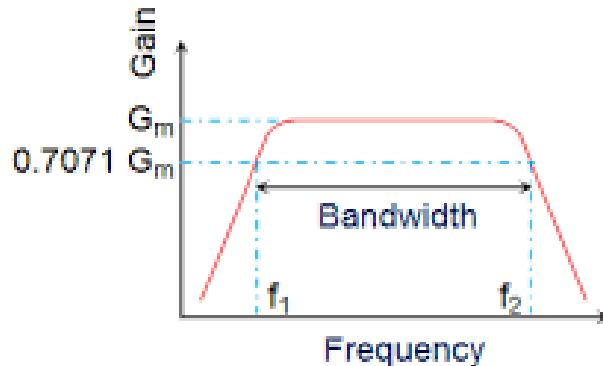


Figure 2 Frequency Response Curve of a RC Coupled Amplifier

As shown above, it is clear that the voltage gain reduces low (less than 50Hz) and high (grater than 20KHz). frequencies whereas it is uniform and high over the midfrequency range.

At low frequencies, the reactance of coupling capacitors becomes very high. Therefore a very small part of the signal will pass from one stage to next stage. Hence, output voltage and voltage gain decreases. At low frequencies the bypass capacitor C_E cannot bypass ac effectively because of its large reactance. Hence ac voltage will develops across R_E and negative feedback occurs due to which voltage gain decreases.

Fall of gain in high frequency range

When the frequency increase, the gain of the amplifier reduces. Several factors affect the reduction in gain. Firstly β of the transistor is frequency dependent. Its value decreases of high frequencies. Second factor is the inter electrode capacitances; these are inherently present in the device. The capacitance C_{bc} between the base and collector connects the output with the input. Because of this negative feedback takes place in the circuit and the gain decreases. The feedback effect is more in high frequencies. The capacitance C_{be} offers low impedance path at high frequencies in the input side. This reduces the input impedance and the affect input signal. Thus gain reduces. Similarly the capacitance C_{ce} produces a shunting effect at high frequencies in the output side. Besides the junction capacitances, there are wiring capacitance C_{w1} and C_{w2} due to the connection wires with air as dielectric, which also add with the inter electrode capacitances.

Decibel Gain

The unit assigned to the gain of an amplifier is bel or decibel. (dB)

The common logarithm (logarithm to the base 10) of power gain is known as bel power gain

$$\text{Power in bel} = \log_{10} \frac{P_{out}}{P_{in}} \text{ bel}$$

$$1 \text{ bel} = 10 \text{ dB}$$

$$\text{Power gain in dB} = 10 \log_{10} \frac{P_{out}}{P_{in}} \text{ dB}$$

$$\text{Voltage gain in dB} = 20 \log_{10} \frac{V_{out}}{V_{in}} \text{ dB}$$

$$\text{Current gain dB} = 20 \log_{10} \frac{I_{out}}{I_{in}} \text{ dB}$$

Advantage of expressing gain in dB

- The unit dB is a logarithmic unit. Our ear response is also logarithmic .Hence this unit matches with the natural response of our ears.
- When the gain is expressed in dB, the overall gain of the multistage amplifier is the sum of individual stages in dB.

Bandwidth

The range of frequency over which the gain is equal to or greater than 70.7% of the maximum gain is known as bandwidth.

For the frequency lying between f_L and f_H , the gain is equal to or greater than 70.7% of maximum gain. Here, f_H is Upper cut-off frequency and f_L is called Lower cut-off frequency. Therefore, $f_H - f_L$ is the bandwidth.

At f_L and f_H , the voltage gain of amplifier falls by 3dB from the maximum gain. Therefore, the frequency f_L and f_H are called 3dB frequencies or half-power frequencies. Because the power at f_L or f_H becomes half of its maximum value. Human ear can only identify a change of gain more than 3dB.

Advantages of R-C coupled amplifier:-

- It has good frequency response. The gain is constant over the audio frequency range.
- Circuit has low loss and is very compact.

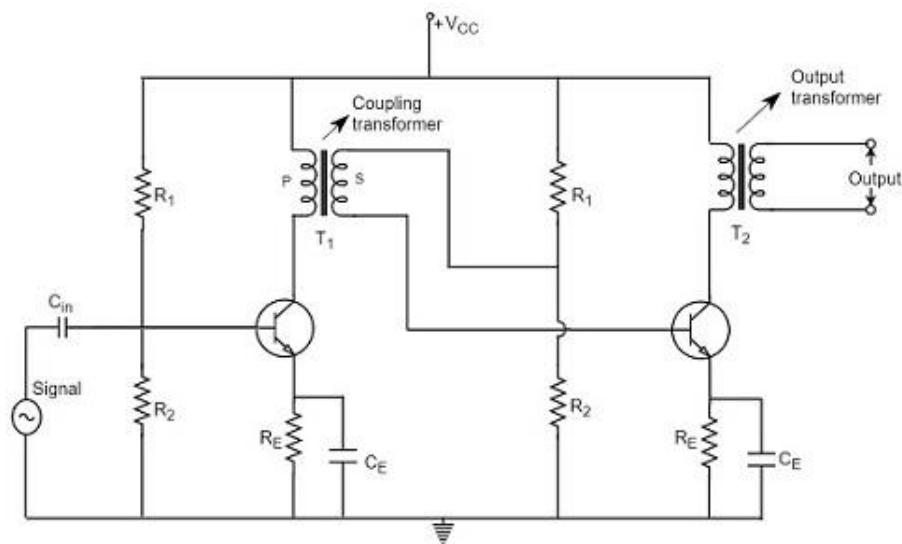
Disadvantages:-

- R-C coupled amplifier has low voltage and power gain.
- Impedance matching is poor.

Applications:-

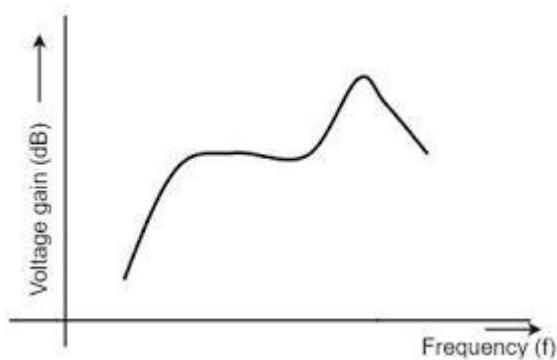
- They are widely used as voltage amplifiers in audio system.

2. Transformer coupled amplifier



Here, transformer is used to couple AC signals and to block DC components. By using transformer, excellent impedance matching can be achieved.

Frequency response of transformer coupled amplifier



As shown above, frequency response is not a good one . Gain is constant only over a small range of frequency. Hence, transformer coupled amplifier introduce frequency distortion.

Advantages:-

- Power loss minimum.
- Excellent impedance matching can be achieved.
- Due to excellent impedance matching, gain is high.

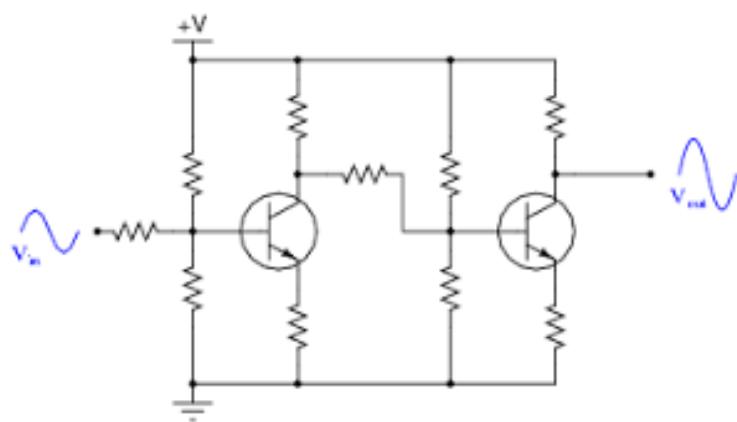
Disadvantages:-

- It has a poor frequency response.
- The coupling transformer is bulky and expensive.
- Transformer coupling introduces hum in the output.

Applications:-

- Used in power amplifier to provide impedance matching.
- Used in radio frequency tuned voltage amplifiers.

3) Direct coupled amplifier



For extremely low frequency applications such as amplification of photo electric current, thermo-coupled current etc, coupling devices such as capacitors and transformers cannot be used. Under such conditions, one stage is directly connected to the next stage without any coupling device. This type of coupling is known as direct coupling.

Advantages:-

- Circuit arrangement is simple.
- Circuit has low cost.

Disadvantages:-

- Output is not free from dc.
- Cannot be used for amplifying high frequencies.

Power amplifier/ large signal amplifier

A transistor amplifier which raises the power level of input signal is called transistor power amplifier.

Performance quantities of power amplifiers

- **Collector efficiency(efficiency)**:- The ratio of AC output power to the DC power supplied by the battery of a power amplifier is known as efficiency.

$$\text{Efficiency } \eta = \text{AC output power} / \text{DC input power}$$

- **Distortion :-** The change of output wave shape from the input wave shape of an amplifier is known as distortion.

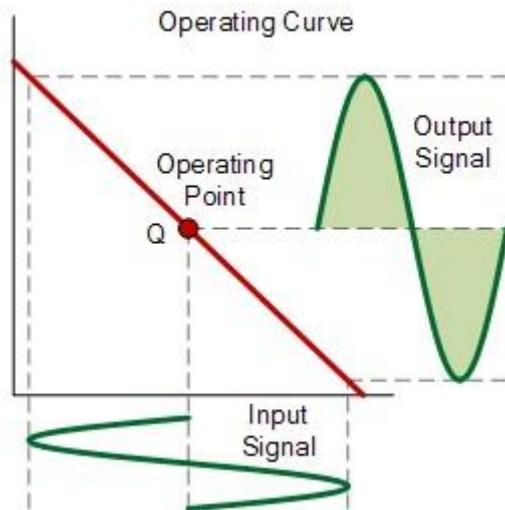
Classification of power amplifiers

Power amplifier are generally classified according to their mode of operation. On this basis ,they are classified as :

- a) Class A power amplifier
- b) Class B power amplifier
- c) Class AB power amplifier
- d) Class C power amplifier

Class A Power Amplifier

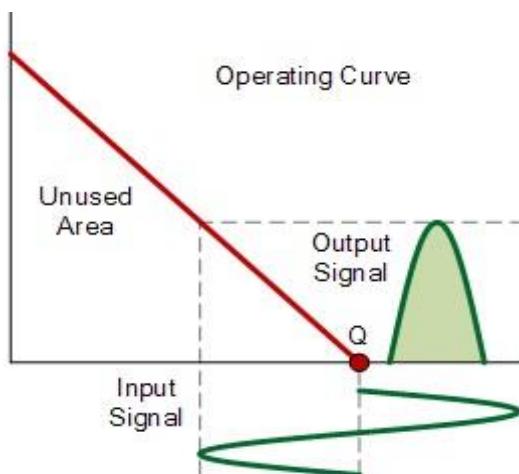
In class A power amplifier, operation point is fixed at the centre of de load line. The collector current flows at all times during the full cycle of the signal. That is ,the angle of condition is 360° .



As the output wave shape is exactly similar to the input wave shape, class A amplifiers have least distortion. As output current I_C flows all the time, it consumes high dc input power. Hence class A amplifiers have lowest efficiency.

Class B power amplifier

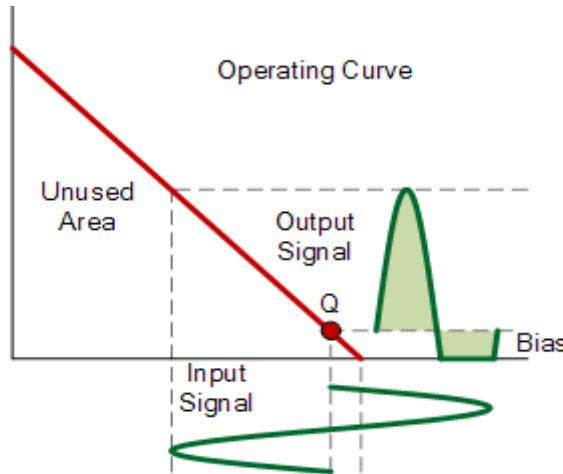
In class B power amplifier, operating point is fixed at the cut-off point. Collector current flows only during the positive half cycle of the input signal. The angle of conduction is 180° .



Class B amplifier have high distortion and high efficiency.

Class A B power amplifier

Class AB power amplifiers operating point is fixed within the active region near to cut-off point.

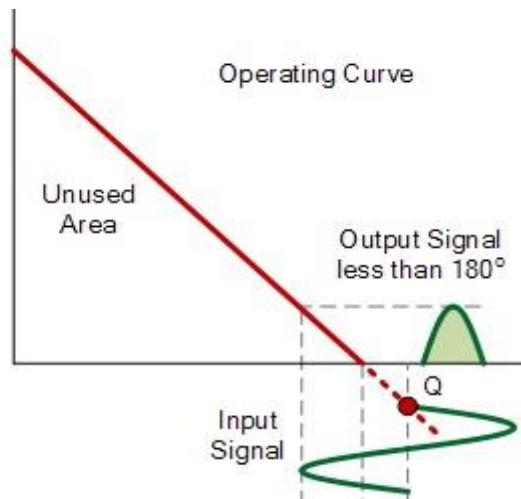


In Class AB amplifiers, collector current flows for more than half but less than the entire cycle of the input signal. The angle of conduction is in between 180° and 360° .

The characteristics of class AB amplifier lie in between those of class A and class B amplifiers .Distortion will be less than that of class B but more than that of class A. Efficiency will be less than that of class A but more than that of class B.

Class C power amplifier

In class C power amplifiers, operating point is fixed below cut-off point within the cut-off region.



In class C power amplifier, collector current flows for less than half cycle for the input signal. Angle of conduction is less than 180° . Class C power amplifiers have highest distortion and efficiency.

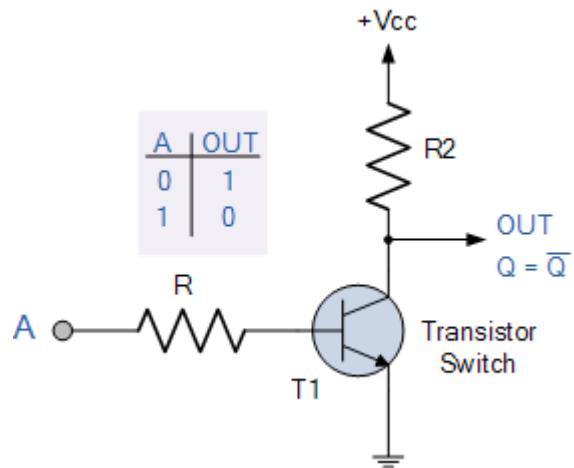
Comparison Between Different Amplifier Classes Of Operation

Parameters	Class A	Class A B	Class B	Class C
Conduction angle or operating cycle	360°	180° - 360°	180°	Less than 180°
Position of Q Point	At the centre of active region.	Near to cut-off point within the active region.	At cut-off point (At the point of intersection between active region and cut-off region.)	Below cut-off point within the cut-off region.
Distortion	Least	Low	High	Highest
Efficiency	very low(25% - 50%)	low (between 50% to 78.5%)	High (78.5%)	Very high(80%)
Applications	Used as AF and RF amplifier in radio, sound system, radar etc.	Used as AF and RF amplifier in radio, sound systems, radar etc.	Used as AF amplifiers. Used as power amplifier in transmitter.	Used as RF amplifier in transmitter.

Comparison, between voltage amplifier and power amplifier

Voltage amplifier	power amplifier
β is high (>100)	B is low(20-50)
Collector load is high($4-10\text{ k}\Omega$)	Collector load is low($5-20\Omega$)
RC coupling is used.	Transformer coupling is used.
Input voltage is low (only a few mV)	Input voltage is high(2-4 v)
Collector current is low (only a few mA)	Collector current is high($>100\text{ mA}$)
Power output is low.	Power output is high.
Output impedance is high (appro.50 $\text{k}\Omega$)	Output impedance is low(about 200Ω)
Amplifies voltage	Amplifier power (current of signal is normally amplified)
Used at initial and intermediate stages	Used at final stages.
For maximum voltage transfer, impedance mismatching is required.	For maximum power transfer, impedance matching is required.
Ordinary transistors are used.	Power transistor is used.
Circuit efficiency is very low.	Circuit efficiency is high.
Low power handling capability	High power handling capability.
Power dissipation or loss is high.	Power dissipation or loss is very low.
Linearity and magnitude of gain is important.	Linearity and efficient power coupling is important.

Transistor as an electronic switch



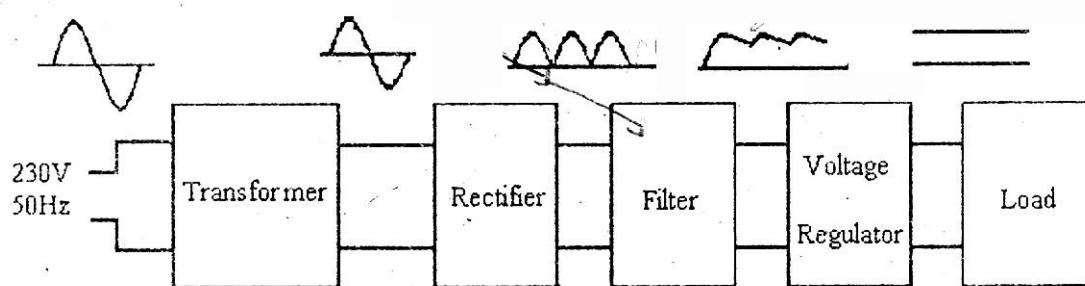
When high input is applied in the above circuit, a large base current $I_B(\text{sat})$ flows and transistor goes into saturation region . A transistor in saturation region is equivalent to a switch in ON condition.

When low input (0v or -5v) is applied, no base current will flow and transistor goes into cut-off region. When transistor is in cut-off region, it is equivalent to a switch in off condition.

UNIT 2

RECTIFIERS

Electrical energy is available in homes and industries in India, in the form of alternating voltage. The supply has a voltage of 220 Volts at a frequency of 50 Hz. For the operation of most of the devices in electronic equipments, a dc voltage is needed. Now a day, almost all electronic



Equipments include a circuit that converts ac voltage of mains supply in to dc voltage. This part of the equipment is called power supply. A block diagram of such a power supply is shown in figure above.

The rectifier circuit is the main part of a power supply. The rectifiers are the circuits, which are used in dc power supply. A rectifier is a circuit, which uses one or more diodes to convert ac voltage into pulsating dc voltage. The unidirectional conducting property of diode is used in rectifier. Rectifiers are two types.

1. Half wave rectifier
2. Full Wave rectifier

1. Half wave rectifier

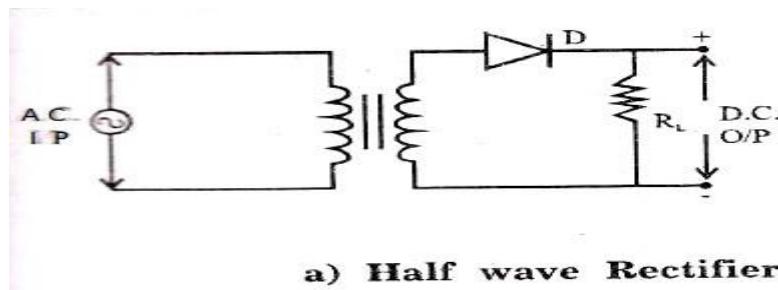


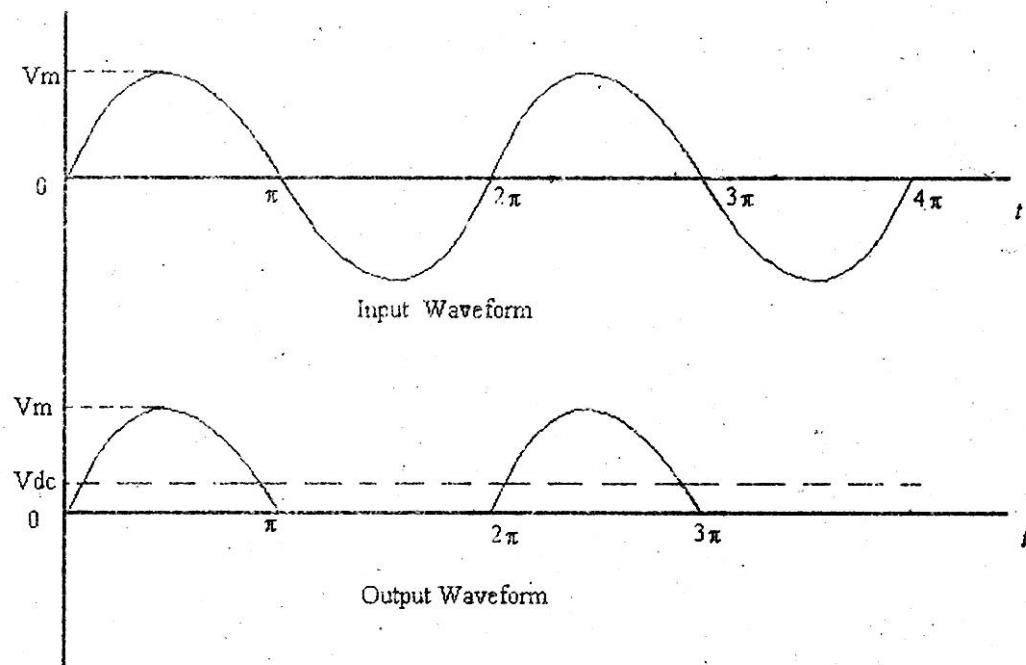
Figure shows the circuit of a half wave rectifier. Most of the electronic circuits use a transformer circuit¹. The transformer coupling provides two advantages.

1. It allows the source voltage to be stepped up or stepped down.
2. The ac power source is electrically isolated from the rectifier circuit. It reduces the risk of electrical shock.

During the positive half cycle of the ac input voltage, the diode D is forward biased and it conducts, current flows through the load resistor R_L and voltage is developed across it.

During negative half cycle of the input voltage, the diode D is reverse biased and no current flows. The voltage across the load resistor during this period is zero. Thus a pure ac signal is converted into a unidirectional signal.

The input and output of the half wave rectifier is shown below.



Peak Inverse Voltage

During the negative half cycle of the input, the diode is reverse biased. The whole of the input voltage appears across the diode. This maximum voltage is known as the Peak Inverse Voltage (PIV).

$$\text{PIV} = V_m$$

Performance of half wave rectifier

RMS value of current $I_{rms} = I_m/2$

DC value of current $I_{dc} = I_m / \pi$

Ripple factor $r = \frac{\text{RMS value of AC component}}{\text{Value of DC component}}$

Value of ripple factor $r = 1.21$

Rectification efficiency $\eta = \frac{\text{dc power output}}{\text{ac power input}} = \frac{P_{dc}}{P_{ac}}$

The value of Rectification efficiency η of half wave rectifier is 40.6%

Full Wave Rectifiers

There are two types of full wave rectifier circuits that are in use. One is called center-tap rectifier and uses two diodes. The other is called bridge rectifier and uses four diodes.

a. Center Tapped Full-wave Rectifier

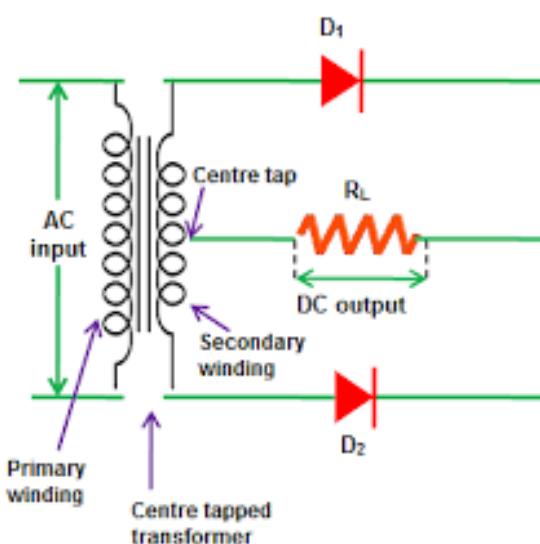


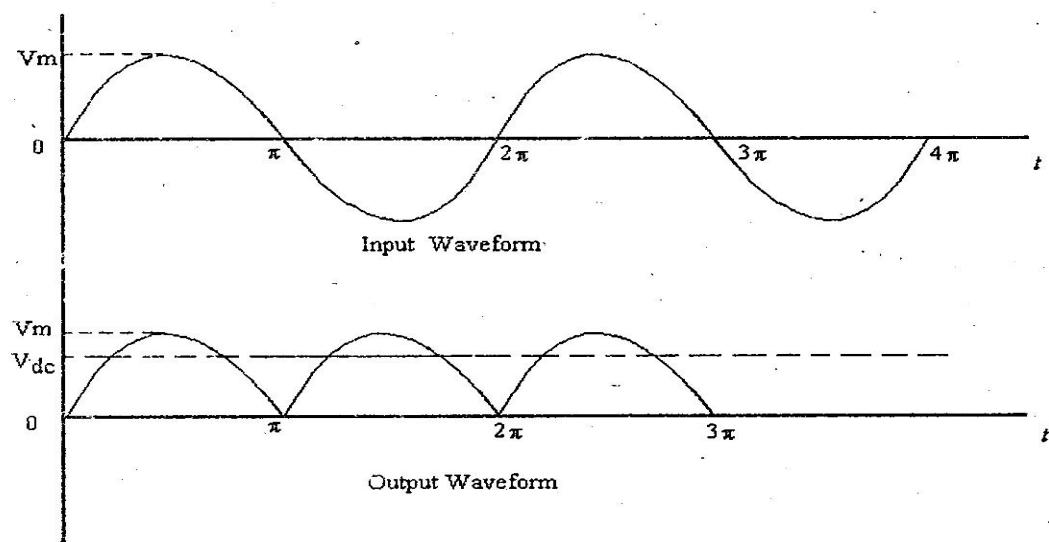
Figure shows the circuit of a center tapped full wave rectifier. The circuit uses two diodes, which are connected to the center-tapped secondary winding of the transformer. The input signal is applied to the primary winding of the transformer.

During the positive input half of the transformer polarity of the secondary voltage is as shown in fig. This forward biases the diode D_1 and reverses biases D_2 .

As a result of this diode D₁ conducts and diode D₂ is off. The current flows through diode D₁, load resistor R_L and upper half of secondary winding.

During the negative input half cycle, the polarities of the secondary voltage are changed. This reverse biases the diode D₁ and forward biases the diode D₂. As a result of this the diode D₁ is off and the diode D₂ conducts and current flows through diode D₂, the load resistor R_L and lower half of secondary winding.. The current through the load flows in the same direction during both the positive and negative half cycles. Therefore a fluctuating unidirectional voltage develops across the load resistor.

The input and output waveforms are given below.

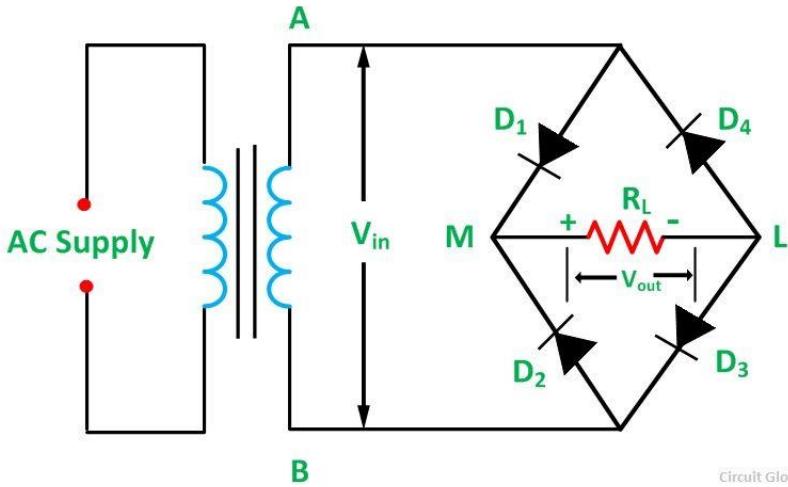


Peak Inverse Voltage

The voltage V_m is the maximum voltage across half of the secondary winding. During the positive half cycle of AC input, diode D₁ conducts and it offers almost zero resistance. The whole of the voltage V_m across the upper half winding appears across the load resistor R_L. Therefore reverse voltage that appears across the non conducting diode D₂ is the sum of the voltage across the lower half winding and the voltage across the load resistor R_L. The voltage is $V_m + V_m = 2V_m$.

Thus Peak Inverse voltage of diode in Center tapped rectifier = $2V_m$.

b. Full wave Bridge Rectifier



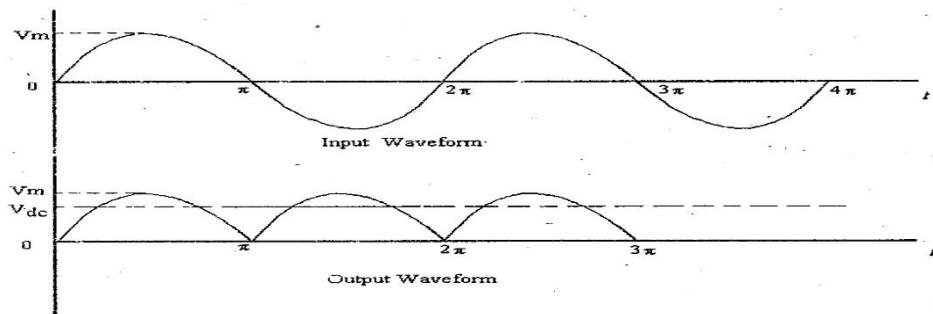
A bridge rectifier requires 4 diodes but avoids the need of a centre tapped transformer.

During the positive half cycle of secondary voltage, diodes D₁ and D₃ are forward biased and diodes D₂ and D₄ are reverse biased. Therefore current flows through diode D₁, load resistor R_L, diode D₃ and secondary winding.

During the negative half cycle of secondary voltage, diodes D₂ and D₄ are forward biased and diodes D₁ and D₃ are reverse biased. Therefore current flows through diode D₂, load resistor R_L, diode D₄ and secondary winding.

In both cases the current passes through the load resistor in the same direction. Therefore a fluctuating unidirectional voltage is developed across the load.

The input and output waveforms are given below.



Peak Inverse Voltage

The figure shows the bridge rectifier circuit at the instant the secondary voltage reaches its positive peak value, V_m. The diodes D₁ and D₃ are conducting, whereas diodes D₂ and D₄ are reverse biased and are non-conducting. The conducting diodes D₁ and D₃ have almost zero resistance and hence zero voltage drop across them. The

entire voltage V_m across the secondary winding appears across the load resistor R_L . The reverse voltage across the non-conducting diodes D_2 and D_4 is also V_m .

Thus Peak Inverse voltage of diode in bridge rectifier is V_m .

Advantages

- 1) The need for centre-tapped transformer is eliminated.
- 2) The PIV is one half that of the centre tapped circuit.

Disadvantages

1. It requires four diodes.
2. As during each half cycle of ac input two diodes that conduct are in series, therefore voltage drop in the internal resistance of rectifying unit will be twice as great as in the centre tap circuit. This is objectionable when secondary voltage is small.

Performance of Full Wave Rectifier

$$\text{RMS or effective value of the current, } I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$$

$$\text{Average value of the current } I_{\text{dc}} = \overline{2I_m}$$

$$\overline{\pi}$$

$$\sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1}$$

$$\text{Ripple factor } r =$$

$$= 0.482$$

Rectification efficiency $\eta = \text{dc power output} / \text{ac power input}$

$$= P_{\text{dc}}/P_{\text{ac}}$$

$$P_{\text{dc}} = \left(2 \frac{I_m}{\pi}\right)^2 R_L$$

$$P_{\text{ac}} = \left(\frac{I_m}{\sqrt{2}}\right)^2 R_L$$

$$\text{Therefore } \eta = 81.2\%$$

Comparison of Rectifiers

	Half wave	Full wave	
		Centre tap	Bridge
Number of diodes	1	2	4
Transformer Necessary	No	Yes	No
Peak secondary Voltage	V_m	V_m	V_m
Peak Inverse Voltage	V_m	$2 V_m$	V_m
RMS current, I_{rms}	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
DC current, I_{dc}	$I_m/\sqrt{2}$	$2I_m/\pi$	$2 I_m/\pi$
Ripple factor, r	1.21	0.4812	0.482
Rectification Efficiency η	40.6 %	81.2 %	81.2 %
Lowest ripple frequency, f_r	f_i	$2f_i$	$2f_i$

2.3 Filters

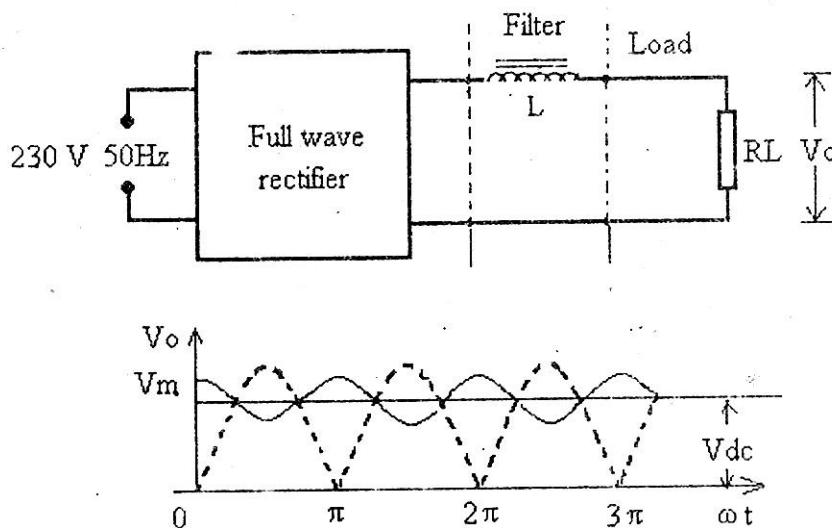
The object of rectification is to provide a steady DC voltage, similar to the voltage from the battery. We have seen that a full-wave rectifier provides dc better than a half wave rectifier. But, even a full-wave rectifier does not provide a ripple-free dc voltage. The rectifier provide that we may call "a pulsating" dc. We can filter or smooth out the ac variations from the rectified voltage. For this we use a filter or smoothing circuit.

The output of a rectifier contains dc as well as c component. A filter circuit that removes the unwanted ac component of the rectifier output and allows only dc component to reach the load.

A filter circuit consists of passive circuit elements that are inductors, capacitors, resistors and their combination. Some of the important filters are

1. Inductor Filter
2. Capacitor filter
3. Inductor-Capacitor or LC filter
4. Π Filter or C-L-C Filter.

Inductor Filter

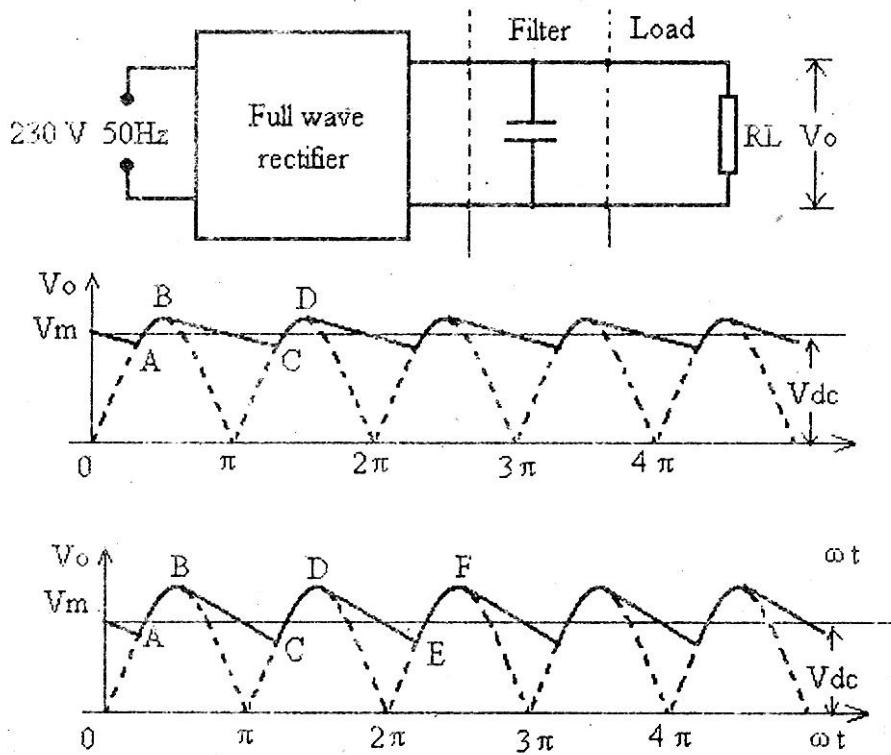


It is also called choke filter, it consists of an inductor (L), which is connected between the rectifier and the load resistance R_L in series. An inductor has the fundamental property of opposing any change in current flowing through it. This property is used in the series inductor filter.

The rectifier output contains ac components as well as dc components. When the output passes through an inductor, it offers a high resistance to the AC components and no resistance to DC components. Therefore ac component of the rectified output is blocked and only dc component reaches at the load. The inductor filter is more effective only for heavy load current that is when the load resistance (R_L) is small. Higher the current flowing through it, better is filtering action.

Capacitor Filter

This is the simplest and the cheapest filter. It consists of a large value capacitor, which is connected, in shunt with the load resistor R_L . The capacitor offers a low-reactance path to the ac components and infinite resistance to dc components. All the dc current passes through the load.

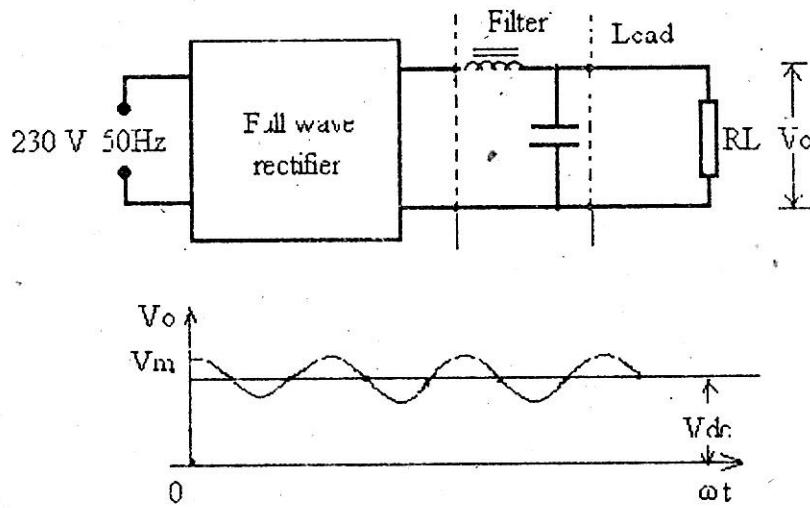


When the rectifier output voltage is increasing the capacitor charges to the peak voltage V_m . Just past the positive peak the rectifier output voltage tries to fall. But at this point the capacitor has $+V_m$ voltage across it. Since the source voltage becomes less than V_m , the capacitor will try to discharge through the load. Thus capacitor continues to discharge until the source voltage become more than the capacitor voltage and the capacitor is again charge to the peak value V_m . So we get a constant of output voltage or dc voltage.

An increase in the load current (i.e. decrease in the value of R_L) makes the time constant of the discharge path smaller. The capacitor discharges more rapidly, and the load voltage is not constant. The ripple voltage increases with increases in the load current.

A much steadier voltage can be obtained if the capacitor value of very large value is used. But the maximum voltage of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be safely handled by the diode is limited by a figure quoted by the manufacturer. This puts the limits on the maximum value, of the capacitance used in the shunt capacitor filter:

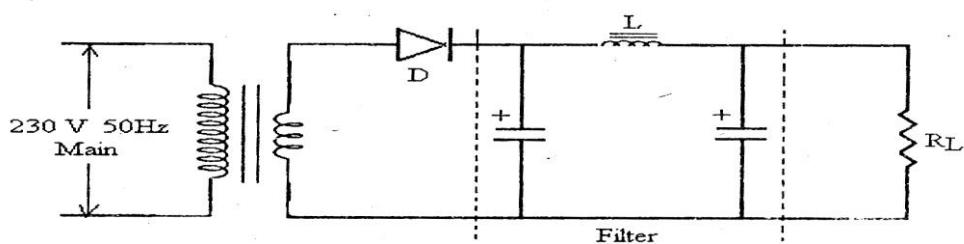
LC Filter



The combination of L and C filter is called LC filter. The LC filter is also known as inductor input filter or choke input filter. This filter uses an inductor L in series and capacitor C in shunt with load.

The choke allows the dc component to pass through it. For dc, the capacitor appears as open circuit and all the dc current passes through the load resistance R_L . The fundamental frequency of the ac component in the output of the rectifier is 100 Hz (twice the line frequency) for this ac, the reactance $X_L (= 2\pi fL)$ is high. The ac current has difficulty in passing through the inductor. Even if some ac current manages to pass through the choke, it flows through the low resistance $X_C (=1/ 2\pi fC)$ rather than through load resistance R_L . The ripples are reduced very effectively because X_L is much greater than X_C and X_C is much smaller than R_L .

Π Filter

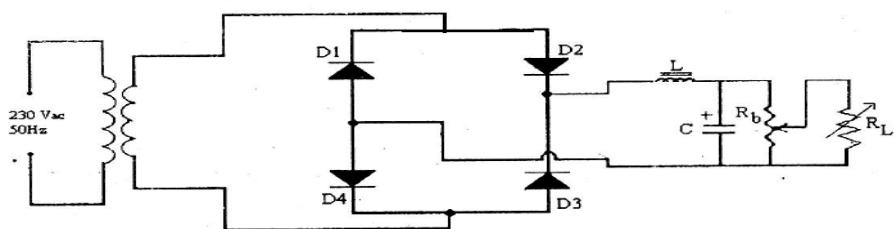


It is also called capacitor input LC filter or CLC filter. It consists of two capacitors C_1 and C_2 and an inductor L connected in the form of π . The pulsating output from the rectifier is applied at the input terminals of the π filter.

Capacitor C_1 offers low reactance to ac component of rectifier output. But it offers infinite resistance to the dc component. Therefore the capacitor C_1 bypasses the ac component to the ground, while dc component moves towards inductor L . It offers a high reactance to the ac components but zero resistance to the dc components. Therefore it allows the dc component to pass through it and block the ac component, which could not be bypassed by the capacitor C_1 . Capacitor C_2 bypasses the ac component of rectifier output, which could not be blocked by an inductor L . As a result, only the dc component is available at the output.

The disadvantages of the capacitor input LC filter are the cost, weight, size and external field produced by the series inductor.

Bleeder Resistor



Since an inductor depends up on current for its operation, it functions best under large current demands. For optimum functioning, the inductor should have a minimum current flowing at all times. If the current through the inductor falls below this minimum value, the output voltage raise sharply. The voltage regulation becomes poor. In order to provide this minimum current through the choke, a bleeder resistor R_b is usually included in the circuit. The above figure shows a bridge rectifier with a choke input filter using a bleeder resistor.

Even if load resistance R_L becomes open circuit the bleeder resistor R_b maintains the minimum current necessary of optimum inductor operation.

The bleeder resistor can serve a number of other functions as well. For example it can be used as a voltage divider for providing a variable output voltage.

It can also serve as a discharge path for the capacitor, so the voltage does not remain across the output terminal after the load has been disconnected and the circuit de-energized. This reduce hazard of electrical shock when the load is connected to the output terminal next time.

Zener Diode as a Voltage Regulator

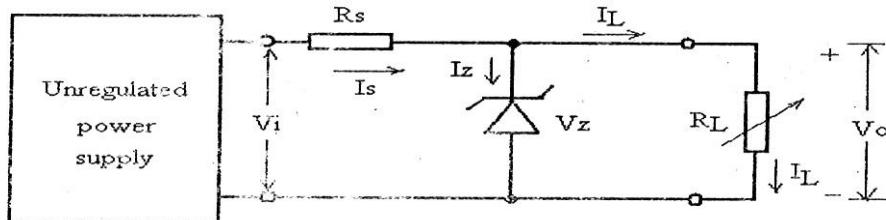
An ordinary diode will not permit current when it is reverse biased. If the reverse biased voltage exceeds the peak inverse voltage rating, diode may get destroyed due to avalanche breakdown. Zener diodes are special kinds of diodes designed to operate in the breakdown region without causing the damage to them.

When a diode is heavily doped its depletion layer becomes very narrow. When the applied reverse bias voltage across the diode is increased, the electric field across the depletion layer becomes very intense and electrons get pulled out from covalent bonds, generating electron-hole pairs. Thus heavy reverse current flows. This phenomenon is called zener breakdown.

Avalanche breakdown takes place when high reverse bias voltage is applied across the diode. Free electrons acquire high kinetic energy from the reverse electric field and they strike out other electrons, which are in covalent bond with other electrons of the neighbor atoms. Thus electron- hole pairs are generated. These electrons also get high kinetic energy and generate other electron-hole pairs. This multiplication goes on and heavy current flow takes place.

Zener diode behaves like an ordinary diode in the forward bias mode. Zener diodes are used as voltage regulators and voltage reference sources.

A Zener diode voltage regulator circuit is given below.



When a zener diode is in reverse breakdown region, the zener voltage V_z remains almost constant irrespective of current I_z through it. Since the load is connected in parallel with the zener diode, the voltage across it also remains constant at V_z .

A series resistor R_s is used to limit the zener current to less than its maximum current rating. The current through R_s is given by the expression $I_s = I_z + I_L$, where I_L is the current through the load resistor R_L . I_z is the current through the zener diode.

Regulation with varying input voltage

When input voltage V_i increases, input current I_s also increases. The current $I_s = I_z + I_L$. Then I_z also increases keeping I_L constant. When I_L remains constant, the output voltage $I_L R_L$ also remains constant.

When input voltage V_i decreases, input current I_s also decreases. Then I_z also decreases keeping I_L constant. When I_L remains constant, the output voltage $I_L R_L$ also remains constant.

Regulation with varying load resistance

When the load resistance R_L is decreased, the current I_L increases. Then zener current I_z decreases keeping I_s constant. When I_s remains constant, the voltage drop across R_s and hence output voltage remains constant.

When the load resistance R_L is increased, the current I_L decreases. Then zener current I_z increases keeping I_s constant. When I_s remains constant, the voltage drop across R_s and hence output voltage remains constant.

* ----- *

UNIT -3 OSCILLATORS

An electronic circuit that generates an alternating voltage is called an oscillator.

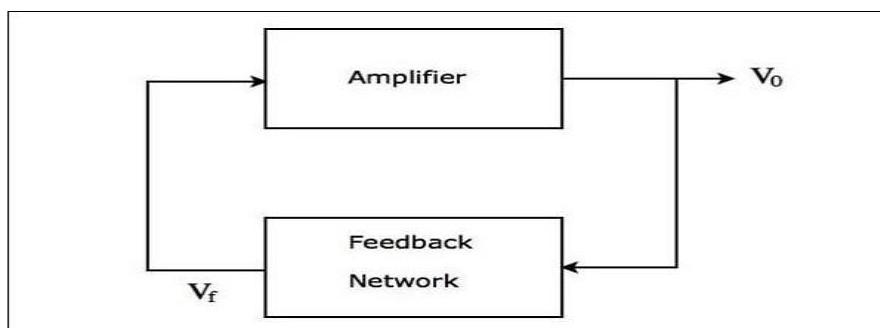
There are mainly two types of oscillators.

1. Sinusoidal oscillators

2. Non-sinusoidal oscillators

A sinusoidal oscillator produces sine waves whereas a non-sinusoidal oscillator produces waves other than sine waves such as square waves, triangular waves etc.

Conditions for Undamped or sustained oscillations (Barkhausen criterion)



1. An amplifier with positive feedback. (ie The total phase shift around the loop is 360° or 0°)
2. $A\beta = 1$. Here A is open loop gain of amplifier and β is feedback fraction ie fraction of output fed back to the input.

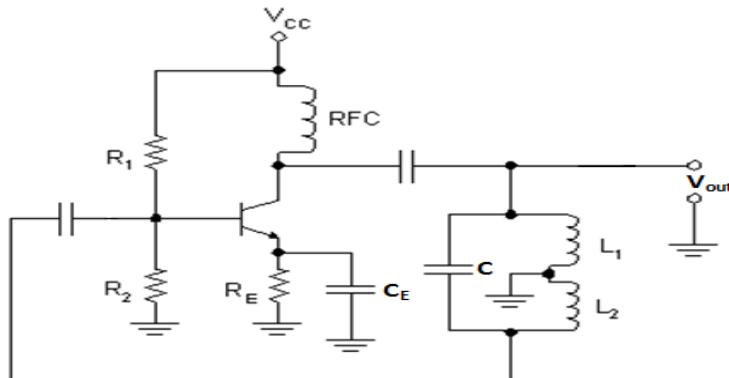
Types of sinusoidal oscillators

1. LC oscillators
2. RC Oscillators
3. Crystal Oscillators

1. LC Oscillators

LC Oscillators are used for generating high frequency oscillations. Therefore LC oscillators are also called high frequency oscillators or radio frequency oscillators. These oscillators use an LC circuit for frequency selection.

a. Hartley oscillator



The circuit consists of a single stage amplifier and a feedback network , which consists of a capacitor in parallel with a tapped inductor. The upper part of tapped inductor is L_1 and lower part is called L_2 . The tap is grounded. L_1 comes at the output of amplifier and L_2 comes at the input. The voltage across L_1 is output voltage V_o and voltage across L_2 is feedback voltage V_f .

When the circuit is switched on, capacitor C charges and then it discharges through inductors L_1 and L_2 , producing oscillation of

$$\text{Frequency} = \frac{1}{2\pi\sqrt{L_T C}}$$

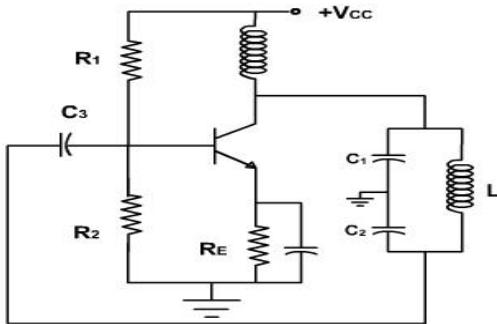
$$\text{where } L_T = L_1 + L_2$$

The voltage across L_2 is connected to the input of amplifier. The single stage amplifier amplifies this voltage and also introduces a phase shift of 180° . The output of amplifier is connected to the feedback network. There will be another phase shift of 180° between the voltages across L_1 and L_2 . Thus the total phase shift around the loop becomes equal to 360° or 0° , satisfying first condition for oscillation.

Here the value of feedback fraction $\beta = V_f / V_o = X_{L2} / X_{L1} = 2\pi f L_2 / 2\pi f L_1 = L_2 / L_1$

If the amplifier gain is made equal to L_1 / L_2 then $A\beta$ becomes equal to 1 , satisfying the second condition for oscillation. Then the circuit will function as a sustained oscillator.

Colpitts Oscillator



The circuit consists of a single stage amplifier and a feedback network , which consists of a tapped capacitor in parallel with an inductor. The upper capacitor is C_1 and lower capacitor is C_2 . The tap is grounded. C_1 comes at the output of amplifier and C_2 comes at the input. The voltage across C_1 is output voltage V_o and voltage across C_2 is feedback voltage V_f .

When the circuit is switched on, capacitors C_1 and C_2 charges and then they discharges through inductor L , producing oscillation of frequency

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Where C is the equivalent value if the capacitance and equal to $\frac{C_1 C_2}{C_1 + C_2}$

$$f = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

The voltage across C_2 is connected to the input of amplifier. The single stage amplifier amplifies this voltage and also introduces a phase shift of 180° . The output of amplifier is connected to the feedback network. There will be another phase shift of 180° between the voltages across C_1 and C_2 . Thus the total phase shift around the loop becomes equal to 360° or 0° , satisfying first condition for oscillation.

Here the value of feedback fraction $\beta = V_f / V_o = X_{C2} / X_{C1} = (1/2\pi f C_2) / (1/2\pi f C_1) = C_1 / C_2$

If the amplifier gain is made equal to C_2 / C_1 then $A\beta$ becomes equal to 1 , satisfying the second condition for oscillation. Then the circuit will function as a sustained oscillator.

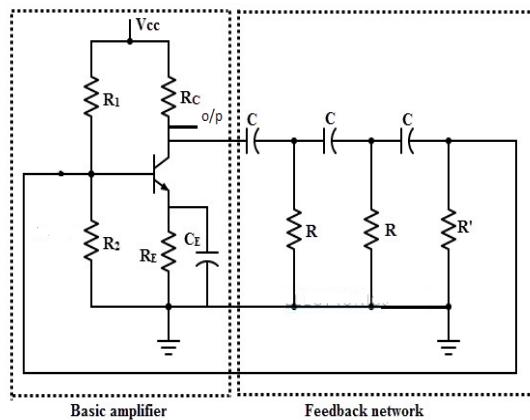
RC Oscillators

For generating low or audio frequencies (20 Hz to 20KHz), RC oscillators are used. In this circuit, the frequency determining network is RC network. Here the starting voltage is noise voltage. Noise voltages are produced due to the random motion of electrons in resistors or within the active device used in the circuit. Almost all sinusoidal frequencies are contained in this noise voltage and have very small amplitude.

The two commonly used RC oscillators are

1. RC Phase shift Oscillator
2. Wein Bridge Oscillator

1. RC Phase shift Oscillator



The circuit consists of a single stage amplifier and a feedback network, which consists of 3 identical RC sections.

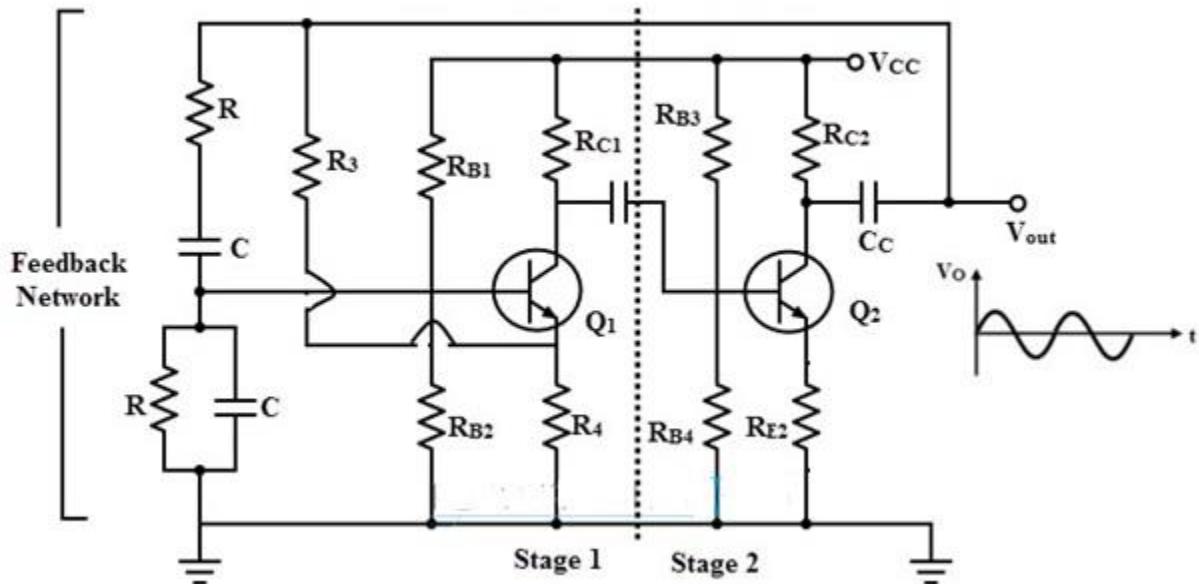
The starting voltage here is noise voltage. The noise voltage contains almost all sinusoidal frequencies.

The noise voltage is amplified by the single stage amplifier. It also introduces a phase shift of 180° . At only one frequency $f = 1/2\pi RC\sqrt{6}$, each RC section introduces a phase shift of 60° . Thus a phase shift of 180° is provided by the feedback network.

Thus the total phase shift around the loop becomes 360° , satisfying the first condition for oscillation.

At the above frequency, the value of feedback fraction is found to be $1/29$. Therefore if the amplifier gain is made equal to 29, $A\beta$ becomes 1, satisfying the second condition for oscillation. Then the circuit will function as a sustained oscillator.

2. Wein bridge Oscillator



The circuit consists of a 2 stage RC coupled amplifier and a feedback network called Wein bridge. The wein bridge consists of 4 arms; RC series network, RC parallel network, R_3 and R_4 .

The starting voltage here is noise voltage. Almost all sinusoidal frequencies are contained in this noise voltage.

The noise voltage is amplified by the two stage amplifier. The two stage amplifier also provides 360° phase shift. Only at one frequency $f = 1 / 2\pi RC$, the RC network provides no phase shift. ie only at frequency $f = 1/2\pi RC$, the first condition of oscillation will be satisfied. Therefore this will be the frequency of oscillation.

At the above frequency, the value of feedback fraction is found to be $1/3$. If the total gain of amplifier is made equal to 3, $A\beta$ becomes 1 and the second condition of oscillation will be satisfied.

To obtain a low gain equal to 3, negative feedback is introduced in the circuit through R_3 & R_4 . Also the emitter resistors of both the amplifier stages are kept unbypassed. To control the amount of negative feedback, R_3 used is a variable resistor.

Limitations of LC & RC Oscillators

In LC & RC oscillators, the frequency of oscillation may change due to the reasons given below.

- When temperature changes, the values of resistors and inductors, which are the frequency determining factors, will change. This causes the change in frequency of oscillation.
- If any component of feedback network (resistor, inductor or capacitor) is replaced, due to the tolerance variations, the frequency of oscillation will change.

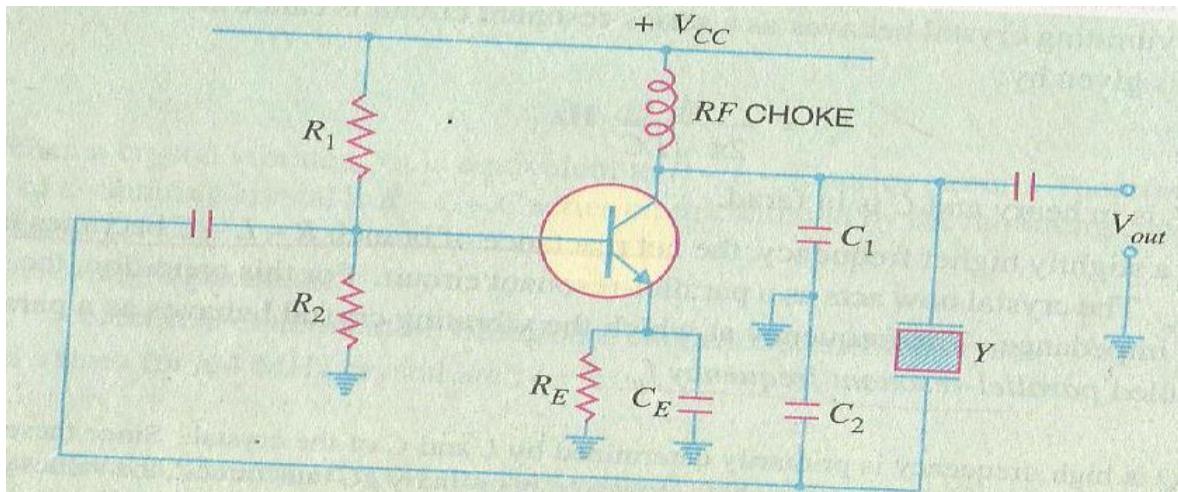
Crystal Oscillator

For highly stable frequency applications, crystal oscillators are preferred over LC & RC oscillators. The frequency of crystal oscillator changes only by less than 0.1% due to temperature and other changes. A crystal oscillator uses a piezo electric crystal for its working. A piezo electric crystal, when it is mechanically forced to vibrate, produces an AC voltage. This phenomenon is called piezo electric effect.

Crystal Oscillator circuit

A colpitts modified crystal oscillator is given below.

The only change here compared to the colpitts oscillator is that a piezo electric



crystal is used instead of inductor in the feedback network. Here the frequency of oscillation will be the parallel resonant frequency f_p of the crystal. At f_p , the impedance of crystal will be maximum. Therefore maximum voltage drop occurs across the capacitor C_1 . This in turn allows maximum feedback through the feedback network.

In this circuit, the amplifier introduces a phase shift of 180° . The output of amplifier is connected to the feedback network. There will be another phase shift of 180° between the voltages across C_1 and C_2 . Thus the total phase shift around the loop becomes equal to 360° or 0° , satisfying first condition for oscillation.

Here the value of feedback fraction $\beta = V_f / V_o = X_{c2} / X_{c1} = (1/2\pi f C_2) / (1/2\pi f C_1) = C_1 / C_2$

If the amplifier gain is made equal to C_2 / C_1 then $A\beta$ becomes equal to 1, satisfying the second condition for oscillation. Then the circuit will function as a sustained oscillator with frequency equal to the parallel resonant frequency f_p of the crystal.

Advantages

- Crystal oscillator has a high frequency stability.
- The quality factor (Q factor) of crystal is very high.

Disadvantages

- They are fragile and can only be used in low power circuits.
- The frequency of oscillator can not be changed.

Applications

Crystal oscillators are used for highly stable frequency applications such as in communication transmitters, receivers, digital watches, clocks etc.

Multivibrators

An electronic circuit that generates square wave or rectangular wave is known as a multivibrator. It is basically a 2 stage amplifier with output of one feedback to input of the other.

Types of multivibrators

The multivibrators are classified as

1. Astable multivibrator
2. Monostable multivibrator
3. Bistable multivibrator

1. Astable multivibrator

The astable or free-running multivibrator has no stable state and alternates automatically between the two states and remains in each state for a time depending up on the circuit constants. It is also called square wave oscillator because it produces square wave output without applying any input.

2. Monostable multivibrator

The monostable or one-shot multivibrator has one stable state and one quasi(or half) stable state. The application of input pulse triggers the circuit into quasi stable state, in which it remains for a time determined by circuit constants. After this period of time, the circuit switches back to the stable state.

Mono stable multivibrators are used to produce pulses with variable pulse width, to provide time delay in digital circuits etc.

3. Bistable multivibrator

A multivibrator which has 2 stable states is called a bistable multivibrator. It will remain in one stable state until a trigger pulse causes it to switch to the other stable state. Another trigger pulse is then required to switch the circuit back to the original stable state.

Bistable multivibrators are used for counting and storing the binary informations.

Astable Multivibrator

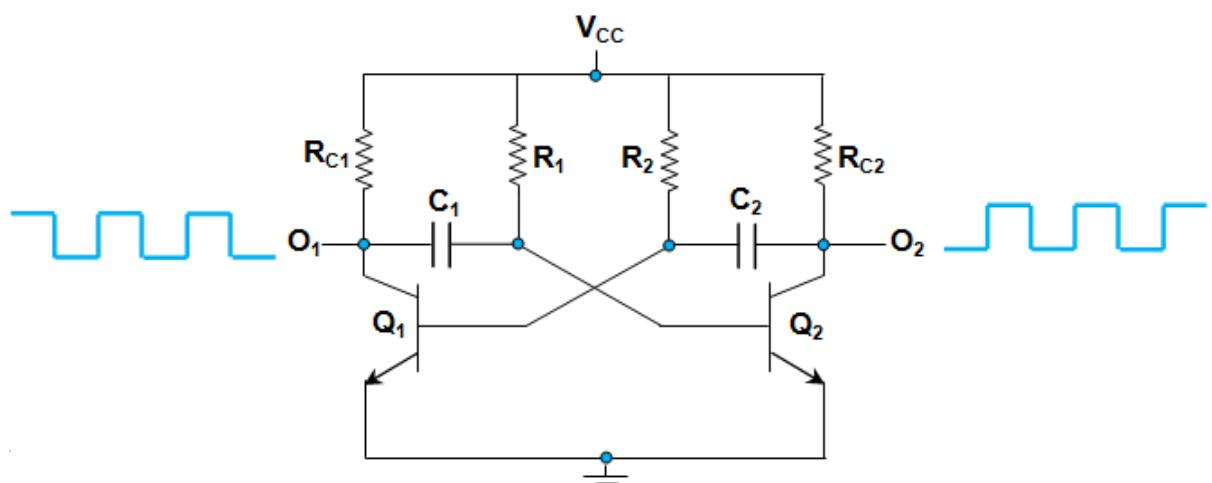


Figure 1 Astable Multivibrator Using BJTs

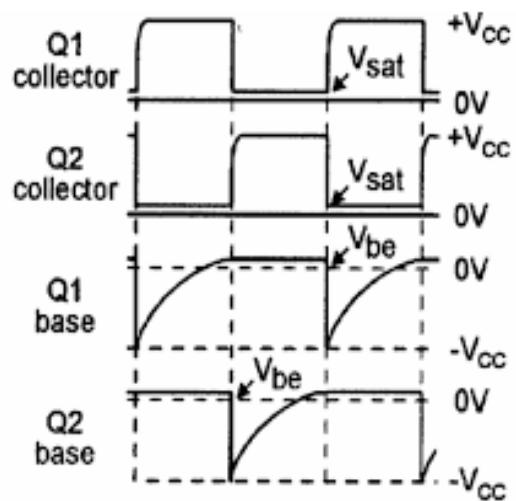
In the above diagram we can find two transistors which is wired as a switch. When a transistor is ON, its collector and emitter act as a short circuit. But when it is OFF they acts as open circuit. So in the above circuit when a transistor is in OFF state its collector will have the voltage V_{cc} and when it is ON its collector will be grounded. When one transistor is ON the other will be OFF. The OFF time of transistor is determined by RC time constant.

When the circuit is switched on, one of the transistor will be more conducting than the other due imbalance in the circuit or difference in the parameters of the

transistor. Gradually the more conducting transistor will be driven to Saturation and the less conducting transistor will be driven to Cutoff.

- When the circuit is switched on one transistor will be driven to saturation (ON) and the other will be driven to cutoff (OFF). Consider Q1 is ON and Q2 is OFF.
- During this time Capacitor C2 is charging to Vcc through resistor R.
- Q2 is OFF due to the -ive voltage from the discharging capacitor C1 which is charged during the previous cycle. So the OFF time of Q2 is determined by R1C1 time constant.
- After a time period determined by R1C1 time constant the capacitor C1 discharges completely and starts charging in reverse direction through R1.
- When the Capacitor C1 charges to a voltage sufficient to provide base emitter voltage of 0.7V to the transistor Q2, it turns ON and capacitor C2 starts discharging.
- The negative voltage from the capacitor C2 turns off the transistor Q1 and the capacitor C1 starts charging from Vcc through resistor R and base emitter of transistor Q2. Thus the transistor Q2 remains in ON state.
- As in the previous state, when the capacitor C2 discharges completely it starts charging towards opposite direction through R2.
- When the voltage across the capacitor C2 is sufficient to turn ON transistor Q1, Q1 will turn ON and capacitor C1 starts discharging.
- This process continues and produces rectangular waves at the collector of each transistors.

The waveforms at the collector and base of transistors Q1 & Q2 are given below



Time period of output square wave, $T = 0.69R_1C_1 + 0.69 R_2C_2$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, $T = 1.38 RC$

The frequency $f = 1 / 1.38RC$

Astable multivibrators are used as square wave generators.

UNIT 4- Digital Electronics

INTRODUCTION

As you know analog signals are also called continuous signals or continuously varying signals. These signals have infinite number of values. Alternating current or voltage wave forms which are of sinusoidal shape are examples of analog signals.

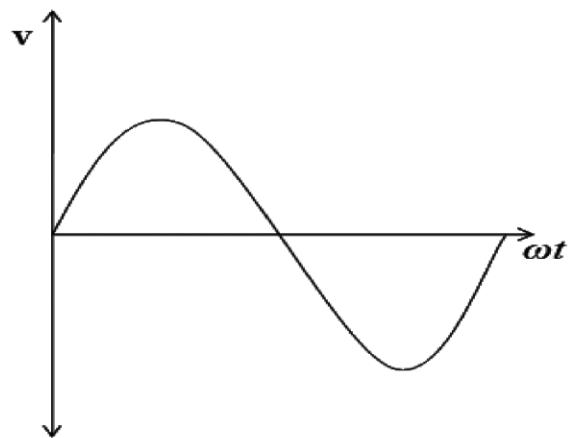


Fig 10.1 Analog Signal

But digital signals have only two states-the 'ON' state and the 'OFF' state. Each of the two states are designated as logic1 and logic 0 states. These can also be characterized as true or false. The signal can be represented as a square wave form as follows.

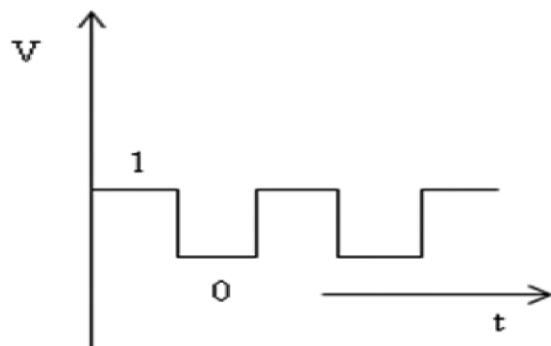


Fig 10.2 Digital Signal

In digital signals, a logic 1 can be represented by a +5v and logic ‘0’ can be represented by a ‘0v’. In analog circuits or devices, the electrical variable such as current or voltage is continuous. That means an analog circuit processes continuously varying signals or analog signals. But in a digital circuit only discrete values of variables are recognized. A digital circuit or device processes digital signal.

NUMBER SYSTEM

Do you know the name of the number system which you use in your daily life? This number system which uses digits from 0 to 9 ie 0,1,2,3,4,5,6,7,8 and 9 is called decimal number system. ‘Deci’ means 10’. This number system is termed as decimal system because the base of this system is ‘10’. Similarly we have a wide variety of number systems. Each of these is based on a specific base or radix. The binary number system is based on the base ‘2’, octal number system is based on the base ‘8’ and hexadecimal number system has the base ‘16’.

Activity 1

Let us examine the formation of the number $(429)_{10}$ where 10 represents its base.

$$(429)_{10} = 4 \times 10^2 + 2 \times 10^1 + 9 \times 10^0$$

$$\text{i.e } 429 = 400 + 20 + 9$$

Here ‘4’ is in the hundredth position ‘2’ is in the tenth position and the digit ‘9’ is in its unit’s position. Similarly we can represent numbers in any other number system using its base.

10.2 BINARY NUMBER SYSTEM

Binary number system is the soul of digital electronics. The base of this number system is ‘2’. A number in this system is represented by ‘0’s and ‘1’s.

Consider a binary number 10110 similar to the previous activity showing the meaning of decimal number. Starting from the least significant bit ‘0’ towards left in the above binary number 10110, ‘0’ is in the unit’s (2^0)th position, ‘1’ is in the 2nd (2^1) position, the next ‘1’ is in the 4th (2^2) position, next ‘0’ is in the 8th (2^3) position and the next 1 is in the 16th (2^4) position. Digital signals are represented by binary number system.

In the system ‘0’ is equivalent to ‘0’ in the decimal system and 1 is equivalent to ‘1’ in the decimal system. The next number is ‘1 0’ in the binary number system which is equivalent to ‘2’ in the decimal system. Similarly the following number is ‘11’ which is equivalent to ‘3’ in the decimal system.

Conversion of a Binary number to a Decimal number

Try to analyse the following table.

Binary	Equivalent decimal
0	0
1	1
10	2
11	3
100	4

Table 10.1

The representation of a binary number and its meaning have been illustrated above. Keeping these in mind the binary number $(10110)_2$, can be converted into a decimal number as follows.

The representation of a binary number and its meaning have been illustrated in the previous section. Keeping these in mind the binary number $(10110)_2$ can be converted into decimal as follows.

$$\begin{array}{ccccc} 1 & 0 & 1 & 1 & 0 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \end{array}$$

$$\begin{aligned} (10110)_2 &= 1*2^4+0*2^3+1*2^2+1*2^1+0*2^0 \\ &= 1*16+0*8+1*4+1*2+0*1 \\ &= (22)_{10} \end{aligned}$$

So $(10110)_2 = (22)_{10}$

Where 22 is the decimal equivalent value of binary number 1 0 1 1 0 .

Check your progress:

Convert the following numbers into decimal number system.

a) $(1111)_2$

b) $(10101)_2$

Conversion from Decimal to Binary

To convert a number in the decimal system into binary ,firstwe have to divide the number by ‘2’. If it is exactly divisible write ‘0’ against the number on its right hand side. If not exactly divisible put ‘1’ against the number. Again divide the result obtained by ‘2’ and proceed until the result is ‘1’. Then read up the number starting from the last resultant digit through all digits on the right hand side. As an example, let us convert $(61)_{10}$ into binary.

we have to multiply by ‘2’. If the product of each number is greater than ‘1’ put a ‘1’ below that number otherwise put a ‘0.’ To understand this, let us consider the following.

Conversion of decimal fraction $(0.8125)_{10}$ into binary:

Number	0.8125	0.625	0.25	0.5
Base	2	2	2	2
	1.6250	1.250	0.50	1.0
Remainder	1	1	0	1

Therefore $(0.8125)_{10} = (0.1101)_2$.

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Therefore $(0.8125)_{10} = (0.1101)_2$.

The arrow shown represents how to read up the binary number .

ie, 1 1 1 1 0 1

$$\text{So } (61)_{10} = (111101)_2$$

Check your progress:

Convert the following numbers into binary number system.

a) $(131)_{10}$

b) $(346)_{10}$

2	61	1	↑
2	30	0	
2	15	1	
2	7	1	
2	3	1	
2	1	1	
			0

Decimal and Binary Fractions

To understand the meaning of representation of decimal fractions let us consider such a number say $(36.2012)_{10}$

The Expansion for this number is

$$(36)_{10} = 3 \times 10^1 + 6 \times 10^0, \text{ and}$$

$$(0.2012)_{10} = 2 \times 10^{-1} + 0 \times 10^{-2} + 1 \times 10^{-3} + 2 \times 10^{-4}$$

So the Positional values of the above number can be shown as below

$$\begin{array}{ccccccc} 3 & 6 & 2 & 0 & 1 & 2 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 10^1 & 10^0 & 10^{-1} & 10^{-2} & 10^{-3} & 10^{-4} \end{array}$$

Similarly the positional values of a binary fraction say 1 0 1 . 1 1 0 1 can be shown as

$$\begin{array}{cccccccc} 1 & 0 & 1 & 1 & 1 & 0 & 1 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 2^2 & 2^1 & 2^0 & 2^{-1} & 2^{-2} & 2^{-3} & 2^{-4} \end{array}$$

Conversion of Binary Fraction to Decimal

Let us Consider the binary fraction $(101.1101)_2$. This may be written as follows

$$(1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0) + (1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4})$$

So the decimal equivalent of this binary becomes

$$5 + (1/2 + 1/4 + 1/16) = (5.08125)_{10}$$

Conversion from Decimal Fraction to Binary

We have studied in the earlier sections that to convert decimal whole number to binary whole number,a division by '2' has to be performed. To convert decimal fractions to binary fractions

we have to multiply by ‘2’. If the product of each number is greater than ‘1’ put a ‘1’ below that number otherwise put a ‘0.’ To understand this, let us consider the following.

Conversion of decimal fraction $(0.8125)_{10}$ into binary:

Number	0.8125	0.625	0.25	0.5
Base	2	2	2	2
	1.6250	1.250	0.50	1.0
Remainder	1	1	0	1

Therefore $(0.8125)_{10} = (0.1101)_2$.

10.3 OCTAL NUMBER SYSTEM

The octal number system uses digits 0,1,2,3,4,5,6 & 7 ie , eight digits. So the base of this number system is ‘8’.

$(127)_8$ which is in octal number system can be represented as

$$(127)_8 = 1 \times 8^2 + 2 \times 8^1 + 7 \times 8^0$$

$$\begin{array}{ccc} 1 & 2 & 7 \\ \downarrow & \downarrow & \downarrow \\ 8^2 & 8^1 & 8^0 \end{array}$$

Conversion from Octal to Decimal

Keeping the above representation in mind, let us find the decimal equivalent of the octal number $(127)_8$ -

$$\begin{aligned} (127)_8 &= 1*8^2 + 2*8^1 + 7*8^0 \\ &= 64+16+7 \\ &= (87)_{10} \end{aligned}$$

So the decimal equivalent of $(127)_8$ is $(87)_{10}$

Conversion from Decimal to Octal

We have already studied how to convert decimal number into binary. Similarly we can convert a decimal number to an octal number by dividing the given number by ‘8’ repeatedly, until the result is less than ‘8’.

Let us convert $(87)_{10}$ to the octal number system.

$$\text{So } (87)_{10} = (127)_8$$

$$\begin{array}{r} 8 \quad | \quad 87 \quad 7 \\ 8 \quad | \quad 10 \quad 2 \\ \quad \quad \quad \quad 1 \end{array}$$

Check your progress:

Convert the following decimal numbers into octal numbers

a) 256

b) 728

Octal to Binary Conversion

To convert an octal number into binary we should first proceed to convert the octal number to decimal. Then the decimal number obtained is to be converted to binary. Consider the octal number $(127)_8$. Let us try to convert this number into a binary number.

For this, first, we have to convert $(127)_8$ to decimal

$$\begin{aligned} \text{ie, } (127)_8 &= 1 \times 8^2 + 2 \times 8^1 + 7 \times 8^0 \\ &= 1 \times 64 + 2 \times 8 + 7 \times 1 \\ &= (87)_{10} \end{aligned}$$

Now $(87)_{10}$ may be converted to binary.

$$(87)_{10} = (1010111)_2$$

$$\begin{array}{r}
 2 \quad | \quad 87 \quad 1 \\
 2 \quad | \quad 43 \quad 1 \\
 2 \quad | \quad 21 \quad 1 \\
 2 \quad | \quad 10 \quad 0 \\
 2 \quad | \quad 5 \quad 1 \\
 2 \quad | \quad 2 \quad 0 \\
 \end{array}$$

1

Therefore $(127)_8 = (1010111)_2$

So the binary equivalent to the octal number 127 is 1 0 1 0 1 1 1

10.4 HEXA DECIMAL NUMBER SYSTEM

The number system with base 16 is called hexa decimal number system. The 16 characters including numbers and alphabets used in this system are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F

The following table illustrates the above fact

Decimal	Hexa decimal
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

Table 10.2

According to this system the next hexadecimal number is 10 which is equivalent to 16 in the decimal system.

$$\text{ie, } (10)_{16} = (16)_{10}$$

$$\text{Similarly } (11)_{16} = (17)_{10}$$

$$(12)_{16} = (18)_{10} \text{ and so on.}$$

Similar to the methods adopted in the earlier sessions we can convert a decimal number to hexa decimal number and vice versa. Let us convert the decimal number $(269)_{10}$ to a hexa decimal number.

$$\begin{array}{r} 16 \longdiv{269} & 13 \\ 16 \longdiv{16} & 0 \end{array}$$

13 is equivalent to D in hexa decimal 1

$$\text{Therefore } (269)_{10} = (10D)_{16}$$

Let us now convert the hexadeciml number F9 into decimal. We know that F is equivalent to 15 in the decimal system, so

$$\begin{aligned}
 (F9)_{16} &= 15 \times 16^1 + 9 \times 16^0 \\
 &= 240 + 9 \\
 &= (249)_{10}
 \end{aligned}$$

Therefore the decimal equivalent of the hexadecimal F9 is 249

Check your progress:

- a) Convert the following decimal numbers to hexadecimal numbers
 - i) 148 ii) 84
- b) Convert the following hexa decimal numbers to decimal numbers
 - i) $(19)_{16}$ ii) $(2C)_{16}$

Converting Hexadecimal to Binary:

Remember hex uses groups of four bits, so we can use the table below for conversions.

Decimal	Binary	Hex
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B

12	1100	C
13	1101	D
14	1110	E
15	1111	F

To convert $D14B_{16}$ to binary,

$$D = 1101, \quad 1 = 0001, \quad 4 = 0100, \quad B = 1011$$

When we put the pieces together, we get: $D14B_{16} = 1101000101001011_2$

Converting Binary to Hexadecimal

The rules for conversion from binary to hexadecimal are as given below:

1. Divide the given binary number into a group of four bits from binary point to left (or from right to left if no fractional part) and from binary point to the right. Append 0's at leading or trailing position if necessary to make each group of 4 bits.
2. Substitute each group of four bits by hexadecimal equivalent symbol (letter or digit) from the table.
3. Collect Hexadecimal symbols to get Hexadecimal equivalent number

Example: convert $(10101011101)_2$ into hexadecimal

Solution:

Dividing the given binary number $(10101011101)_2$ into groups of 4 bits from binary point to left and binary point right and appending 0's at leading or at trailing position

to make each group of four bits,

0101 0101 1101

Now assign each group its corresponding Hex value.

$0101 = 5$, $0101 = 5$, $1101 = D$

When put together we get the Hex value $55D_{16}$

Conversion from octal to hexadecimal (base 8 to base 16):

Actually, there is no direct method for converting from octal to hexadecimal so first, convert octal into binary or decimal and then convert binary or decimal to hexadecimal.

Conversion of hexadecimal to octal (base 16 to base 8):

There is no direct method for converting from hexadecimal to octal, so first convert hexadecimal into binary or decimal and then convert binary or decimal to octal.

Logic Gates

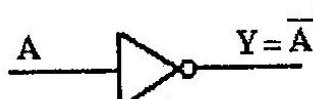
The logic functions frequently involved in the design of digital systems are : AND, OR, NOT, NAND , NOR AND EXCLUSIVE-OR. Each of these functions is performed by an electronics circuit known as gate, such as AND gate, OR gate etc. The logic gates are the basic building blocks of digital systems. Knowledge of these gates is essential in the study of digital electronics.

BASIC GATES

NOT gate, AND gate & OR gates are called basic gates.

NOT Gate

The inverter (NOT circuit) performs a logic function called inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level. That is to change 1 to 0 or 0 to 1. The standard symbol for the NOT gate is given below.

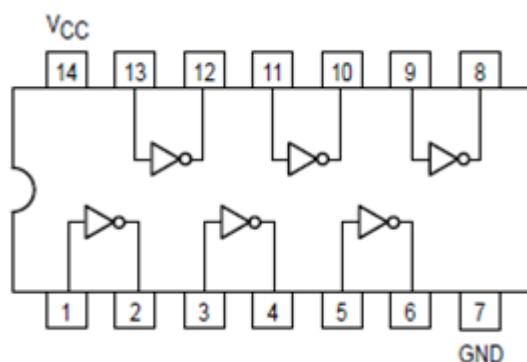


When a HIGH level is applied to an inverter input, a LOW level will appear on its output. When a LOW level is applied to the input, a HIGH will appear on the output.

This operation is summarized in the table given below, which shows the output for each possible input in terms of levels and bits. Such a table showing the operation of a digital device is called its truth table. The truth table will have column for entering the input values and another one for showing the corresponding outputs. Truth table of a NOT gate is shown below.

Input	Output
0	1
1	0

The IC number of NOT gate is 7404. Its internal diagram with pin number is given below.



AND Gate

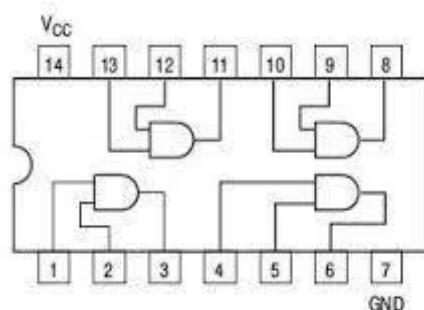
The AND gate performs a logical multiplication, more commonly known as the AND function. The AND gate is composed of two or more inputs and a single output. The AND gate with two inputs A and B can be indicated using the logic symbol shown in figure. Inputs are on the left and the output is on the right of the symbol.



The operation of the AND gate is such that the output is high is only when all of the inputs are HIGH. When any of the inputs are LOW, the output is LOW. Therefore the basic purpose of an AND gate is to determine when the certain conditions are simultaneously true, as indicated by HIGH levels on all of its inputs, and to produce a HIGH on its output indicating this condition. The truth table of a two input AND gate is given below.

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The IC number of AND gate is 7408. Its internal diagram with pin number is given below.



OR Gate

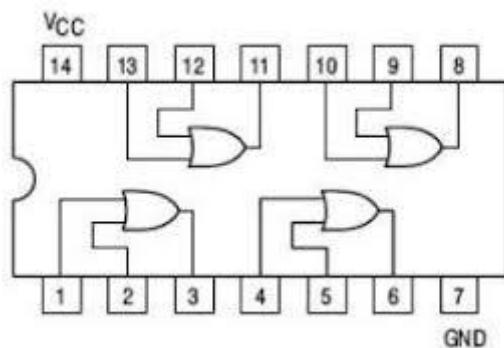
The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more inputs and one output. The figure shows the logic symbol of an OR gate with two inputs A and B. Inputs are on the left and output on the right of the symbol.



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

The operation of the OR gate is such that a HIGH output is produced when any of the inputs are HIGH. The output is Low only when all the inputs are LOW. Therefore the purpose of an OR gate is to determine when one or more of its inputs are HIGH and to produce a HIGH on its output to indicate the condition.

The IC number of OR gate is 7432. Its internal diagram with pin number is given below.



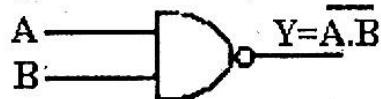
UNIVERSAL GATES

NAND & NOR gates are called universal gates, because using these gates we can implement the functions of any other gates.

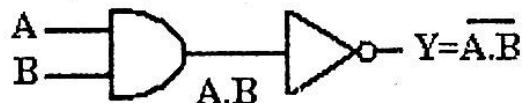
NAND Gate

The NAND gate is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output. The standard logic symbol for a two input

NAND gate and its equivalent circuit with an AND gate followed by an inverter is shown in figure.



Logical symbol for NAND gate



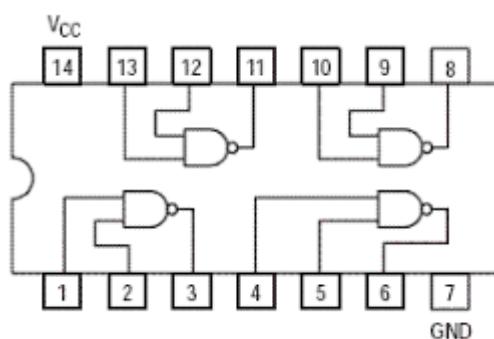
Equivalent circuit of a NAND gate
using AND and NOT gates

The NAND gate is very popular logic function because it is universal' function. That it can be use to construct and AND gate, an OR gate, an inverter (NOT) or any combination of these functions.

The logical operation of a NAND gate is such that a LOW output occurs only when all inputs are HIGH. When any of the inputs are LOW, the output will be HIGH. The truth table for the two input NAND gate is shown below.

Input		Output
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The IC number of NAND gate is 7400. Its internal diagram with pin number is given below.

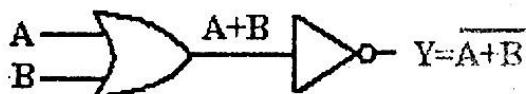


NOR Gate

The NOR gate is a contraction of NOT-OR and implies an OR function with an inverted output. The standard logic symbol of a two input NOR gate and its equivalent OR gate followed by an inverter is shown in figure. The NOR gate is also considered as “Universal” gate because of its capability to implement other logical operations.



Logical symbol for NOR gate

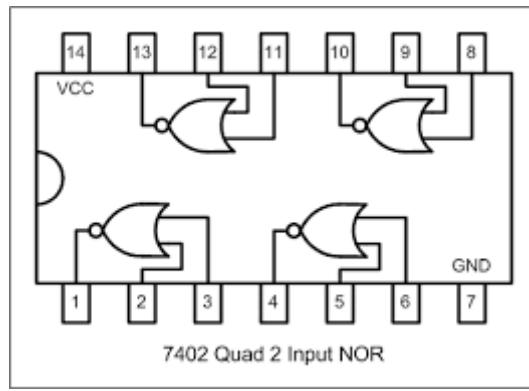


Equivalent circuit of a NOR gate
using OR and NOT gates

The logical operation of the NOR gate is such that a LOW output occurs when any of the inputs are HIGH. Only when all inputs are LOW, the output is HIGH. The truth table for the two input NOR gate is shown below.

Input		Output
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The IC number of NOR gate is 7402. Its internal diagram with pin number is given below.



EXCLUSIVE-OR gate

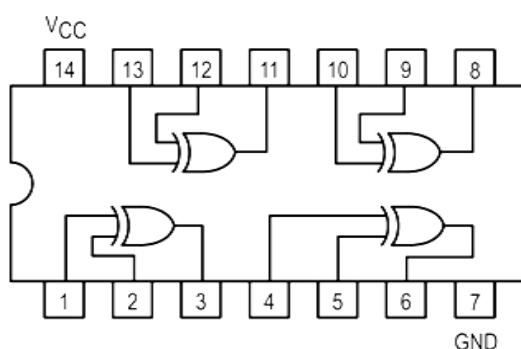
The EX-OR gate is a combinational logic, is widely used function for special arithmetic operations. Its logic symbol is shown in figure.



The logic operation of the EX-OR gate such that a HIGH output occurs when inputs are different. If inputs are equal out put will be LOW. The output expression of an EX-OR gate with two inputs A and B is given by $Y = A \bar{B} + \bar{A} B$. The truth table of the EX-OR gate is shown below.

Input		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

The IC number of EX-OR gate is 7486. Its internal diagram with pin number is given below.



EX-NOR Gate

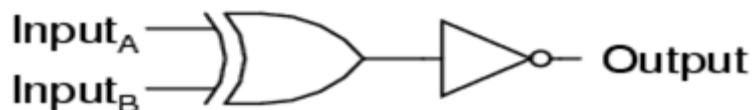
EX- NOR gate is formed by placing a NOT gate at the output of EX-OR gate. Its output is HIGH if the inputs are same and LOW if the inputs are different. In simple words, the output is 1 if the inputs are the same, otherwise the output is 0.

Exclusive-NOR gate

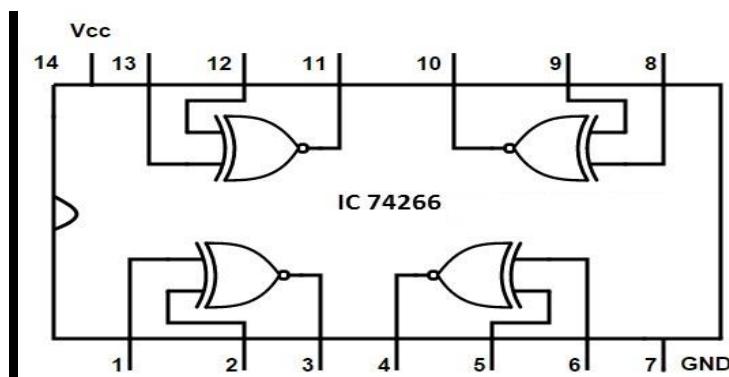


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Equivalent gate circuit



The IC number of EX-NOR gate is 74266. Its internal diagram with pin number is given below.



NOR gate as OR, NOT and gates

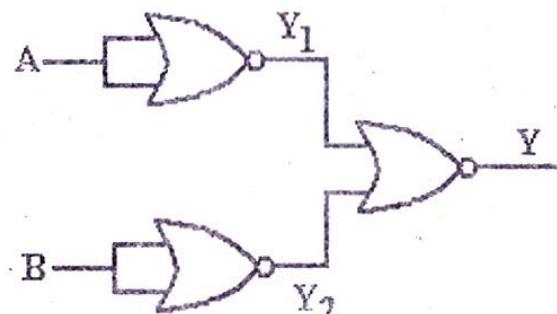
In order to convert a NOR gate into NOT circuit all the input's are connected together.

$$\text{If } A = 0, \text{ then } Y = \overline{0+0} = \overline{0} = 1 = \overline{A}$$

$$\text{If } A = 1, \text{ then } Y = \overline{1+1} = \overline{1} = 0 = \overline{A}$$



In order to convert a NOR gate into a AND gate, the inputs are first passed through a NOT operation and then to a NOR operation.



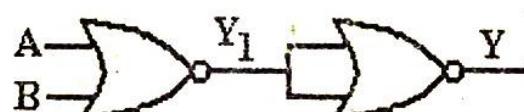
$$\text{Here } Y_1 = \overline{A} \text{ and } Y_2 = \overline{B}$$

$$\therefore Y = \overline{Y_1 + Y_2} = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}\overline{B}} = A \cdot B = A \cdot B$$

To convert a NOR gate onto OR gate, its inputs are fed to a NOR gate and then into a NOT operation. Here,

$$Y_1 = \overline{A+B}$$

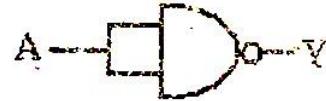
$$Y = \overline{Y_1} = \overline{\overline{A+B}} = A+B$$



NAND gate as OR, NOT and AND gates

While using NAND gate as an inverter (NOT operation), all the inputs are connected together.

If $A = 0$, then $Y = \overline{0.0} = \overline{0} = 1 = \overline{A}$

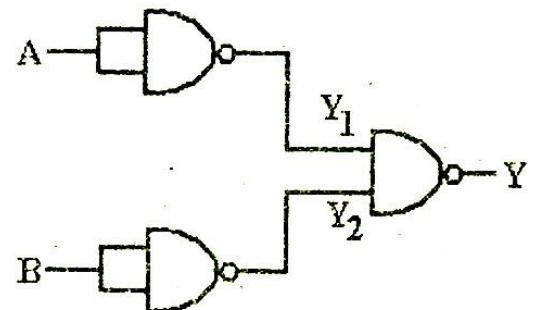
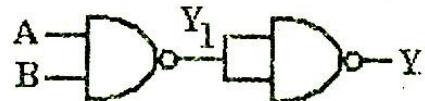


If $A = 1$, then $Y = \overline{1.1} = \overline{1} = 0 = \overline{A}$

To use NAND gate to simulate AND gate, its inputs are first passed through a NAND gate and then through a NOT gate.

$$Y_1 = \overline{\overline{A} \cdot \overline{B}}$$

$$Y = \overline{Y_1} = \overline{\overline{\overline{A} \cdot \overline{B}}} = \overline{\overline{\overline{A}} \cdot \overline{\overline{B}}} = A \cdot B$$



To use NAND gate to simulate OR gate, we use two NAND gates as NOT gate and the output of these NAND gates is again put through another NAND gate.

Here $Y_1 = \overline{\overline{A}}$ and $Y_2 = \overline{\overline{B}}$

$$\therefore Y = \overline{Y_1 \cdot Y_2} = \overline{\overline{\overline{A}}} + \overline{\overline{\overline{B}}} = \overline{\overline{\overline{A}}} + \overline{\overline{\overline{B}}} = \overline{\overline{\overline{A} + B}} = A + B$$

Boolean Expression for Gate Networks

A Boolean expression can be used to indicate a gate network, with a number of AND, OR and NOT gates connected in a particular manner. The form of the

Boolean expression does determine how many logic gates are used, what type of gates are used, and how they are connected together. The more complex the expression, the more complex the gate network will be. It is therefore an advantage to simplify an expression as much as possible in order to have the simplest gate network. There are certain forms of Boolean expressions that are more commonly used. The most important of these are the sum-of-products and the product-of-sums forms.

Sum-of-Products forms (SOP)

A product of two or more variables or their compliments is simply the AND function of those variables. The product of two variables can be expressed as AB , The product of three variables as ABC , the product of four variables $ABCD$, and so on. Similarly the sum in Boolean algebra is the same as the OR function. Therefore the sum-of-products expression is two or more AND functions OR-ed together. For example $(SC+BD)$ is a Sum-of-Products expression. It is a straight forward method as simple OR-ing of AND functions.

Product-of-Sums forms (POS)

The product-of-sums form can be thought of as the dual of the sum-of-products. It is, in terms of logic functions, the AND of two or more OR functions. For example $(A+C)(B+D)$ is a product-of-sums expression. This form is also leading itself to straightforward implementation with logic gates because it involves simply AND-ing two or more OR terms. A two level gate network will always result.

Boolean Algebra

In Boolean algebra, the binary digits are utilized to represent the two levels that occur within digital logic circuits. A binary 1 will represent a HIGH level and, a binary 0 will represent a LOW level in Boolean equations.

A bar can represent the compliment of a variable over the letter or using an apostrophe to the letter. For instance, for a variable represented by A , the compliment of A is \bar{A} (or $A!$). So; if $A = 1$, then $\bar{A} = 0$; or if $A = 0$ then $\bar{A} = 1$.

Boolean Addition and Multiplication

Addition in Boolean algebra involves variables having values of either a binary 1 or binary 0. The basic rules for Boolean addition are as follows.

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 1$$

In the application of Boolean algebra to logic circuits, Boolean addition is the same as the OR. But it differs from binary addition in the case where two 1s are added.

Multiplication in Boolean algebra involves the same basic rules governing binary multiplication. That is,

$$0 \cdot 0 = 0$$

$$0 \cdot 1 = 0$$

$$1 \cdot 0 = 0$$

$$1 \cdot 1 = 1$$

Boolean multiplication is same as the logical AND operation.

Logic Expressions

The operation of an inverter (NOT gate) can be expressed as follows. If the input variable is called A and the output variable is called Y, then, $Y = \bar{A}$ This expression states that the output is the complement of the input, so that, If $A = 0$, then $Y = 1$, and if $A = 1$, then $Y = 0$

The operation of a two input AND gate can be expressed in Boolean equation form as follows. If one input is A, the other input variable is B and the output variable is Y, then the Boolean expression for this basic gate function is $Y = A \cdot B$

The operation of two input OR gate can be expressed in Boolean equation form as follows. If one input is A and the other input is B, and the output is Y, then the Boolean expression is $Y = A + B$.

The Boolean expression for a two input NAND gate with inputs A and B, and output Y is given by $Y = \overline{AB}$

The Boolean expression for a two input NOR gate with input A and B, and output Y is given by $Y = \overline{A + B}$

Rules and Laws of Boolean algebra

The basic laws of Boolean algebra are the same as in ordinary algebra,

1. The commutative law
2. The associative law
3. The distributive law

Commutative Law

The commutative law of addition for two variables is written algebraically as,

$$A + B = B + A$$

This states that the order in which the variables are OR-ed makes no difference.
The commutative law of multiplication of two variables is,

$$A \cdot B = B \cdot A$$

This states that the order in which the variable and AND-ed make no differences.

Associative Law

The associative law of addition is stated as follows for three variables:

$$A + (B + C) = (A + B) + C$$

This law states that in the OR-ing of several variables the result is the same, regardless of the grouping of the variables. The associative law of multiplication is stated as follow for three variables

$$A(BC) = (AB)C$$

This law states that, it make no difference in what order the variables are grouped when AND-ing several variables.

Distributive Law

The distributive law is written for three variables as follows :

$$A(B+C) = AB + AC$$

This law states that OR-ing several variables and AND-ing the result with a single variable is equivalent to AND-ing the single variables with each of the several variables and then OR-ing the products.

Boolean Identities

The basic Boolean identities are

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A \cdot 0 = 0$
4. $A \cdot 1 = A$
5. $A + A = A$
6. $A + \bar{A} = 1$
7. $A \cdot A = A$
8. $A \cdot \bar{A} = 0$
9. $\bar{\bar{A}} = A$
10. $A + AB = A$
11. $A \cdot (A + B) = A$
12. $A + \bar{A}B = A + B$
13. $A \cdot (\bar{A} + B) = AB$
14. $(A + B)(A + C) = A + BC$

De'Morgans Theorems

The De'Morgans theorems for two variables A and B can be stated as follows.

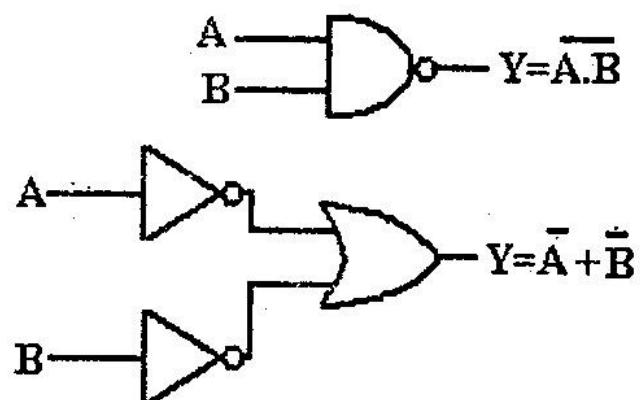
$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

The first theorem states that the complement of a product is equal to the sum of complements. In other words, it states that the compliment of two or more variables AND-ed is the same as OR-ing of the complements of each individual variable.

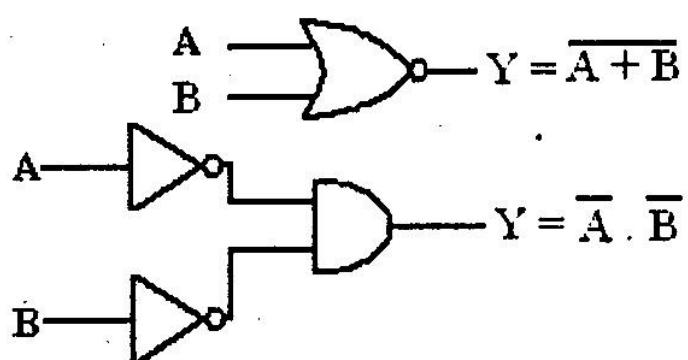
The second theorem states that, the complement of a sum is equal to the product of the complements. In other words, it states that the complement of two or more variables OR-ed is the same as the AND-ing of the complements of each individual variable.

These theorems are illustrated by the gate equivalencies and the truth tables as shown below.

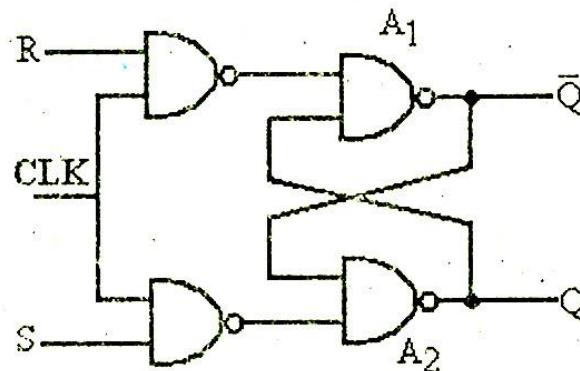


A	B	$\bar{A} \cdot \bar{B}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

A	B	$\bar{A} + \bar{B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0



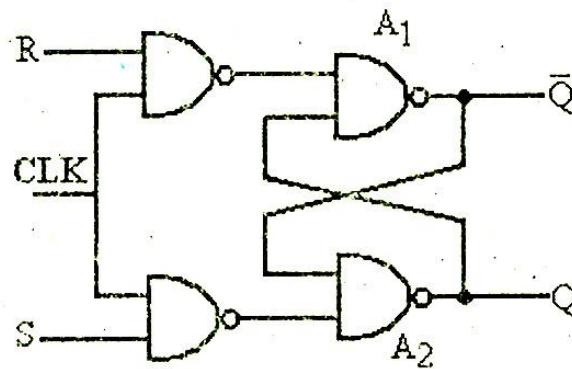
SR Flip - Flops using NAND Gates



S	R	Q	\bar{Q}
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Invalid	

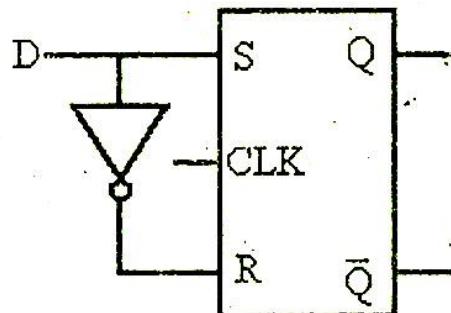
The normal assumption is that if the inputs are 0, then there should be no change in the outputs. However, for the SR latches using NAND gates, the input R=S=0 is forbidden or invalid, as they producing the switching action. So the inversion is required in the normal truth table of the SR latch to produce the above requirement. Hence, we can add two more NAND invertors as shown to produce the required inversion. See that the inversion has also changed the position of S and R. The truth table for this may be written as given below.

See also that the state (1, 1) is now illegal or forbidden . This circuit is generally called SR flop-flop. The circuit described just now is an asynchronous sequential circuit. An SR flop-flop can be converted into a synchronous sequential circuit by modifying the connections as shown in the figure below.



The circuit will be enabled if and only if clock input CLK = 1. If CLK = 0, both input NAND gates are disabled and the circuit will not function at all. Once CLK = 1, both the input NAND gate are enabled and the circuit will function as a normal SR flip-flop.

The Delay Flip-Flop (D flip –flop)



Consider the figure above, which shown an inverter between the JK or SR inputs. The new flip-flop is called as D flip-flop. It has only one input D and of this conversation it has only two of the four possible states for JK or SR inputs. That is, either $J=S=1$ or $K=R=0$. This is the set or reset condition. Thus the truth table will have only four entries as shown in table below.

As can be seen from the truth – table, when the input D is 0, whatever be the output, it will return to zero after the stipulated propagation delay t_p . Similarly if $D = 1$, output will jump to 1, irrespective of the previous value of the output. We thus find the flip-flop produces an output equal to that of the input, after a time-delay equal to t_p . This delay has given the flip-flop its name D or Delay flip-flop.

It may be noted that no ambiguous state is possible for the D flip-flop.

Application of D flip-flop

1. As a storage device in the shift registers.
2. As counting element in binary counters.
3. As delay element in computers.

UNIT -5 Field Effect Transistors

The field effect transistor is a three terminal device used for a variety of applications that match with that of bipolar junction transistor(BJT). It is a voltage-controlled device having three terminals: source, drain and gate.

It is unipolar device depending on either electron or hole conduction. For the FET an electric field is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities. One of the most important characteristics of FET is its high input impedance. The FETs are usually smaller in construction that is suitable for, making ICs.

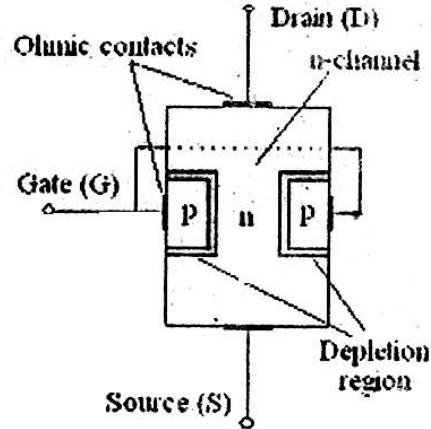
FETs can be classified as: The junction Field Effect Transistor (JFET) and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) The MOSFET category is further broken down into depletion and Enhancement type.

Comparison between BJT and FET

BJT	FET
Bipolar device	Unipolar device
Current controlled device	Voltage controlled device
Low input impedance	High input impedance
More noisy	Less noisy
Less stable to temperature variations	More stable to temperature variations
Occupies more space in ICs	Occupies less space in ICs
More size	Less size

Junction Field Effect Transistor (JFET)

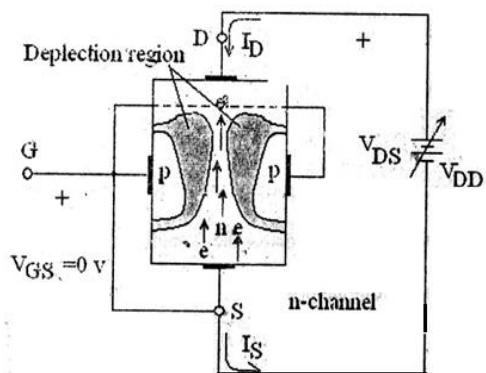
The JFET is a three terminal device with one terminal capable of controlling the current between the other two. The basic construction of an N-channel JFET is shown below.



The major part of the structure is the N type material that forms the channel between the embedded layers of P type material. The top of the N-type channel is connected through an ohmic contact to the terminal referred to as the Drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). Those two P-type materials are connected together and to the Gate (G) terminal. ie The Drain and Source are connected to the ends of the N-type channel and the gate to the two layers of P-types material.

Working of JFET

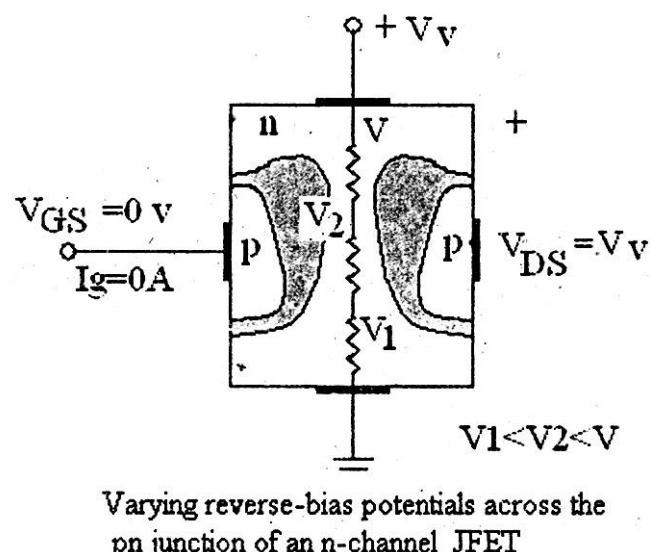
In the absence of any applied potential, the JFET has two PN junctions under no bias conditions. The result is depletion regions at each junction are shown in above figure. That resembles the same region of diode under no bias conditions.



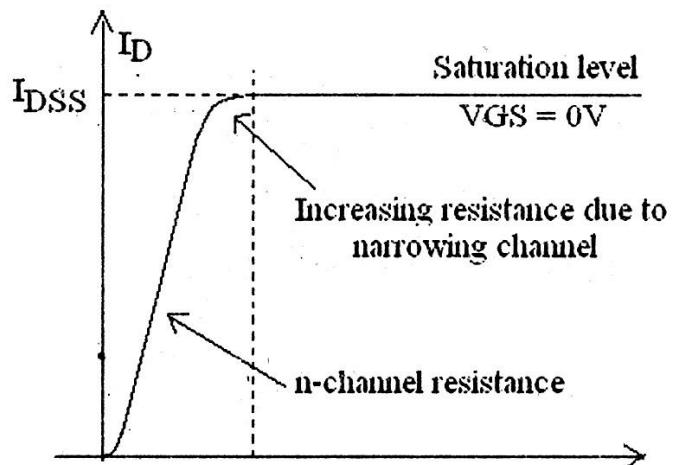
a. $V_{GS} = 0V$, V_{DS} some positive value

In the above figure a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS} = 0V$. The result is a gate and Source terminal at the same potential and a depletion region in the low end of the each P material similar to the distribution of the no bias conditions. The instant the voltage V_{DS} is applied, the electron will be drawn to the Drain terminal, establishing the conventional current I_D . The path of charge flow clearly reveals that the Drain and Source currents are equitant ($I_D = I_S$). Under these conditions a resistance of the N-channel between the Drain and Source limits the flow of charge.

It is important to note that the depletion region is wider near the top of both P-type materials. The reason for the changing in width of the region can be explained with the help of below figure. Assuming a uniform resistance in the N-channel, the resistance of the channel can be broken down to a number of divisions.



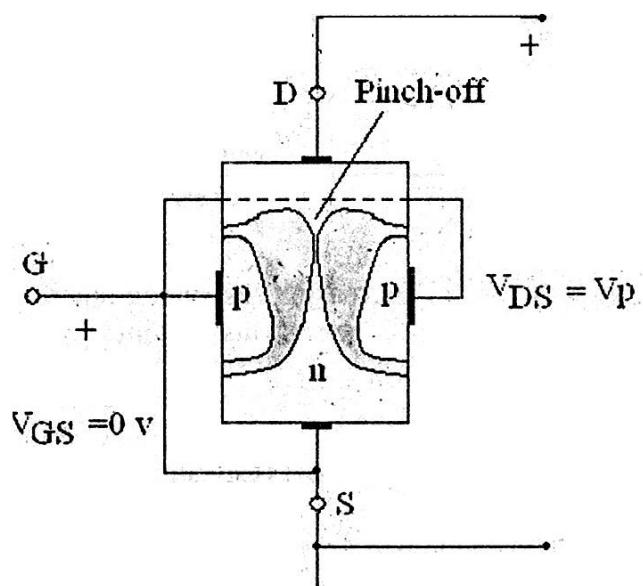
The current I_D will establish the voltage levels through the channel as shown in the figure. The voltage drop will be high at the drain end of channel than at the source end. This voltage drop reverse biases the PN junction. Thus the reverse bias and hence width of depletion region will be more at the drain end, the width of depletion region decreases gradually from drain end to source end of channel.



As the voltage V_{DS} is increased from a zero to a few volt the current will increases determined by Ohm's low and the plot of I_D verses V_{DS} will appear as shown in the above.

The relative straightness of the plot reveals that for the region of low values, the resistance is essentially constant.

As V_{DS} increases and approaches a level referred to as V_P , the depletion region will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of above figure to occur.



If V_{DS} were increased to a level where it appears that the two depletion regions would touch as shown in the above figure, a condition referred to, as pinch-off will

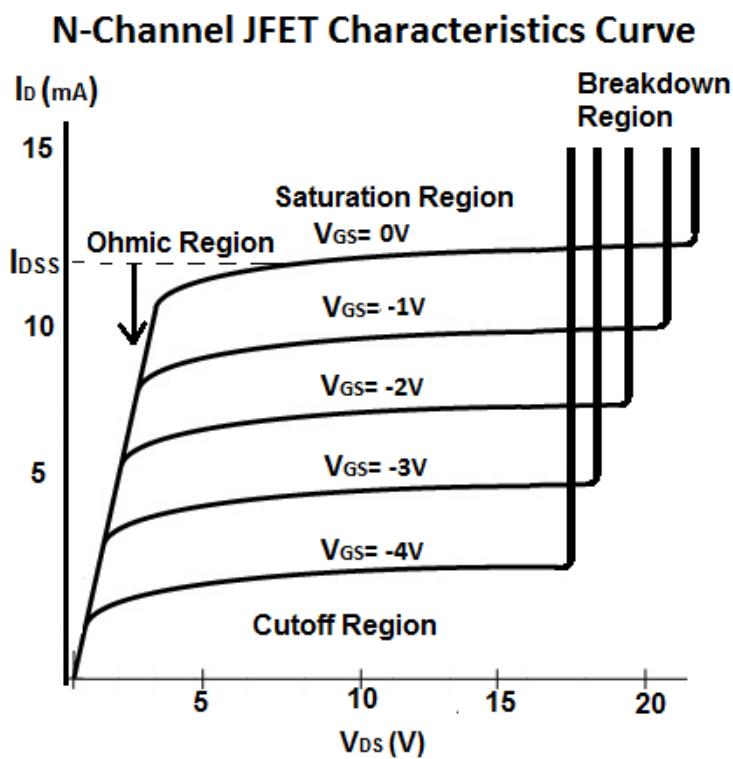
result. The level of V_{DS} that establish this condition is referred to as the pinch-off voltage and is denoted by V_P , as shown in the above figure,. In this case I_D maintains a saturation level defined as I_{DSS} . It is the maximum drain current for a JFET and is defined by the condition $V_{GS} = 0V$ and $V_{DS} > V_P$. That is the drain to source current with a short circuit connection from gate to source.

As V_{DS} is increased beyond V_P , the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains the same. In essence once $V_{DS} > V_P$ the JFET has the characteristics of a current source.

b. $V_{GS} < 0V$ and V_{DS} some positive value

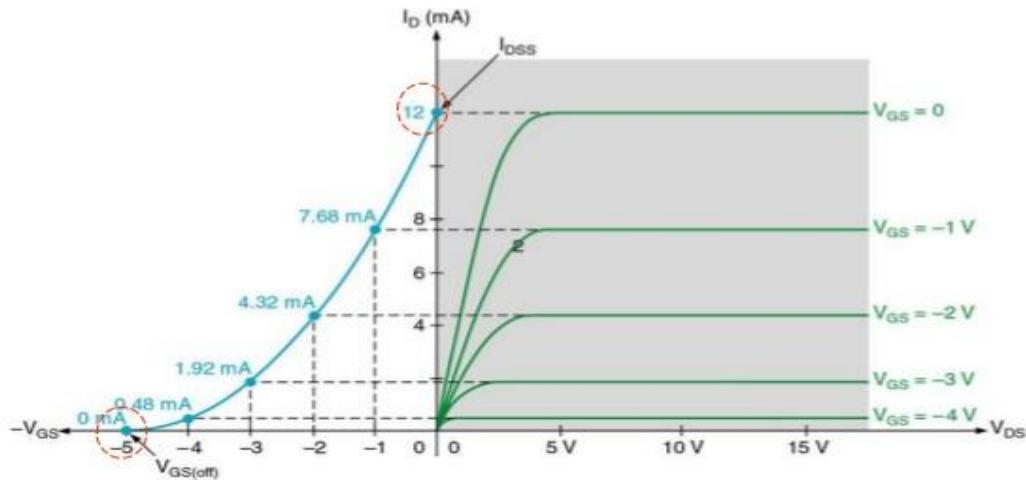
The voltage from Gate to Source V_{GS} is the controlling voltage of the JFET for the N-channel device. If V_{GS} is made negative, the pinch off will occur for lesser values of V_{DS} . Also the maximum possible current will be less. The equation of I_D for various values of V_{GS} is $I_D = I_{DSS} [1 - (V_{GS} / V_p)]^2$

Drain characteristics of N channel JFET



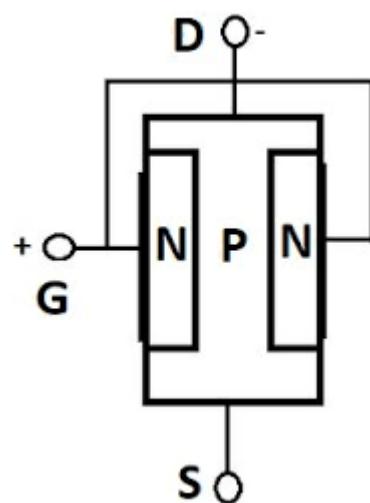
JFET Transfer Characteristic

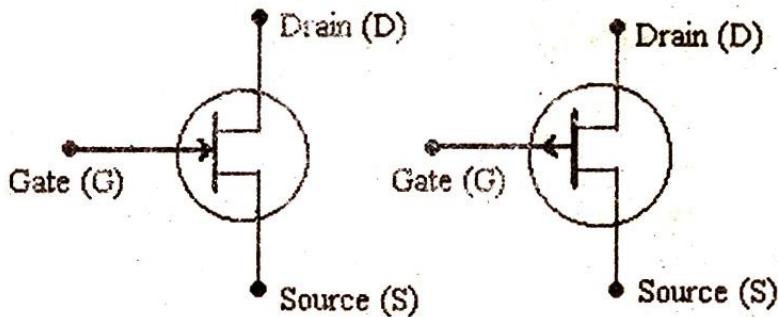
For an *n*-channel JFET, $V_{GS(off)}$ is negative. The relation between V_{GS} and I_D is known as the [transfer characteristic curve](#) (taken from the [drain characteristic curve](#)):



P-channel JFET

In P channel, JFET is constructed exactly in the same manner as the N-channel device with a reversal of the P and N type materials as shown in the above figure. In this type the pinch-off take place with a positive potential at its Gate terminal with respect to the Source. The structure of P channel JFET and symbols for the N-channel and P-channel JFETs are shown below figure.





Symbols of N-Channel JFET and P-Channel JFET

Important terms

1. Shorted gate drain current (I_{DSS})

It is the drain current with $V_{GS} = 0V$ and $V_{DS} \geq V_p$

2. Pinch off voltage (V_p)

It is the minimum value of V_{DS} with $V_{GS} = 0V$ at which pinch-off condition occurs and drain current becomes constant.

3. Gate-Source cut-off voltage ($V_{GS\text{ cut-off}}$)

It is the value of V_{GS} at which the channel is completely cut-off or blocked and drain current becomes zero.

Important Parameters of JFET

The main parameters of JFET are

1. AC drain resistance (r_d)

It is the ratio of change in drain-source voltage to the change in drain current at constant gate-source voltage.

$$r_d = (\Delta V_{DS} / \Delta I_D) \quad \text{with } V_{GS} = \text{constant}$$

2. Trans conductance or mutual conductance (g_m)

It is the ratio of change in drain current to the change in gate-source voltage at constant drain-source voltage.

$$g_m = (\Delta I_D / \Delta V_{GS}) \quad \text{with } V_{DS} = \text{constant}$$

3. Amplification factor (μ)

It is the ratio of change in drain-source voltage to the change in gate-source voltage at constant drain current.

$$\mu = (\Delta V_{DS} / \Delta V_{GS}) \quad \text{with } I_D = \text{constant}$$

Relation between JFET parameters

$$r_d g_m = (\Delta V_{DS} / \Delta I_D) . (\Delta I_D / \Delta V_{GS}) = (\Delta V_{DS} / \Delta V_{GS}) = \mu$$

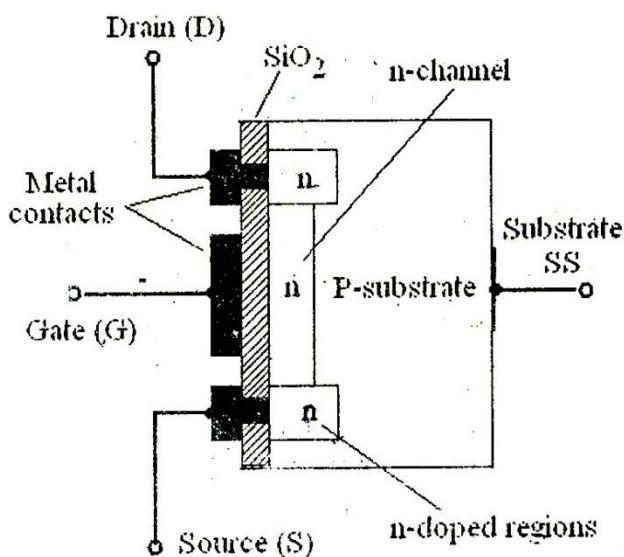
$$\text{ie } \mu = r_d \cdot g_m$$

MOSFET

The MOSFETs are broken down according to their basic mode of operation are depletion type and enhancement type, while the label MOSFET stands for Metal-Oxide-Semiconductor FET. Their characteristics and operation are different from each other.

Depletion type MOSFET

The basic construction the N-channel depletion type MOSFET is provided in the below figure.



A slab of P-type material is formed from a silicon base and is referred as the substrate. It is the foundation up on which the device will be constructed.

In some cases, the substrate is internally connected to the source terminal. The source and Drain terminals are connected through metallic contact through N-doped regions linked by an N-channel as shown in figure. The gate is also connected to the metal contact surface but remains isolated from the N-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field. The fact that SiO_2 layer is an insulating layer reveals that

- 1) There is no direct electrical connection between the gate terminal and the channel of a MOSFET
- 2) It is the insulating layer of SiO_2 in the MOSFET construction that
- 3) accounts for the very desirable high input impedance of the device.

Working of Depletion type MOSFET

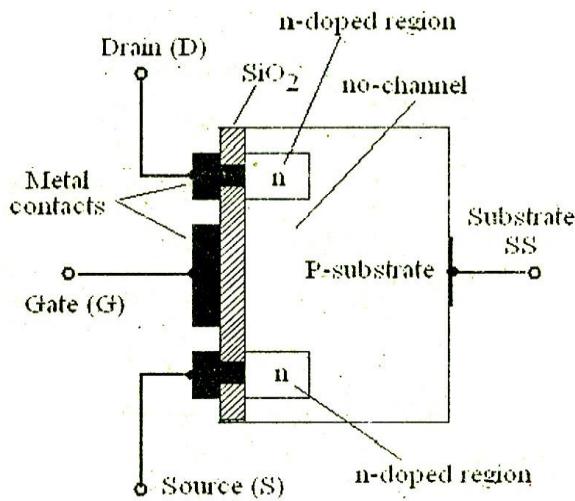
Depletion type MOSFET can be operated with $V_{GS} = 0$, $V_{GS} = -\text{ve}$ & $V_{GS} = +\text{ve}$. The V_{DS} is always +ve. The substrate is always short circuited to source.

When V_{GS} is 0V, electrons start to flow from source to drain through the N channel and a drain current similar to that established within the JFET flows from drain to source..

When V_{GS} is negative, electrons are repelled from N channel towards P substrate and holes are repelled from P substrate towards N channel. Then recombination occurs and due to which electrons within the N channel reduce or depleted. Then conductivity of N channel and hence drain current reduces. This mode of operation is called **depletion mode of operation**.

When V_{GS} is positive, minority electrons within the P substrate are repelled towards N channel. These electrons are deposited in the N channel thereby increasing its conductivity. Then drain current increases or enhances. This mode of operation is called **enhancement mode of operation**.

Enhancement type MOSFET



The figure above shows the basic construction of an N-channel enhancement type MOSFET. A slab of P-type materials formed from a silicon base and is referred to the substrate. As with the depletion type MOSFET the substrate is sometimes internally connected to the Source terminal, while in the other cases a fourth lead is made available for external control of its potential level. The Source and Drain terminals are again connected through metallic contact to N doped region but in the absence of a channel between the two N doped regions. This is the primary difference between the construction of a depletion type and enhancement type MOSFET – in the absence of a channel as a constructed element. The SiO₂ layer is still present to isolate the gate metallic platform form the region between the drain and source, but now it is simply separated from a section of the P type material. In short the construction of an Enhancement MOSFET is quite similar to that of the depletion type except for the absence of a channel between the Drain and Source terminals.

Working of Enhancement MOSFET

If V_{GS} is set 0V and a voltage applied between the Drain and Source of the device, in the absence of an N channel with free carriers, will result in a current of effectively 0A.

If positive voltage is applied between gate and source and source connected to substrate, the minority carriers within the outer region of P substrate are repelled

towards the inner regions of substrate , near the SiO_2 layer opposite to the gate. This forms a thin layer of electrons which stretches from source to drain. This effect is equivalent to produce a thin layer of N type channel in the P substrate. This layer of free electrons is called N type inversion layer.

The minimum value of gate to source voltage (V_{GS}), which produces the inversion layer is called threshold voltage represented by $V_{GS(th)}$ or V_T . When the voltage V_{GS} is less than V_T , no current will flow from drain to source even when a positive voltage is applied between drain and source. If V_{GS} is greater than V_T , the inversion layer connects drain and source and significant value of drain current flows. The value of Drain current will be high for greater values of V_{GS} . Thus the enhancement MOSFET works **only in enhancement mode**.

Applications of JFET & MOSFETs

JFET & MOSFETs are widely used as

- Electronic Switch
- Buffer amplifier
- RF amplifier
- Oscillator.

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