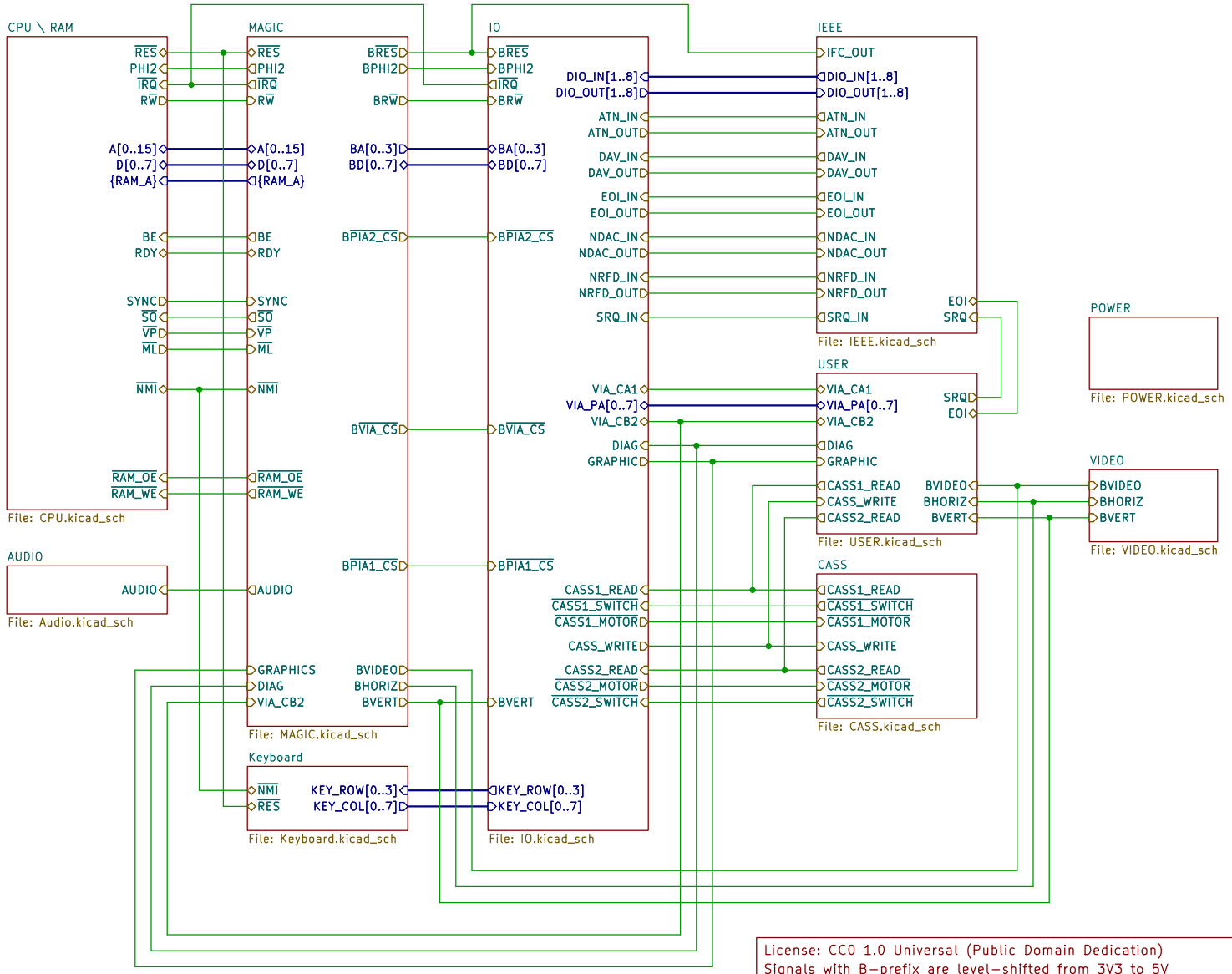
System Block Diagram



"If you don't use a current limiting resistor the LED will light up orange! Because of the fire! Because sometimes Daddy makes mistakes."

– Milo, Age 4.5

License: CC0 1.0 Universal (Public Domain Dedication)
Signals with B–prefix are level–shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher
https://is.gd/6hpvh6

Sheet: /
File: Mainboard.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023–10–01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 1/17

CPU and RAM operate at 3V3 so that the system bus and CPU control signals can be directly shared with the FPGA.

Level shifters are used for connections to the 5V I/O section. This design avoids needing level shifters for A[5..16].

The FPGA deasserts BE (Bus Enable) to transition the CPU's Address, Data, and RW buffers to high-Z when the FPGA drives the bus.

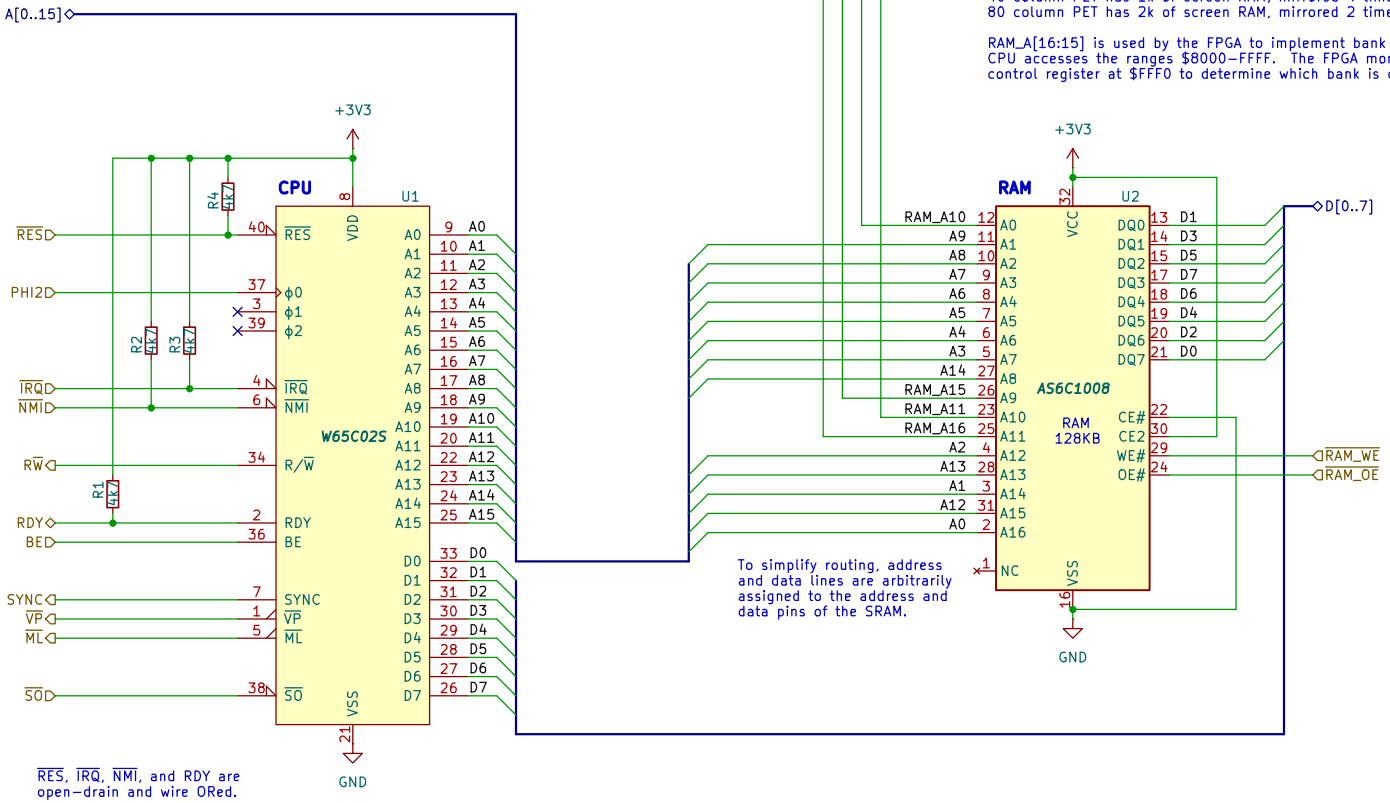
A single 128KB SRAM chip is used for the 32K main RAM, 64K expansion RAM, 2K display RAM, 2K character ROM and 26K system ROM. ROMs are initialized by the MCU on POR (via SPI -> bus bridge provided by the FPGA).

A[15:0] are the address of the shared system bus, which is connected to the CPU, IO, FPGA and most RAM address pins. The exceptions are RAM_A[16:15,11:10], which are driven exclusively by the FPGA.

RAM_A[11:10] is used by the FPGA to mirror display RAM when the CPU accesses the range $8000-8FFF.

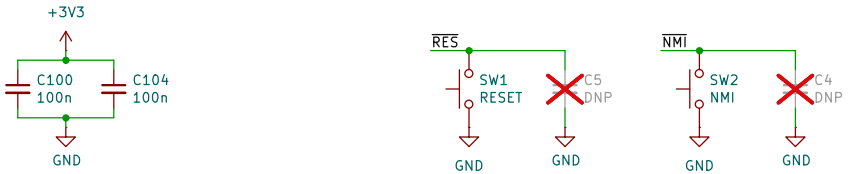
40 column PET has 1k of screen RAM, mirrored 4 times.
80 column PET has 2k of screen RAM, mirrored 2 times.

RAM_A[16:15] is used by the FPGA to implement bank switching when the CPU accesses the ranges $8000-FFFF. The FPGA monitors writes to the control register at $FFF0 to determine which bank is currently selected.



$\overline{RES}$, $\overline{IRQ}$, $\overline{NMI}$, and RDY are open-drain and wire ORed.

$\overline{SO}$ is driven high by the FPGA.

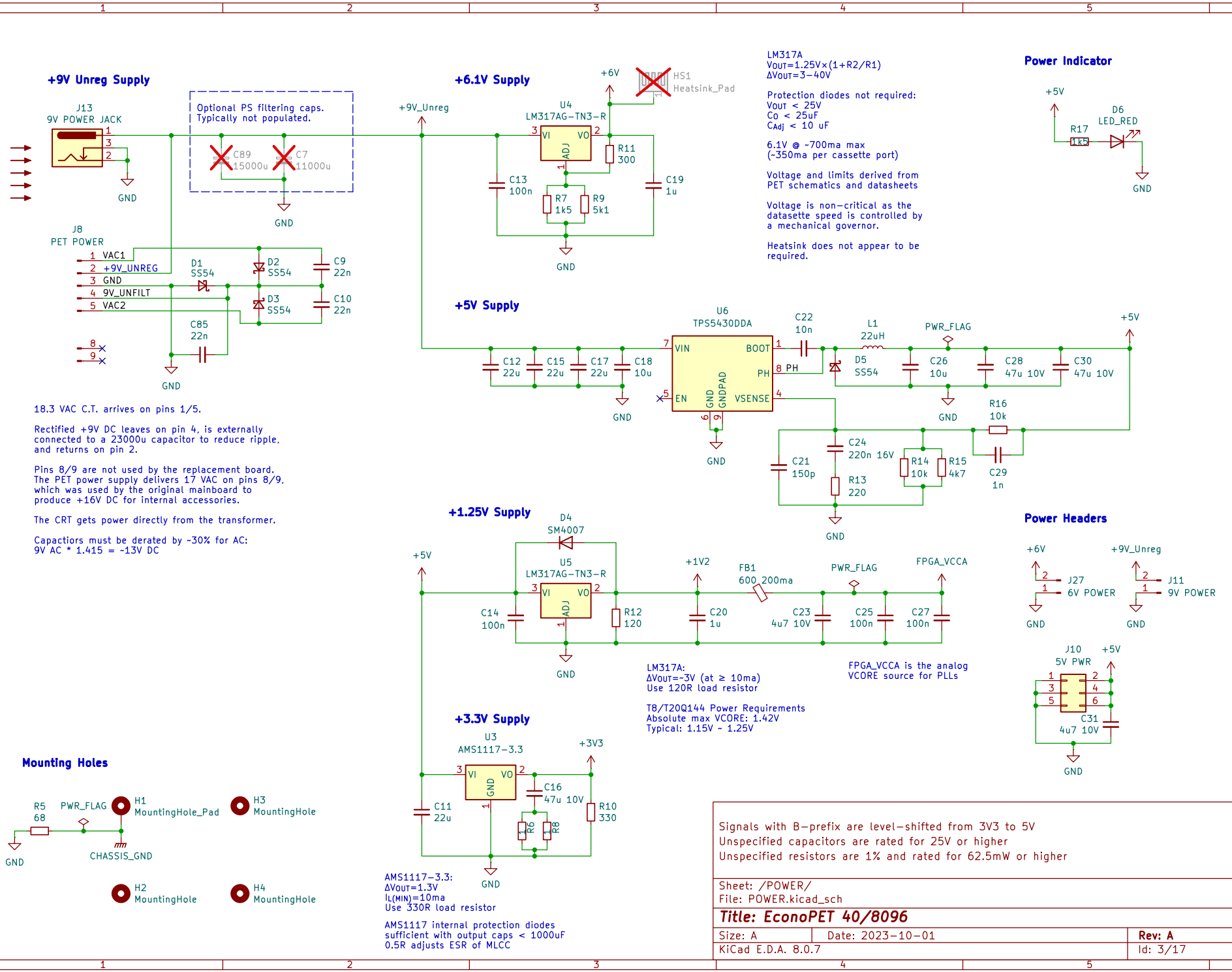


Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

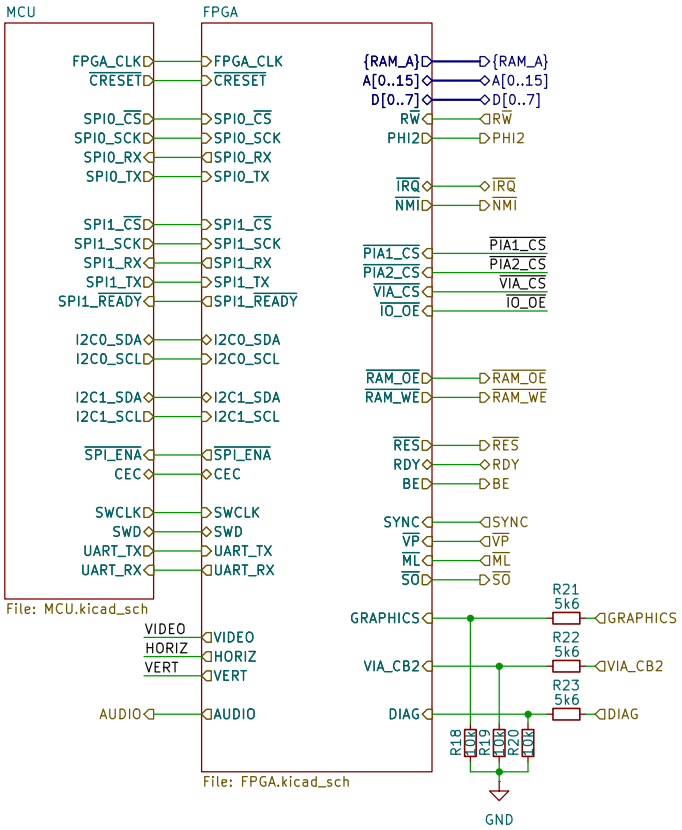
Sheet: /CPU \ RAM/
File: CPU.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 2/17


+9V Unreg Supply
J13
9V POWER JACK
Optional PS filtering caps.
Typically not populated.
C89
15000u
C7
11000u
GND
J8
PET POWER
1 VAC1
2 +9V_UNREG
3 GND
4 9V_UNFILT
5 VAC2
D1
SS54
D2
SS54
D3
SS54
C9
22n
C10
22n
C85
22n
18.3 VAC C.T. arrives on pins 1/5.
Rectified +9V DC leaves on pin 4, is externally connected to a 23000u capacitor to reduce ripple, and returns on pin 2.
Pins 8/9 are not used by the replacement board. The PET power supply delivers 17 VAC on pins 8/9, which was used by the original mainboard to produce +16V DC for internal accessories.
The CRT gets power directly from the transformer.
Capactiors must be derated by ~30% for AC:
9V AC * 1.415 = ~13V DC
+9V_Unreg
+6.1V Supply
U4
LM317AG-TN3-R
VI
VO
ADJ
R11
300
R7
1k5
R9
5k1
C13
100n
C19
1u
+6V
HS1
Heatsink_Pad
LM317A
VOUT=1.25V×(1+R2/R1)
ΔVOUT=3–40V
Protection diodes not required:
VOUT < 25V
CO < 25uF
CAdj < 10 uF
6.1V @ ~700ma max
(~350ma per cassette port)
Voltage and limits derived from PET schematics and datasheets
Voltage is non-critical as the datasette speed is controlled by a mechanical governor.
Heatsink does not appear to be required.
Power Indicator
+5V
D6
LED_RED
R17
1k5
GND
+5V Supply
U6
TPS5430DDA
VIN
BOOT
PH
EN
VSENSE
GND
GNDPAD
C12
22u
C15
22u
C17
22u
C18
10u
C22
10n
L1
22uH
D5
SS54
PWR_FLAG
C26
10u
C28
47u 10V
C30
47u 10V
R16
10k
C29
1n
C24
220n 16V
R13
220
C21
150p
R14
10k
R15
4k7
+1.25V Supply
D4
SM4007
U5
LM317AG-TN3-R
C14
100n
R12
120
C20
1u
+1V2
FB1
600_200ma
C23
4u7 10V
C25
100n
C27
100n
FPGA_VCCA
LM317A:
ΔVOUT=~3V (at ≥ 10ma)
Use 120R load resistor
T8/T20Q144 Power Requirements
Absolute max VCORE: 1.42V
Typical: 1.15V ~ 1.25V
FPGA_VCCA is the analog VCORE source for PLLs
Power Headers
J27
6V POWER
J11
9V POWER
J10
5V PWR
C31
4u7 10V
+3.3V Supply
U3
AMS1117-3.3
C11
22u
C16
47u 10V
R10
330
R6
R8
+3V3
AMS1117-3.3:
ΔVOUT=1.3V
IL(MIN)=10ma
Use 330R load resistor
AMS1117 internal protection diodes sufficient with output caps < 1000uF
0.5R adjusts ESR of MLCC
Mounting Holes
H1
MountingHole_Pad
H2
MountingHole
H3
MountingHole
H4
MountingHole
R5
68
PWR_FLAG
CHASSIS_GND
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher
Sheet: /POWER/
File: POWER.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 3/17

Magic



MCU responsibilities:
- Generate FPGA_CLK
- Configure FPGA at POR
- Initialize SRAM with ROM images
- Read back video RAM and output to HDMI (bit-banged DVI)
- Report USB keyboard matrix to FPGA

FPGA responsibilities:
- Timing / address decoding
- Native PET video generation / CRTC
- Expose sysem bus to MCU (via SPI)
- Intercept PIA1 to inject USB keyboard

SRAM is shared between the 6502 and the FPGA by using an effective bus speed of 8 MHz taking turns in round-robin fashion.

From the CPU and I/O chip's perspective, PHI2 is "stretched" with a 1/8th duty cycle. From the FPGA's perspective, there is an 8 MHz clock and 8 clock enable signals, which are used as follows:

0: Read/write to SRAM to service SPI request from MCU
1: Read even character from VRAM
2: Read even character bitmat from "ROM"
3: Read odd character from VRAM
4: Read odd character from "ROM"
5: Read/write to SRAM to service SPI request from MCU
6: Setup for next CPU cycle
7: Pulse PHI2

(Note: Above subject to change with firmware updates.)

Shift 5V -> 3V3:

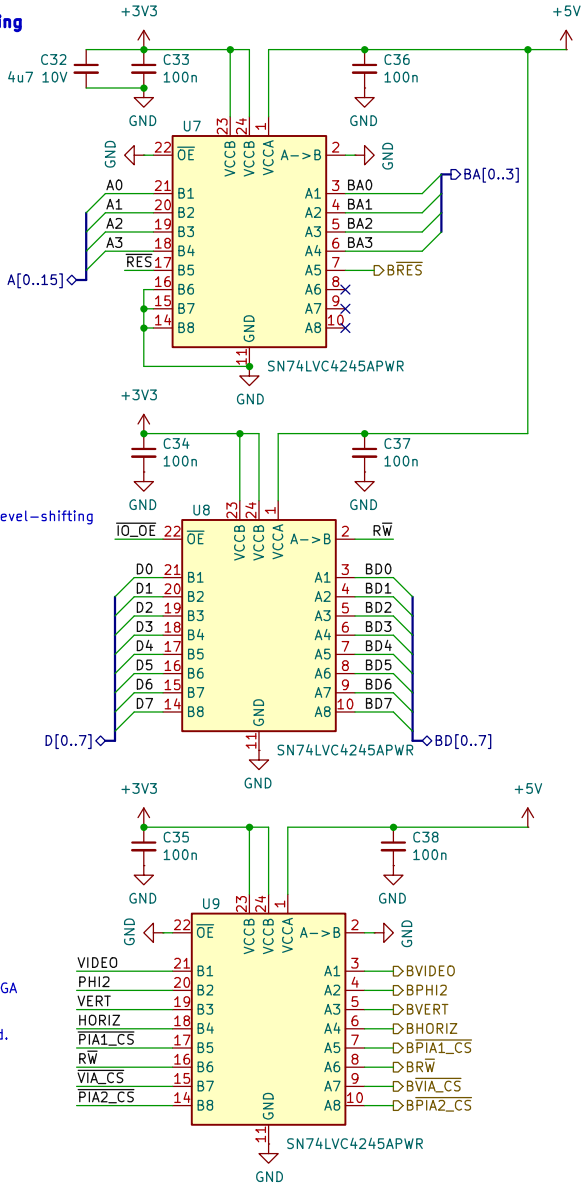
VOUT = VIN * (R2 / (R1 + R2)
VIN = 5.1V
R1 = 5.6k - 1%
R2 = 10k + 1%
VOUT = 3.29V

PIAs and VIA operate at 5V logic levels for compatible I/O.

CPU and RAM operate at the same 3V3 logic levels as the FPGA and MCU to reduce the amount of level shifting required.

D[0..7] are the only bidirectional lines that need to be shifted. The direction of D[0..7] is controlled by RW.

Level Shifting



IO_OE does not require level-shifting (high @ 2V)

Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /MAGIC/
File: MAGIC.kicad_sch

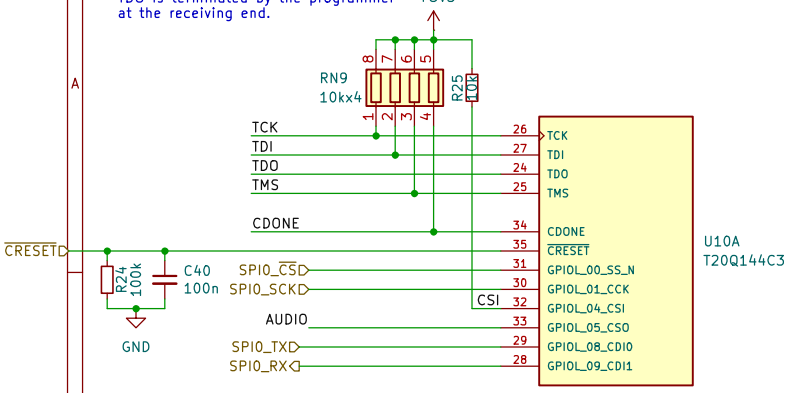
Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 4/17

CDONE is open drain and requires
pullup to enter user mode.

TDO is terminated by the programmer
at the receiving end.

TODO: Cleanup

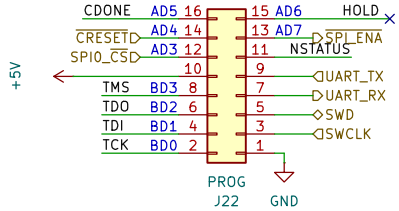


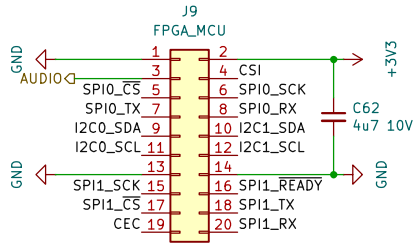
Pull CRESET low to reset FPGA until MCU is ready.
Note that MCU drives CRESET through 10k resistor
so it can be overridden by programmer when connected.

Pull CSI high to enable FPGA configuration
Pull TEST_N high to deactivate test mode
Pull CBUS[2:0] high for SPI x1
Leave CBSEL[1:0] floating (not using multi-image)

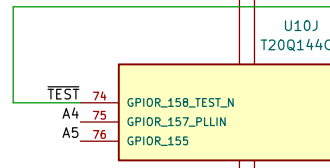
MCU config:
MCU drives SS_N low to select passive SPI
MCU transitions CRESET_N low -> high to begin (320 ns)
MCU sends bitsteam via CCK and CDIO
FPGA asserts CDONE on success, NSTATUS on error

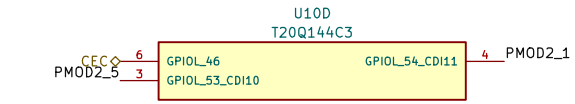
PROG drives SPI_EN low during SPI Passive or JTAG
programming. We use this to reset the MCU.

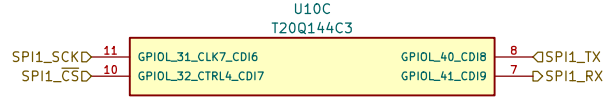


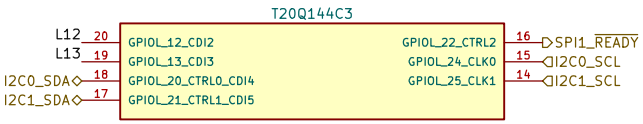


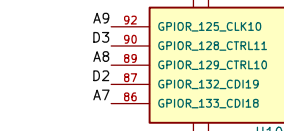
During configuration, all GPIO
The LVDS as GPIO pins are tri

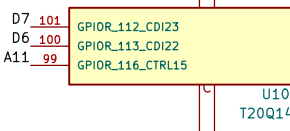


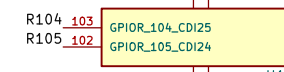


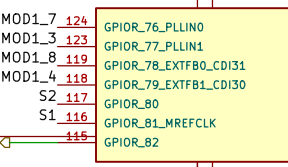


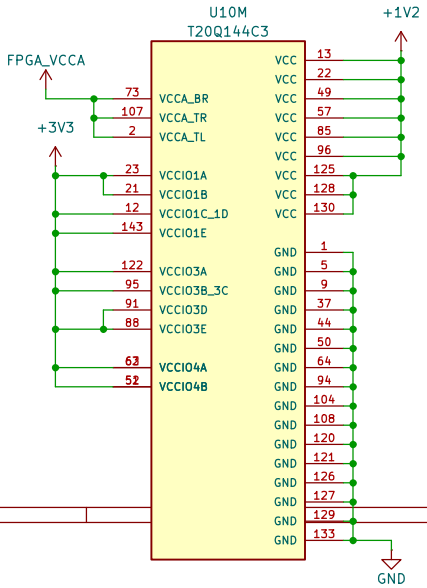


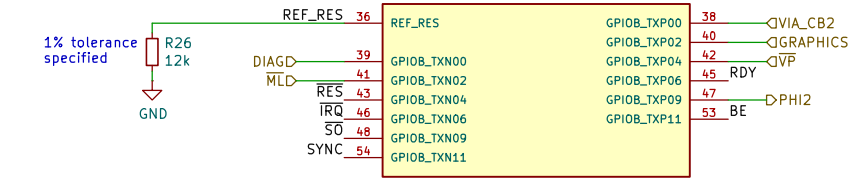


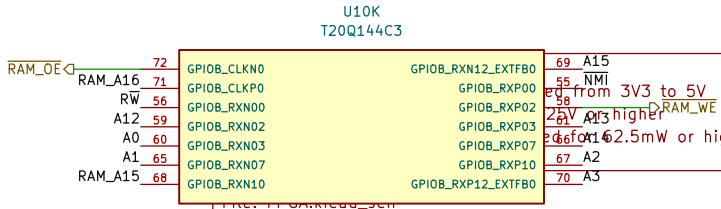


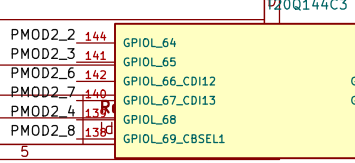








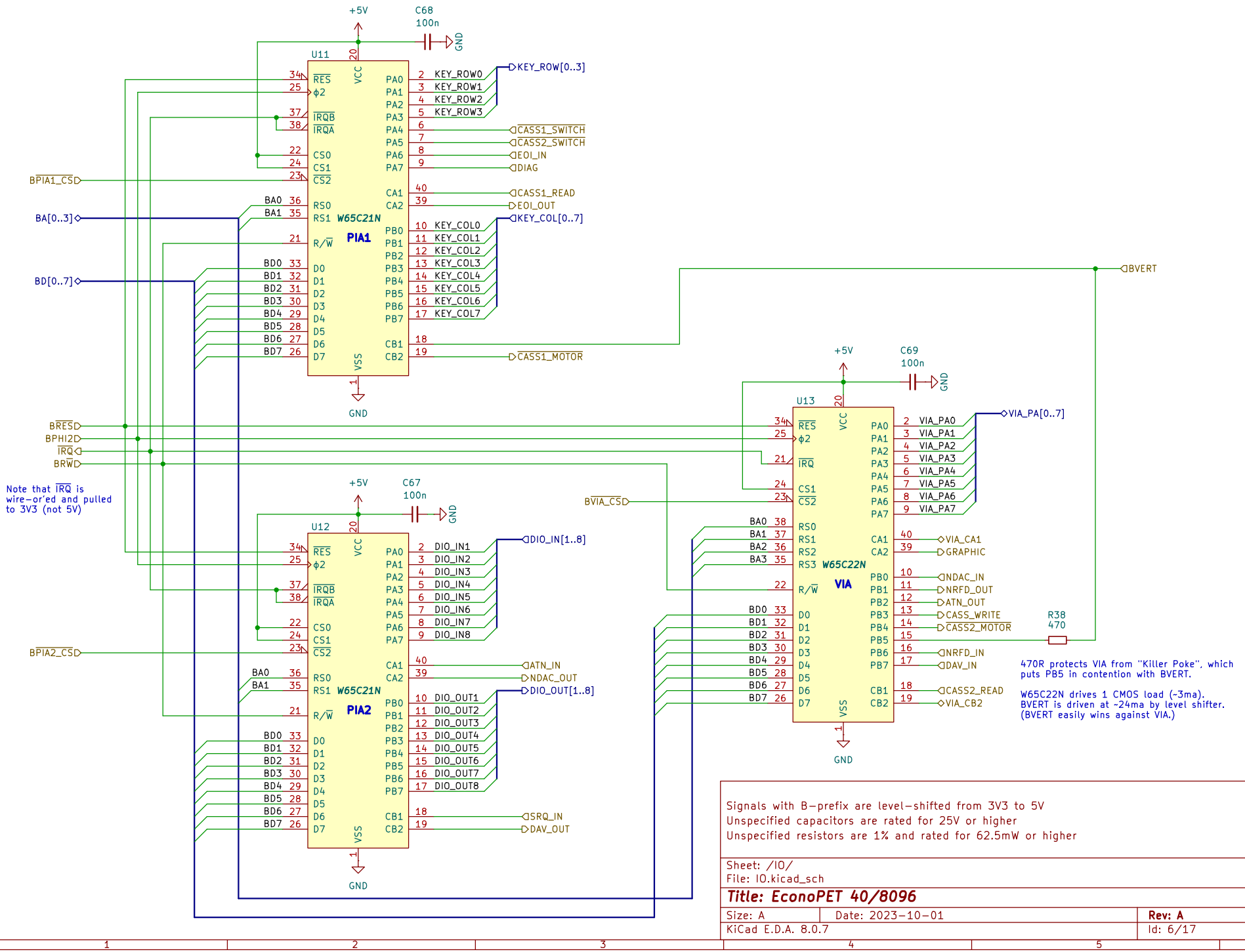


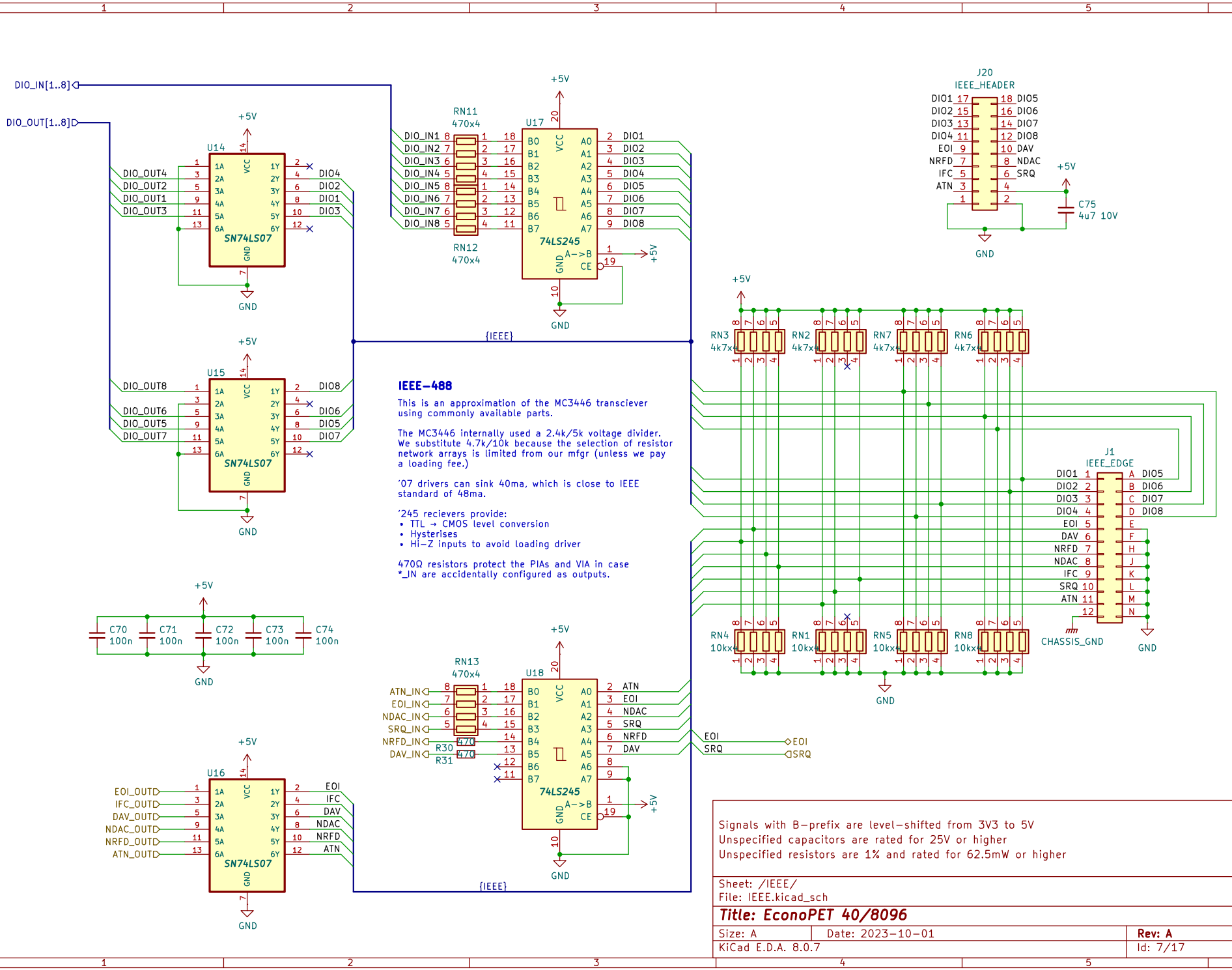


ed from 3V3 to 5V
25V or higher
for 62.5mW or higher

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01
KiCad E.D.A. 8.0.7	

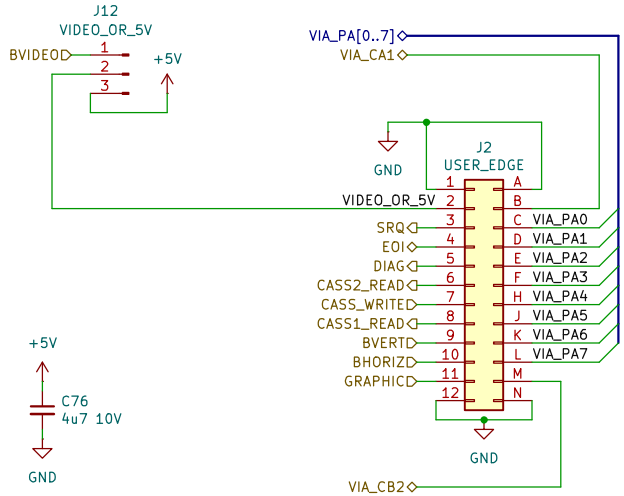

U11
W65C21N
PIA1
U12
W65C21N
PIA2
U13
W65C22N
VIA
+5V
GND
C68
100n
C67
100n
C69
100n
BPIA1_CS
BPIA2_CS
BVIA_CS
BA[0..3]
BD[0..7]
BRES
BPHI2
IRQ
BRW
BVERT
KEY_ROW[0..3]
KEY_COL[0..7]
CASS1_SWITCH
CASS2_SWITCH
EOI_IN
DIAG
CASS1_READ
EOI_OUT
CASS1_MOTOR
DIO_IN[1..8]
DIO_OUT[1..8]
ATN_IN
NDAC_OUT
SRQ_IN
DAV_OUT
VIA_PA[0..7]
VIA_CA1
GRAPHIC
NDAC_IN
NRFD_OUT
ATN_OUT
CASS_WRITE
CASS2_MOTOR
NRFD_IN
DAV_IN
CASS2_READ
VIA_CB2
R38
470
Note that IRQ is wire-or'ed and pulled to 3V3 (not 5V)
470R protects VIA from "Killer Poke", which puts PB5 in contention with BVERT.
W65C22N drives 1 CMOS load (~3ma).
BVERT is driven at ~24ma by level shifter.
(BVERT easily wins against VIA.)
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher
Sheet: /IO/
File: IO.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 6/17

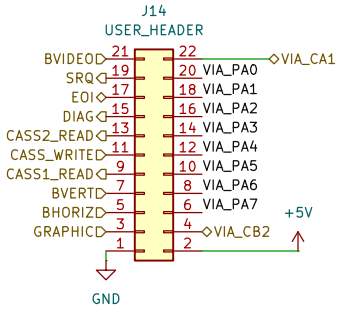

DIO_IN[1..8]
DIO_OUT[1..8]
U14
SN74LS07
DIO_OUT4
DIO_OUT2
DIO_OUT1
DIO_OUT3
DIO4
DIO2
DIO1
DIO3
U15
DIO_OUT8
DIO_OUT6
DIO_OUT5
DIO_OUT7
DIO8
DIO6
DIO5
DIO7
U16
EOI_OUT
IFC_OUT
DAV_OUT
NDAC_OUT
NRFD_OUT
ATN_OUT
EOI
IFC
DAV
NDAC
NRFD
ATN
RN11
470x4
RN12
470x4
U17
74LS245
DIO_IN1
DIO_IN2
DIO_IN3
DIO_IN4
DIO_IN5
DIO_IN6
DIO_IN7
DIO_IN8
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
{IEEE}
RN13
470x4
U18
74LS245
ATN_IN
EOI_IN
NDAC_IN
SRQ_IN
NRFD_IN
DAV_IN
R30
R31
470
ATN
EOI
NDAC
SRQ
NRFD
DAV
{IEEE}
C70
C71
C72
C73
C74
100n
RN3
RN2
RN7
RN6
RN4
RN1
RN5
RN8
4k7x4
10kx4
J20
IEEE_HEADER
DIO1
DIO2
DIO3
DIO4
EOI
NRFD
IFC
ATN
DIO5
DIO6
DIO7
DIO8
DAV
NDAC
SRQ
C75
4u7 10V
J1
IEEE_EDGE
CHASSIS_GND
GND
+5V
IEEE-488
This is an approximation of the MC3446 transciever using commonly available parts.
The MC3446 internally used a 2.4k/5k voltage divider. We substitute 4.7k/10k because the selection of resistor network arrays is limited from our mfgr (unless we pay a loading fee.)
'07 drivers can sink 40ma, which is close to IEEE standard of 48ma.
'245 recievers provide:
• TTL → CMOS level conversion
• Hysterises
• Hi-Z inputs to avoid loading driver
470Ω resistors protect the PIAs and VIA in case *_IN are accidentally configured as outputs.
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher
Sheet: /IEEE/
File: IEEE.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 7/17

USER PORT

The VIDEO_OR_5V jumper allows partial compatibility
with VIC-20 and C64 user port peripherals by delivering
+5V on PIN_2 instead of PET video.

(Example: TexElec SNES adapter)



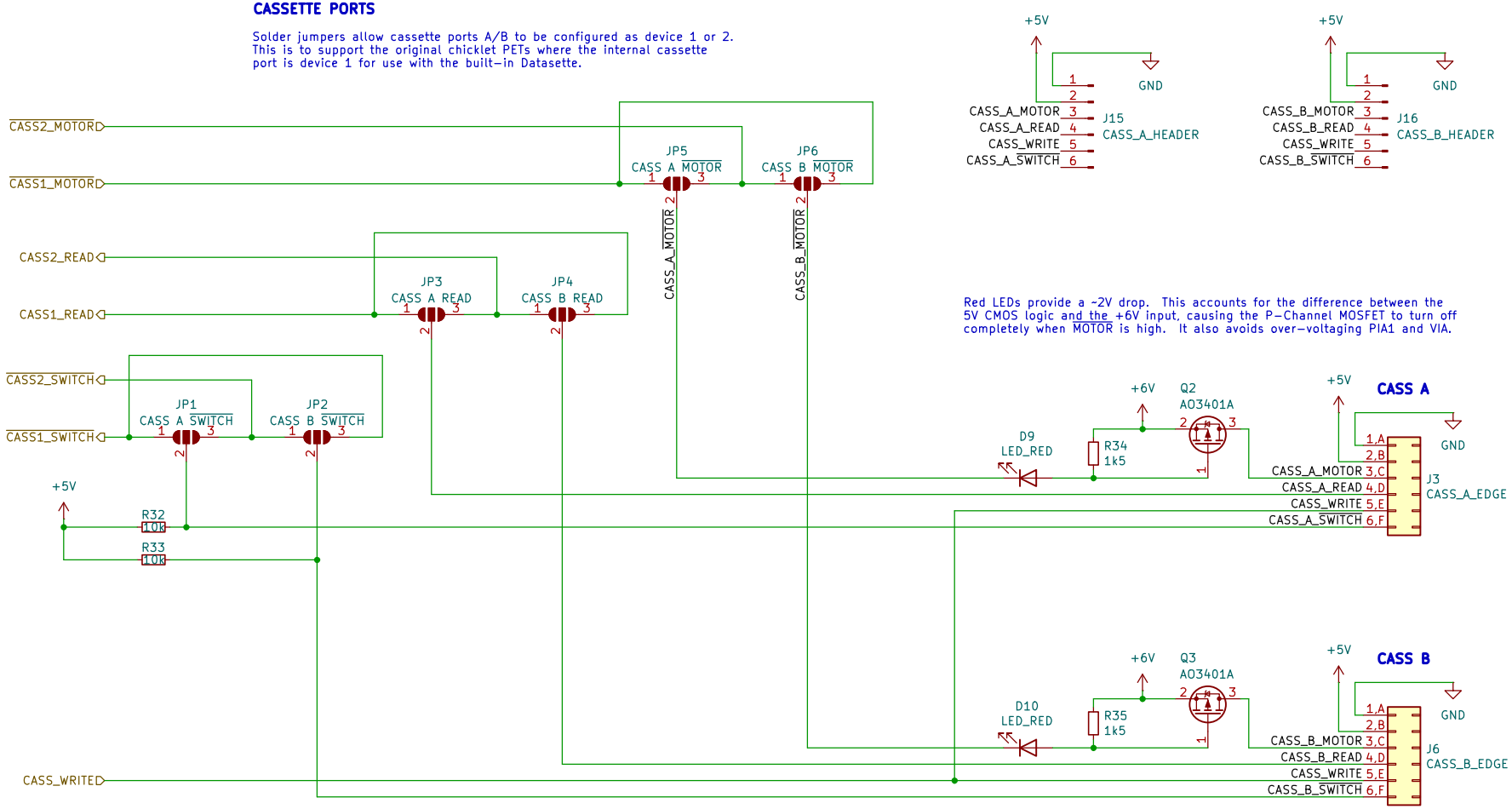


Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /USER/		
File: USER.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 8/17

CASSETTE PORTS

Solder jumpers allow cassette ports A/B to be configured as device 1 or 2.
This is to support the original chicklet PETs where the internal cassette
port is device 1 for use with the built-in Datasette.



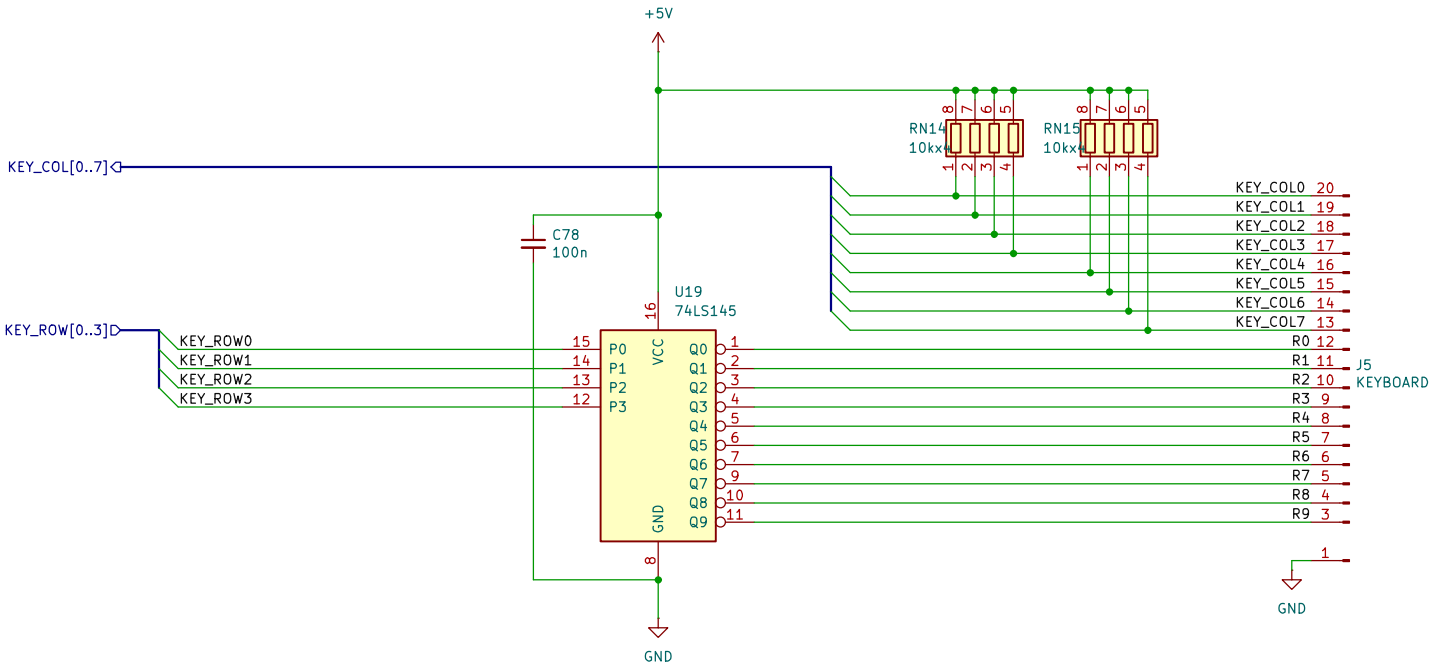
Place decoupling cap near CASS_B connector.
CASS_A has sufficient decoupling nearby.

Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /CASS/
File: CASS.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 9/17



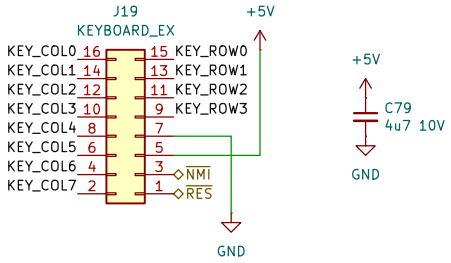
KEYBOARD

The PET uses a 74LS145 BCD-to-decimal to sink the active row of an 8x10 keyboard matrix. When a key in the selected row is pressed, it sinks the 10k pullup of the corresponding column.

The '145 is active low / open collector, capable of sinking an excessive 80ma for driving lamps in the pre-LED era. This is more than enough to sink all eight of the 10k pullups if the user pushes all keys for currently select row.

The KEYBOARD_EX header conveniently exposes the PA[3:0] and PB[7:0] lines for users interested in building adapters to support non-PET keyboards. It also exposes NMI for RESTORE and RES for reset.

http://www.6502.org/users/sjgray/projects/petexpkbd/index.html



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /Keyboard/
File: Keyboard.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 10/17

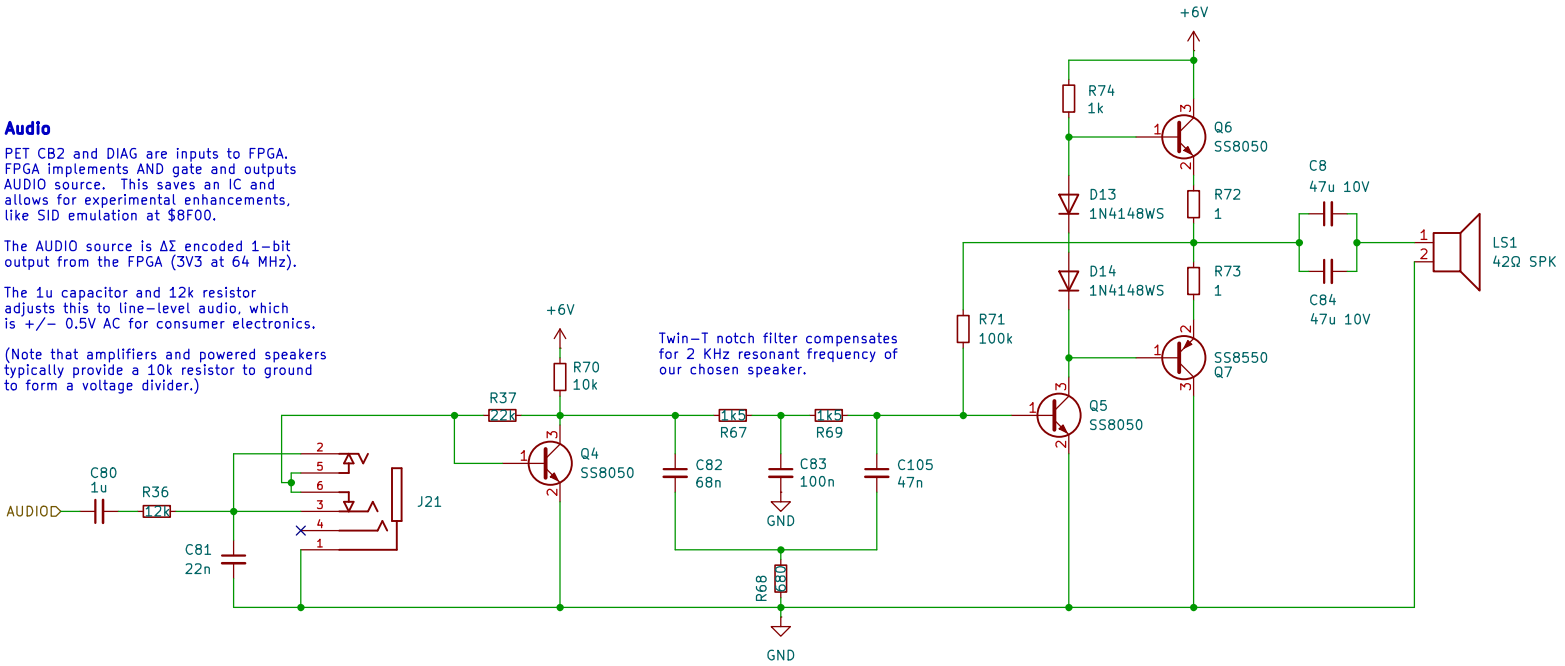
Audio

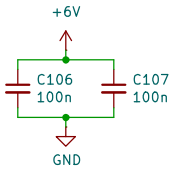
PET CB2 and DIAG are inputs to FPGA.
FPGA implements AND gate and outputs
AUDIO source. This saves an IC and
allows for experimental enhancements,
like SID emulation at $8F00.

The AUDIO source is ΔΣ encoded 1-bit
output from the FPGA (3V3 at 64 MHz).

The 1u capacitor and 12k resistor
adjusts this to line-level audio, which
is +/- 0.5V AC for consumer electronics.

(Note that amplifiers and powered speakers
typically provide a 10k resistor to ground
to form a voltage divider.)





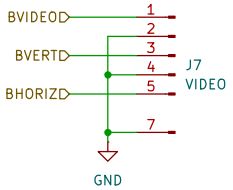
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /AUDIO/
File: Audio.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 11/17

VIDEO HEADER



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /VIDEO/
File: VIDEO.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 12/17

MCU

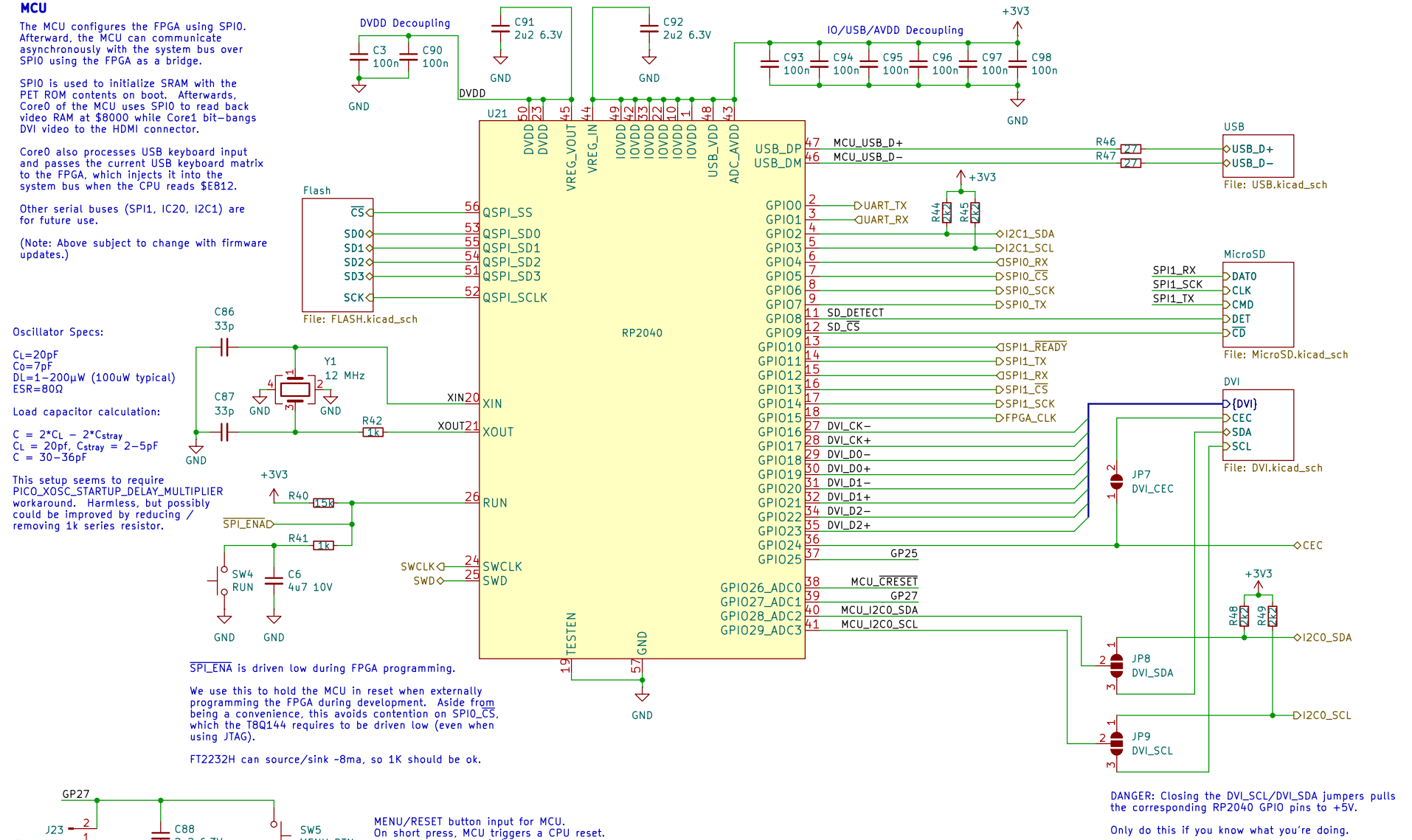
The MCU configures the FPGA using SPI0. Afterward, the MCU can communicate asynchronously with the system bus over SPI0 using the FPGA as a bridge.

SPI0 is used to initialize SRAM with the PET ROM contents on boot. Afterwards, Core0 of the MCU uses SPI0 to read back video RAM at $8000 while Core1 bit-bangs DVI video to the HDMI connector.

Core0 also processes USB keyboard input and passes the current USB keyboard matrix to the FPGA, which injects it into the system bus when the CPU reads $E812.

Other serial buses (SPI1, IC20, I2C1) are for future use.

(Note: Above subject to change with firmware updates.)



Oscillator Specs:

C_L=20pF
C_0=7pF
DL=1-200µW (100uW typical)
ESR=80Ω

Load capacitor calculation:

$C = 2*C_L - 2*C_{stray}$
C_L = 20pf, C_{stray} = 2-5pF
C = 30-36pF

This setup seems to require PICO_XOSC_STARTUP_DELAY_MULTIPLIER workaround. Harmless, but possibly could be improved by reducing / removing 1k series resistor.

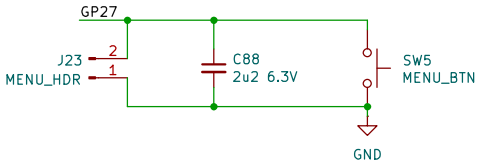
$\overline{SPI\_ENA}$ is driven low during FPGA programming.

We use this to hold the MCU in reset when externally programming the FPGA during development. Aside from being a convenience, this avoids contention on SPI0_$\overline{CS}$, which the T8Q144 requires to be driven low (even when using JTAG).

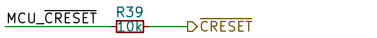
FT2232H can source/sink ~8ma, so 1K should be ok.

DANGER: Closing the DVI_SCL/DVI_SDA jumpers pulls the corresponding RP2040 GPIO pins to +5V.

Only do this if you know what you're doing.

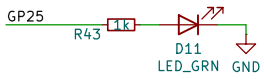


MENU/RESET button input for MCU.
On short press, MCU triggers a CPU reset.
On long press, MCU (re)enters boot menu.



10k resistor on $\overline{CRESET}$ enables programmer to override MCU during development.

MCU status LED visible when looking into the PET expansion slot. (Other LEDs are only visible when the PET case is open.)



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

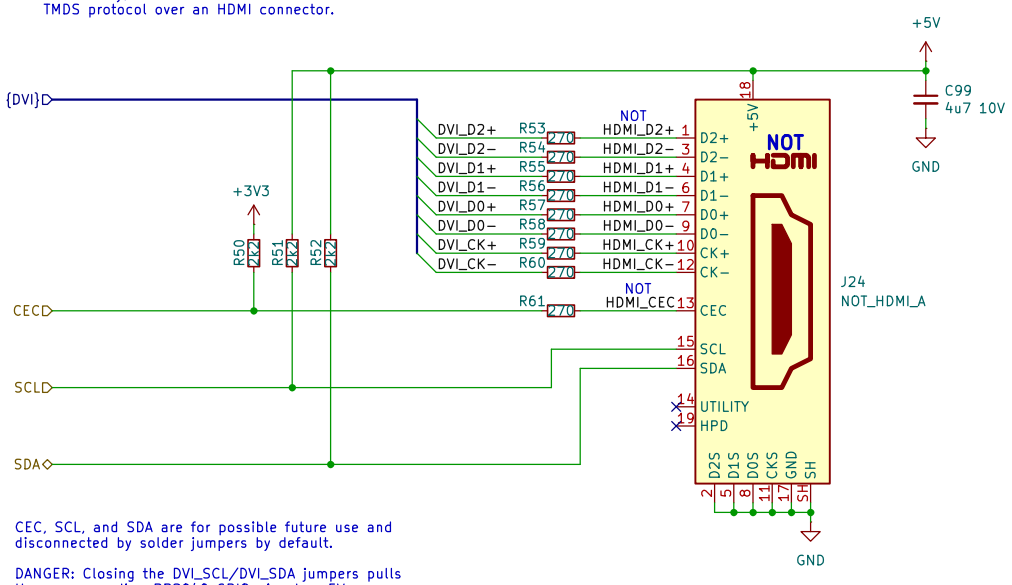
Sheet: /MAGIC/MCU/
File: MCU.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	Rev: A
KiCad E.D.A. 8.0.7		Id: 13/17

DVI VIDEO

Technically, not true HDMI. This is the DVI TMDS protocol over an HDMI connector.



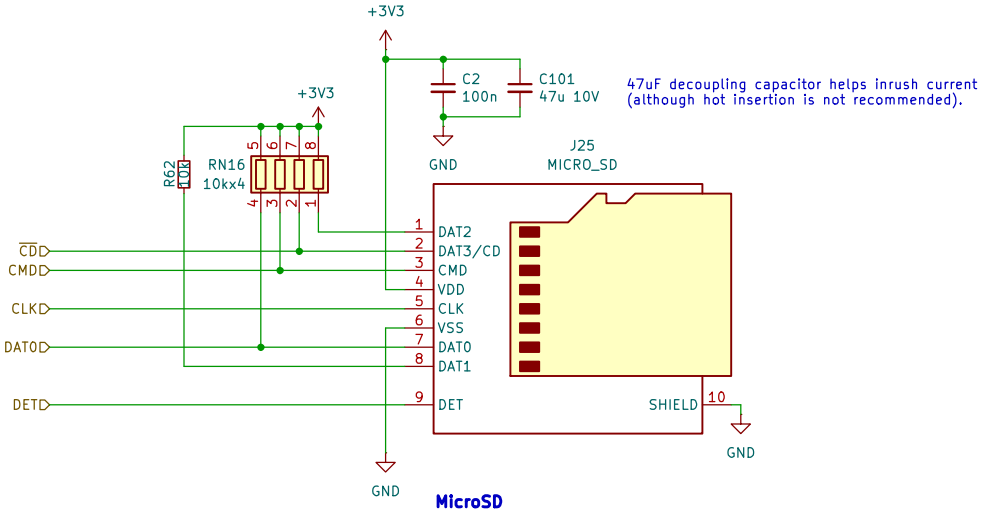
CEC, SCL, and SDA are for possible future use and disconnected by solder jumpers by default.

DANGER: Closing the DVI_SCL/DVI_SDA jumpers pulls the corresponding RP2040 GPIO pins to +5V.

Only do this if you know what you're doing.

Signals with B−prefix are level−shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /MAGIC/MCU/DVI/		
File: DVI.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023−10−01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 14/17



MicroSD

DAT[0] : (POCI) is open-drain output that requires pullup.
DAT[2:1] : Unused inputs in SPI mode. Pullups recommended to avoid current draw due to metastablitiy.
DAT[3] : (CS) has built-in 22-50k pullup to ensure card is deselected by default.
CMD : (PICO) input in SPI mode.
CLK : (SCK) always an input. Never gets pullup.

For reference, CM1624 uses:
25k pullup for DAT[0:3] and CMD
40 Ohm termination for DAT[0:3], CMD, and CLK

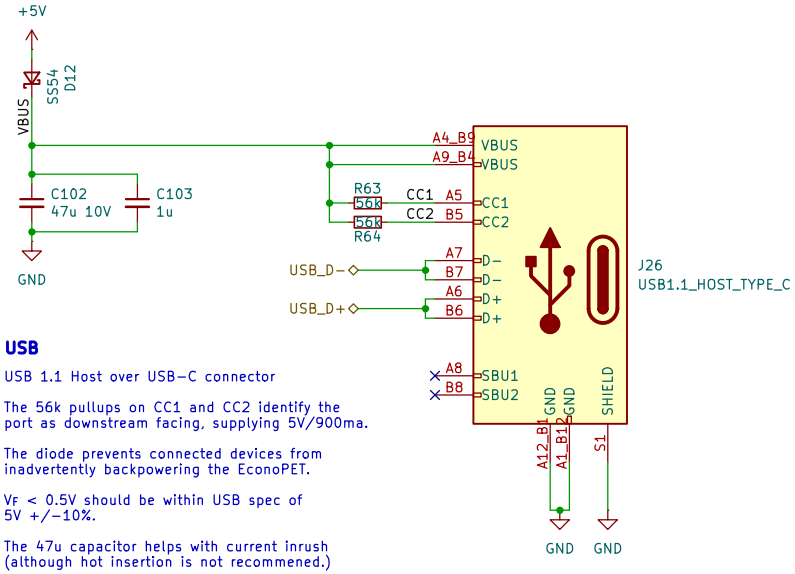
10k pullups common (e.g., ExpressIf documentation).

Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /MAGIC/MCU/MicroSD/
File: MicroSD.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 15/17



USB

USB 1.1 Host over USB−C connector

The 56k pullups on CC1 and CC2 identify the port as downstream facing, supplying 5V/900ma.

The diode prevents connected devices from inadvertently backpowering the EconoPET.

V_F < 0.5V should be within USB spec of 5V +/−10%.

The 47u capacitor helps with current inrush (although hot insertion is not recommened.)

Consider using an independently powered USB hub as an extra layer of protection.

Signals with B−prefix are level−shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /MAGIC/MCU/USB/
File: USB.kicad_sch

Title: EconoPET 40/8096

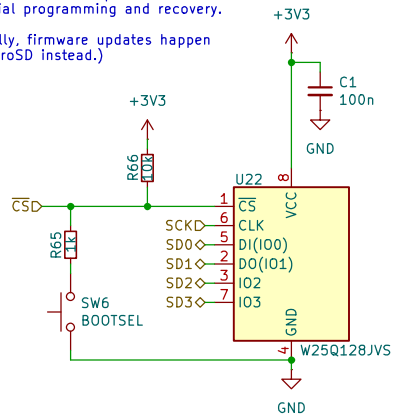
Size: A	Date: 2023−10−01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 16/17

Flash

16MiB Quad SPI flash memory for MCU.

Holding BOOTSEL at power on puts the MCU into programming mode, allowing new firmware to be uploaded via USB for initial programming and recovery.

(Typically, firmware updates happen via microSD instead.)



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors are rated for 25V or higher
Unspecified resistors are 1% and rated for 62.5mW or higher

Sheet: /MAGIC/MCU/Flash/		
File: FLASH.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 17/17