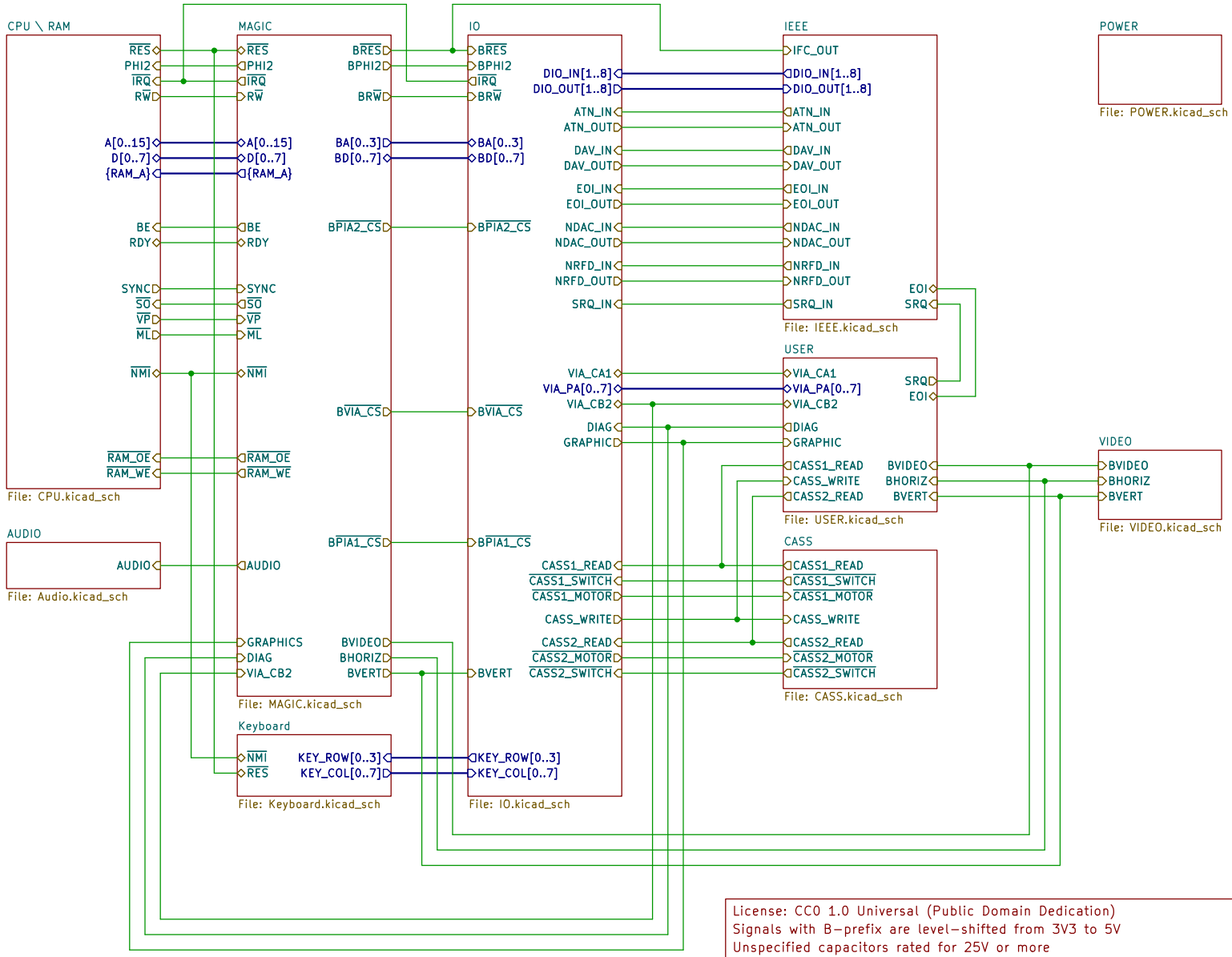


"If you don't use a current limiting resistor the
LED will light up orange! Because of the fire!
Because sometimes even daddies make mistakes."

– Milo, Age 4.5

License: CC0 1.0 Universal (Public Domain Dedication)
Signals with B–prefix are level–shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more
https://is.gd/6hpvh6

Sheet: /
File: Mainboard.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023–10–01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 1/17

The bus is shared with the FPGA. The FPGA deasserts BE (Bus Enable) to transition the CPU's Address, Data, and RW buffers to high-Z while the FPGA drives the bus.

CPU and RAM operate at 3V3 to interface directly with the FPGA. Level shifters are used for connections to the 5V I/O section. This split avoids needing level shifters for A[5..16].

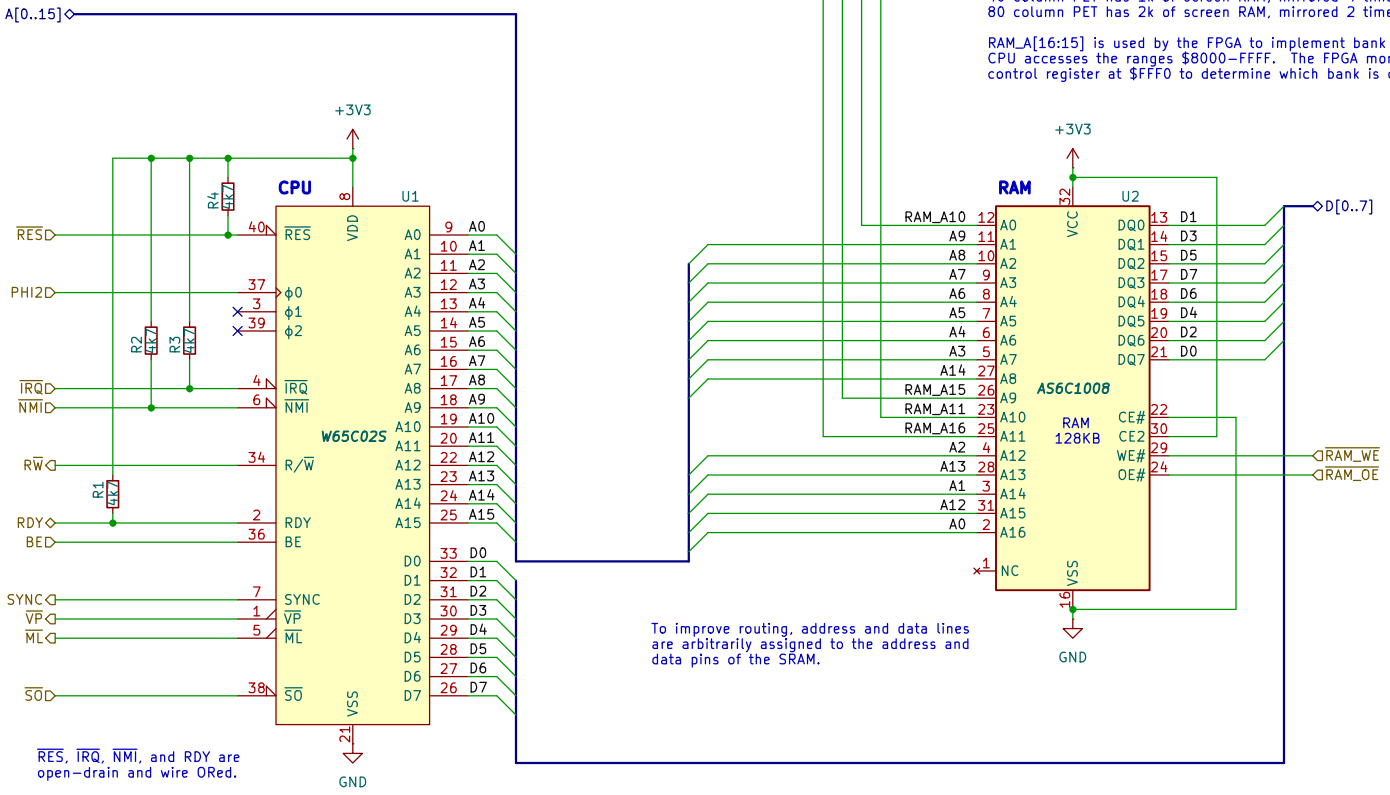
A single 128KB SRAM chip is used for the 32K main RAM, 64K expansion RAM, 2K display RAM, 2K character ROM and 26K system ROM. ROMs are initialized by the MCU on POR (via SPI -> bus bridge provided by the FPGA).

A[15:0] are the address of the shared system bus, which is connected to the CPU, IO, FPGA and most RAM address pins. The exceptions are RAM_A[16:15,11:10], which are driven exclusively by the FPGA.

RAM_A[11:10] is used by the FPGA to mirror display RAM when the CPU accesses the range $8000-8FFF.

40 column PET has 1k of screen RAM, mirrored 4 times.
80 column PET has 2k of screen RAM, mirrored 2 times.

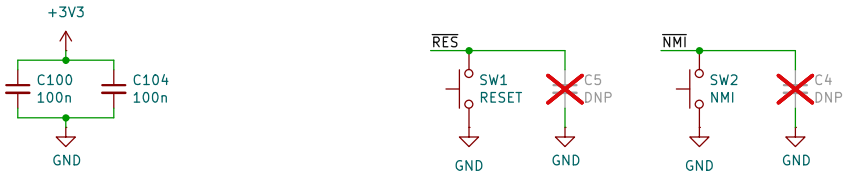
RAM_A[16:15] is used by the FPGA to implement bank switching when the CPU accesses the ranges $8000-FFFF. The FPGA monitors writes to the control register at $FFF0 to determine which bank is currently selected.



To improve routing, address and data lines are arbitrarily assigned to the address and data pins of the SRAM.

$\overline{RES}$, $\overline{IRQ}$, $\overline{NMI}$, and RDY are open-drain and wire ORed.

$\overline{SO}$ is pulled high by the FPGA.

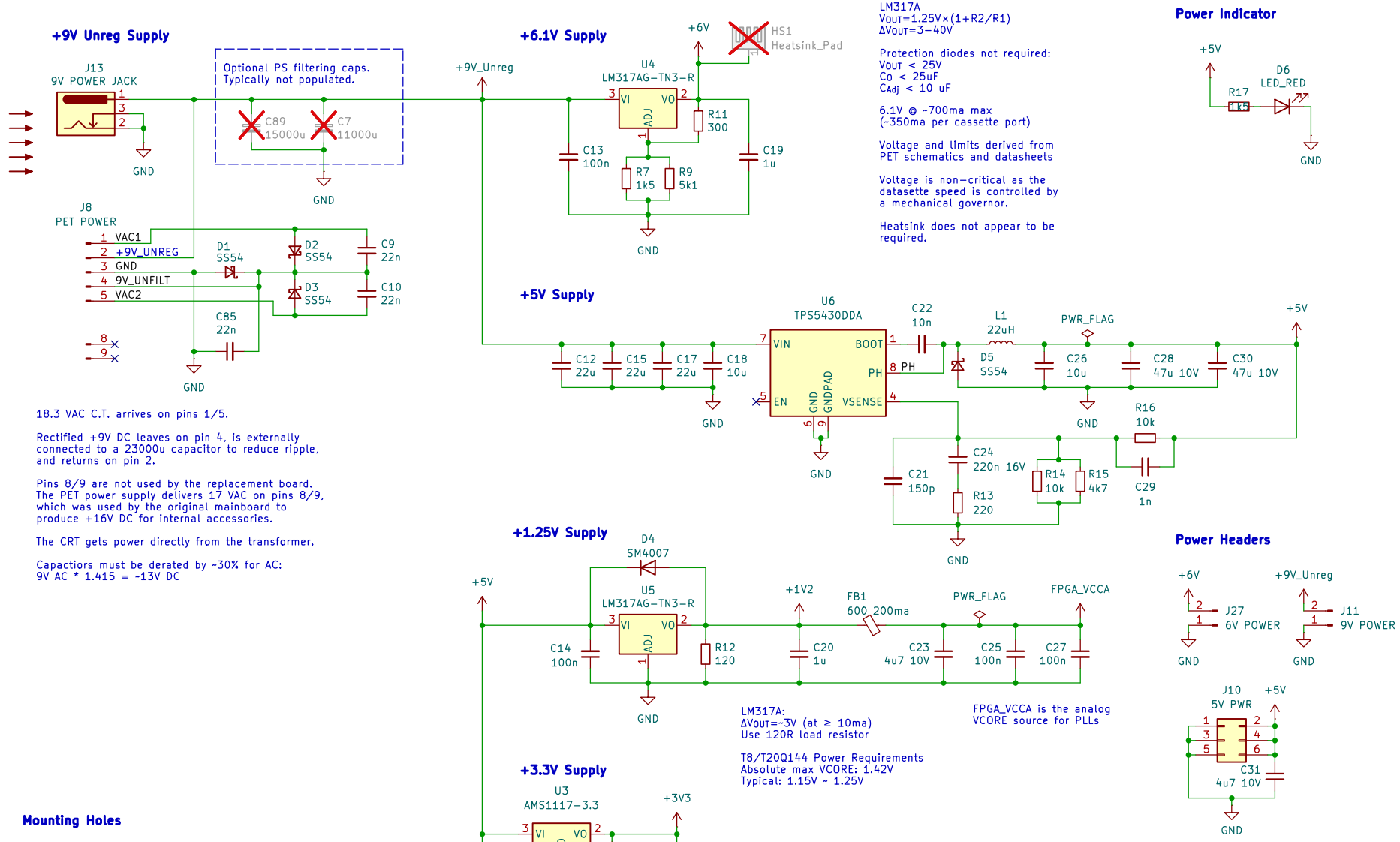


Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

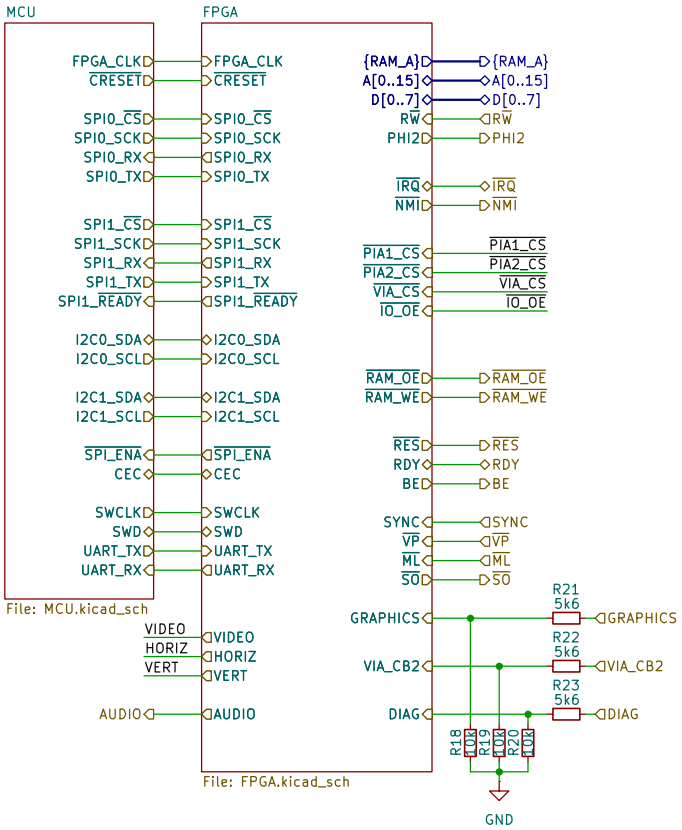
Sheet: /CPU \ RAM/
File: CPU.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 2/17


+9V Unreg Supply
J13
9V POWER JACK
Optional PS filtering caps.
Typically not populated.
C89
15000u
C7
11000u
GND
J8
PET POWER
1 VAC1
2 +9V_UNREG
3 GND
4 9V_UNFILT
5 VAC2
D1
SS54
D2
SS54
D3
SS54
C9
22n
C10
22n
C85
22n
18.3 VAC C.T. arrives on pins 1/5.
Rectified +9V DC leaves on pin 4, is externally connected to a 23000u capacitor to reduce ripple, and returns on pin 2.
Pins 8/9 are not used by the replacement board. The PET power supply delivers 17 VAC on pins 8/9, which was used by the original mainboard to produce +16V DC for internal accessories.
The CRT gets power directly from the transformer.
Capactiors must be derated by ~30% for AC:
9V AC * 1.415 = ~13V DC
+9V_Unreg
+6.1V Supply
U4
LM317AG-TN3-R
VI
VO
ADJ
R11
300
R7
1k5
R9
5k1
C13
100n
C19
1u
+6V
HS1
Heatsink_Pad
LM317A
VOUT=1.25V×(1+R2/R1)
ΔVOUT=3–40V
Protection diodes not required:
VOUT < 25V
CO < 25uF
CAdj < 10 uF
6.1V @ ~700ma max
(~350ma per cassette port)
Voltage and limits derived from PET schematics and datasheets
Voltage is non-critical as the datasette speed is controlled by a mechanical governor.
Heatsink does not appear to be required.
Power Indicator
+5V
D6
LED_RED
R17
1k5
GND
+5V Supply
U6
TPS5430DDA
VIN
BOOT
PH
EN
VSENSE
GND
GNDPAD
C12
22u
C15
22u
C17
22u
C18
10u
C22
10n
L1
22uH
D5
SS54
PWR_FLAG
C26
10u
C28
47u 10V
C30
47u 10V
R16
10k
C29
1n
C24
220n 16V
R13
220
C21
150p
R14
10k
R15
4k7
+1.25V Supply
D4
SM4007
U5
LM317AG-TN3-R
+1V2
FB1
600_200ma
FPGA_VCCA
R12
120
C14
100n
C20
1u
C23
4u7 10V
C25
100n
C27
100n
LM317A:
ΔVOUT=~3V (at ≥ 10ma)
Use 120R load resistor
T8/T20Q144 Power Requirements
Absolute max VCORE: 1.42V
Typical: 1.15V ~ 1.25V
FPGA_VCCA is the analog VCORE source for PLLs
Power Headers
+6V
J27
6V POWER
+9V_Unreg
J11
9V POWER
J10
5V PWR
C31
4u7 10V
+3.3V Supply
U3
AMS1117-3.3
+3V3
C11
22u
C16
47u 10V
R10
330
R6
R8
AMS1117-3.3:
ΔVOUT=1.3V
IL(MIN)=10ma
Use 330R load resistor
AMS1117 internal protection diodes sufficient with output caps < 1000uF
0.5R adjusts ESR of MLCC
Mounting Holes
R5
68
PWR_FLAG
H1
MountingHole_Pad
H2
MountingHole
H3
MountingHole
H4
MountingHole
CHASSIS_GND
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more
Sheet: /POWER/
File: POWER.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 3/17

Magic



MCU responsibilities:
- Generate FPGA_CLK
- Configure FPGA at POR
- Initialize SRAM with ROM images
- Read back video RAM and output to HDMI (bit-banged DVI)
- Report USB keyboard matrix to FPGA

FPGA responsibilities:
- Timing / address decoding
- CRTC emulation / native PET video generation
- Expose sysem bus to MCU (via SPI)
- Intercept PIA1 to inject USB keyboard

SRAM is shared between the 6502 and the FPGA by using an effective bus speed of 8 MHz taking turns in round-robin fashion.

From the CPU and I/O chip's perspective, PHI2 is "stretched" with a 1/8th duty cycle. From the FPGA's perspective, there is an 8 MHz clock and 8 clock enable signals, which are used as follows:

0: Read/write to SRAM to service SPI request from MCU
1: Read even character from VRAM
2: Read even character bitmat from "ROM"
3: Read odd character from VRAM
4: Read odd character from "ROM"
5: Read/write to SRAM to service SPI request from MCU
6: Setup for next CPU cycle
7: Pulse PHI2

(Note: Above subject to change with firmware updates.)

Shift 5V -> 3.3V:

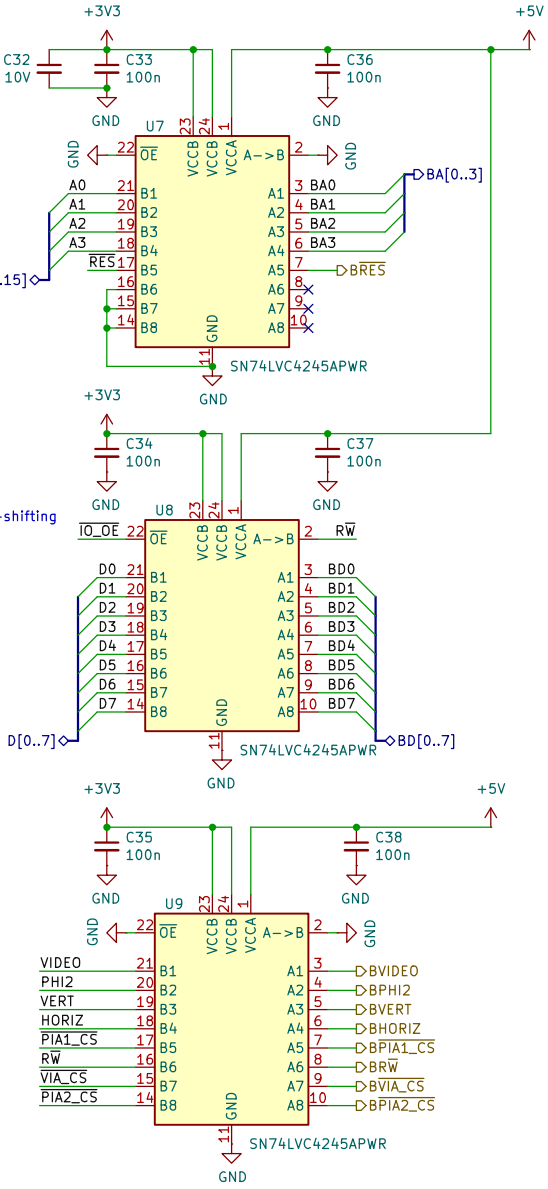
VOUT = VIN * (R2 / (R1 + R2)
VIN = 5.1V
R1 = 5.6k - 1%
R2 = 10k + 1%
VOUT = 3.29V

PIAs and VIA operate at 5V logic levels for compatible I/O.

CPU and RAM operate at the same 3.3V logic levels as the FPGA and MCU to reduce the amount of level shifting required.

D[0..7] are the only bidirectional lines that need to be shifted. The direction of D[0..7] is controlled by RW.

Level Shifting



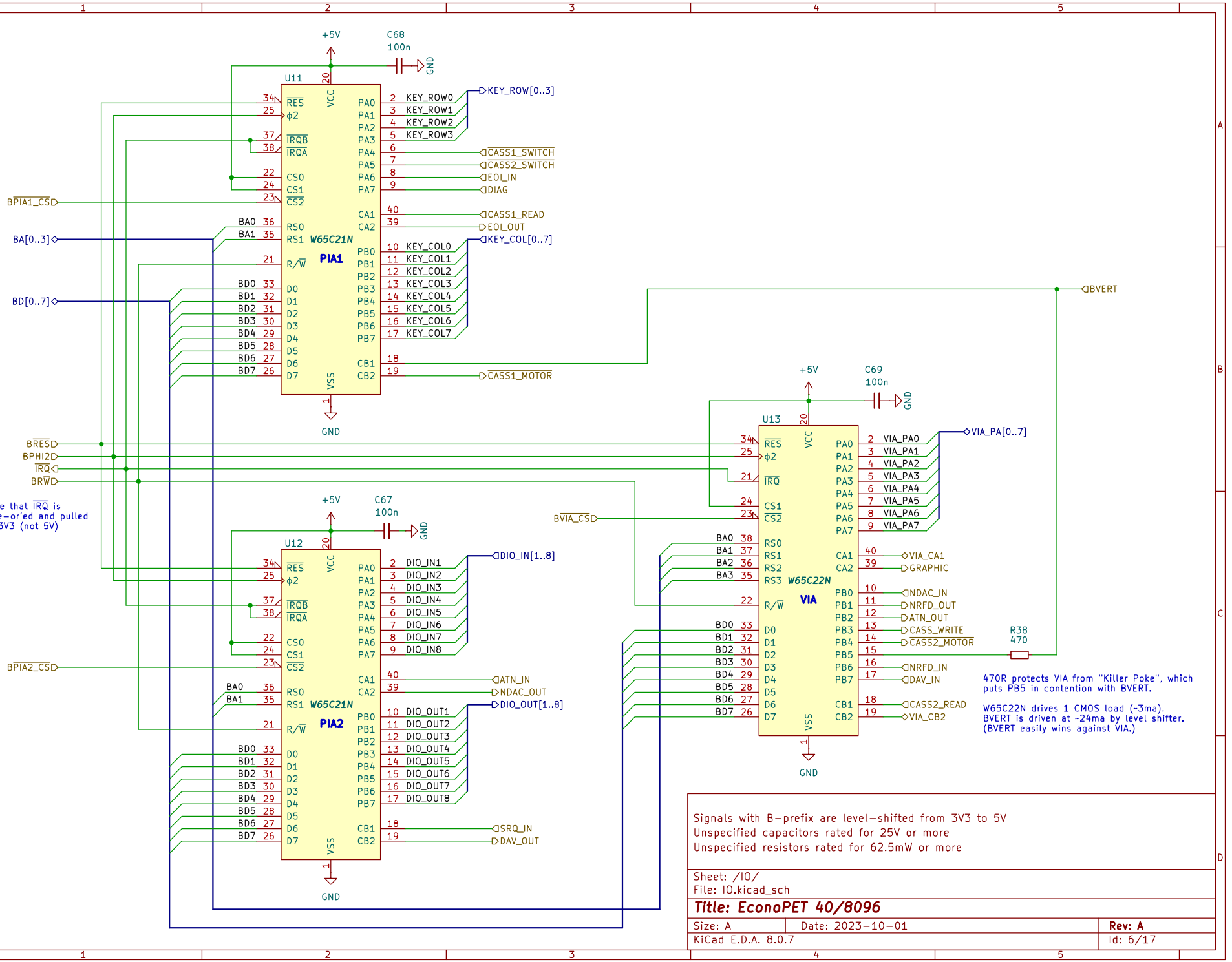
IO_OE does not require level-shifting (high @ 2V)

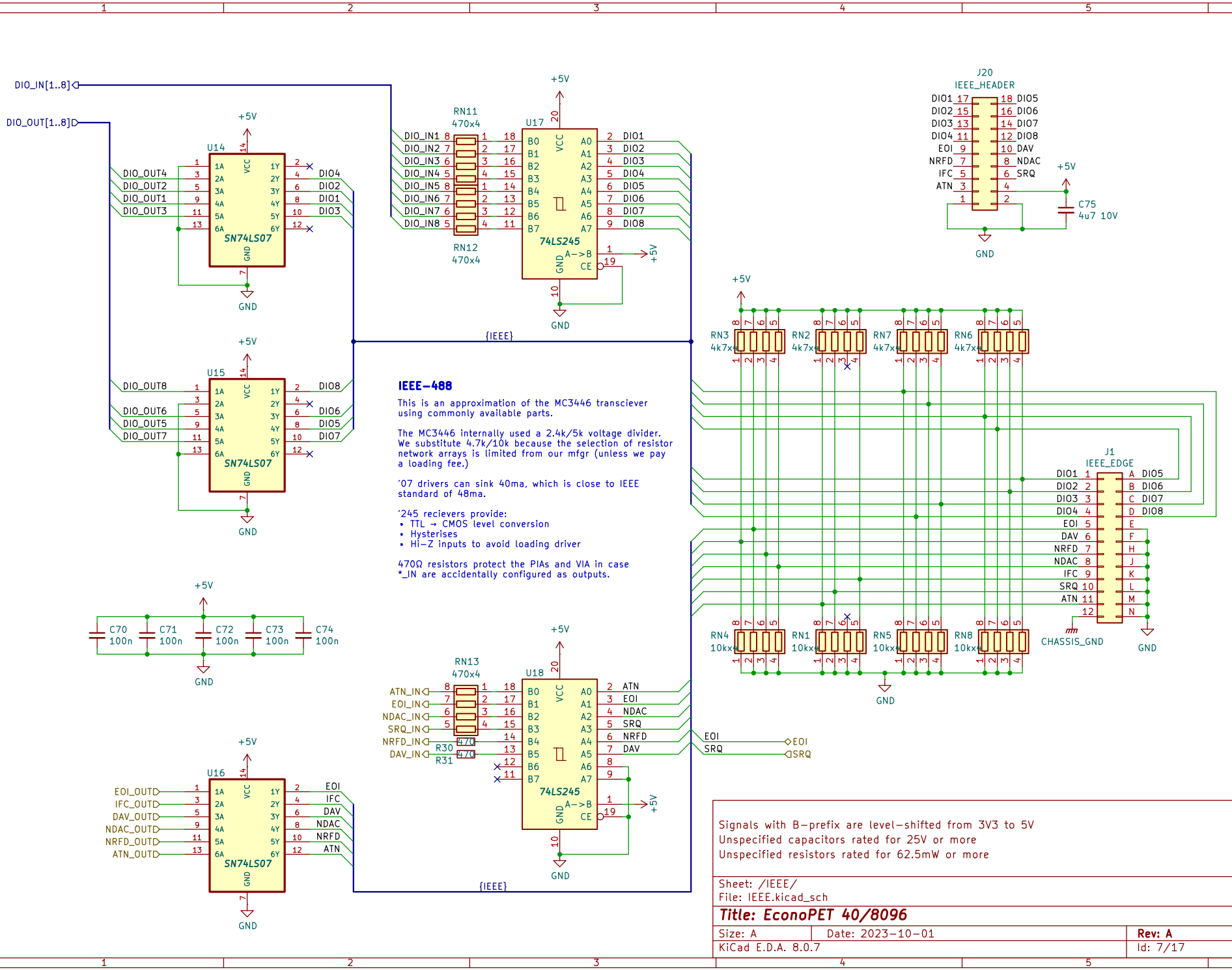
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /MAGIC/
File: MAGIC.kicad_sch

Title: EconoPET 40/8096

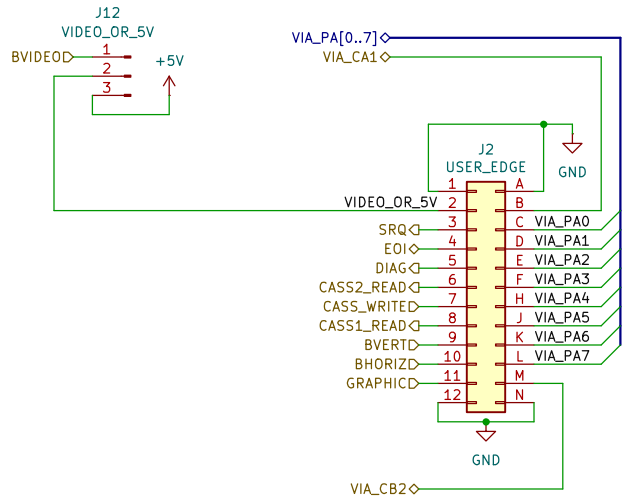
Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 4/17

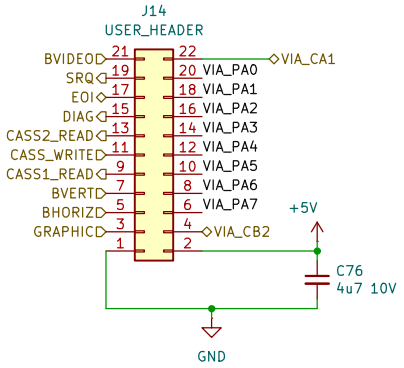

U11
PIA1
W65C21N
+5V
C68
100n
GND
KEY_ROW[0..3]
KEY_ROW0
KEY_ROW1
KEY_ROW2
KEY_ROW3
CASS1_SWITCH
CASS2_SWITCH
EOI_IN
DIAG
CASS1_READ
EOI_OUT
KEY_COL[0..7]
KEY_COL0
KEY_COL1
KEY_COL2
KEY_COL3
KEY_COL4
KEY_COL5
KEY_COL6
KEY_COL7
CASS1_MOTOR
BPIA1_CS
BA[0..3]
BD[0..7]
BVERT
U13
VIA
W65C22N
C69
VIA_PA[0..7]
VIA_PA0
VIA_PA1
VIA_PA2
VIA_PA3
VIA_PA4
VIA_PA5
VIA_PA6
VIA_PA7
VIA_CA1
GRAPHIC
NDAC_IN
NRFD_OUT
ATN_OUT
CASS_WRITE
CASS2_MOTOR
NRFD_IN
DAV_IN
CASS2_READ
VIA_CB2
BVIA_CS
R38
470
BRES
BPHI2
IRQ
BRW
Note that IRQ is wire-or'ed and pulled to 3V3 (not 5V)
U12
PIA2
C67
DIO_IN[1..8]
DIO_IN1
DIO_IN2
DIO_IN3
DIO_IN4
DIO_IN5
DIO_IN6
DIO_IN7
DIO_IN8
ATN_IN
NDAC_OUT
DIO_OUT[1..8]
DIO_OUT1
DIO_OUT2
DIO_OUT3
DIO_OUT4
DIO_OUT5
DIO_OUT6
DIO_OUT7
DIO_OUT8
SRQ_IN
DAV_OUT
BPIA2_CS
470R protects VIA from "Killer Poke", which puts PB5 in contention with BVERT.
W65C22N drives 1 CMOS load (~3ma).
BVERT is driven at ~24ma by level shifter.
(BVERT easily wins against VIA.)
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more
Sheet: /IO/
File: IO.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 6/17


DIO_IN[1..8]
DIO_OUT[1..8]
U14
SN74LS07
DIO_OUT4
DIO_OUT2
DIO_OUT1
DIO_OUT3
DIO4
DIO2
DIO1
DIO3
U15
DIO_OUT8
DIO_OUT6
DIO_OUT5
DIO_OUT7
DIO8
DIO6
DIO5
DIO7
U16
EOI_OUT
IFC_OUT
DAV_OUT
NDAC_OUT
NRFD_OUT
ATN_OUT
EOI
IFC
DAV
NDAC
NRFD
ATN
RN11
470x4
RN12
470x4
U17
74LS245
DIO_IN1
DIO_IN2
DIO_IN3
DIO_IN4
DIO_IN5
DIO_IN6
DIO_IN7
DIO_IN8
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
{IEEE}
RN13
470x4
U18
74LS245
ATN_IN
EOI_IN
NDAC_IN
SRQ_IN
NRFD_IN
DAV_IN
R30
R31
470
ATN
EOI
NDAC
SRQ
NRFD
DAV
{IEEE}
J20
IEEE_HEADER
DIO1
DIO2
DIO3
DIO4
EOI
NRFD
IFC
ATN
DIO5
DIO6
DIO7
DIO8
DAV
NDAC
SRQ
C75
4u7 10V
RN3
4k7x4
RN2
4k7x4
RN7
4k7x4
RN6
4k7x4
RN4
10kx4
RN1
10kx4
RN5
10kx4
RN8
10kx4
J1
IEEE_EDGE
CHASSIS_GND
C70
100n
C71
100n
C72
100n
C73
100n
C74
100n
+5V
GND
IEEE-488
This is an approximation of the MC3446 transciever using commonly available parts.
The MC3446 internally used a 2.4k/5k voltage divider. We substitute 4.7k/10k because the selection of resistor network arrays is limited from our mfgr (unless we pay a loading fee.)
'07 drivers can sink 40ma, which is close to IEEE standard of 48ma.
'245 recievers provide:
• TTL → CMOS level conversion
• Hysterises
• Hi-Z inputs to avoid loading driver
470Ω resistors protect the PIAs and VIA in case *_IN are accidentally configured as outputs.
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more
Sheet: /IEEE/
File: IEEE.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023-10-01
Rev: A
KiCad E.D.A. 8.0.7
Id: 7/17

USER PORT

The jumper allows partial compatibility with VIC-20 and C64 user port peripherals by delivering +5V on PIN_2 instead of PET video.



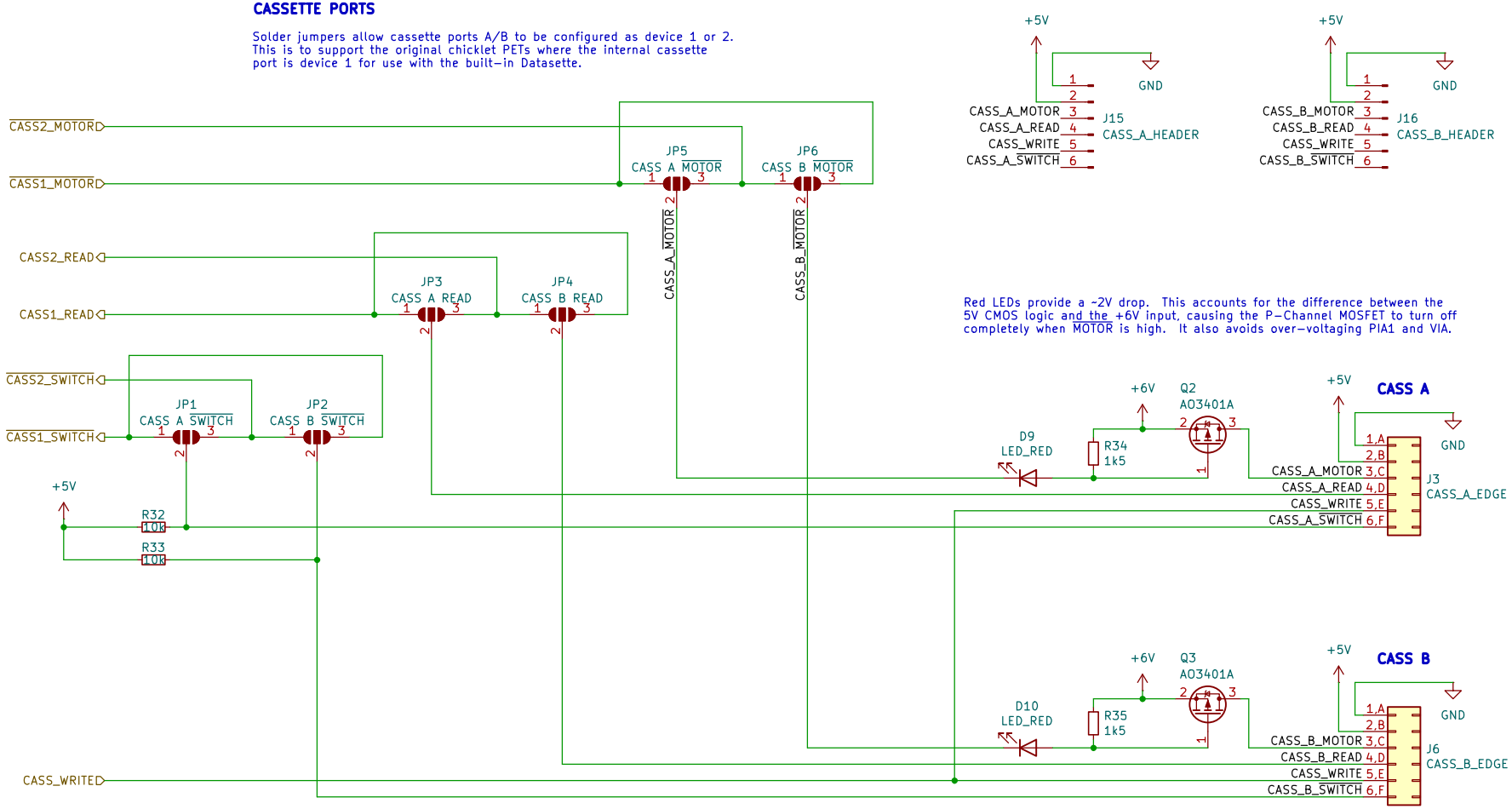


Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /USER/ File: USER.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 8/17

CASSETTE PORTS

Solder jumpers allow cassette ports A/B to be configured as device 1 or 2.
This is to support the original chicklet PETs where the internal cassette
port is device 1 for use with the built-in Datasette.



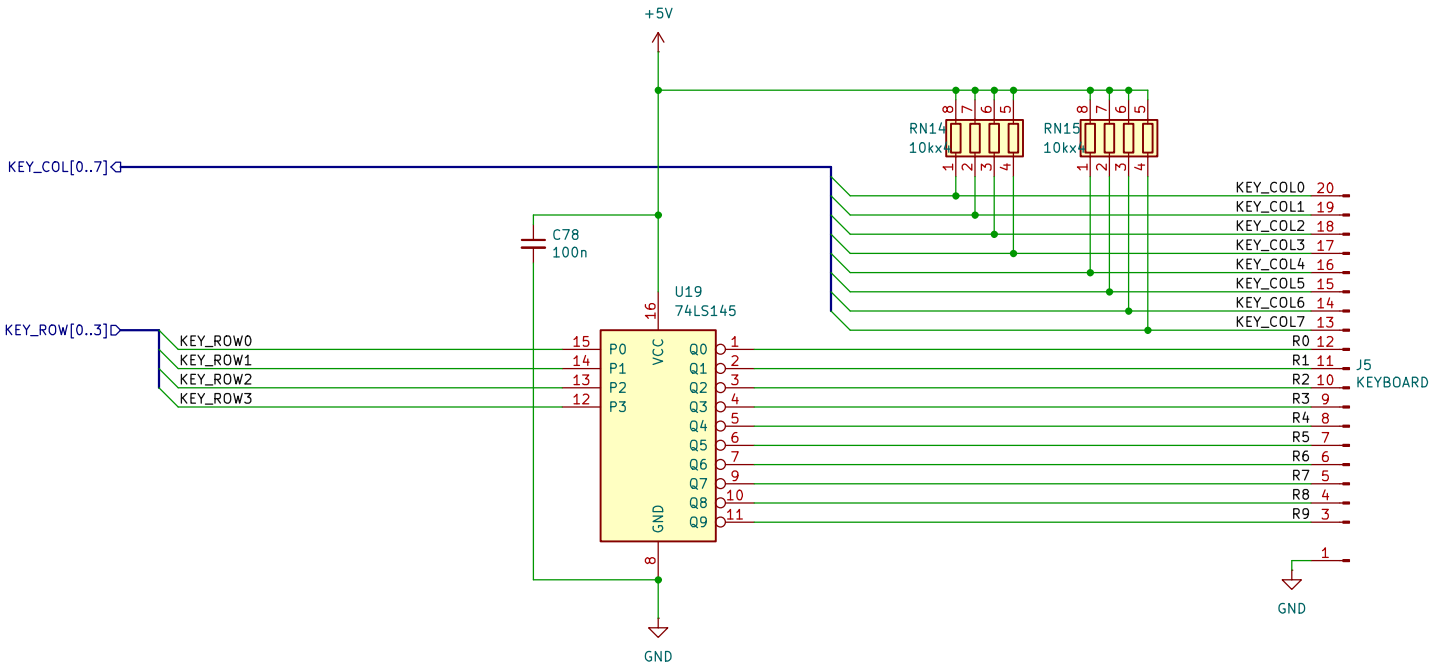
Place decoupling cap near CASS_B connector.
CASS_A has sufficient decoupling nearby.

Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /CASS/
File: CASS.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 9/17



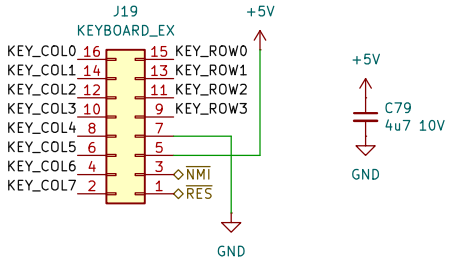
KEYBOARD

The PET uses a 74LS145 BCD-to-decimal to sink the active row of an 8x10 keyboard matrix. When a key in the selected row is pressed, it sinks the 10k pullup of the corresponding column.

The '145 is active low / open collector, capable of sinking an excessive 80ma for driving lamps in the pre-LED era. This is more than enough to sink all eight of the 10k pullups if the user pushes all keys for currently select row.

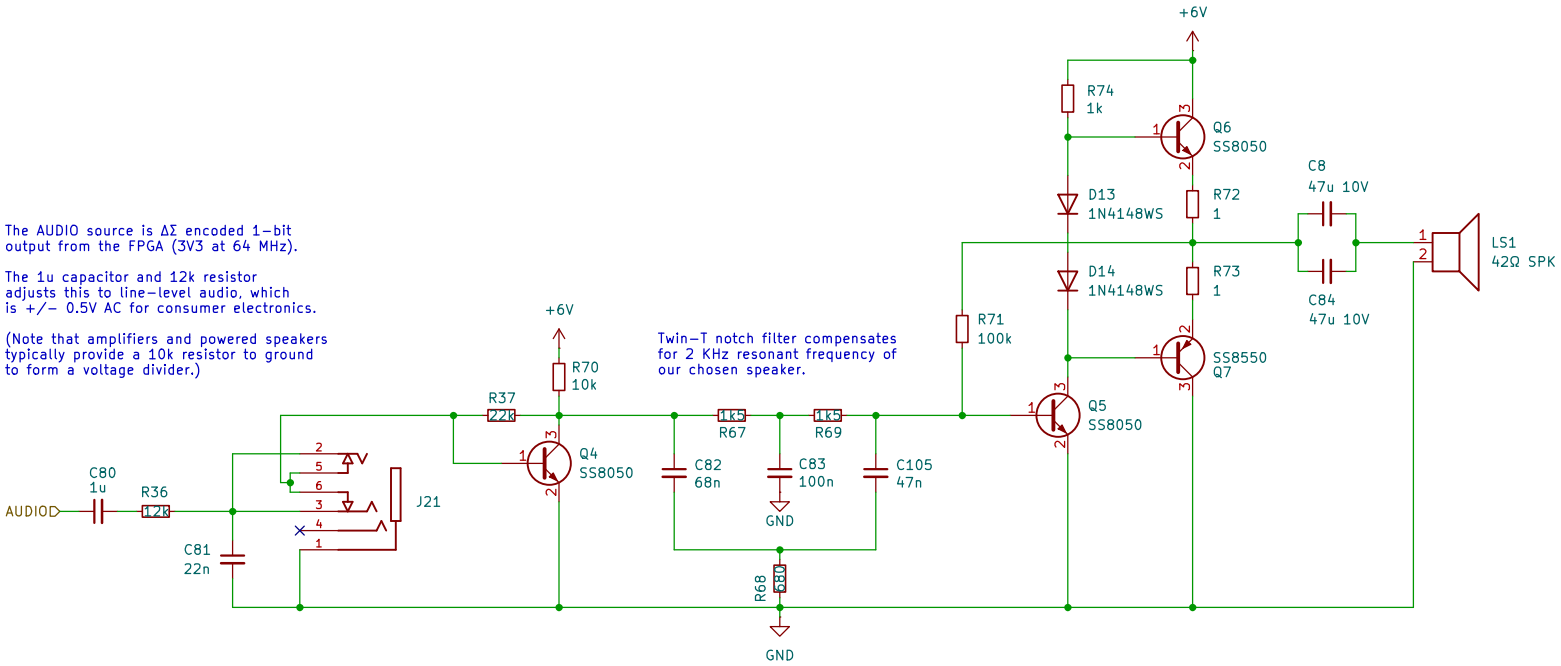
The KEYBOARD_EX header conveniently exposes the PA[3:0] and PB[7:0] lines for users interested in building adapters to support non-PET keyboards. It also exposes NMI for RESTORE and RES for reset.

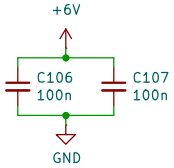
http://www.6502.org/users/sjgray/projects/petexpkbd/index.html



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /Keyboard/		
File: Keyboard.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 10/17





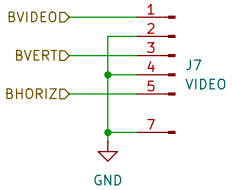
Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /AUDIO/
File: Audio.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 11/17

VIDEO HEADER

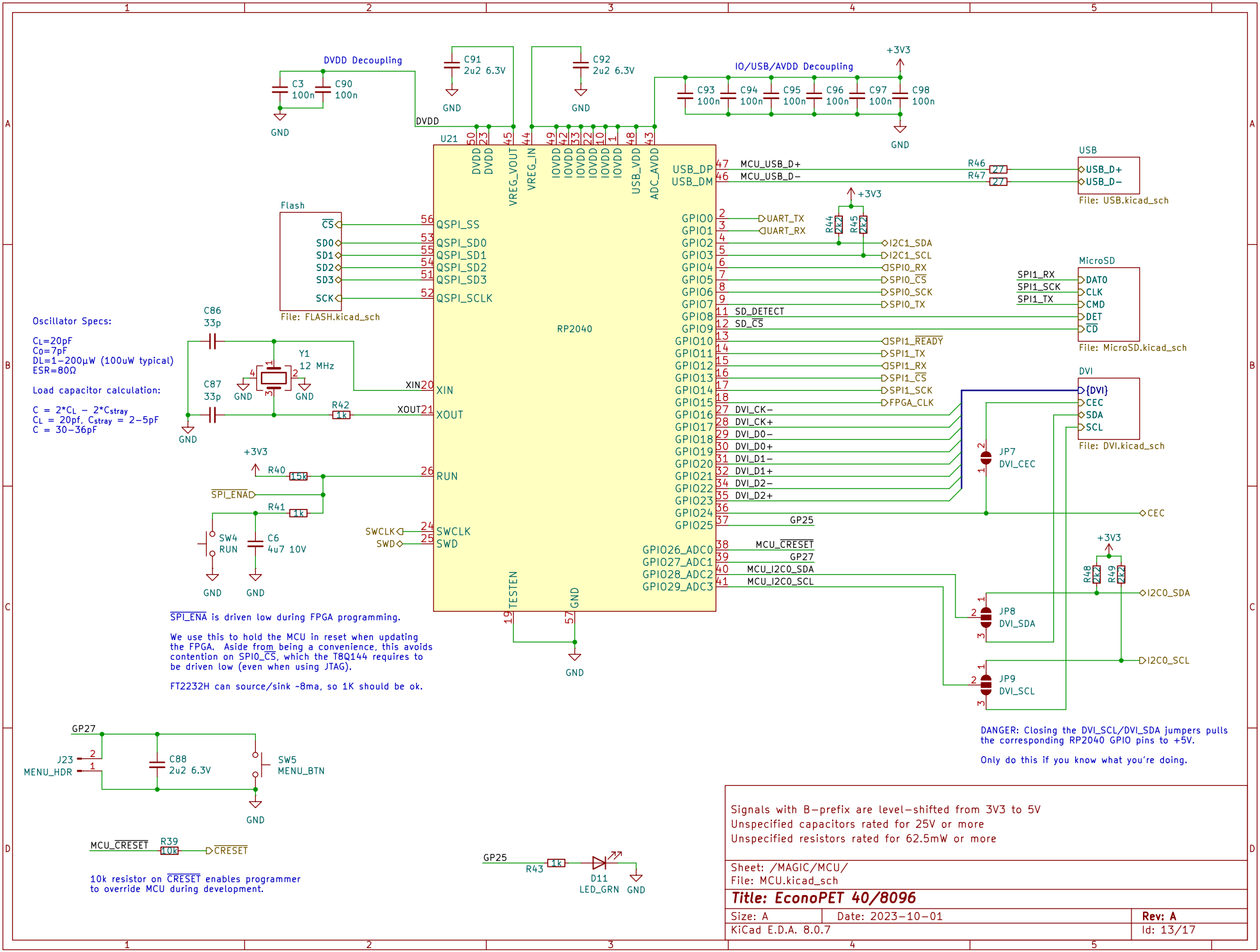


Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /VIDEO/
File: VIDEO.kicad_sch

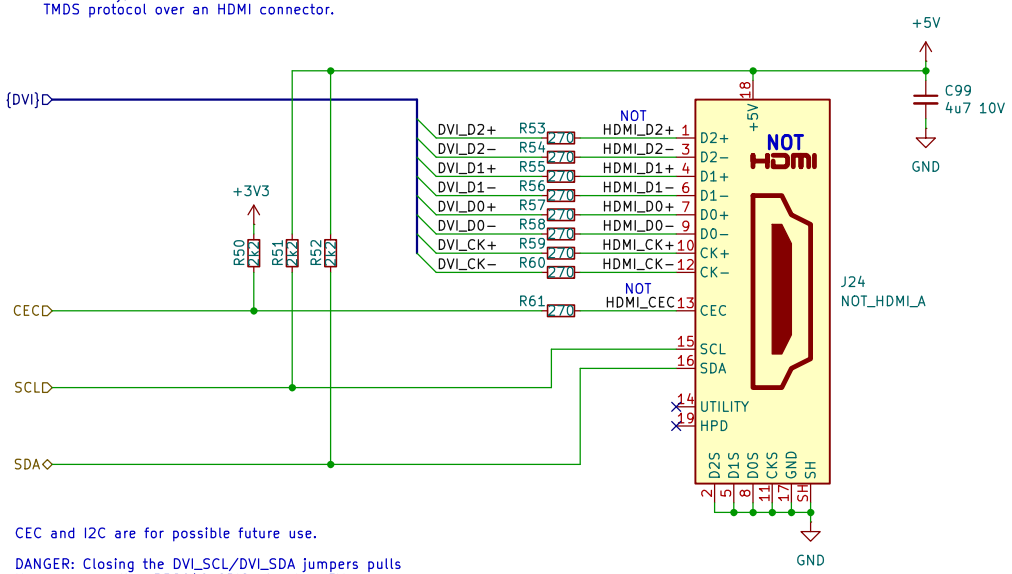
Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 12/17


DVDD Decoupling
C3 100n
C90 100n
C91 2u2 6.3V
C92 2u2 6.3V
IO/USB/AVDD Decoupling
C93 100n
C94 100n
C95 100n
C96 100n
C97 100n
C98 100n
+3V3
GND
DVDD
U21
RP2040
DVDD
VREG_VOUT
VREG_IN
IOVDD
USB_VDD
ADC_AVDD
USB_DP
USB_DM
MCU_USB_D+
MCU_USB_D−
R46 27
R47 27
USB
USB_D+
USB_D−
File: USB.kicad_sch
Flash
CS
SD0
SD1
SD2
SD3
SCK
QSPI_SS
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
QSPI_SCLK
File: FLASH.kicad_sch
GPIO0
GPIO1
UART_TX
UART_RX
R44 2k2
R45 2k2
GPIO2
GPIO3
I2C1_SDA
I2C1_SCL
GPIO4
GPIO5
GPIO6
GPIO7
SPI0_RX
SPI0_CS
SPI0_SCK
SPI0_TX
MicroSD
SPI1_RX
SPI1_SCK
SPI1_TX
DAT0
CLK
CMD
DET
CD
File: MicroSD.kicad_sch
GPIO8
SD_DETECT
GPIO9
SD_CS
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
SPI1_READY
SPI1_TX
SPI1_RX
SPI1_CS
SPI1_SCK
FPGA_CLK
DVI
{DVI}
CEC
SDA
SCL
File: DVI.kicad_sch
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
DVI_CK−
DVI_CK+
DVI_D0−
DVI_D0+
DVI_D1−
DVI_D1+
DVI_D2−
DVI_D2+
JP7 DVI_CEC
CEC
GP25
GPIO26_ADC0
GPIO27_ADC1
GPIO28_ADC2
GPIO29_ADC3
MCU_CRESET
GP27
MCU_I2C0_SDA
MCU_I2C0_SCL
R48 2k2
R49 2k2
I2C0_SDA
I2C0_SCL
JP8 DVI_SDA
JP9 DVI_SCL
XIN
XOUT
RUN
SWCLK
SWD
TESTEN
Y1 12 MHz
C86 33p
C87 33p
R42 1k
R40 15k
R41 1k
SPI_ENA
SW4 RUN
C6 4u7 10V
Oscillator Specs:
CL=20pF
C0=7pF
DL=1−200µW (100uW typical)
ESR=80Ω
Load capacitor calculation:
C = 2*CL − 2*Cstray
CL = 20pf, Cstray = 2−5pF
C = 30−36pF
SPI_ENA is driven low during FPGA programming.
We use this to hold the MCU in reset when updating the FPGA. Aside from being a convenience, this avoids contention on SPI0_CS, which the T8Q144 requires to be driven low (even when using JTAG).
FT2232H can source/sink ~8ma, so 1K should be ok.
DANGER: Closing the DVI_SCL/DVI_SDA jumpers pulls the corresponding RP2040 GPIO pins to +5V.
Only do this if you know what you're doing.
GP27
J23 MENU_HDR
C88 2u2 6.3V
SW5 MENU_BTN
MCU_CRESET
R39 10k
CRESET
10k resistor on CRESET enables programmer to override MCU during development.
GP25
R43 1k
D11 LED_GRN
Signals with B−prefix are level−shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more
Sheet: /MAGIC/MCU/
File: MCU.kicad_sch
Title: EconoPET 40/8096
Size: A
Date: 2023−10−01
Rev: A
KiCad E.D.A. 8.0.7
Id: 13/17

DVI VIDEO

Technically, not true HDMI. This is the DVI
TMDS protocol over an HDMI connector.



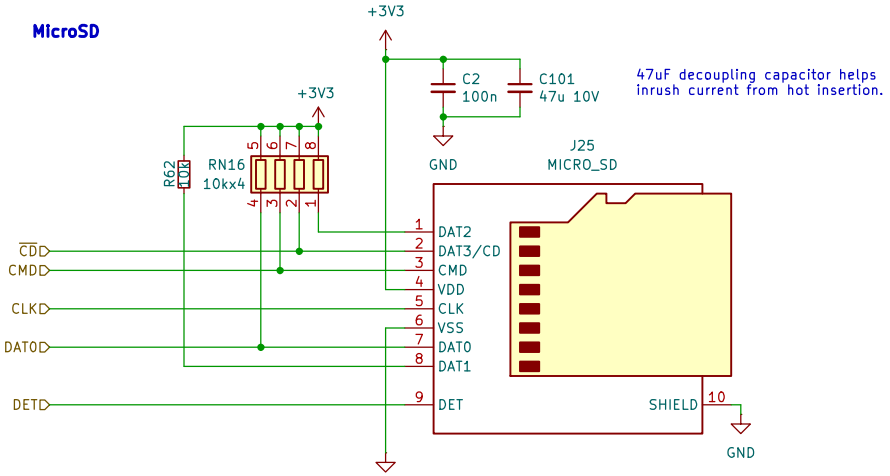
CEC and I2C are for possible future use.

DANGER: Closing the DVI_SCL/DVI_SDA jumpers pulls
the corresponding RP2040 GPIO pins to +5V.

Only do this if you know what you're doing.

Signals with B−prefix are level−shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /MAGIC/MCU/DVI/		
File: DVI.kicad_sch		
Title: EconoPET 40/8096		
Size: A	Date: 2023−10−01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 14/17



DAT[0] : (POCI) is open-drain output that requires pullup.
DAT[2:1] : Unused inputs in SPI mode. Pullups recommended to avoid current draw due to metastablitiy.
DAT[3] : (CS) has built-in 22-50k pullup to ensure card is deselected by default.
CMD : (PICO) input in SPI mode.
CLK : (SCK) always an input. Never gets pullup.

For reference, CM1624 uses:
25k pullup for DAT[0:3] and CMD
40 Ohm termination for DAT[0:3], CMD, and CLK

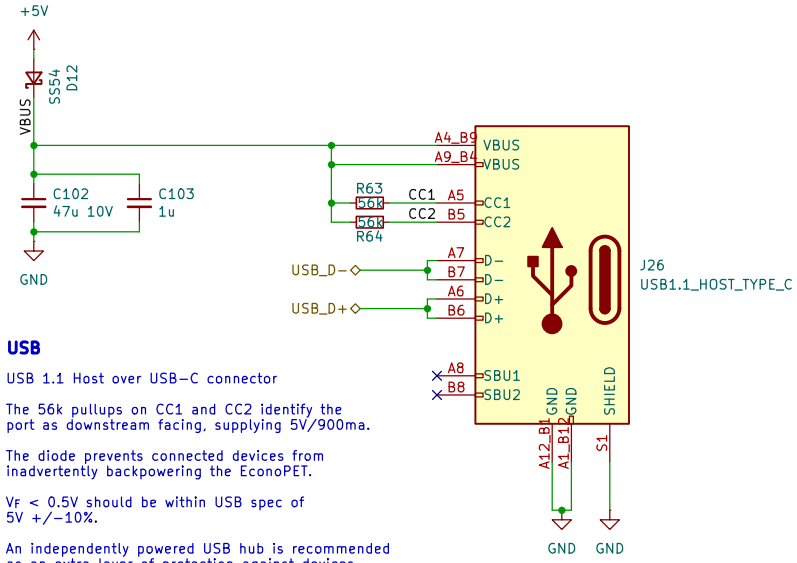
10k pullups common (e.g., Expressif documentation).

Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /MAGIC/MCU/MicroSD/
File: MicroSD.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 15/17



USB

USB 1.1 Host over USB−C connector

The 56k pullups on CC1 and CC2 identify the port as downstream facing, supplying 5V/900ma.

The diode prevents connected devices from inadvertently backpowering the EconoPET.

V_F < 0.5V should be within USB spec of 5V +/−10%.

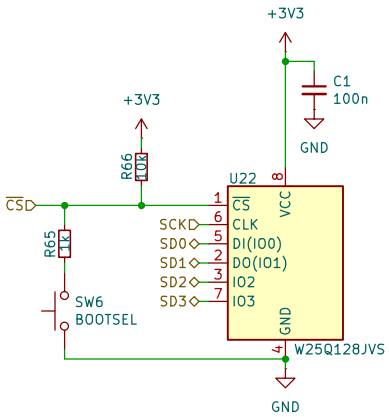
An independently powered USB hub is recommended as an extra layer of protection against devices that incorrectly draw excessive current.

Signals with B−prefix are level−shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /MAGIC/MCU/USB/
File: USB.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023−10−01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 16/17



Signals with B-prefix are level-shifted from 3V3 to 5V
Unspecified capacitors rated for 25V or more
Unspecified resistors rated for 62.5mW or more

Sheet: /MAGIC/MCU/Flash/
File: FLASH.kicad_sch

Title: EconoPET 40/8096

Size: A	Date: 2023-10-01	**Rev: A**
KiCad E.D.A. 8.0.7		Id: 17/17