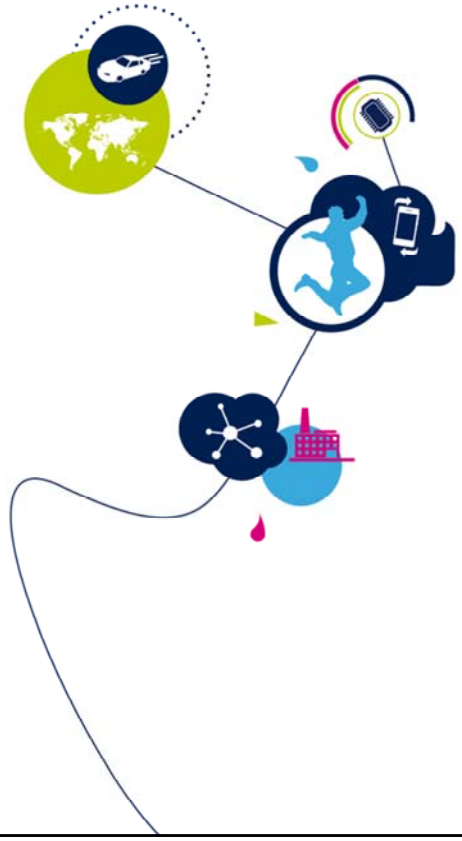
STM32L5 - PWR

Power control

Revision 1.0



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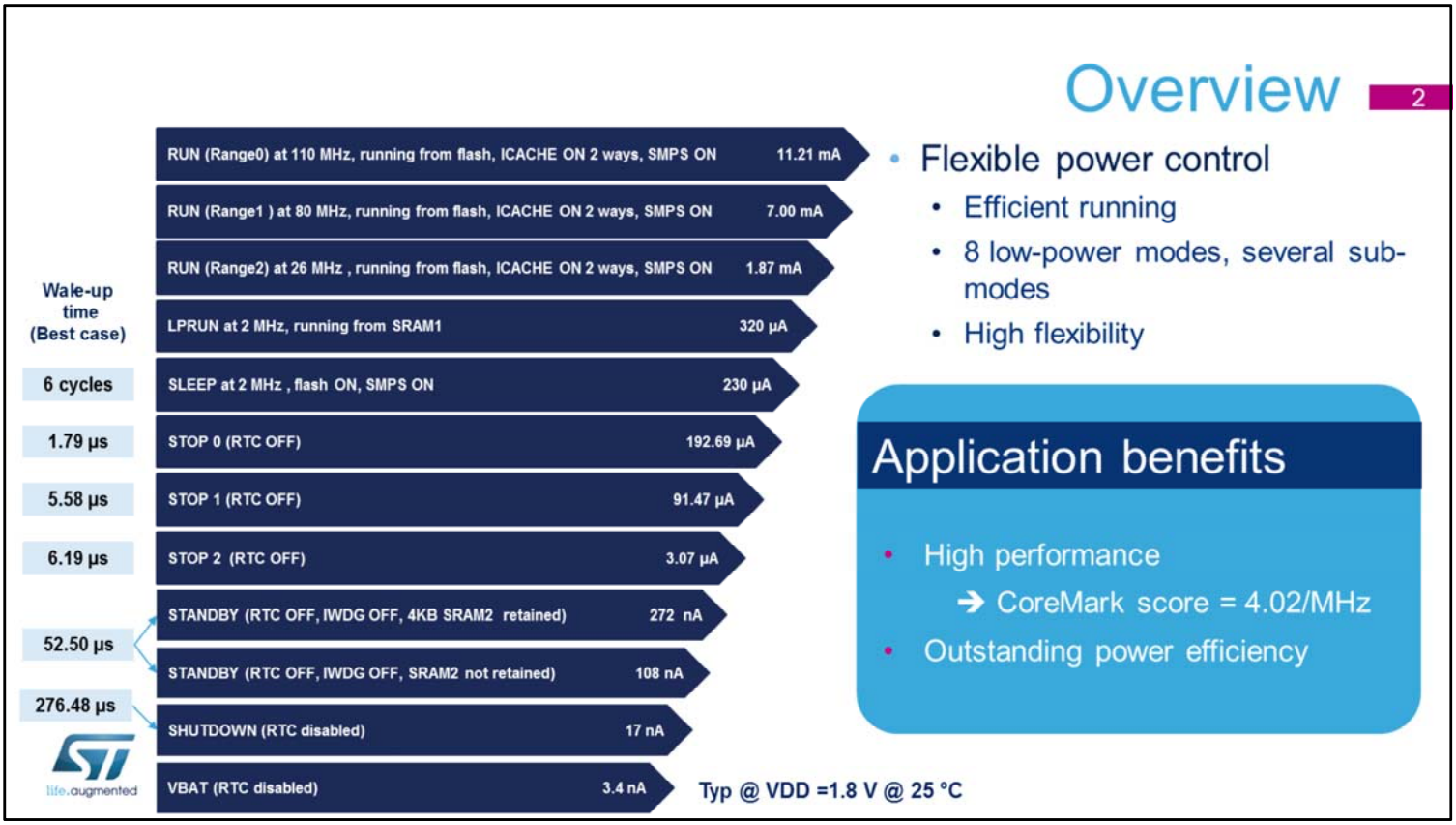
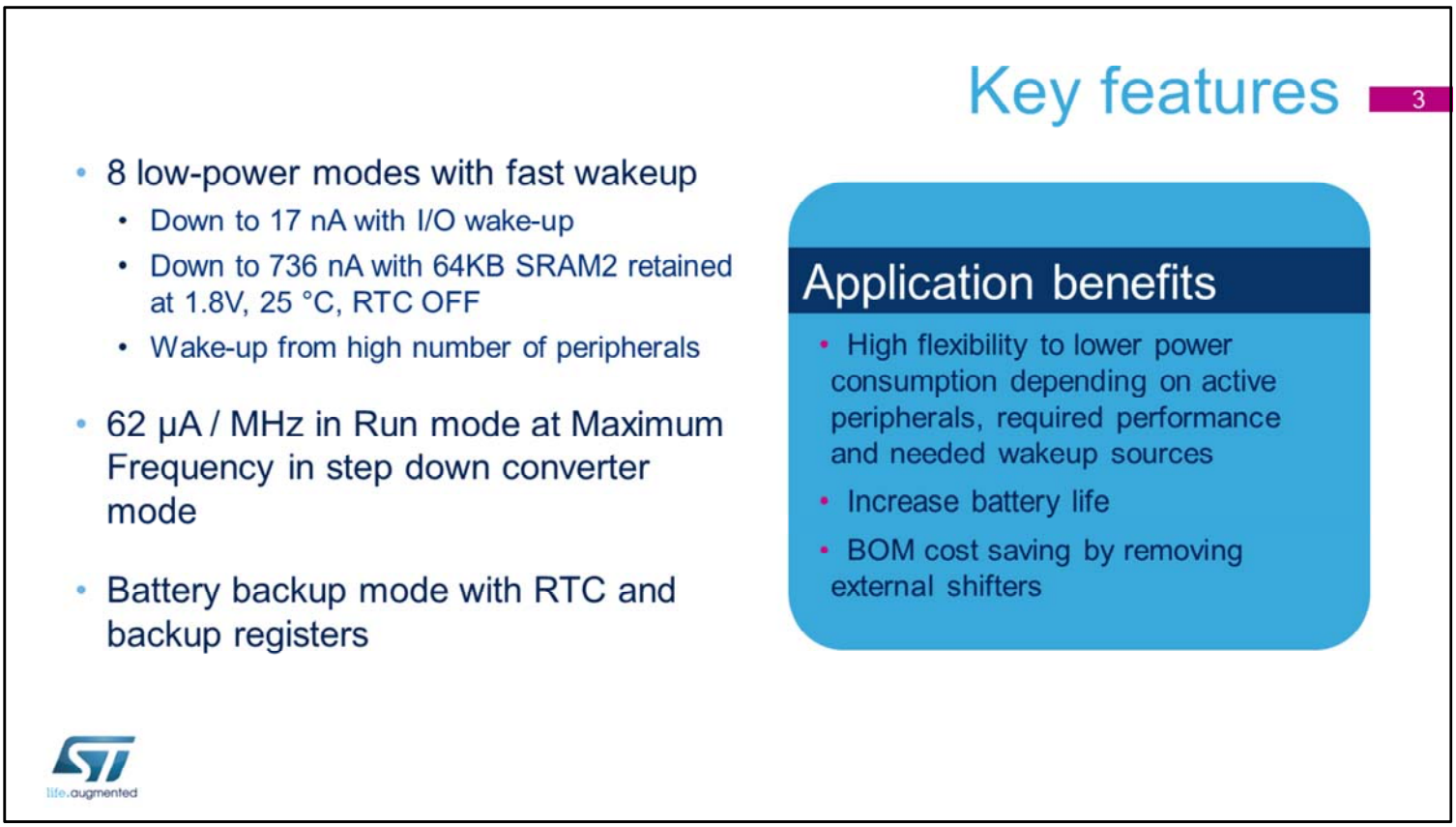
Hello, and welcome to this presentation of the STM32L5 power controller.
The STM32L5's power management functions and all low power modes are also covered in this presentation.



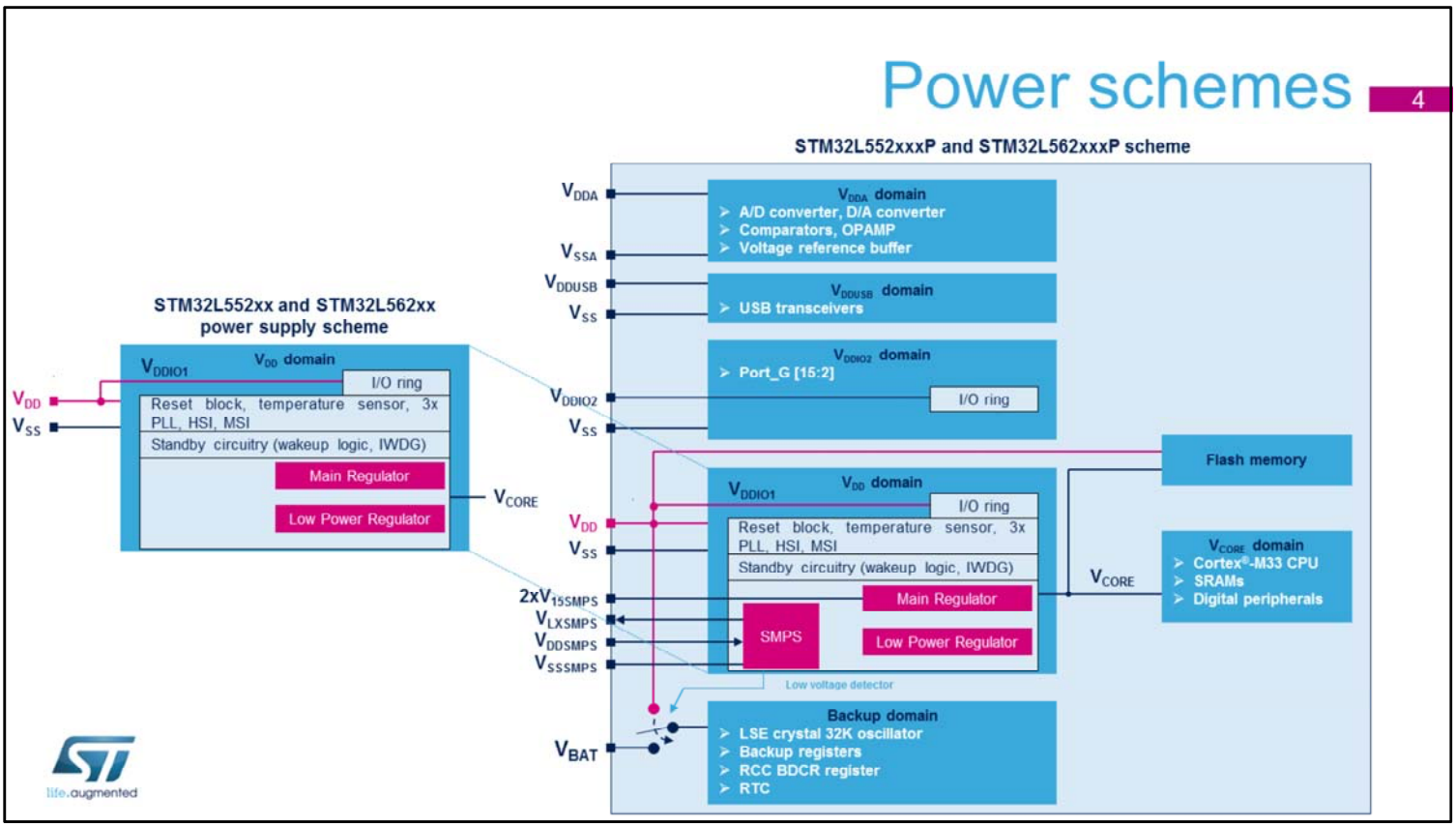
STM32L5 devices feature a flexible power control, which increases flexibility in power mode management and further reduces the overall application consumption.
This slide details the consumption in the various power modes for the STM32L562.
Run mode can support a system clock running at up to 110 MHz, with only 11.21 mA.
The consumption is even lower when frequency and voltage are decreased: 7 mA in range 1 at 80 MHz and 1.87 mA in range 2 at 26 MHz.
STM32L5 devices support 8 main low-power modes: Low-power run, Sleep, Low-power sleep, Stop 0, Stop 1, Stop 2, Standby and Shutdown modes.
Each mode can be configured in many ways, providing several additional sub-modes.
In addition, STM32L5 devices support a battery backup domain, called VBAT.
The high flexibility in power management provides both high

performance with a CoreMark score equal to 4.02/MHz, together with an outstanding power efficiency.



The STM32L5 has several key features related to power management:
Several low-power modes, down to 17 nA while it is still possible to wake up the MCU with an event on an I/O.
For only 668 nA, 64 kilobytes of SRAM2 can be retained assuming a 1.8V VDD power supply.
A large number of peripherals can wake up from the various low-power modes.
Dynamic consumption is down to 62 µA/MHz, when the internal step down converter is used.
A battery backup domain, called VBAT, includes the RTC and the backup registers.
Several power supplies are independent, enabling the reduction of the MCU power consumption while some peripherals are supplied at higher voltages.
Thanks to the large number of power modes, STM32L5 devices offer high flexibility to minimize the power consumption and adjust it depending on the active

peripherals, required performance and required wake-up sources.



STM32L5 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying almost all I/Os except those part of the VBAT domain and port G pads 15 down to 2.

VDD also supplies the flash memory, the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog.

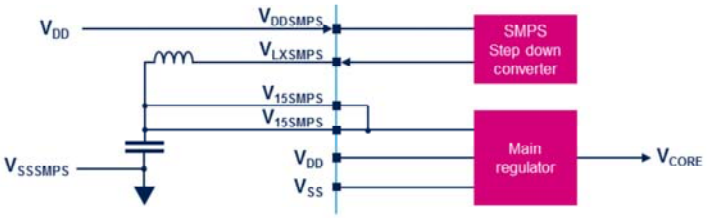
The built-in Switched Mode Power Supply (SMPS) step down converter is a power-efficient DC/DC non-linear switching regulator that improves low-power performance when the VDD voltage is high enough.

The SMPS step down converter automatically enters into Bypass mode when the VDD voltage falls below a VDD minimum value following the selected voltage range and switches back to the selected operating mode when VDD rises above the minimum value.

Only STM32L552xxxP and STM32L562xxxP support SMPS.
The other STM32L5 microcontrollers only rely on integrated regulators or external SMPS power supplies.
VCORE supplies most of the digital peripherals, SRAMs and Flash memory controller.
VDDA voltage supplies the analog peripherals.
The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters.
It is also the output of the internal voltage reference buffer when enabled.
The USB transceiver and Port G pins 15 down to 2 also have their own independent power domains, powered by VDDUSB and VDDIO2 respectively.
A backup battery can be connected to the VBAT pin to supply the backup domain.

Power Supply – DC/DC SMPS devices

- SMPS Step-down convertor power supply pins
  - VDDSMPS is the external power supply for the SMPS step down converter
    - It must be connected to VDD
  - VLXSMPS is the switched SMPS step down converter output
  - V15SMPS are the power supplies for the system regulator
    - It is provided externally through the SMPS step down converter VLXSMPS output.
    - An external coil with typical value of 4.7 µF must be connected
  - VSSSMPS is an isolated supply ground
  - SMPS Step down converter available on specific packages



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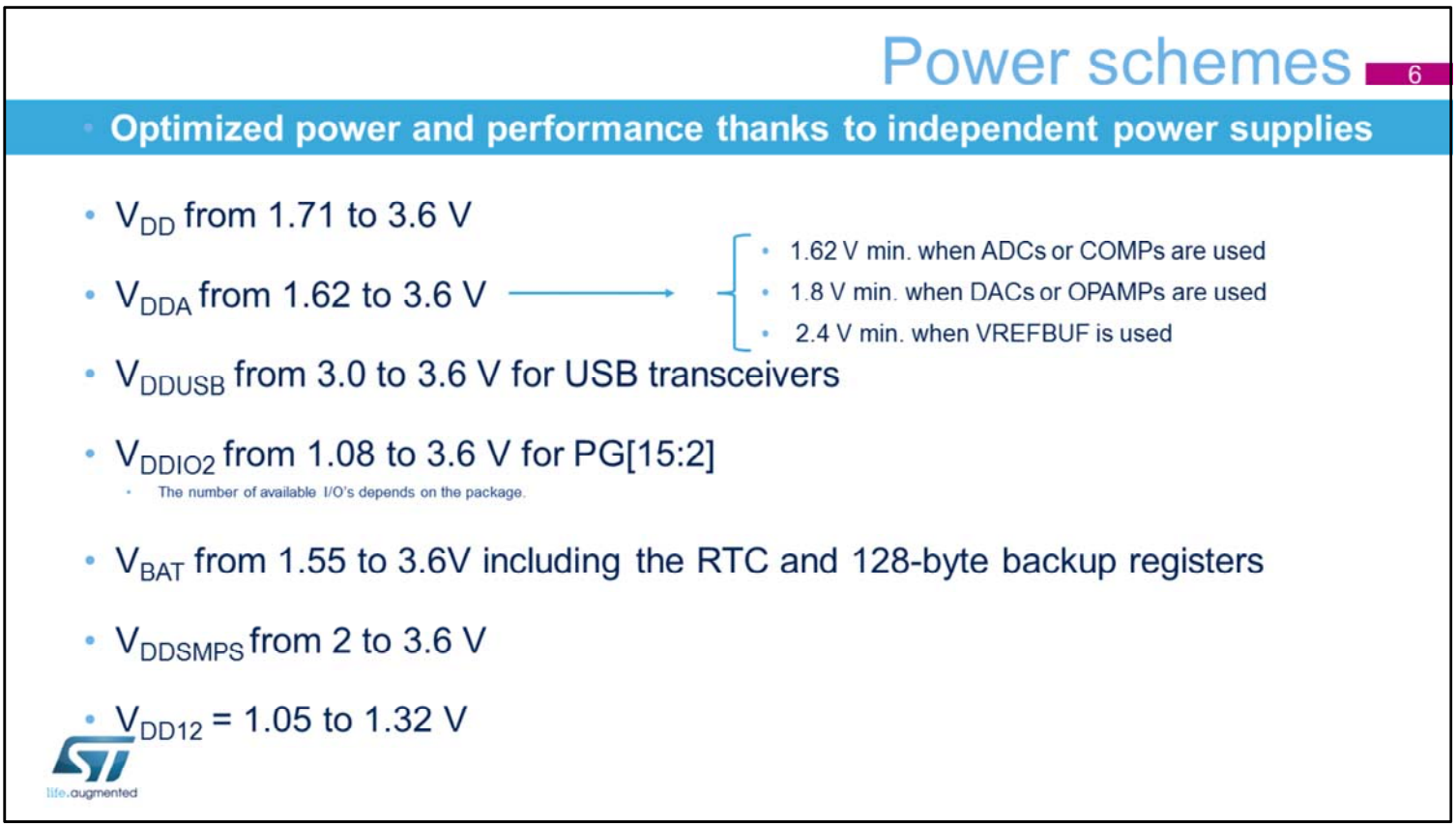
This slide explains the pinout of Switched Mode Power Supply (SMPS) power supply.
VDDSMPS is provided externally through VDDSMPS supply pin, and shall be connected to the same supply as VDD.
VLXSMPS is the switched SMPS step down converter output.
V15SMPS are the power supplies for the system regulator. It is provided externally through the SMPS step down converter VLXSMPS output.
The SMPS power supply pins are only available on a specific package with SMPS step down converter option. When it is not present, the main regulator is connected to VDD.

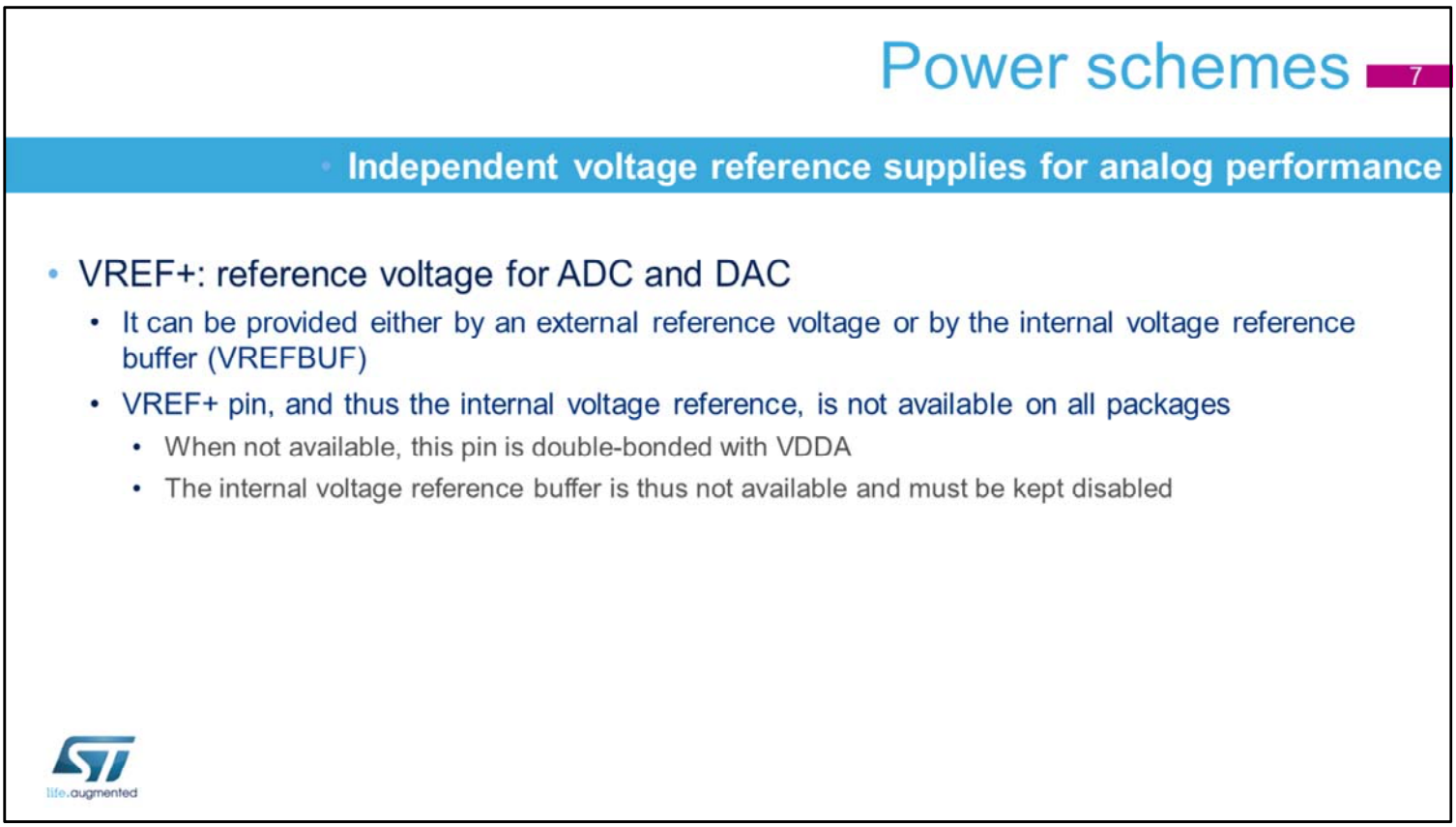


The main power supply, VDD, ensures full feature operation in all power modes from 1.71 up to 3.6 V, enabling it to be supplied by an external 1.8 V regulator. Device functionality is guaranteed down to 1.6 V, the minimum voltage after which a power-down reset is generated. Other independent supplies are provided to enable peripherals to operate at different voltages.

VDDA is the external analog power supply for Analog to Digital converters, Digital to Analog converters, voltage reference buffer, operational amplifiers and comparators. When the analog-to-digital converters or comparators are used, the VDDA voltage must be greater than 1.62 V. When the digital-to-analog converters or operational amplifiers are used, VDDA must be greater than 1.80 V. When the voltage reference buffer is used, VDDA must be greater than 2.4 V.

VDDUSB must be in the range 3.0 to 3.6 V. The VDDUSB power supply may not be present as a dedicated pin, but

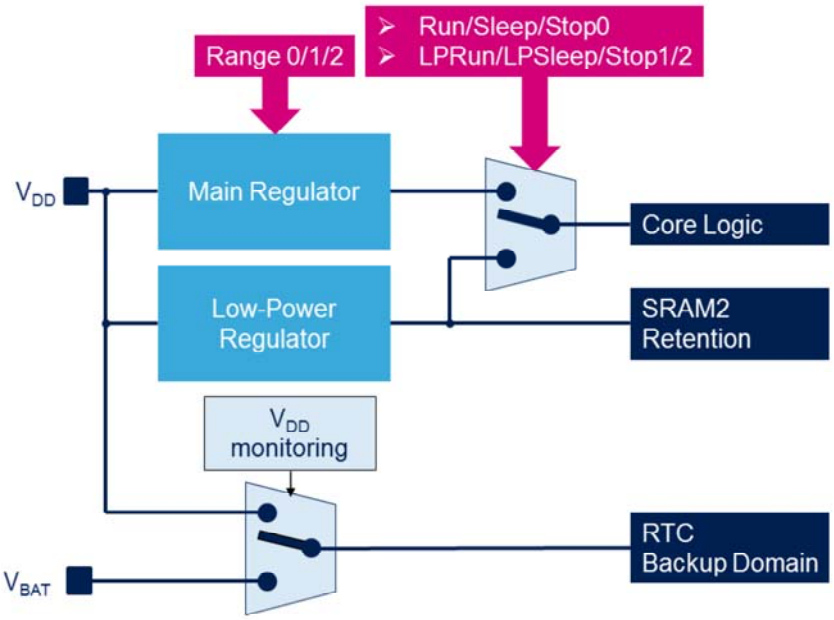
internally bonded to VDD. For such devices, VDD has to respect the VDDUSB supply range when the USB controller is used.
VDDIO2 must be in the range 1.08 to 3.6V.
VDDSMPS is the external power supply for the SMPS step down converter.
A backup domain is supplied by VBAT, which must be greater than 1.55 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator and the Tamp block containing the 128-byte backup registers. VBAT is internally bonded to VDD for small packages without dedicated pin.
VDD12 is the external power supply bypassing the internal regulator when connected to an external SMPS



The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer.
This improves the performance of the converters by providing an isolated and independent reference voltage.
The VREF+ pin and thus the internal voltage reference, is not available on certain packages.
In those packages, the VREF+ pin is double-bonded with VDDA and the internal voltage buffer must be kept disabled.
The voltage reference can be provided through the VDDA pin in those packages.

Voltage regulators

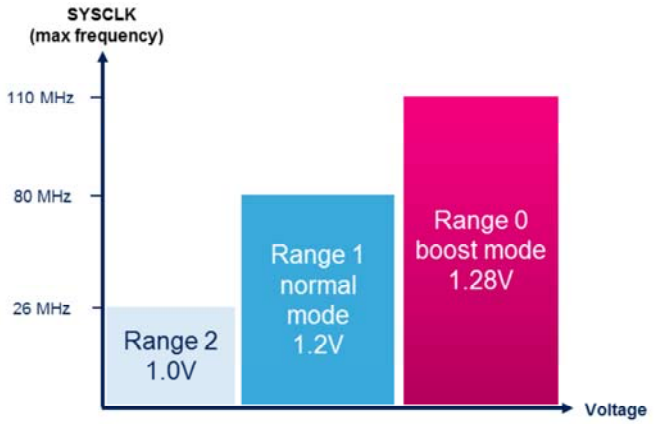
- Two Voltage Regulators
- One Main regulator with three voltage ranges for Dynamic Voltage Scaling; used in Run, Sleep and Stop 0 modes
- One Low-power regulator for Low-power run, Low-power sleep, Stop 1, and Stop 2 modes as well as for SRAM2 retention in Standby



Two embedded linear voltage regulators supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (V_{CORE}) can be programmed by software to three different values depending on the performance and the power consumption requirements. This is called Dynamic Voltage Scaling.
Depending on the application mode, V_{CORE} is provided either by the Main voltage regulator for Run, Sleep and Stop 0 modes, or by the Low-power regulator for Low-power run, Low-power sleep, Stop 1 and Stop 2 modes.
The regulators are OFF in Standby and Shutdown mode. When SRAM2 content is preserved in Standby mode, the Low-power regulator remains ON and provides the SRAM2 supply.

Main regulator: Voltage scaling range

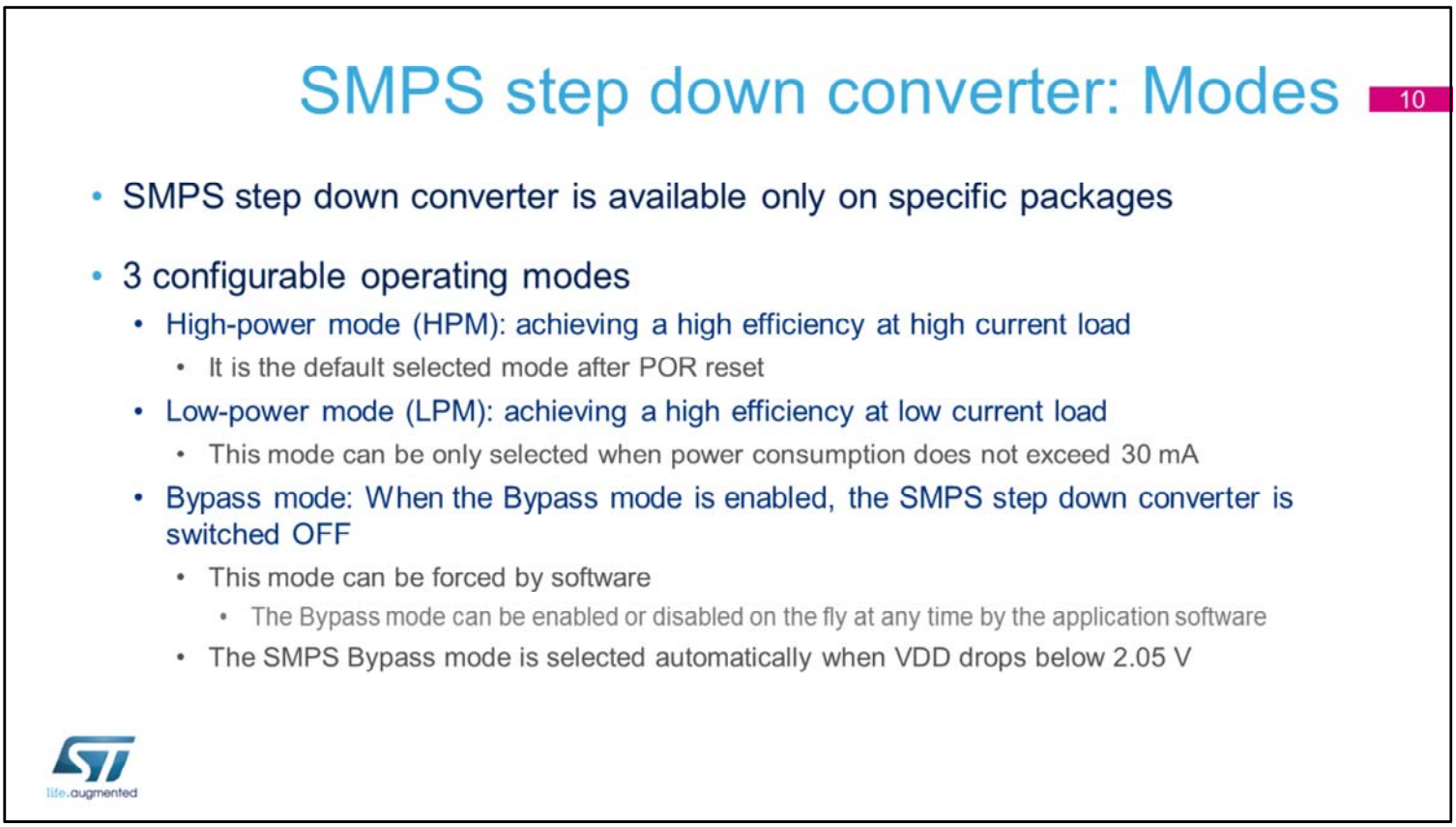
- Main regulator output voltage:
  - Range 0 :1.28V
  - Range 1 :1.2V
  - Range 2: 1.0V (default after reset)
- Voltage scaling is selected through the VOS[1:0] bits in the PWR_CR1 register



The dynamic voltage scaling is a power management technique which consists in increasing or decreasing the voltage used for the digital peripherals (VCORE), according to the application performance and power consumption needs

Here are the supported voltage and frequency pairs:

- Range 0: voltage is 1.28 V and frequency up to 110 MHz
- Range 1: voltage is 1.2 V and frequency up to 80 MHz
- Range 2: voltage is 1.0 V and frequency up to 26 MHz.



The SMPS step down converter is used to step down the V_{DD} supply.
When the SMPS step down converter is enabled, it can be configured in:

- High-power mode (HPM):
- Low-power mode (LPM):
- Bypass mode.

HPM achieves a high efficiency at high current load. SMPS high-power mode is used in all ranges (0, 1 and 2). It is the default selected mode after POR reset.
LPM achieves a high efficiency at low current load. When enabled, the voltage scaling must not be modified. This mode shall be only selected in Range 2 and when power consumption does not exceed 30 mA.
When the Bypass mode is enabled, the SMPS step down converter is switched OFF and it is possible to change the voltage scaling. This mode can be forced by software by setting the SMPSBYP bit in PWR_CR4 register. In Range 0

and Range 1, the SMPS Bypass mode is selected automatically when VDD drops below 2.05 V.
There is no automatic SMPS bypass in Range 2.
The Bypass mode can be enabled or disabled on the fly at any time by the application software

SMPS step down converter: States

System operating mode	SMPS step down converter state	Description
Run, Sleep	ON	SMPS in HPM or LPM mode and it switches to bypass mode following VDD minimum value versus the selected voltage range
Stop 0	ON	SMPS in HPM or LPM mode
Stop 1, Stop 2	Open	SMPS is bypassed, LPR regulator is used
Standby and Shutdown	Open	SMPS is bypassed

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During Stop 1, Stop 2, Standby and Shutdown modes the SMPS step down converter is switched to Open mode.
When exiting from low-power modes (except Shutdown) the SMPS step down converter is set by hardware to the mode selected prior to the low-power mode selection.
After POR reset, the SMPS step down converter is in High-power mode.

POR/PDR & BOR

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- **Safe and ultra-low-power reset management**
  - POR (Power On Reset)
    - Supervises V_{DD}
    - Fixed level to disable reset when V_{DD} level rises above threshold
  - PDR (Power Down reset)
    - Supervises V_{DD}
    - Fixed level to generate reset when V_{DD} level drops below threshold
  - BOR
    - Supervises V_{DD}
    - Brown-out reset is always enabled in all modes except Shutdown mode
    - Ensure reset as soon as V_{DD} drops below a selected threshold, regardless of the V_{DD} slope
    - 5 thresholds selected by the option byte **BOR_LEV[2:0],** from V_{BOR0} = 1.7 V to V_{BOR4} = 2.8 V

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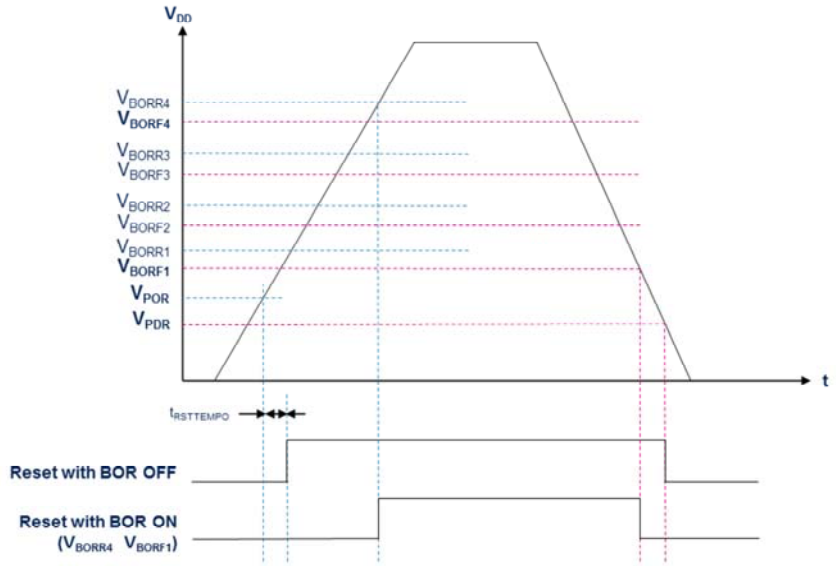
The Power reset (BOR and POR) resets all registers except those in the Backup domain powered by VBAT which contain the RTC and TAMP blocks and the external low-speed oscillator LSE.
When exiting Standby mode, all registers powered by the Main regulator are reset.
When exiting Shutdown mode, a Power reset is generated.
Five BOR levels can be selected via the option byte.
During power-on, the BOR keeps the device under reset until the supply voltage VDD reaches the specified VBORx threshold.
When VDD drops below the selected threshold, a device reset is generated.
When VDD is above the VBORx upper limit, the device reset is released and the system can start.
POR/PDR are always On, except in shutdown mode.

Brown Out and Power On/Down Reset



Active low reset

Five BOR levels can be selected through option bytes.
When VDD goes beyond the VBOR rising edge threshold value, the reset is negated.
When VDD goes below the VBOR falling edge threshold value, the reset is asserted.

Power Voltage Detector /Peripheral voltage monitor

- Power Voltage Detector, monitoring VDD, active in all modes except Standby and Shutdown
  - 7 thresholds + external pin, selectable by software
- Peripheral Voltage Monitor for V_{DDA}, V_{DDUSB}, V_{DDIO2} compares supply with selected threshold, with wakeup capability from Stop modes

PWM	Power supply	PVM threshold
PVM1	V_{DDUSB}	VPVM1: 12 V
PVM2	V_{DDIO2}	VPVM2: 09 V
PVM3	V_{DDA}	VPVM3: 165 V
PVM4	V_{DDA}	VPVM4: 18 V

- Two new STM32L5 features: temperature threshold monitoring and upper VDD voltage threshold monitoring

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A Power Voltage Detector (or PVD) can generate an interrupt when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby and Shutdown modes. The threshold is selected by software among seven possible values.
In addition, comparisons can be done between VREFINT and the PVD_IN external pin.
The VDDA power supply can be independent from VDD and can be monitored with two Peripheral Voltage Monitors (or PVM).
VDDIO2 and VDDUSB can also be monitored by dedicated PVMs.
Each PVM output is connected to an EXTI line and can generate an interrupt if enabled through the EXTI registers
This is a new feature, compared to STM32L4 microcontrollers.
The STM32L5 also supports two new features to enhance the power supply supervision:

- Temperature threshold monitoring
- Upper VDD threshold monitoring.

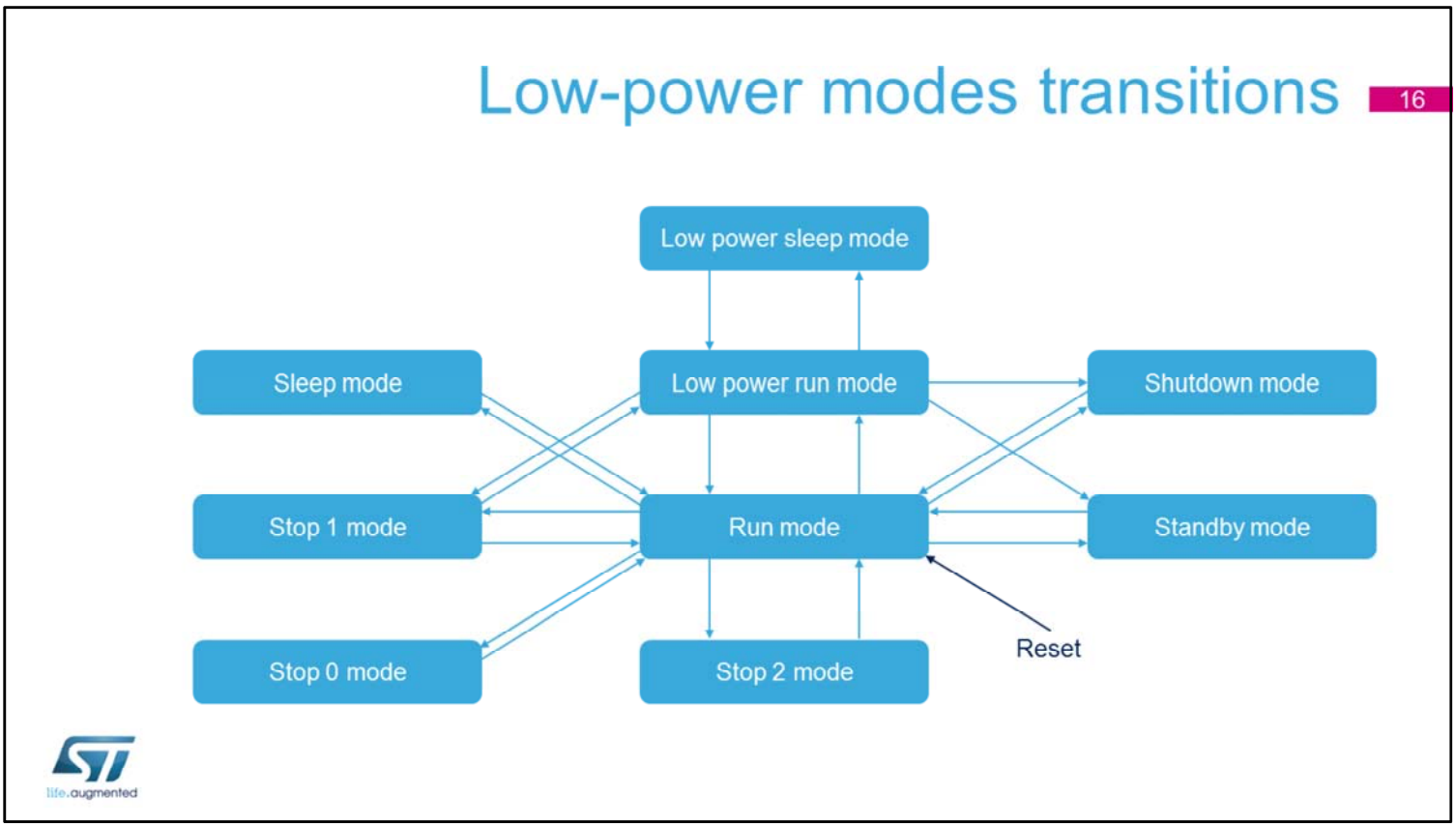
Whenever these monitors detect an abnormal condition, they can generate an internal tamper event.

Low Power modes

Flexibility between required performance and consumption

	STM32L552xx/562xx	STM32L4Rxxx/4Sxxx	STM32L476/486xx
Low Power Modes	STOP0		
	STOP1		
	STOP2	STOP2 SRAM3 OFF	STOP2
		STOP2 SRAM3 ON	
	STANDBY SRAM2 ON/OFF	STANDBY , SRAM2 ON/OFF	
	STANDBY SRAM2- Upper 4KB	NA	
	SHUTDOWN		

The STM32L5 offers a new feature compared to STM32L4: the SRAM2 can be entirely or partially retained in STANDBY mode.
Either 64 KB or the upper 4KB can be preserved.



From Run mode, it is possible to access all low-power modes except Low-power sleep mode.
In order to enter Low-power sleep mode, it is first required to enter Low-power run mode and execute a Wait for Interrupt or Wait for Event instruction while the regulator is the low-power regulator.
Similarly, when exiting Low-power sleep mode, the STM32L5 transits via Low-power run mode.
When the device is in Low-power run mode, it is possible to transition to all low-power modes except Sleep, Stop 0 and Stop 2 modes.
Stop 0 and Stop 2 modes can only be entered from Run mode.
If the device enters Stop 1 mode from Low-power run mode, it will exit in Low-power run mode.
If the device enters Standby or Shutdown, it will exit in Run mode.

Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF
  - After reset, all peripheral clocks are OFF, except Flash interface clock
  - SRAM clocks are always ON in Run mode
- When running from SRAM (in Run or Low-power run):
  - Flash memory can be put in Power-down mode (only in Low-Power run)
  - Flash interface clock can be switched off
  - Interrupt vectors must then be re-mapped to SRAM

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Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes.
By default all peripherals clocks are OFF, except the Flash interface clock.
The SRAM clock is always ON in Run mode.
When running from SRAM (in Run or Low-power run modes), the Flash memory can be put in Power-down mode, and the Flash clock can be switched off.
The Flash memory must not be accessed when it is switched off, consequently interrupt vectors must be mapped in SRAM, using the Cortex-M33 Vector Table Offset Register.

Run and Low-power run modes

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory (depending on the address of executed code)
  - Device configuration (depending on the application)
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash memory or SRAM
    - When execution from Flash memory: Accelerator configuration (Cache, Prefetch)
    - ➢ Energy efficiency better with Prefetch + Cache ON
    - When execution from SRAM:
    - ➢ Energy efficiency better versus Flash

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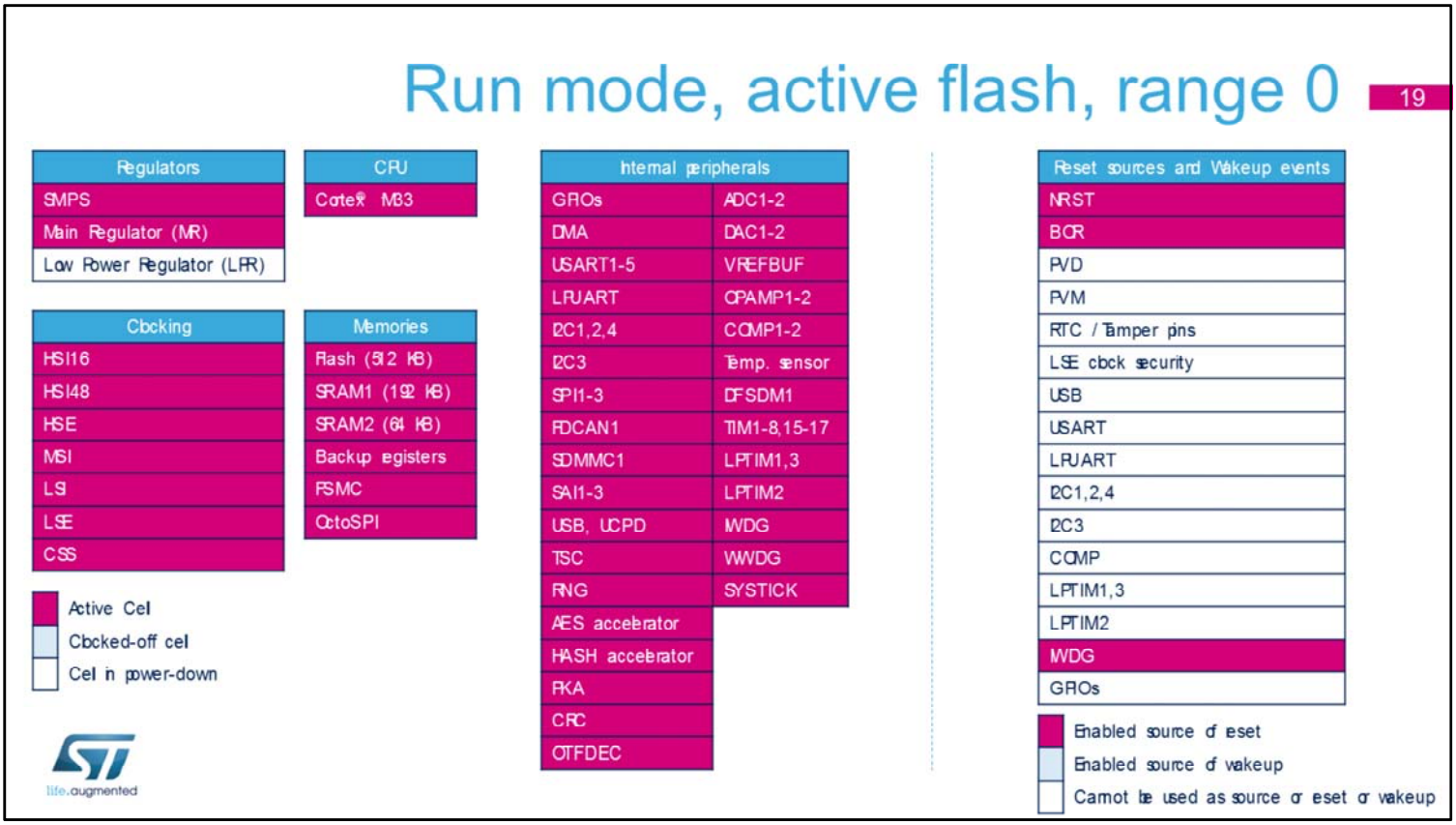
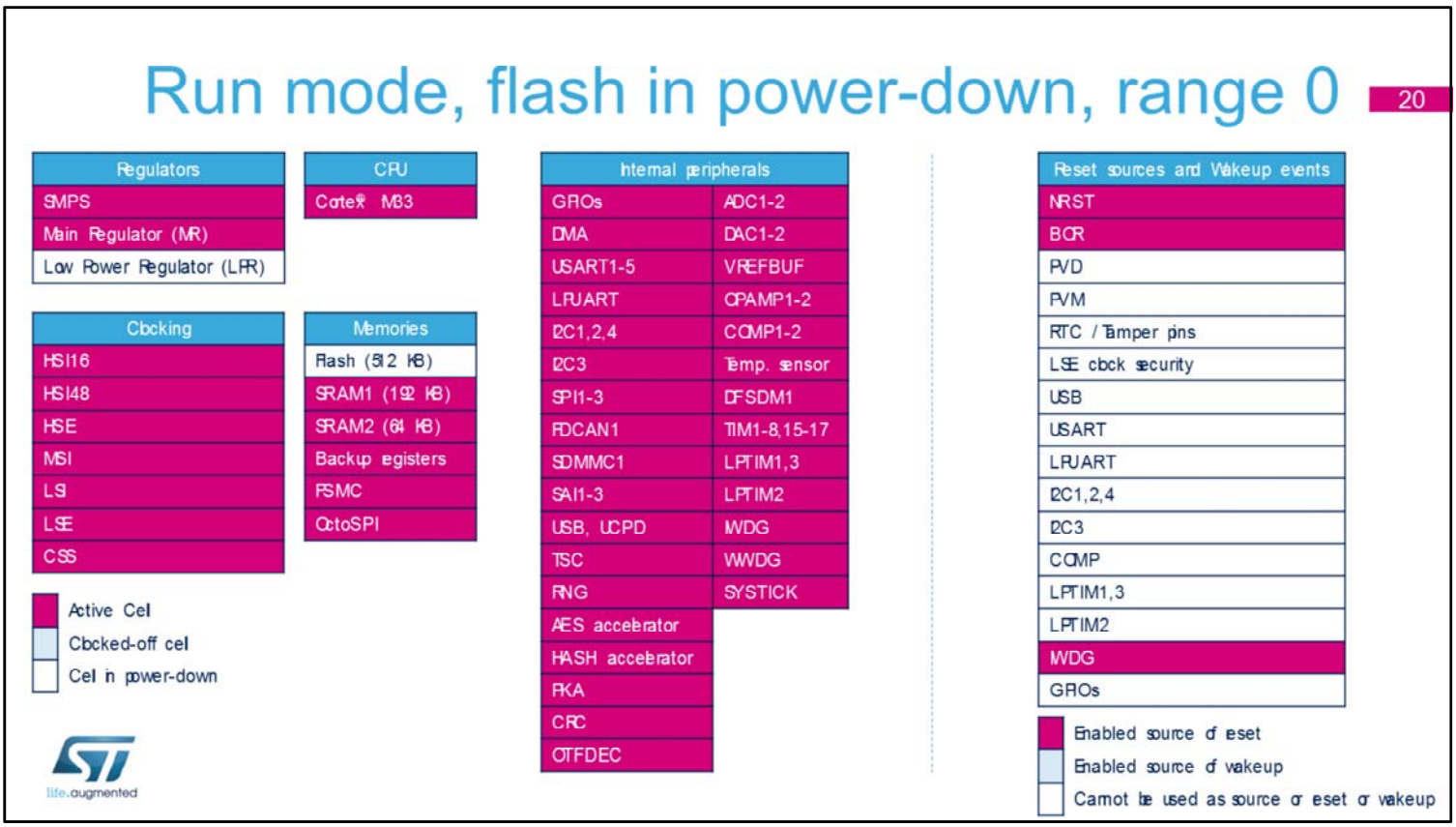
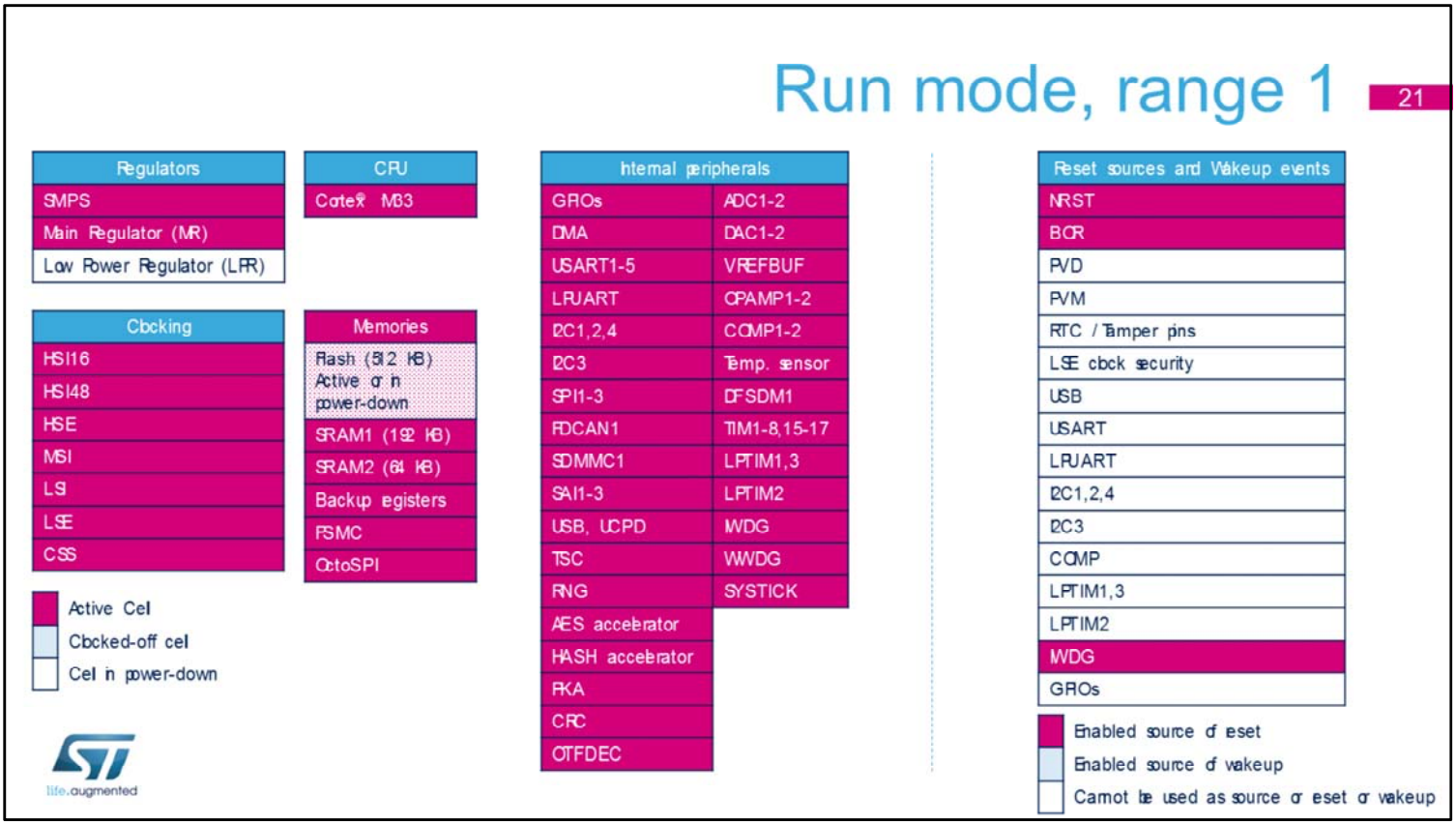
The current consumption in Run or Low-power run modes depends on several parameters: first the executed binary code, that means the program itself plus the compiler impact. Then it depends on the program location in the memory, the device software configuration, the I/O pin loading and switching rate and the temperature.
The consumption also depends on whether the code is executed from Flash memory or from SRAM. Energy efficiency is better when the Flash prefetch and the instruction cache are enabled. Executing from flash consumes more than executing from SRAM because the flash memory belongs to the VDD power domain while the SRAM belongs to the Vcore power domain.



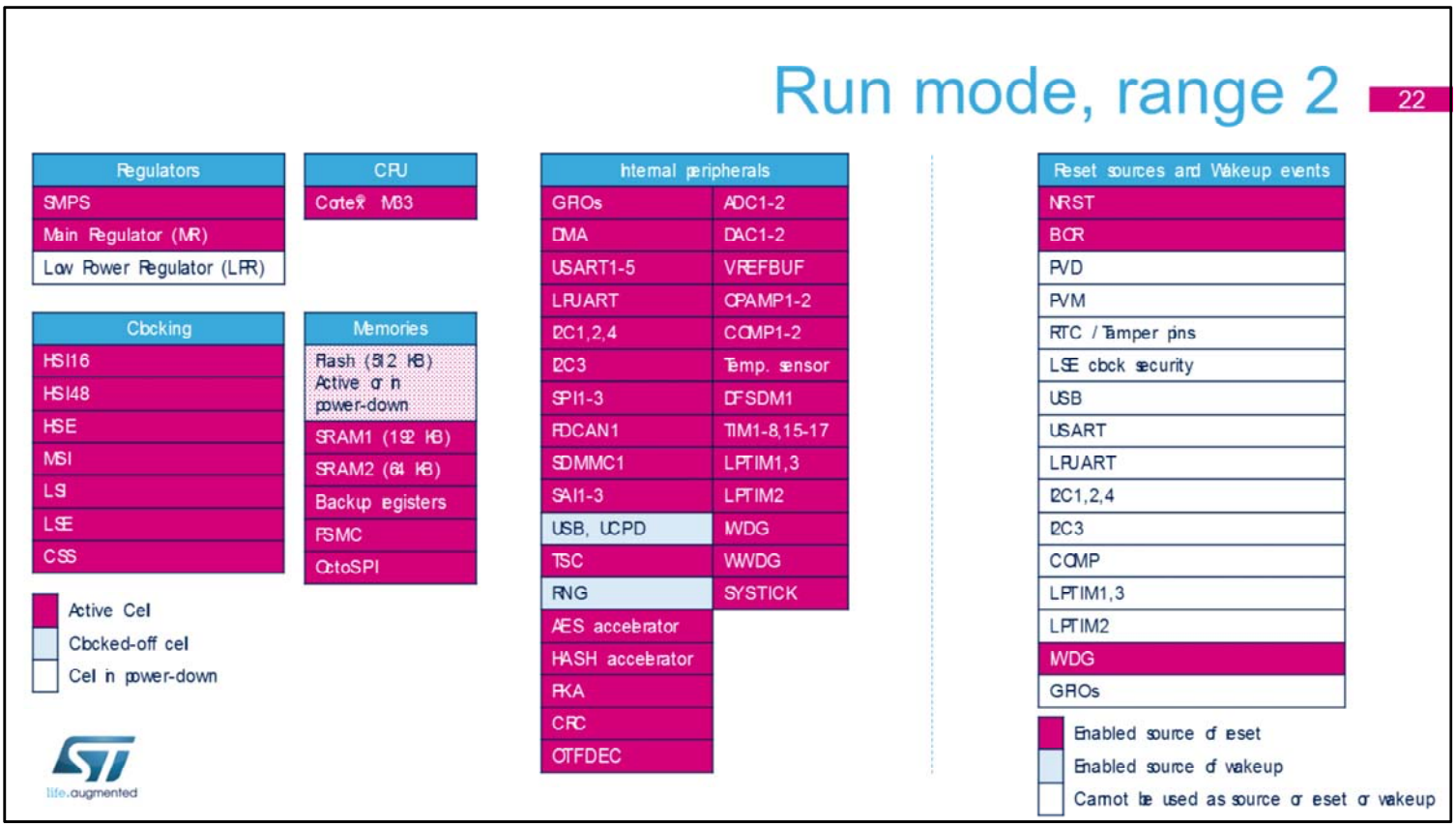
In Run mode, the CPU is clocked and program code can be executed from FLASH or SRAM Memory.
In Range 0, the system clock frequency is up to 110 MHz
All peripherals can be activated in Range 0.
In STM32L552xx and STM32L562xx, only the main regulator is active.
In STM32L552xxxP and STM32L562xxxP, both the main regulator and the SMPS are active.



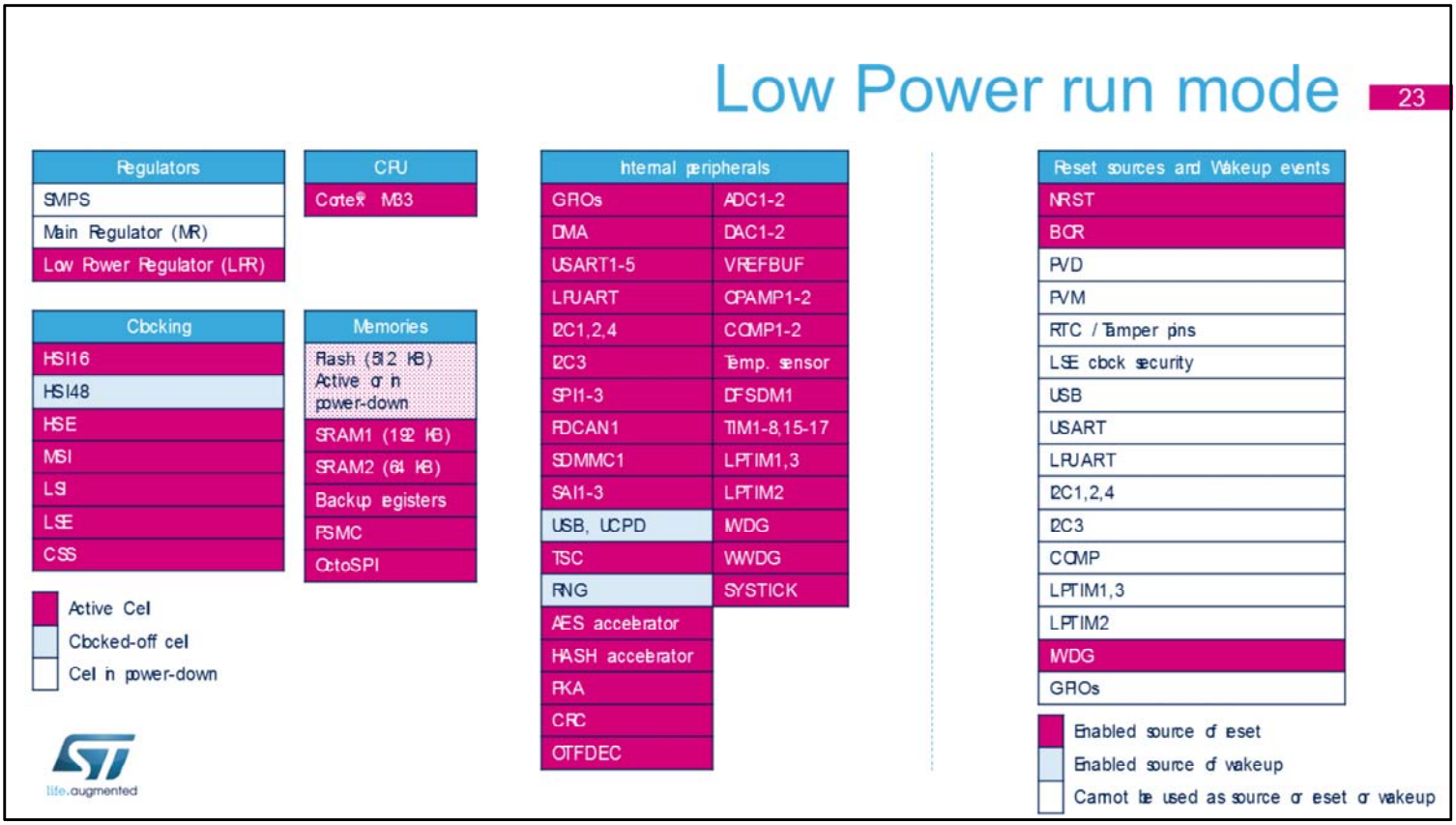
In range 0, when the internal flash memory is not needed, it can be powered down.



In Run mode, the voltage scaling Range 1 is the medium performance range, enabling a system clock frequency from 26 MHz to 80 MHz.
As in Range 0 mode, the internal flash memory can be powered down.
All peripherals can be activated.
All clocks can be enabled.



In Range 2, the system clock is up to 26 MHz.
All peripherals can be activated except the USB device and Random Number Generator.
All clocks can be enabled.



In Low Power Run mode, the CPU is clocked and program code can be executed from FLASH or SRAM, additionally the FLASH can be completely unpowered to save power.
The system clock is limited to 2 MHz.
The Main Regulator is switched off and supply to digital blocks is provided by the Low Power Regulator.
In Low Power mode, all peripherals except the USB device and Random Number Generator can be active.

Sleep and Low-power sleep modes

All peripherals available and fastest wakeup time

- Core is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing **WFI** (Wait For Interrupt) or **WFE** (Wait For Event)
- Two mechanisms to enter this mode:
  - **Sleep Now**: MCU enters Sleep mode as soon as WFI/WFE instruction are executed
  - **Sleep on Exit**: MCU enters Sleep mode as soon as it exits the lowest priority Interrupt Service Routine
    - The stack is not popped before entering Sleep mode, and nor will it be pushed when the next interrupt occurs, saving on running time
  - Controlled by Cortex®-M33 **SLEEPONEXIT bit in the System Control Register**

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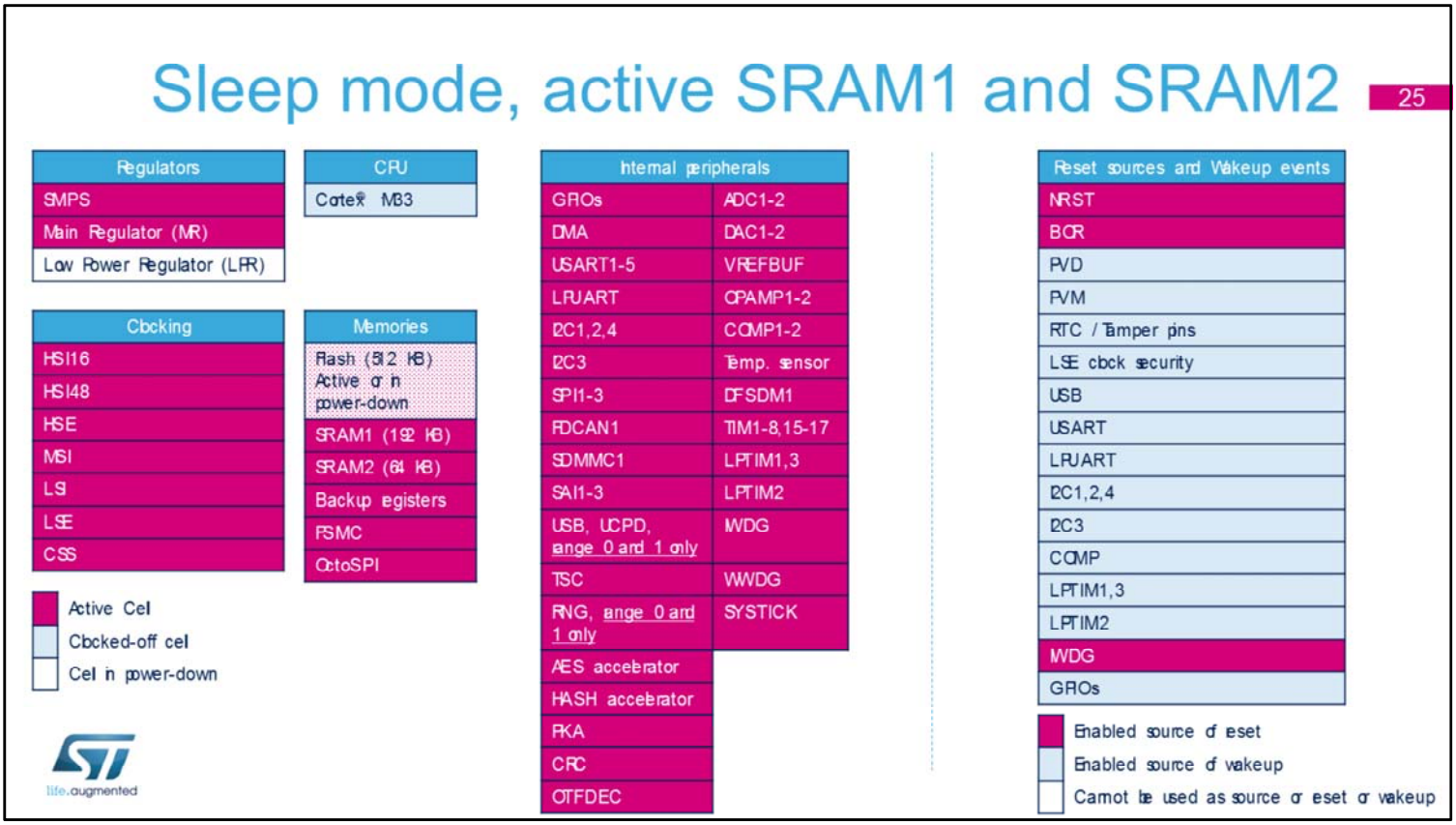
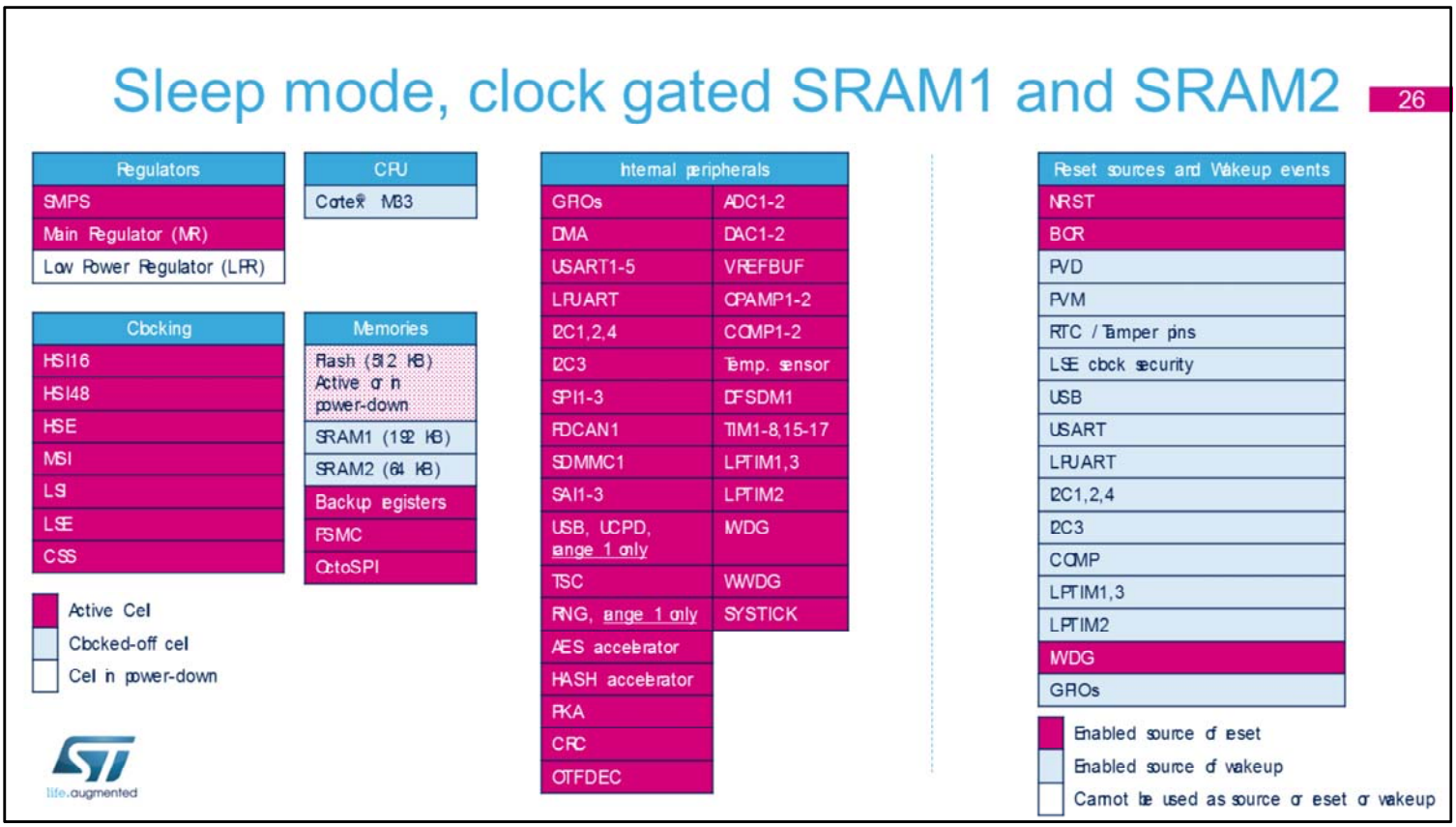
Sleep and Low-power sleep modes enable all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembly instruction Wait for Interrupt (or WFI) or Wait for Event (or WFE). When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the Cortex®-M33 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration saves time and consumption by avoiding the need to pop and push the stack when exiting the low power mode. However all computations must be done in Cortex®-M33 handler mode, because the thread mode is no longer used.

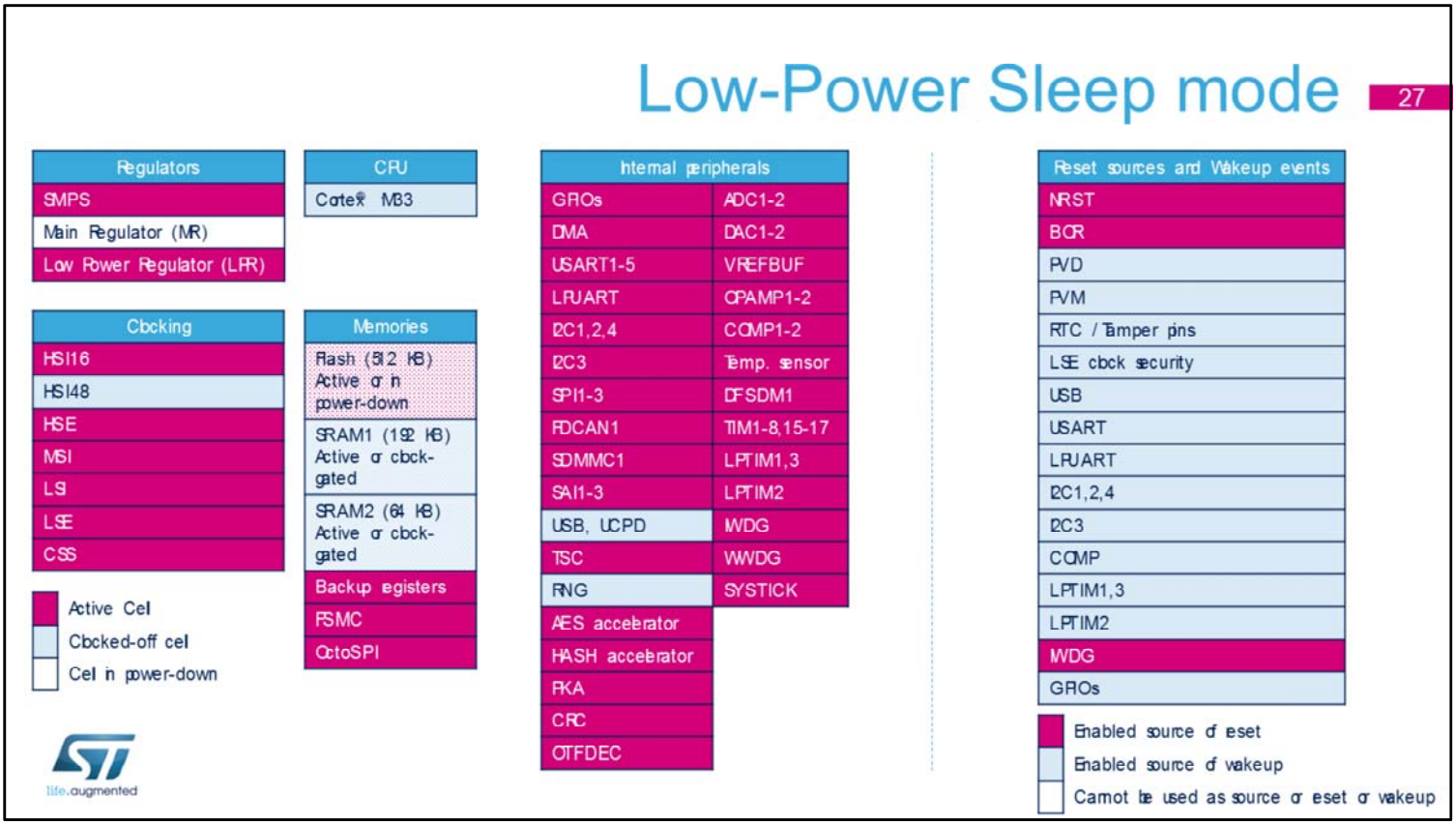


In Sleep mode, the CPU clocks are OFF.
In Range 0, the system clock is up to 110 MHz, in Range 1 it is up to 80 MHz and in Range 2, it is up to 26 MHz.
By default, the SRAM clocks are enabled.
They can be individually gated off during Sleep mode.
All peripherals can be activated in Range 0 and 1.
In STM32L552xx and STM32L562xx, only the main regulator is active.
In STM32L552xxxP and STM32L562xxxP, both the main regulator and the SMPS are active.

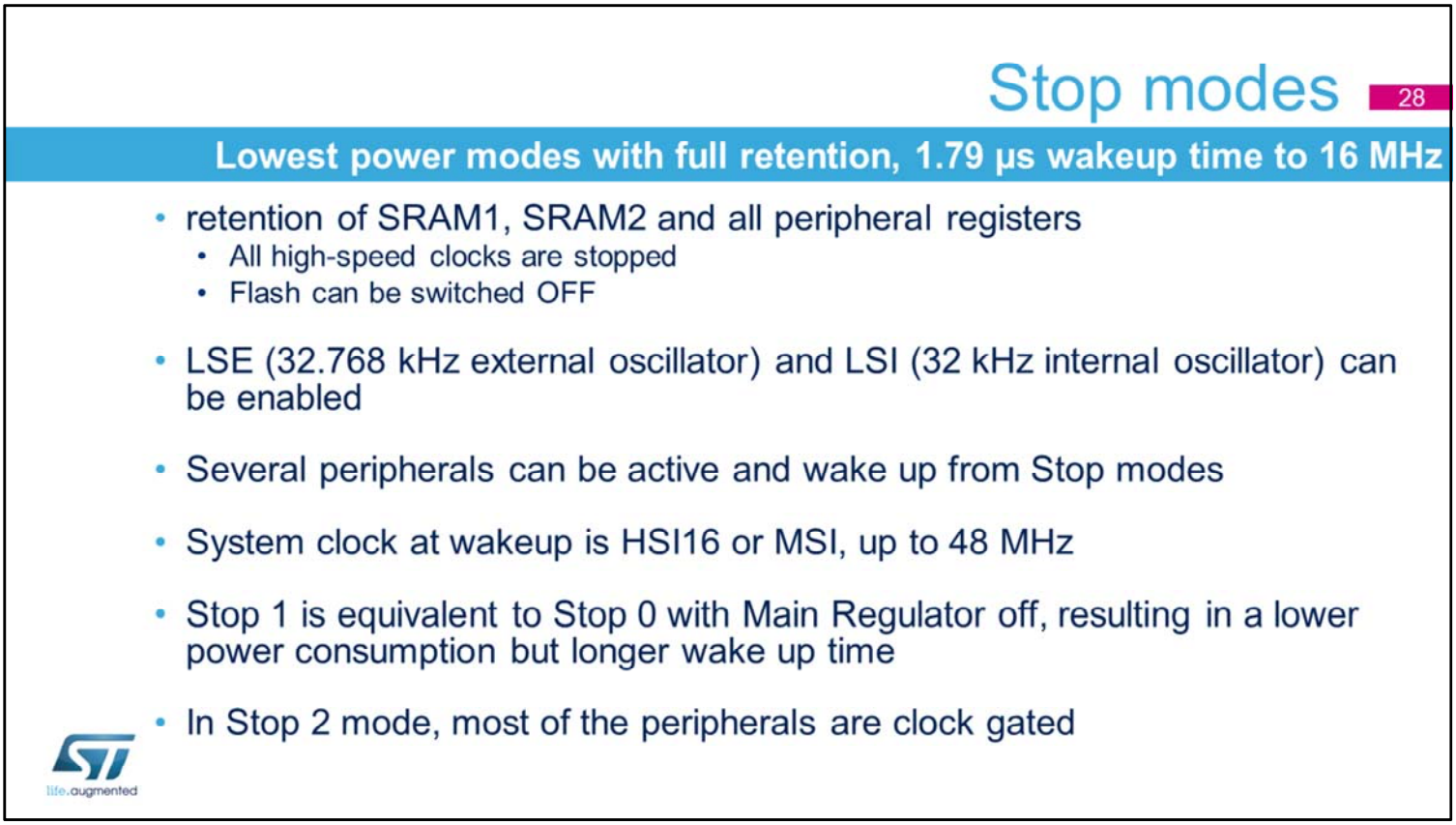
Sleep mode, clock gated SRAM1 and SRAM2



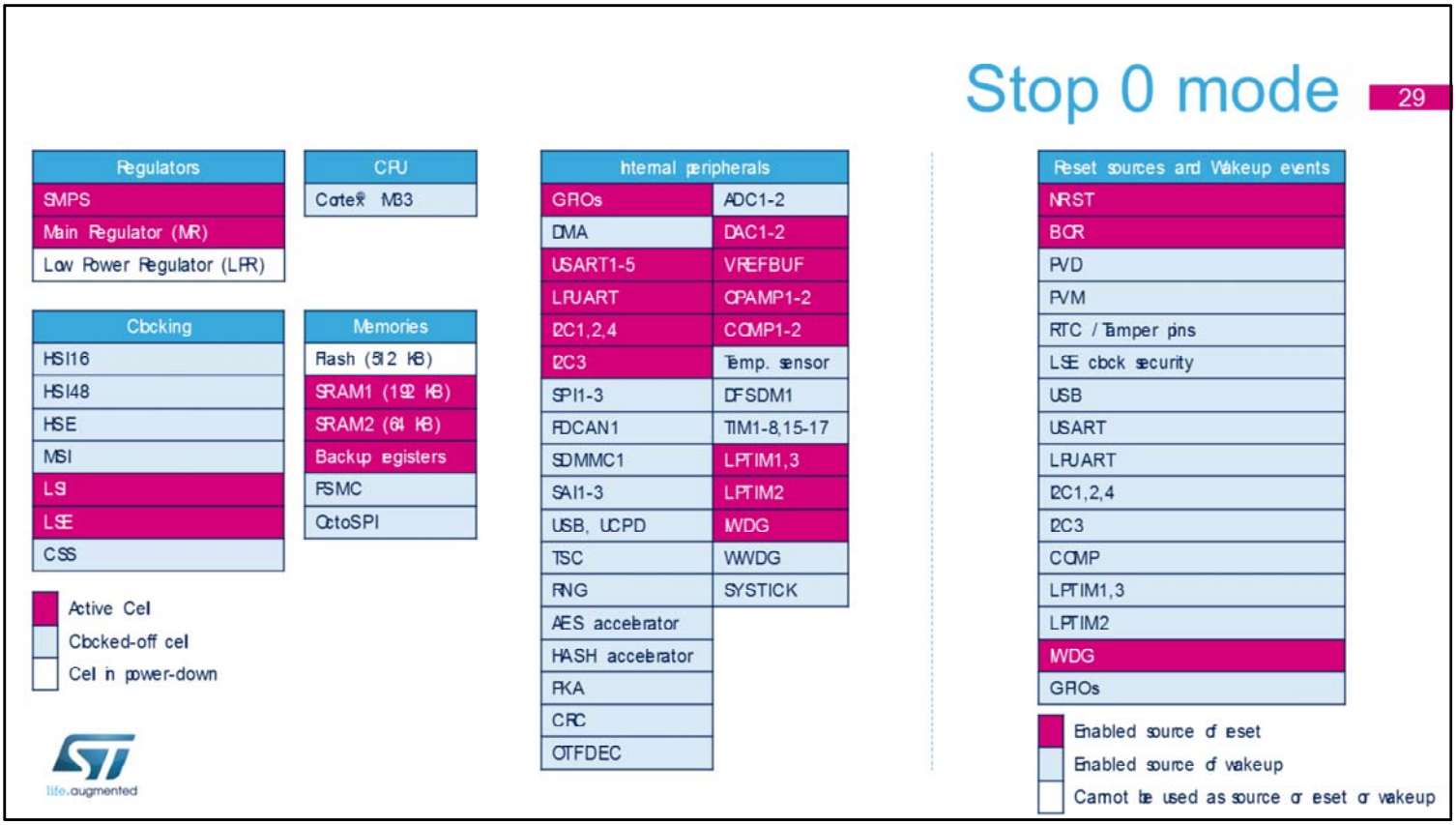
Clock gating is supported for SRAM1 and SRAM2 when Sleep mode is active.



In Low-power sleep mode, the CPU clock is OFF and the logic is supplied by the low-power regulator. The system clock is up to 2 MHz.
Flash memory can be configured in Power down and can be gated off; SRAMs can be gated off.
All peripherals can be activated except the USB OTG and Random Number Generator.

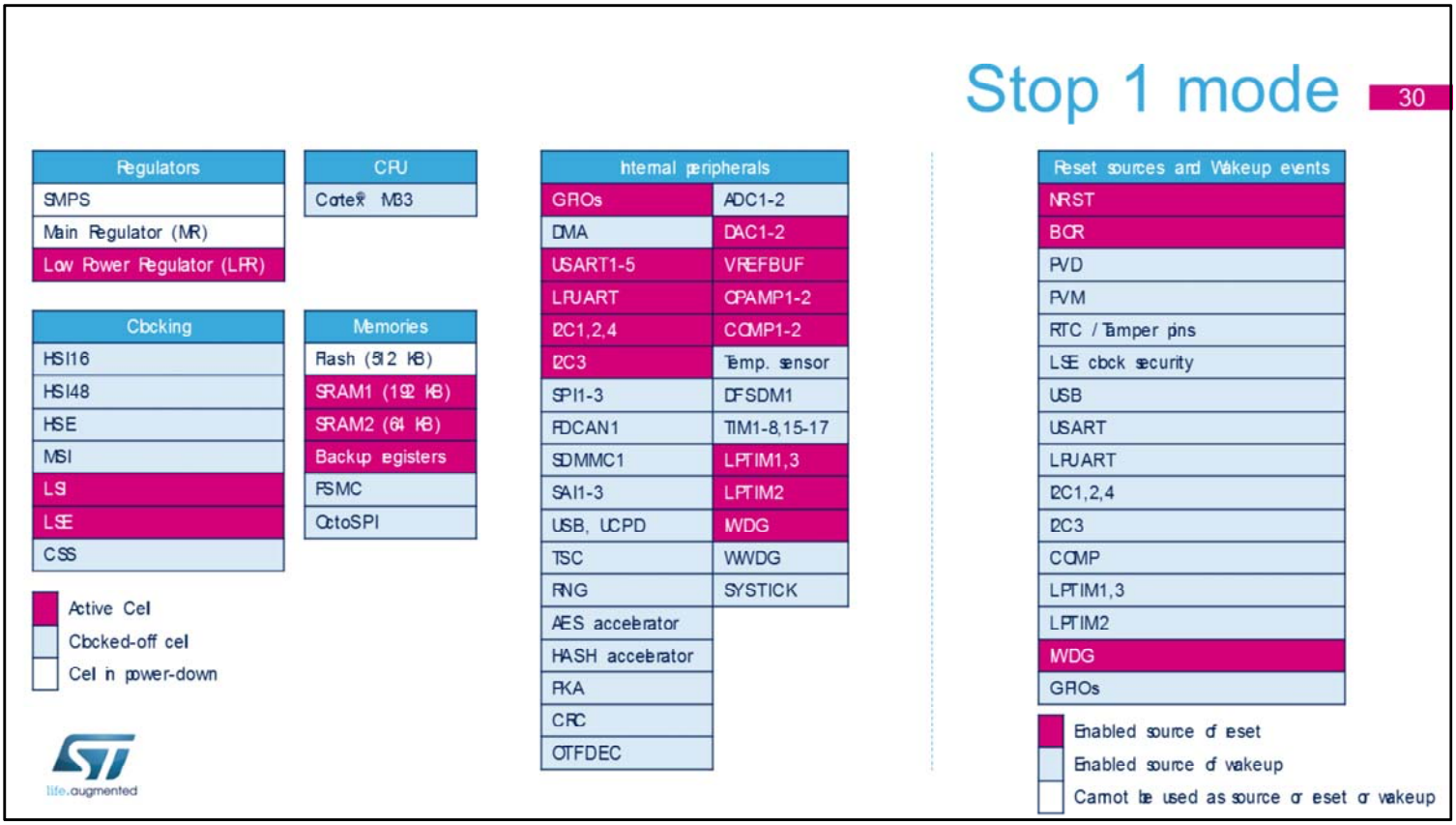


STM32L5 devices feature three Stop modes: Stop 0, 1, and 2, which are the lowest power modes with full retention and wakeup time of only a few µs to Run mode.
The contents of SRAM and all peripherals registers are preserved in Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop mode.
System clock on wake-up is the internal high-speed oscillator at 16 MHz or MSI up to 48 MHz.
Stop 1 is similar to Stop 0 with the Main regulator switched OFF.
In Stop 2, only LPUART, LP timers 1 and 3, I2C3 and comparators peripherals remain active.

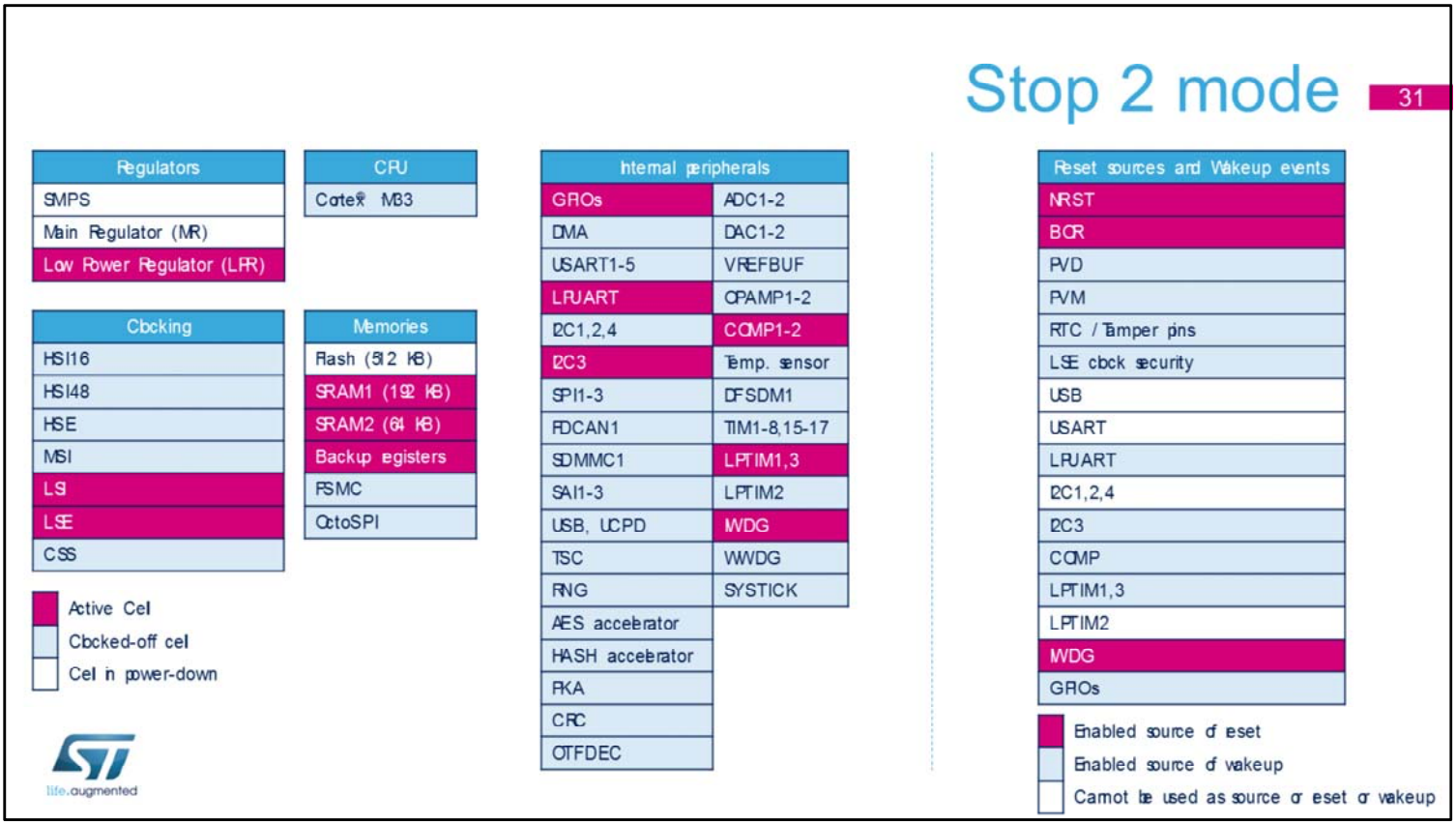


The voltage regulator is configured in main regulator mode
All clocks in the VCORE domain are stopped; the PLL and the HSE, HSI16, HSI48, MSI oscillators are disabled.
The RTC, clocked by the internal or external low-speed oscillator, can remain active.
The brown-out reset is always enabled. Most of the peripheral clocks are gated off.
Several peripherals can be functional in Stop 0 mode: Power voltage detector, Peripheral Voltage Monitor, digital to analog converters, operational amplifiers, comparators, VREFBUF, independent watchdog, low power timer, I2C, UART and low-power UART.
The events from all I/Os can wake up from Stop 0 mode, as well as the interrupt generated by the active peripherals. The I2C, UART, or LPUART can switch the HSI16 ON during the Stop mode in order to recognize their wakeup condition and switch off the HSI16 after receiving the frame if it is not a wakeup frame. In this case, the HSI16 clock is propagated

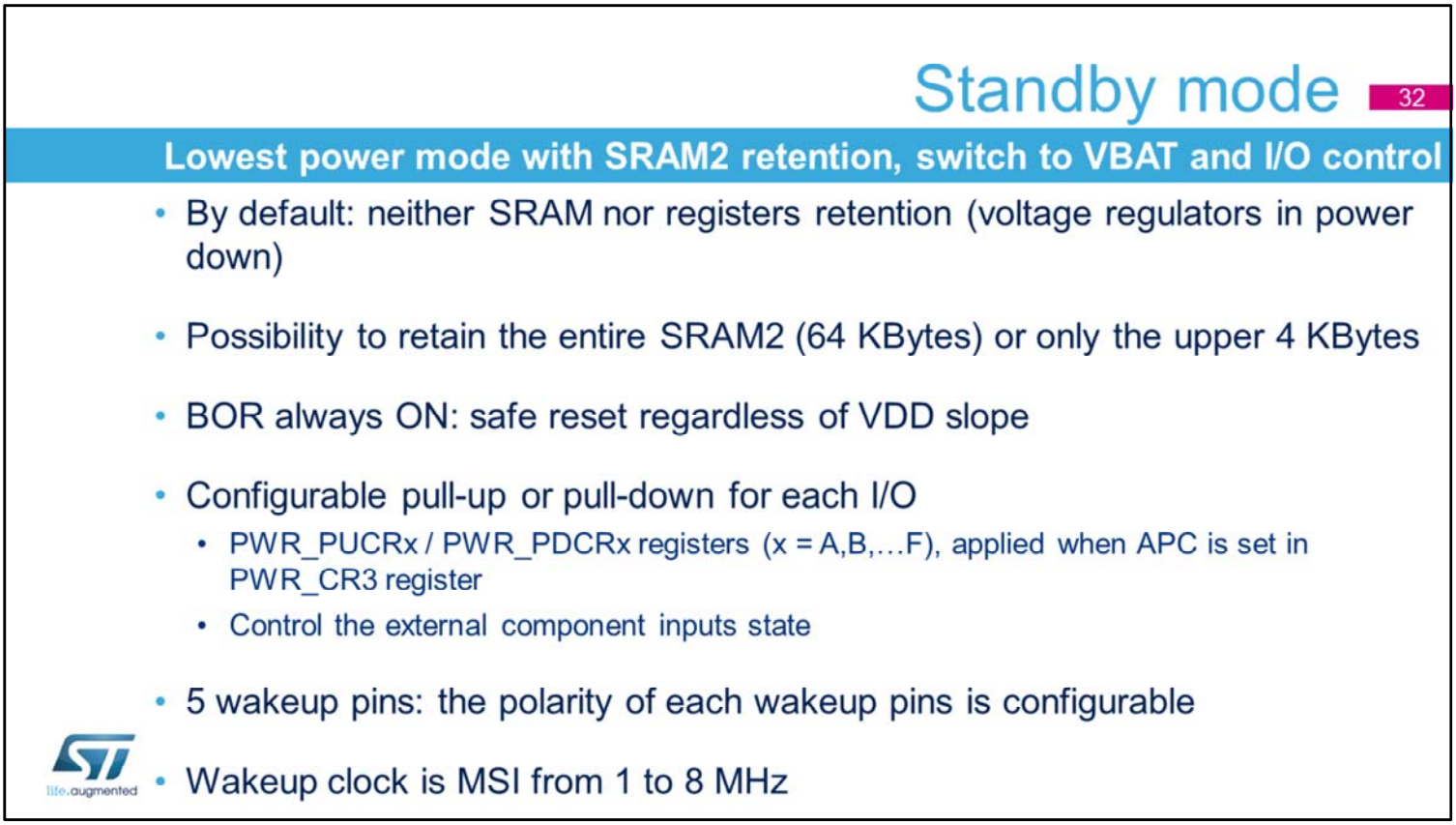
only to the peripheral requesting it.
The system clock, when exiting from Stop 0, Stop 1 or Stop 2 mode, can be either MSI up to 48 MHz or HSI16, depending on the software configuration.
In STM32L552xx and STM32L562xx, only the main regulator is active.
In STM32L552xxxP and STM32L562xxxP, both the main regulator and the SMPS are active.



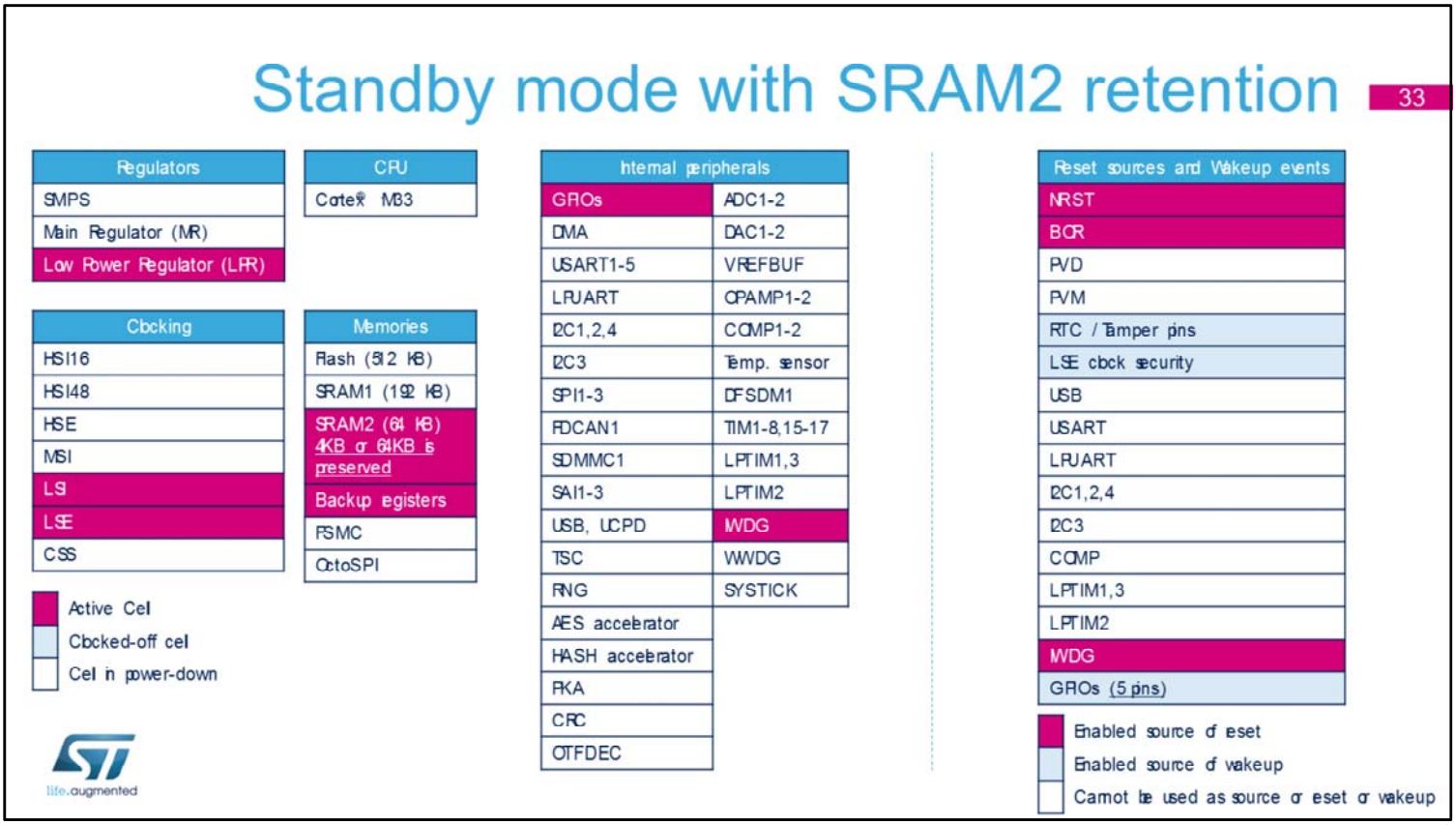
Stop 1 mode is very similar to Stop 0 except that the power figures are much lower as the main regulator is stopped and replaced by the Low Power Regulator.



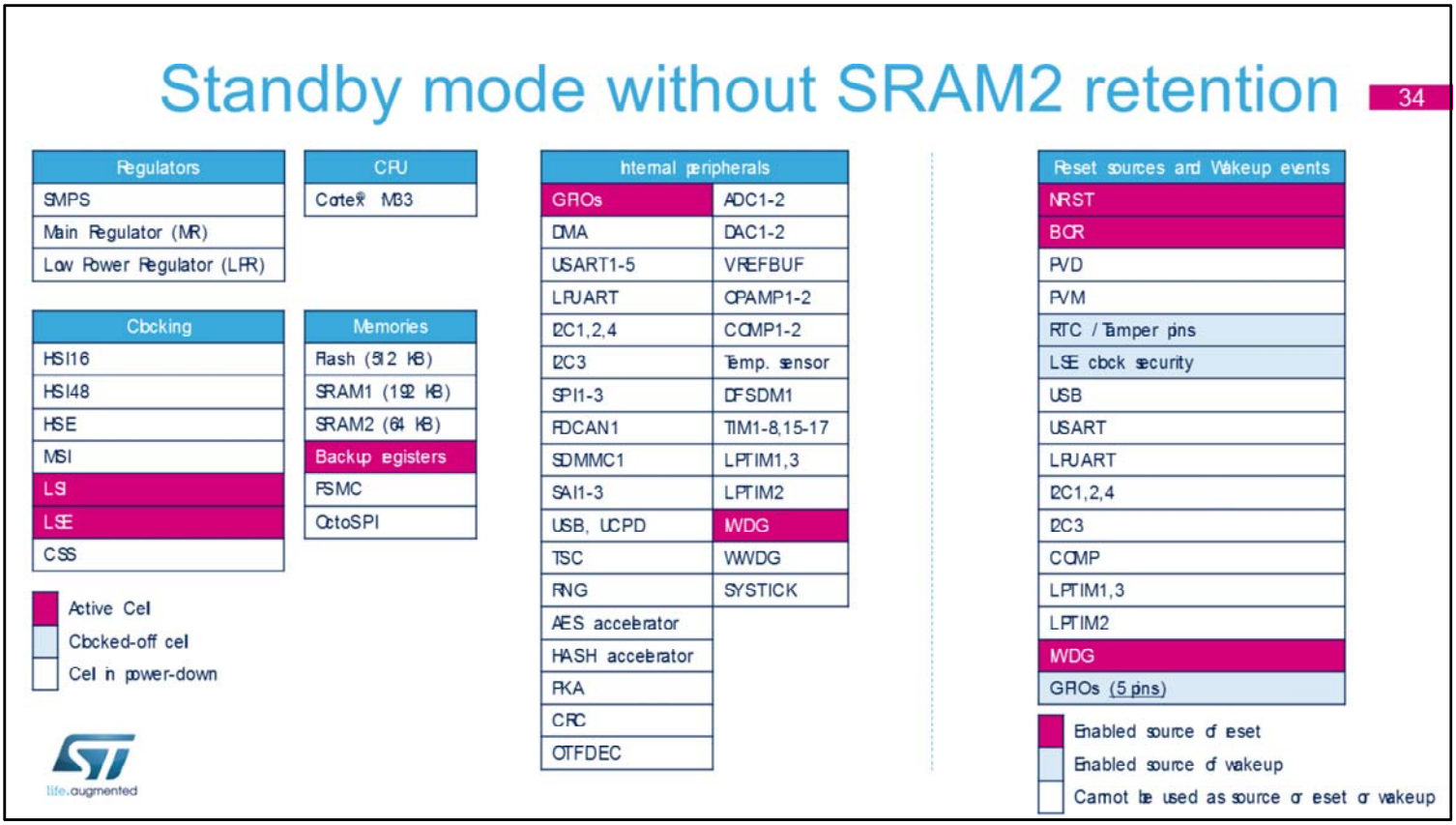
In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.
LPUART reception is functional in Stop 2 mode, and generates a wakeup interrupt on Start, address match or received frame event.
I2C3 address detection is functional in Stop mode, and generates a wakeup interrupt in the case of an address match.
During Stop 2, Standby and Shutdown modes, it is possible to set the BOR and PVD in Ultra-low-power mode to further reduce the power consumption.



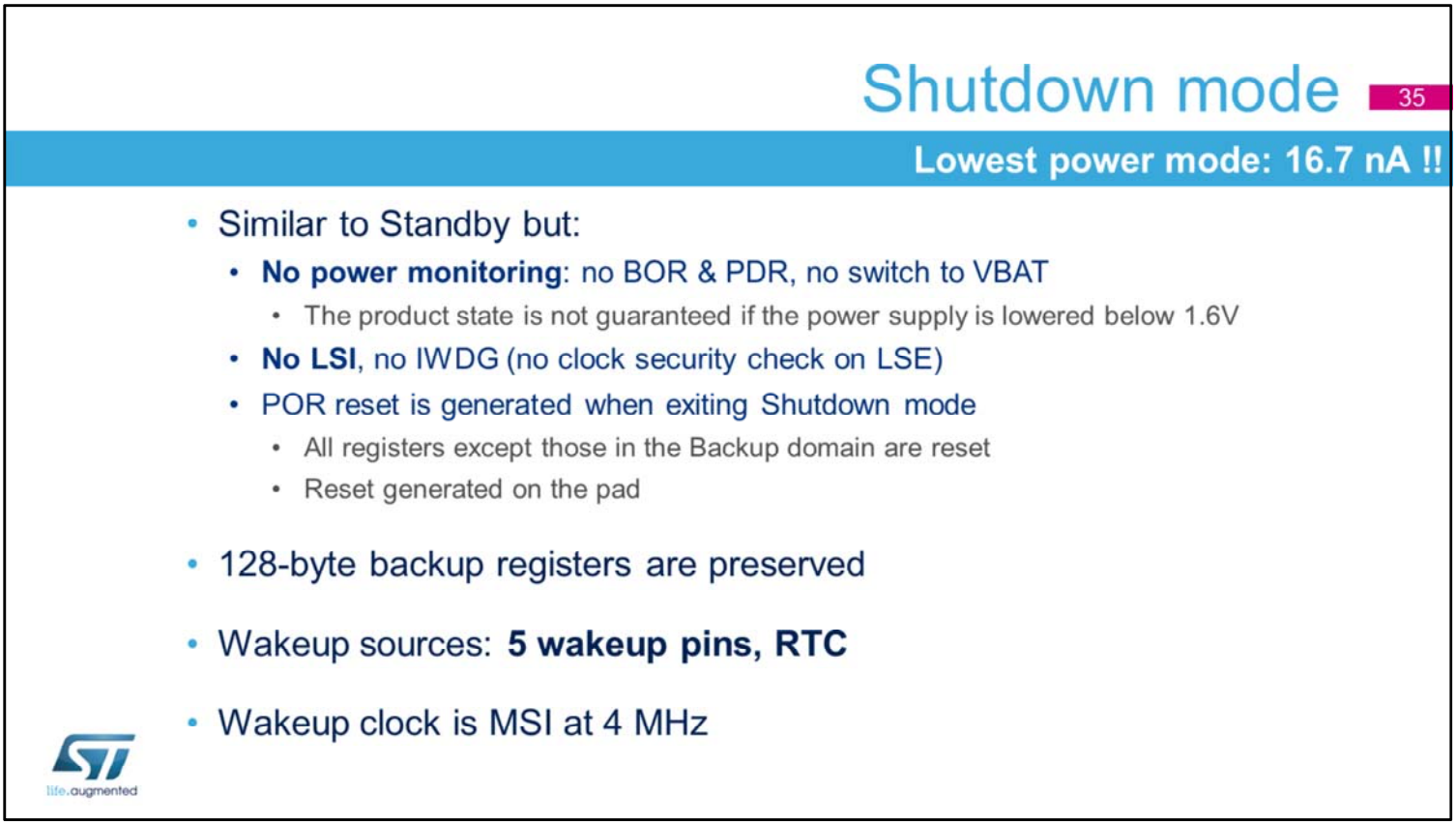
The Standby mode is the lowest power mode in which the contents of SRAM2 can be entirely or partially retained, the automatic switch from VDD to VBAT is supported and the I/Os level can be configured by independent pull-up and pull-down circuitry.
By default, the voltage regulators are in Power down mode and the contents of SRAM and peripheral registers are lost. The 128-byte backup registers are always retained.
The brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
Each I/O can be configured with or without a pull-up or pull-down, which is applied and released thanks to the APC control bit. This controls the input state of external components even during Standby mode.
5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of the 5 wakeup pins is configurable.
The wakeup clock is MSI from 1 to 8 Megahertz.



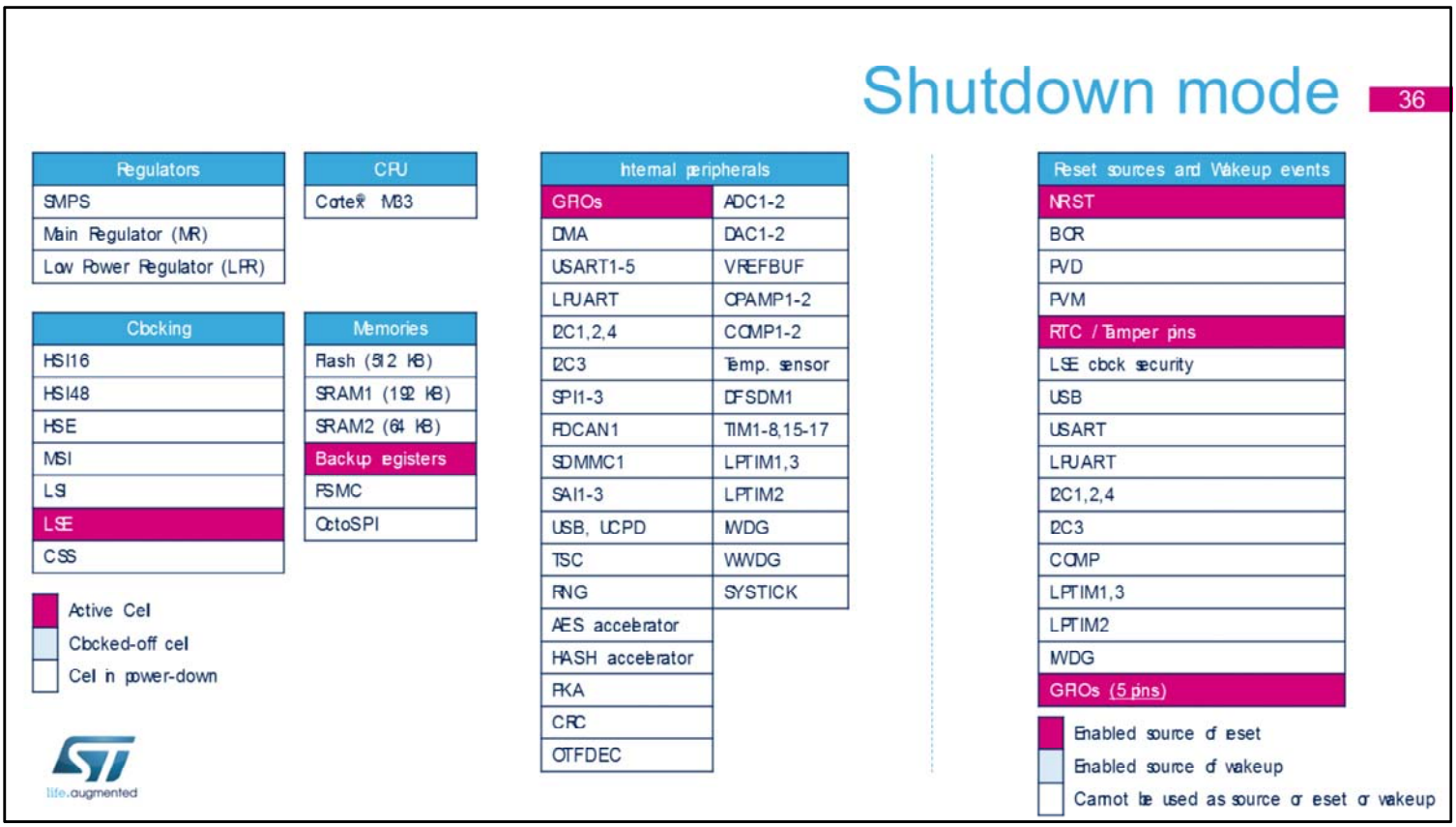
In Standby mode with SRAM2 retention, the main regulator is powered down and the low power regulator supplies the SRAM2 to preserve its content.
The RTC, clocked by the internal or external low-speed oscillator, may remain active.
The brown-out reset is always enabled. The independent watchdog can also be enabled in Standby mode.
Reset, brown-out reset, RTC and tamper detection, independent watchdog, LSE clock security and any event on the 5 wakeup pins can cause the microcontroller to exit Standby mode.
I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.



In Standby mode without SRAM2 retention, both main and low power regulators are powered down.
Wake-up events and available peripherals as well as wake-up sources are the same as in Standby mode with SRAM.



The shutdown mode is the lowest power mode of the STM32L5, with only 17 nA at 1.8 V.
This mode is similar to Standby mode but without any power monitoring: the power down reset is disabled and the switch to VBAT is not supported in Shutdown mode. Hence the product state is not guaranteed in case the power supply is lowered below 1.6V.
The LSI is not available, and consequently the independent watchdog is also not available.
A power reset is generated when the device exits Shutdown mode: all registers are reset except those in the backup domain, and a reset signal is generated on the pad.
The 128-byte backup registers are retained in Shutdown mode.
The wakeup sources are the 5 wakeup pins and the RTC events including tampers.
When exiting Shutdown mode, the wakeup clock is MSI at 4 MHz.



In Shutdown mode, the main regulator and the low-power regulator are powered down.
The RTC, clocked by the external low-speed oscillator, can remain active.
The brown-out reset is deactivated. Only the external low-speed clock can be enabled.
The wakeup events are the RTC and tamper events, the reset and the 5 wakeup pins.
I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals
Run	MR Range 0	Yes	ON(1)	ON	Any	All
	MR Range 1					All except USB, RNG
	MR Range 2					
LPRun	LPR	Yes	ON(1)	ON	Any except PLL	All except USB, RNG
Sleep	MR Range 0	No	ON(1)	ON(2)	Any	All Any interrupt or event
	MR Range 1					
	MR Range 2					
LPSleep	LPR	No	ON(1)	ON(2)	Any except PLL	All Any interrupt or event
Stop 0	MR	No	OFF	ON	LSE/LSI	Reset pin, all I/Os, BOR, PVD, PVM, RTC, IWDG, COMPx, DACx, OPAMPx, USARTx, LPUART, I2Cx, LPTIM1, USB, UCPD
Stop 1	LPR					Reset pin, all I/Os, BOR, PVD, PVM, RTC, IWDG, COMPx, DACx, OPAMPx, LPUART, I2C3, LPTIM1 and 3
Stop 2	LPR					
Standby	LPR	DOWN	OFF	SRAM2 ON	LSE/LSI	Reset pin, 5 WKUPx pins BOR, RTC, IWDG
	OFF			DOWN		
Shutdown	OFF	DOWN	OFF	DOWN	LSE	Reset pin, 5 WKUPx pins RTC

1. Can be put in power-down and clock can be gated off
2. SRAM1 and SRAM2 can be gated off independently

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Here you can see the summary of all the STM32L5 power modes.

VBAT backup domain

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **3 tamper pins**
  - **128 bytes backup registers**
  - Reset through the RCC_BDCR
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on
- Internal connection to ADC for voltage monitoring ($V_{BAT}/3$)
- VBAT battery charging

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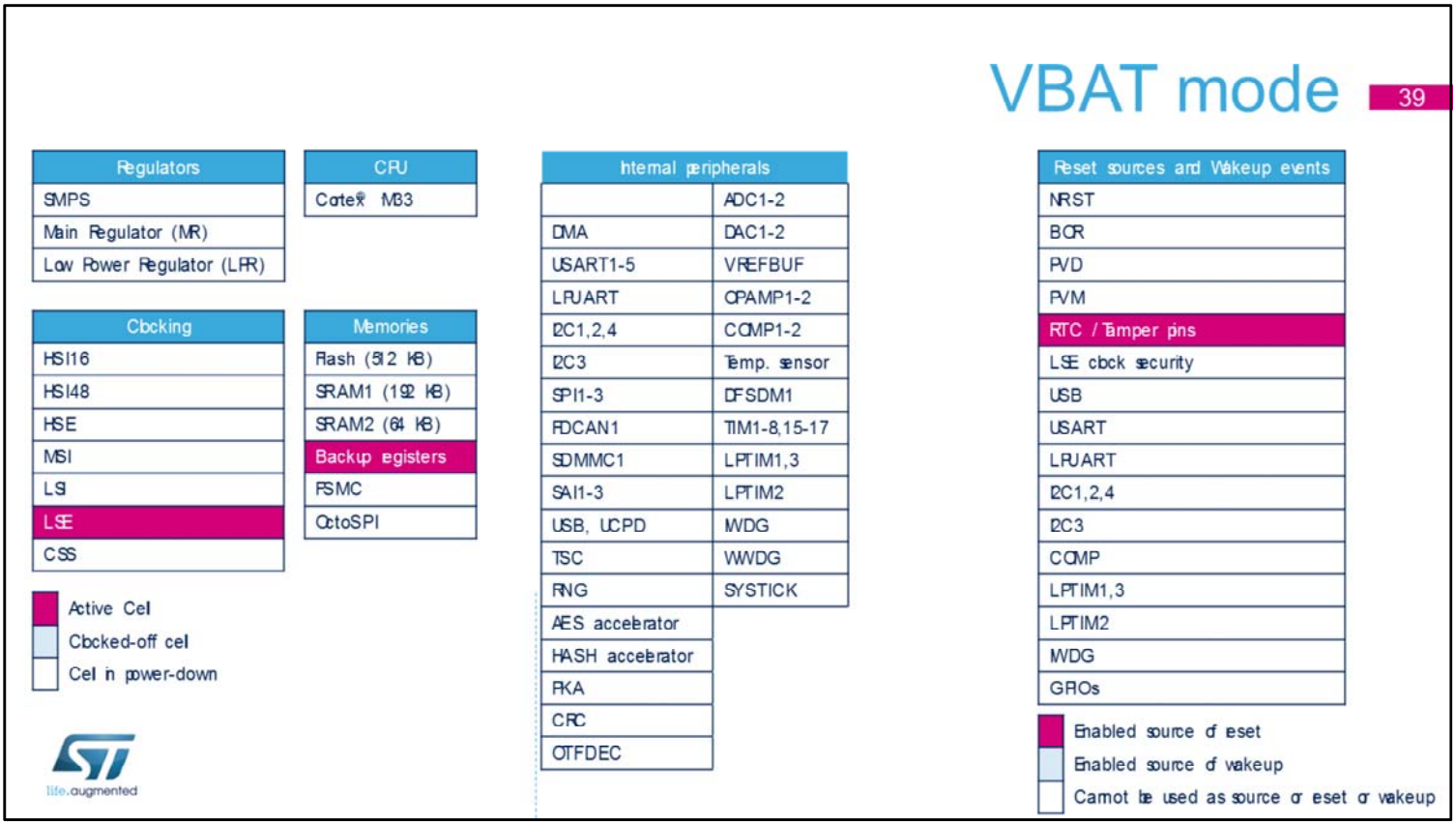
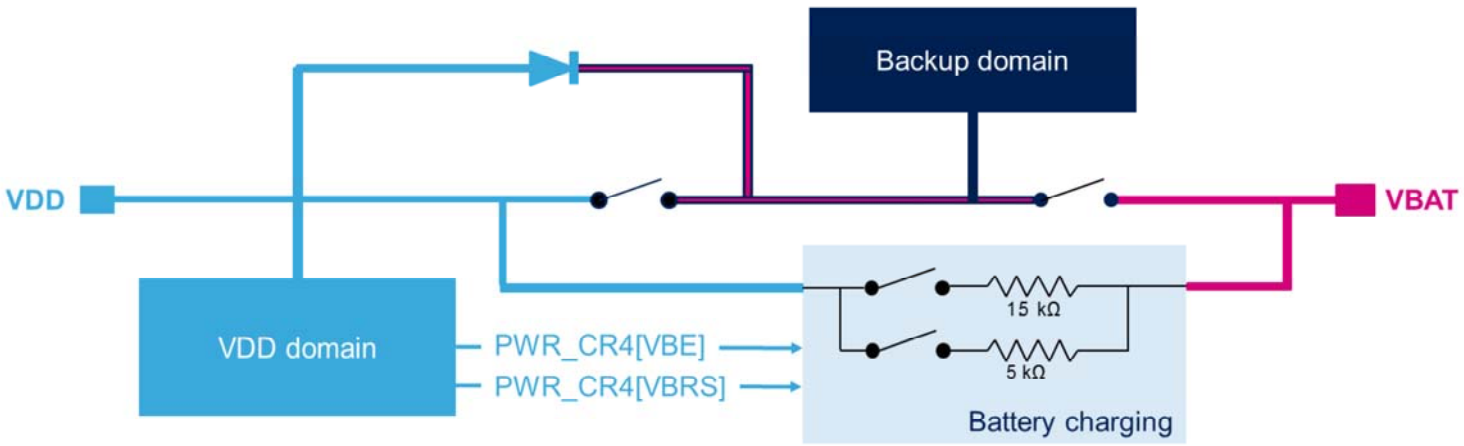
The backup domain keeps the RTC fully functional and preserves the backup registers if the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz.
Three tamper pins are functional in VBAT mode, and will erase the 128-byte backup registers also included in the VBAT domain, in the case of an intrusion detection.
The backup domain also contains the RTC clock control logic.
If VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When VDD is present, the battery connected to VBAT can be charged from the VDD supply.



In VBAT mode, the main regulator and the low-power regulator are powered down.
The RTC and Tamper, clocked by the external low-speed oscillator, can remain active.
Only the external low-speed clock can be enabled.
The only powered block is the backup domain that includes RTC and Tampers, and the return to normal execution happens once VDD supply is provided.
The VBAT consumption without RTC is typically around 3.4 nA at 1.8 V.

VBAT backup domain

- VBAT battery charging: enables the charging of a super-capacitor on VBAT through an internal resistor when V_{DD} is present.



The battery charging feature enables the charging of a super-capacitor connected to VBAT pin through the internal resistor when VDD supply is present.
The charging is enabled by software and is done either through a 5kΩ or 1.5kΩ resistor depending on the software.
Battery charging is automatically disabled in VBAT mode.
The VBE bit field of the PWR_CR4 register enables battery charging.
The VBRS bit field of the PWR_CR4 register selects the resistance value.
During the startup phase, if VDD is established in less than tRSTTEMPO and VDD is greater than VBAT + 0.6 V, a current may be injected into VBAT through an internal diode connected between VDD and the power switch (VBAT).
If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin

Option bytes

- 3 option bits can be configured in Flash option bytes to prohibit a given low-power mode:
  - nRST_SHDW: When cleared, a Reset is generated when entering Shutdown mode
  - nRST_STDBY: When cleared, a Reset is generated when entering Standby mode
  - nRST_STOP: When cleared, a Reset is generated when entering Stop modes

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Three bits are available in the Flash option bytes to prohibit a given low-power mode.
When cleared, a reset is generated instead of entering the related low-power modes.

Debug information

- Three bits in the DBGMCU_CR register enable debugging in Sleep, Stop, Standby and Shutdown modes:
  - DBG_STANDBY: When set, the digital part is not powered down in Standby and Shutdown modes, and HCLK and FCLK remain ON, provided by internal RC
    - In addition, the MCU in under system reset in Standby/Shutdown mode
  - DBG_STOP: When set, HCLK and FCLK remain ON in Stop modes, provided by internal RC
- When these bits are set, the connection with debugger is kept during the low-power mode
  - After wakeup, debug is still possible

The microcontroller integrates special means allowing the user to debug software in low-power modes.
Three bits are available in the Debug Control Register, in order to allow debugging in Stop, Standby and Shutdown modes. When the related bit is set, the regulator is kept ON in Standby and Shutdown modes, and the HCLK and FCLK clocks remain ON to keep the debugger active. This maintains the connection with the debugger during the low-power modes, and continues debugging after wakeup.
Remember to clear these bits when the MCU is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the clocks and the regulators to remain enabled

PWR: TrustZone Security

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- Independent security bits to secure PWR fonctionalities, in the PWR_SECCFGR register:
  - Low-power mode, Wake-up (WKUP) pins, Voltage detection and monitoring, VBAT mode
- Additional PWR configuration bits are automatically secure:
  - If System clock selection is secure in RCC:
    - The voltage scaling (VOS) configuration in PWR is secure
  - If a GPIO is configured as secure:
    - Its corresponding bit in PWR for Pull-up/Pull-down configuration in Standby mode is secure
  - If the RTC is secure:
    - The backup domain write protection DBP bit in PWR is secure
  - If the UCPD is secure:
    - The UCPD_DBDIS bit (USB Type-C and power delivery dead battery disable) and UCPD_STDBY bit (USB Type-C and power delivery Standby mode) in PWR are secure

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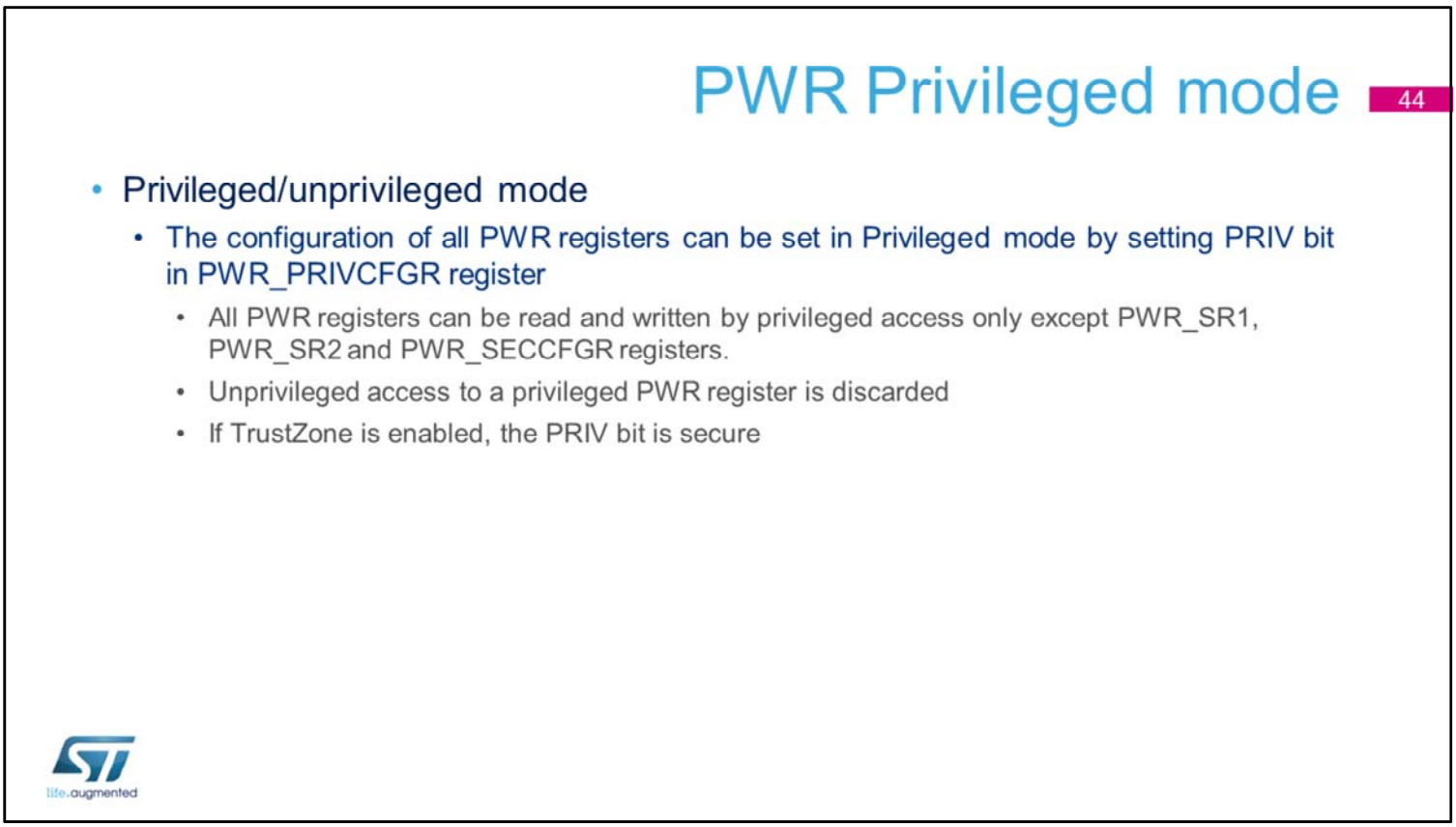
The PWR is a trustzone-aware module.
When the TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register, some PWR register fields can be secured against non-secure access.
The PWR TrustZone security secures the following features through the security configuration register PWR_SECCFGR: Low-power mode, Wake-up (WKUP) pins, Voltage detection and monitoring and VBAT mode.
Other PWR configuration bits are secure when:

- The system clock selection is secure in RCC, the voltage scaling (VOS) configuration is secure
- A GPIO is configured as secure, its corresponding bit for Pull-up/Pull-down configuration in Standby mode is secure
- The RTC is secure, the backup domain write protection DBP bit in PWR_CR1 register is secure
- The UCPD is secure, the UCPD_DBDIS and UCPD_STDBY bits are secure in the PWR_CR3 register.

A non-secure write access to PWR_SECCFGR register is Write Ignored and generates an illegal access event.



The PWR registers can be can be read and written by privileged and unprivileged accesses depending on PRIV bit in PWR_PRIVCFGR register.

- When the PRIV bit is reset, all PWR registers could be read and written by both privileged or unprivileged access
- When the PRIV bit is set, all PWR registers could be read and written by privileged access only (except PWR_SR1, PWR_SR2 and PWR_SECCFGR registers)

Unprivileged access to a privileged registers is read as zero, write ignore.

Related peripherals

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- Refer to the following list of training presentations for more details of their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Real-time clock (RTC)
  - Tamper (TAMP)
  - STM32CubeMX, the Power consumption calculator

In addition to this training, you can refer to the following presentations:

- Reset and Clock Control
- Real-Time Clock
- Tamper
- STM32CubeMX, focusing on the description of the power consumption calculator.