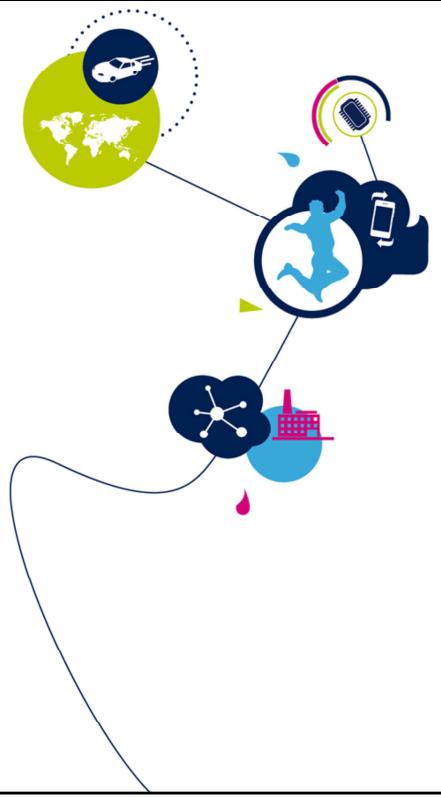


STM32L5 - RCC

Reset and clock controller



Hello, and welcome to this presentation of the STM32L5 reset and clock controller (or RCC).

- The STM32L5 reset and clock controller manages system and peripheral clocks
 - 4 internal oscillators
 - 2 external oscillators (crystal or resonator)
 - 3 PLLs
 - Many peripherals have independent clocks
- The RCC manages the various system and peripheral resets

Application benefits

- High flexibility in choice of clock sources to meet consumption and accuracy requirements
- Many independent peripheral clocks allow for power consumption adjusting without impacting communication baud rates, and to keep some peripherals active in low-power modes
- Safe and flexible reset management



The STM32L5 reset and clock controller manages system and peripheral clocks.

STM32L5 microcontrollers embed 4 internal oscillators, 2 oscillators for an external crystal or resonator, and three phase-locked loops (or PLLs).

Many peripherals have their own clock, independent of the system clock.

The RCC also manages the various resets present in the device.

The STM32L5 RCC provides high flexibility in the choice of clock sources, which allows the system designer to meet both power consumption and accuracy requirements.

The numerous independent peripheral clocks allow a designer to adjust the system power consumption without impacting the communication baud rates, and also to keep some peripherals active in low-power modes.

Finally, the RCC provides safe and flexible reset management.

Reset key features

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Safe and flexible reset management without external components

- Manages three types of reset:
 - System reset
 - Power reset
 - Backup domain reset
- Peripherals have individual reset control bits



Safe and flexible reset management without any need for external components reduces application costs.

The RCC manages three types of resets: the system reset, the power reset and the backup domain reset.

The peripherals have individual reset control bits.

- System reset
 - Resets all registers except the reset flags in the RCC control/status register (RCC_CSR) and the registers in the Backup domain.
 - Reset sources
 - Low level on the NRST pin (external reset)
 - WWDG event
 - IWDG event
 - A software reset (through NVIC)
 - Low-power-mode security reset
 - Option byte loader reset
 - Brown-out reset
 - The Reset Source flag is in the RCC_CSR register



The first type of reset is the System Reset, which resets all the registers except the reset flags in the RCC_CSR register. It also does not reset the Backup domain.

The system reset sources are the external reset (generated by a low level on the NRST pin), a window watchdog event, an independent watchdog event, a software event through the Nested Vectored Interrupt Controller, a low-power-mode security reset (which is generated when Stop, Standby or Shutdown mode is entered but is prohibited by the option byte configuration), an option byte loader reset, and a brown-out reset.

The reset source flag can be found in the RCC Control and Status register.

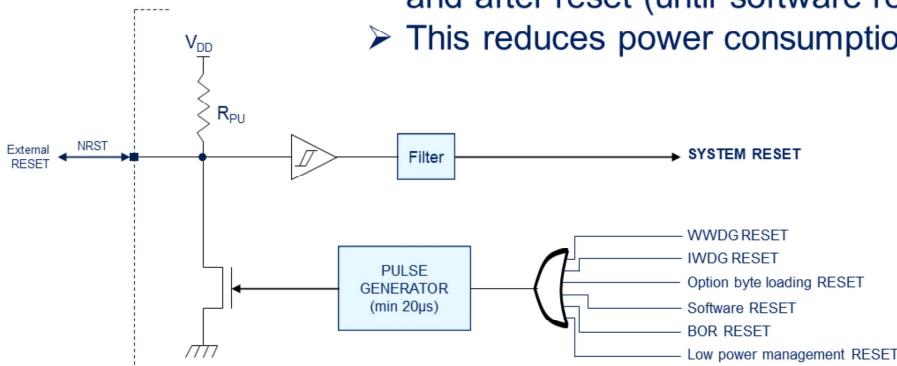
Reset sources

5

No external components are needed due to internal filter and power monitoring

System reset sources can reset external components

- Dedicated reset pin
 - Reset pull-up deactivated during internal reset
 - I/Os in analog mode (no Schmitt trigger) during and after reset (until software reconfiguration).
- This reduces power consumption under reset



Here is the simplified block diagram of the system reset. All internal reset sources provide a reset signal on the NRST pin, which can be used to reset other components of the application board. In addition, no external reset circuitry is needed due to the internal glitch filter and the safe power monitoring feature which guarantees the reset of the application when VDD is below the selected threshold. The internal pull-up on the NRST pin, which maintains a high level when no reset signal is driven low, is deactivated when an internal reset is driven in order to reduce power consumption under reset. Additionally, all I/O pins are placed in analog mode during and after reset to eliminate power consumption through the Schmitt trigger when the I/Os are floating under reset and before software initialization.

- Power reset
 - Sources
 - Brown-out reset (BOR)
 - Resets all registers except those in the Backup domain
 - Exit from Standby
 - Resets all registers in the VCORE domain
 - Registers outside the VCORE domain (RTC, WKUP, IWDG, and Standby/Shutdown mode control) are not impacted.
 - Exit from Shutdown generates a BOR reset
 - Backup domain reset
 - Resets Backup domain RTC registers, Backup registers, SRAM2, LSE oscillator and the RCC BDCR register
 - Sources
 - Software reset triggered by setting the BDRST bit in the RCC BDCR register
 - VDD or VBAT power on, if both supplies have previously been powered off



The second type of reset is the power reset. The Brown-out reset (or BOR), it resets all registers except those in the Backup domain powered by VBAT which contains the RTC and the external low-speed oscillator. When exiting Standby mode, all registers powered by the regulator are reset. When exiting Shutdown mode, a Brown-out reset is generated.

The third type of reset is the Backup domain reset, which resets the RTC registers, the Backup registers, the SRAM2, the LSE oscillator and the RCC Backup Domain Control Register. This reset occurs when the BDRST bit is set in the RCC Backup Domain control register. It also occurs when VDD and VBAT are powered on if both supplies have previously been powered off.

Clock key features

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Choice of clock sources for low-power, accuracy, and performance

- Four internal clock sources
 - High-Speed Internal 16 MHz RC oscillator (HSI16)
 - High-Speed Internal 48 MHz RC oscillator (HSI48)
 - Multi-Speed Internal 100 KHz – 48 MHz oscillator (MSI)
 - Low-Speed Internal 32 KHz RC oscillator (LSI)
- Two external oscillators
 - High-speed external 4 to 48 MHz oscillator (HSE) with clock security system
 - Low-speed external 32.768 KHz oscillator (LSE) with clock security system
- Three PLLs, with three independent outputs



The RCC offers a large choice of clock sources, which can be selected depending on the low-power, accuracy, and performance requirements.

STM32L5 microcontrollers embed four internal clock sources: a high-speed internal 16 Megahertz RC oscillator (HSI16), a high-speed internal 48 Megahertz oscillator (HSI48), a multi-speed internal oscillator (MSI) and a low-speed internal 32 kilohertz RC oscillator (LSI).

STM32L5 devices embed two oscillators for use with an external crystal or resonator: a high-speed external 4 to 48 Megahertz oscillator (HSE) with a clock security system and a low-speed external 32.768 kilohertz oscillator (LSE) also with a clock security system.

When enabled, the clock security system can detect failures on external clock sources and automatically switch to an internal oscillator: HSI16 or MSI in case of HSE

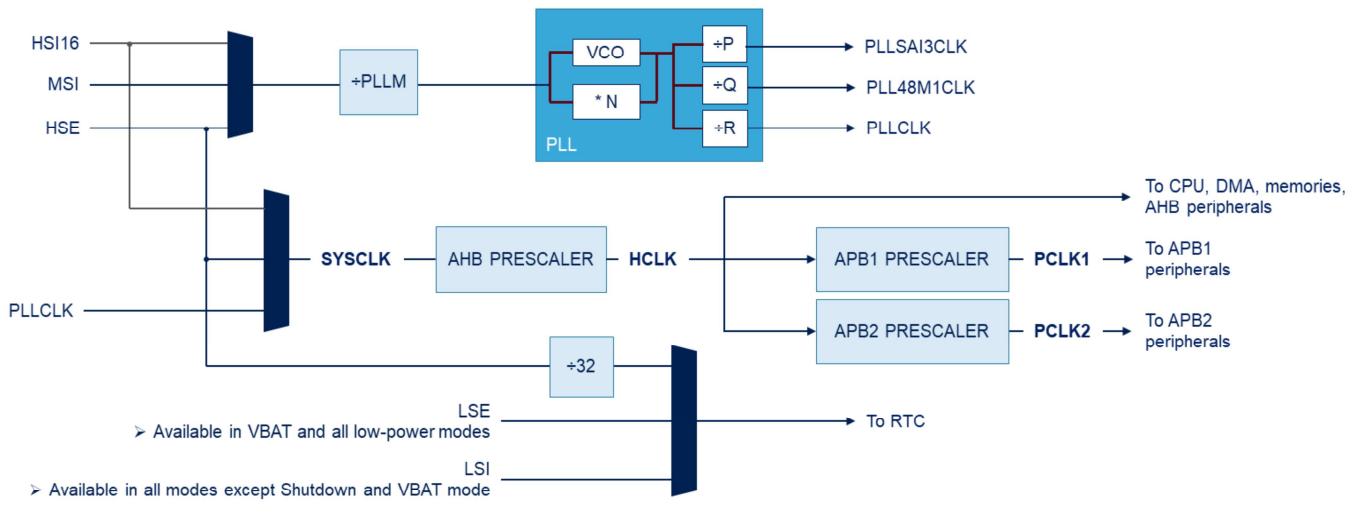
failure and LSI in case of LSE failure.

If a failure is detected on the HSE clock, a clock failure event is sent to the break input of the advanced-control timers, and an non-maskable interrupt is generated to inform the software about the failure.

The PLLs present in the STM32L5 have three independent outputs, in order to offer different frequency options to the CPU and peripherals.

Simplified clock tree (1/2)

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The system clock can be derived from the high-speed internal 16 MHz RC oscillator (HSI16), from the high-speed external 4 to 48 MHz oscillator (HSE), from the multiple-speed oscillator (MSI) or from the PLLCLK output of the PLL.

The AHB clock, called HCLK, is derived by dividing the system clock by a programmable prescaler.

The APB clocks, called PCLK1 and PCLK2, are generated by dividing the AHB clock by programmable prescalers.

The RTC clock is generated by the low-speed external 32.768 kHz oscillator (LSE), the low-speed internal 32 kHz RC oscillator (LSI), or the HSE divided by 32. This selection cannot be modified without resetting the Backup domain.

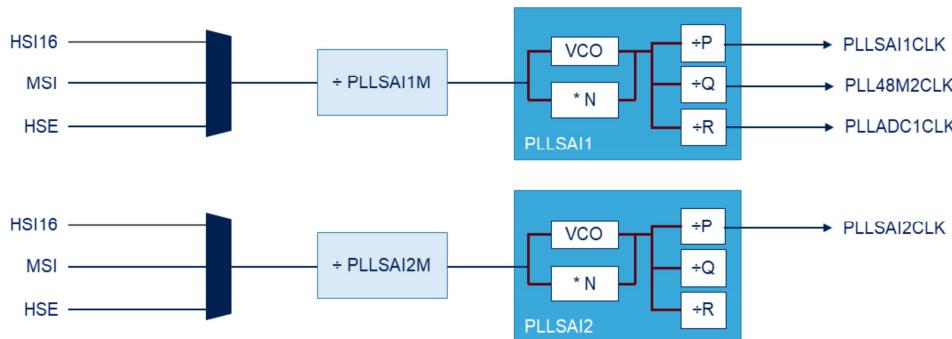
The LSE can remain enabled in all low-power modes and in VBAT mode.

The LSI can remain enabled in all modes except Shutdown and VBAT modes.

Note that the P, Q and R dividers present in the PLL are outside the closed loop and therefore they can be changed without unlocking the PLL.

Simplified clock tree (2/2)

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- The internal PLLs can be used to multiply the HSI16, HSE or MSI output clock frequency
 - The PLLs input frequency must be between 4 and 16 MHz
 - The selected clock source for each PLL is divided by a dedicated programmable factor PLLM, PLLSAI1M, PLLSAI2M, from 1 to 8 to provide a clock frequency in the requested input range



The two additional PLLs called PLLSAI1 and PLLSAI2 have the same input stage: the input clock is either HSI16 or MSI or HSE.

They can be used to multiply the frequency of these reference clocks.

The PLL input frequency must be between 4 and 16 MHz. The value of the divider located after the clock multiplexer has to be chosen accordingly.

The three outputs of PLLSAI1 are available as root clocks for SAI, USB and ADCs.

PLLSAI2 has a unique output called PLLSAI2CLK that can be used as a root clock for SAI.

High-Speed Internal (HSI16) clock

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1% accuracy and fast wakeup time

- HSI16 16 MHz, factory- and user-trimmed
- HSI16 can be selected as
 - Wakeup clock from Stop 0, Stop 1 and Stop 2 modes
 - Backup clock for Clock Security System (CSS)
- Can be automatically started when exiting Stop modes
- I2C, U(S)ART, LPUART can enable the HSI16 during Stop mode to detect their wakeup from Stop sequence
 - HSI16 remains off during Stop mode except for the peripheral wakeup sequence detection



The high-speed internal oscillator is a 16 MHz RC oscillator which provides 1% accuracy and fast wakeup times. The HSI16 is trimmed during production testing, and can also be user-trimmed.

The HSI16 can be selected as the clock at wakeup from Stop 0, Stop 1 or Stop 2 modes, and as a backup clock if an HSE failure is detected by the Clock Security System.

The HSI16 can be automatically awoken when exiting Stop mode in order to make it available for peripherals when it is not used as the system clock.

The HSI16 is requested by the I2C and the U(S)ART/LPUART peripherals to support wakeup from Stop 0, Stop 1 or Stop 2 modes. HSI16 is enabled only for the wakeup sequence detection and remains disabled outside of this wakeup sequence.

High-Speed Internal (HSI48) clock

11

- The HSI48 clock signal is generated from an internal 48 MHz RC oscillator and can be used directly for USB and for random number generator (RNG) as well as SDMMC
- The internal 48 MHz RC oscillator is mainly dedicated to provide a high-precision clock to the USB peripheral by means of a special clock recovery system (CRS) circuitry
 - The CRS can use the USB SOF signal, the LSE or an external signal to automatically and quickly adjust the oscillator frequency on the fly
 - It is disabled as soon as the system enters Stop or Standby mode
 - When the CRS is not used, the HSI48 RC oscillator runs at its default frequency which is subject to manufacturing process variations



The HSI48 is generated from an internal 48-MHz RC oscillator.

48 MHz is a canonical frequency for a USB module.
HSI48 can also be used as the reference clock for the RNG and SDMMC modules.

The HSI48 is associated with a special Clock Recovery System (CRS) circuitry that dynamically adjusts the frequency according to the receipt of USB Start of Frame packet or the LSE or an external signal.

Multiple-Speed Internal (MSI) clock

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- The MSI clock signal is generated from an internal RC oscillator
 - Its frequency range can be adjusted by software
 - Twelve frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz
- The MSI clock is used as system clock after restart from Reset, wakeup from Standby and Shutdown low-power modes
 - After restart from Reset, the MSI frequency is set to its default value of 4 MHz
 - The MSI clock can be selected as the system clock after a wakeup from Stop mode
 - It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails
- In PLL-mode with the LSE, it provides a very accurate clock source that can be used by the USB FS device, and feed the main PLL to run the system at the maximum speed 110 MHz



The MSI is generated from an internal oscillator. Its frequency is programmable, from 100 KHz to 48 MHz. This is default clock source after a reset, and wakeup from standby and shutdown low power modes. The MSI can be selected as the clock at wakeup from Stop 0, Stop 1 or Stop 2 modes, and as a backup clock if an HSE failure is detected by the Clock Security System. In addition, when used in PLL-mode with the LSE, it provides a very accurate clock source, better than $\pm 0.25\%$ accuracy, that can be used by the USB FS device, and feed the main PLL to run the system at the maximum speed 110 MHz.

Low-Speed Internal (LSI) clock

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- The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC
 - The LSI clock accuracy is $\pm 5\%$
- The clock frequency is either 32 kHz or 250 Hz
 - When using the IWDG, only the 32 kHz LSI clock is selected and forced on



The Low Speed Internal (LSI) oscillator is the unique clock of the independent watchdog and can be the clock of the RTC.

It can be kept running in all Stop and Standby modes.

Accuracy of the frequency is plus or minus 5 %.

The clock frequency is either 32 KHz or 250 Hz. When using the independent watchdog, 32-KHz operation is selected and forced on.

High-Speed External (HSE) clock

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Safe crystal system clock

- HSE 4-48MHz
 - External source (Bypass mode) up to 48 MHz
 - External crystal/ceramic resonator (4 - 48 MHz)
- Clock Security System (CSS)
 - Automatic detection of HSE failure with
 - Non-maskable interrupt generation
 - Break input to TIM1/TIM8/TIM15/TIM16/TIM17: critical applications such as motor control can be put in a safe state
 - Backup clock is HSI16 or MSI oscillator
 - Application software does not stop in case of crystal failure.



The high-speed external oscillator provides a safe crystal system clock.

The HSE supports a 4 to 48 MHz external crystal or ceramic resonator, and also an external source in bypass mode.

A clock security system allows an automatic detection of an HSE failure. In this case a Non-Maskable Interrupt is generated, and a break input can be sent to timers in order to put critical applications such as motor control in a safe state. When an HSE failure is detected, the system clock is automatically switched to an internal oscillator: either HSI16 or MSI, so the application software does not stop in case of crystal failure.

Low-Speed External (LSE) clock

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32.768 kHz configurable for low-power or high-drive

Available in all power modes and in VBAT mode

- The LSE can be used with external quartz or resonator, or with external clock source in bypass mode
 - Clock Security System on LSE:** available in all modes except Shutdown and VBAT, operates under reset
- The LSE can be used for RTC, USARTs, LPUART, and LPTIM

Mode	Maximum critical crystal gm ($\mu\text{A/V}$)	Consumption (nA)
Ultra-low power	0.5	250
Medium-low driving	0.75	315
Medium-high driving	1.7	500
High driving	2.7	630



The 32.768 kHz low-speed external oscillator can be used with an external quartz or resonator, or with an external clock source in bypass mode.

It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The oscillator driving capability is programmable. Four modes are available, from ultra-low power mode with a consumption of only 250 nanoamps, to high-driving mode. A clock security system monitors for failure of the LSE oscillator. In case of failure, the application can switch the RTC clock to the LSI. The CSS is functional in all modes except Shutdown and VBAT. The CSS on LSE failure is detected by a tamper event.

It is also functional under reset.

The LSE can be used to clock the RTC, the USARTs or

low-power UART peripherals, and the low-power timer.

System clock

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- Selected between MSI/HSI16/HSE/PLL
- System clock, AHB, APB1, and APB2 maximum frequency: 110 MHz
- Voltage scaling:

Voltage range		MSI	HSI16	HSE	PLL/PLLSAI1/PLLSAI2
Range 0	Main regulator (MR)	48 MHz	16 MHz	48 MHz	110 MHz
Range 1		48 MHz	16 MHz	48 MHz	80 MHz
Range 2		24 MHz range	16 MHz	26 MHz	26 MHz



The system clock is selected between the MSI, HSI16, HSE and PLL output. MSI is chosen by default.

The maximum system clock frequency is 110 MHz.

The APB1 and APB2 bus frequencies are also up to 110 MHz.

The voltage scaling range is adjusted to HCLK frequency as follows:

The system clock is limited to 110 MHz in Range 0 mode, 80 MHz in Range 1 mode, 26 MHz in Range 2 mode.

System Clock Selection

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- Switching from Low to High speed or from High to Low speed system clock, **it is recommended to use a transition state with a medium speed clock for at least 1 μ s**
- Clock source switching conditions:
 - Switching from HSE or HSI or MSI to PLL with AHB frequency (HCLK) higher than 80 MHz
 - Switching from PLL with HCLK higher than 80 MHz to HSE or HSI or MSI
- Transition state to increase the frequency:
 - Set the AHB prescaler HPRE[3:0] bits to divide System frequency by 2
 - Switch system clock to PLL
 - Wait for at least 1 μ s and reconfigure AHB prescaler bits to needed HCLK frequency



In STM32L5 devices, it is recommended to use a transition state when switching from Low to High speed or from High to Low speed system clock.

This slide presents the recommended sequence for the transition state.

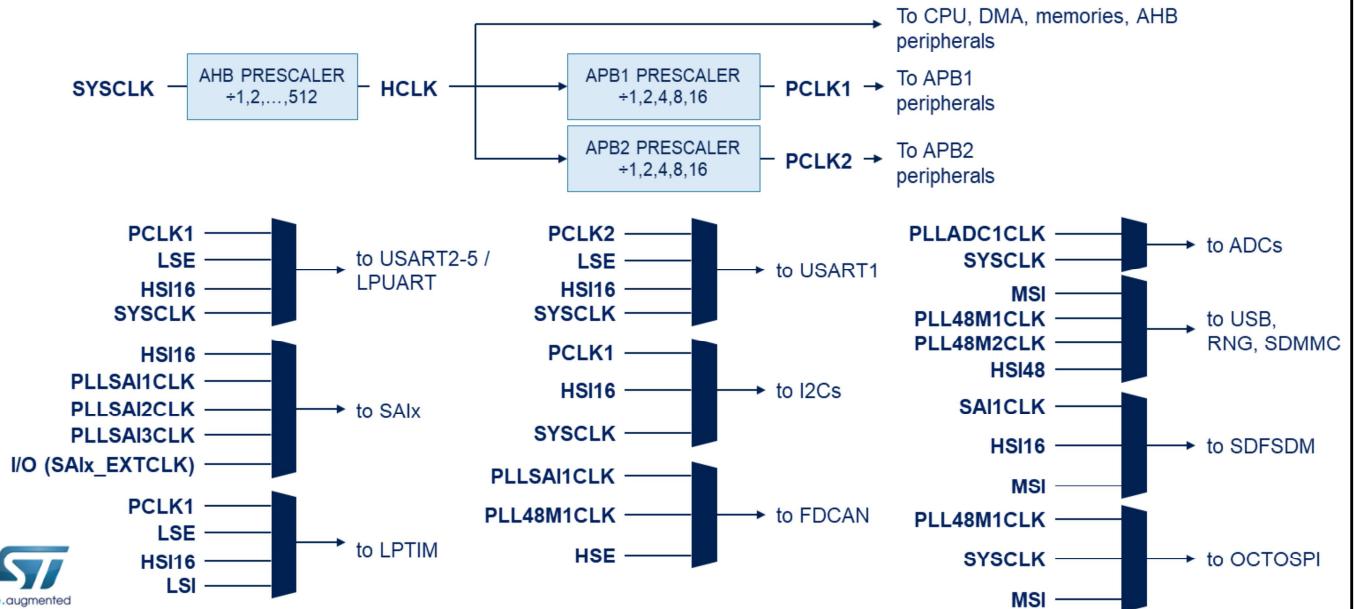
To increase the frequency, the AHB clock frequency has to be divided by two prior to switching the system clock to PLL.

After a one microsecond delay, the prescaler providing the AHB clock can be set to the targeted frequency.

This is needed when switching from HSE or HSI or MSI to PLL and the system frequency becomes higher than 80 MHz.

Clock tree

18



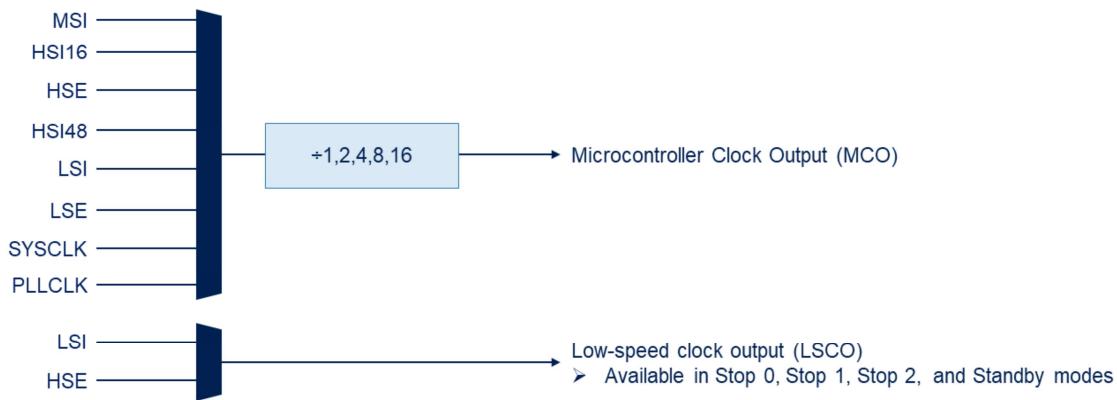
The AHB prescaler divides the system clock to obtain the AHB clock (HCLK).

APB clocks, called PCLK1 and PCLK2 are obtained by applying a programmable prescaler ratio to HCLK.

This slide also describes the multiplexers in charge of selecting the clock of various peripherals.

Clock-out capability

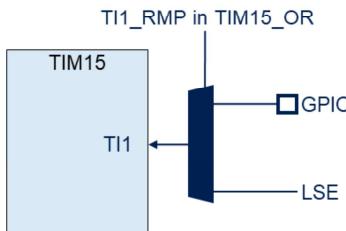
19



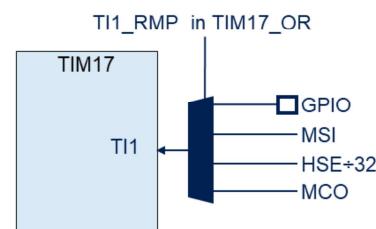
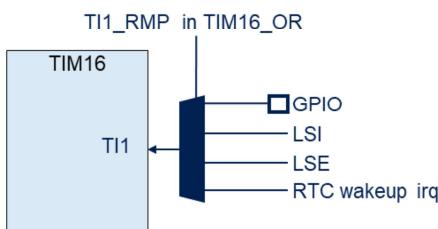
The various clocks can be output on an I/O pad.
The Microcontroller Clock Output feature enables the external output of one of these seven clocks: MSI, HSI16, HSI48, HSE, LSI, LSE, SYSCLK, and PLLCLK.
The low-speed clock output feature enables the external output of the LSI or LSE clock.
The low-speed clock output is available in Stop 0, Stop 1, Stop 2 and Standby modes.

Internal/external clock measurement with Timers

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- Each device is calibrated at the ST factory for 1 % accuracy at an ambient temperature of 25°C



It is possible to indirectly measure the frequency of all on-board clock sources by means of the TIM15, TIM16 or TIM17 channel 1 input capture.

These measurements can be used to calibrate the LSI, MSI and HSI16 frequencies.

Concerning HSI16 and MSI, RC oscillator frequencies can vary from one chip to another due to manufacturing process variations, this is why each device is calibrated at the ST factory for 1 % accuracy at an ambient temperature of 25°C

After reset, the HSI16 and MSI factory calibration value is automatically loaded.

If the application is subject to voltage or temperature variations, software can perform clock trimming.

Dynamic consumption optimization in (LP)Run and (LP)Sleep modes

- Peripheral clock enable registers
 - Peripherals clocks disabled by default (except Flash memory)
 - Registers read and write access not supported when the clock is disabled
- Peripheral clock enable registers in Sleep and Stop modes
 - Enables or disables the peripheral clocks in Sleep, LPSleep, Stop 0/1/2 modes
 - No effect if the corresponding peripheral clock enable bit is cleared
 - Controls both bus and kernel clocks
 - Affects Sleep and Stop modes (for peripheral with independent clock active in Stop mode)
 - Caution: SRAM1 and SRAM2 clocks are enabled by default in Sleep/LPSleep modes



The dynamic power consumption can be optimized by using peripheral clock gating.

Each peripheral clock can be gated ON or OFF in Run and Low-power run mode.

By default, the peripheral's clock is disabled, except the Flash memory clock which is enabled.

When a peripheral's clock is disabled, the peripheral's registers cannot be read or written.

Other registers allow the configuration of the peripheral's clock during the Sleep and Low-power sleep modes.

This also affects Stop 0, Stop 1 and Stop 2 modes for peripherals with an independent clock active in Stop modes.

These control bits have no effect if the corresponding peripheral clock enable bit is cleared.

By default the SRAM1, SRAM2 and CCM SRAM clocks

are enabled in Sleep and Low-power sleep modes.
If they are not needed, the SRAM clock enable bits should
be disabled to reduce power consumption.

RCC register protection

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- The RCC is able to protect register bitfields from being modified by non-secure and unprivileged accesses

RCC_SECCFGR register	Description
RMVFSEC, HSI48SEC, CLK48MSEC, PLLSAI2SEC, PLLSAI1SEC, PLLSEC, PRESCSEC, SYSCLKSEC, LSESEC, LSISEC, MSISEC, HSESEC, HSISEC	This bit can only be set or cleared by a secure software =0: Non secure resource =1: Secure resource
RCC_CR register	Description
PRIV	This bit can only be changed by a privilege software =0: RCC registers can be accessed by a privileged or non-privileged access. =1: RCC registers can be accessed only by a privileged access except RCC_AHBxSECSR, RCC_APBx_SECSR and RCC_SECSR

- When a peripheral is configured as secure, its related clock, reset, clock source selection and clock enable during low-power modes control bits are also secure



Some control and status register bitfields support two levels of protection: security and privilege.

The RCC register bitfields that can be protected against non-secure accesses are the following ones:

6 System Clocks: HSI, HSE(+CSS), MSI, LSI, LSE(+CSS), RC48

4 System configurations: PLLSYS, PLLSAI1, PLLSAI2, Prescalers (AHB/APB1/APB2)

2 System Multiplexor setting: SYSCLK(+MCO), SEL48

1 Reset Flag: RMVF.

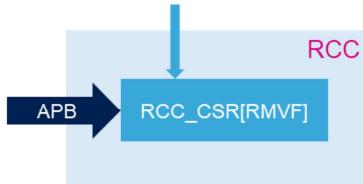
Security violations are reported to the Global TrustZone Controller, GTZC. A maskable interrupt can also be generated.

When a peripheral is configured as secure in the TZSC, the bitfields related to this peripheral in the RCC inherit this secure attribute.

RCC register protection

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RCC_SECCFGR [RMVFSEC] and RCC_CR[PRIV] determine the access permissions of RCC_CSR[RMVF] bitfield



RCC_SECCFGR[RMVFSEC]	RCC_CSR[PRIV]	RCC_CSR[RMVF] bit access permissions			
		NS unpriv	NS priv	S unpriv	S priv
0	0	Y	Y	Y	Y
0	1	N	Y	N	Y
1	0	N	N	Y	Y
1	1	N	N	N	Y



In order to explain the access permissions, let us focus on the Remove reset flag bit, called RMVF present in the RCC_CSR register. By setting this bit to one, all reset status flags are cleared.

The table on the right indicates the access permissions of this particular control bit according to the RMVFSEC attribute and the RCC privilege attribute.

Interrupt event	Description
rcc_it	General interrupt line providing events when the PLLs are ready or when the oscillators are ready <ul style="list-style-type: none">➢ LSI ready, LSE ready, HSI ready, HSE ready, MSI ready, HSI48 ready➢ PLL ready, PLLSAI1 ready, PLLSAI2 ready
rcc_hsecss_it	Interrupt line dedicated to the failure detection of the HSE CSS (clock security system)
rcc_lsecss_it	Interrupt line dedicated to the failure detection of the LSE CSS



This slide lists the RCC interrupts.

The LSE and HSE clock security systems can generate an interrupt request.

rcc_it typically reports PLL ready, and oscillator ready events.

Related peripherals

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- Refer to these trainings linked to this peripheral, if any
 - STM32L5 Power control (PWR)
 - STM32L5 Interrupts (NVIC-EXTI)
 - STM32L5 Global TrustZone® controller (GTZC)



In addition to this training, you may find the Power Control, Interrupt Controller and Global TrustZone controller trainings useful.

References 26

- For more details, please refer to following sources
 - STM32L5xx reference manual RM0438
 - AN2867 Oscillator design guide for STM8S, STM8A and STM32 microcontrollers



For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers.