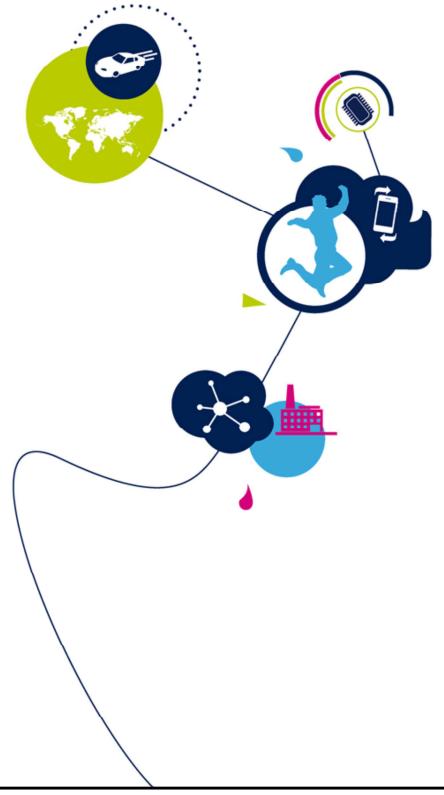
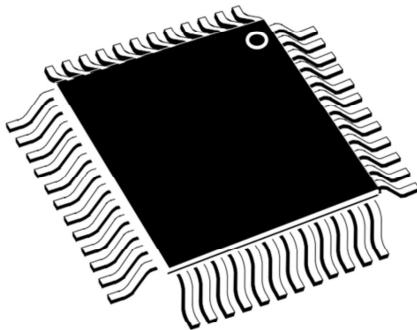


STM32L5 - GPIO

General-purpose input/output interface
Revision 1.0



Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the microcontroller.



- Provides interface for interaction with external environment
 - Fully configurable
 - With interrupt and wake-up capability

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB2 allows fast toggle/sampling response

The general-purpose I/O pins of STM32 microcontrollers provide an interface with the external environment. This configurable interface is used by the MCU and also all other embedded peripherals to interface with both digital and analog signals.

Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key features

3

- Bi-directional operation of up to $8 \times 16 = 128$ I/O pins ⁽¹⁾
 - Shared across up to 8 GPIO ports
 - GPIOA to GPIOH, 16 I/O pins per port
 - All pins support external interrupt and wake-up capabilities
 - Atomic bit set and bit reset using BSRR and BRR registers
 - Independent configuration for each I/O pin
 - I/O pin in Analog mode after reset and alternate functions are not active
- GPIOx directly connected to AHB2 bus
- Most I/O pins are 5 V tolerant

⁽¹⁾ : depends on part numbers and packages



General-purpose I/Os provide bidirectional operation – input and output – with an independent configuration for each I/O pin. They are shared across up to 8 ports named GPIOA to GPIOH. Each of them hosts up to 16 I/O pins, I/O ports support atomic bit set and reset operations through BSRR and BRR registers.

I/O ports are directly connected to the AHB2 bus, in order to allow fast I/O pin operations capable of changing every two clock cycles.

Most of the I/O pins are 5 V tolerant.

Operating modes

4

Flexible operating modes to best fit application needs

- Input mode
 - Floating (no pull resistor), input with pull-up/down, analog input with optional pull-down
- Output mode
 - Push-pull, open drain with optional pull-up/down
- Configurable output slew rate speed up to 100 MHz
- Alternate function mode (AF mode)
- Locking mechanism to freeze the I/O port configuration (GPIOx_LCKR)



General-purpose I/O pins can be configured into several operating modes.

An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input with optional pull down.

An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.

For each I/O pin, the slew rate speed can be selected from 4 different ranges to ensure the best compromise between maximum speed and emissions from the I/O switching and to adjust the application's EMI performance.

I/O pins are also used by other integrated peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.

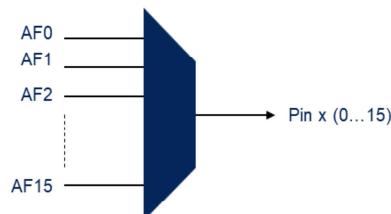
The configuration of the I/O ports can be locked to increase application robustness. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin's configuration cannot be modified until the next reset.

Alternate functions

5

Structure of I/O pins is used as interface by other embedded peripherals

- Several integrated peripherals share the same I/O pins
 - For instance USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, ...
- Alternate function multiplexer selects the peripheral connected to the I/O pin
 - Only one alternate function is connected to a specific I/O pin at a single time
 - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers (x = A...H)



Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.

Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time. Of course, this selection can be changed while the application is running through the GPIOx_AFRL and AFRH registers.

IO pin configuration

6

I/O configuration				
MODE(i)[1:0]	OTYPE(i)	PUPD(i)[1:0]		
0b01	0	0b00	General Purpose output	Push-Pull
	0	0b01		Push-Pull + Pull-Up
	0	0b10		Push-Pull + Pull-Down
	0	0b11	Reserved	
	1	0b00	General Purpose output	Open-Drain
	1	0b01		Open-Drain + Pull-Up
	1	0b10		Open-Drain + Pull-Down
	1	0b11	Reserved (GP output Open-Drain)	
0b10	0	0b00	Alternate Function	Push-Pull
	0	0b01		Push-Pull + Pull-Up
	0	0b10		Push-Pull + Pull-Down
	0	0b11	Reserved	
	1	0b00	Alternate Function	Open-Drain
	1	0b01		Open-Drain + Pull-Up
	1	0b10		Open-Drain + Pull-Down
	1	0b11	Reserved	
0b00	x	0b00	Input	Floating
	x	0b01		Pull-Up
	x	0b10		Pull-Down
	x	0b11	Reserved (input floating)	
	x	0b00	Input/output	Analog
	x	0b01		
	x	0b10	Reserved	
	x	0b11		



The configuration of any IO pin is achieved through 4 32-bit registers: GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR.

- Register GPIOx_MODER selects the functionality of the IO pin: digital input, digital output, alternate function or analog.
- Register GPIOx_OTYPER is relevant when the pin is an output: it selects open drain vs push-pull operation.
- Register GPIOx_OSPEEDR selects the speed of the signal received or transmitted by the pin.
- Register GPIOx_PUPDR enables /disables pull-up or pull-down resistors whatever the I/O direction.

Special considerations for I/O pins

7

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
 - I/O ports default to analog mode
 - Saves current consumption during and after reset (Schmitt trigger is off)
- Only JTAG/SWD (Serial Wire Debug) pins remain in Alternate Function pull-up/pull-down configuration
 - PA13: JTMS/SWDIO
 - PA14: JTCK/SWCLK
 - PA15: JTDI
 - PB3: JTDO
 - PB4: NJTRST



During and after reset, the alternate functions are not active, only debug pins can be used in Alternate Function mode.

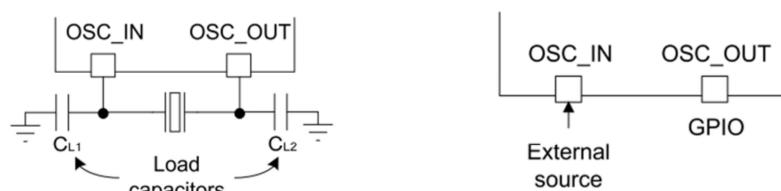
JTAG/Serial Wire Debug (SWD) pins remaining in alternate function configuration mode are listed in this slide.

Special considerations for HSE/LSE pins

8

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
 - Valid for both HSE / LSE. This state is the default one after reset.
- When the HSE or LSE oscillator is switched ON, the oscillator takes control of its associated pins and the GPIO configuration of these pins has no effect.
- When user external clock mode is used, the second pin behaves as an I/O pin
 - Only OSC_IN (HSE) or OSC32_IN (32 KHz LSE) is used as clock source
 - OSC_OUT and OSC32_OUT are standard I/O pins



When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after a device reset.

When an external clock source is used instead of a crystal oscillator, only the related OSC_IN or OSC32_IN pin is used for the clock and the OSC_OUT or OSC_32 pin can be used as a standard I/O pin.

Special considerations for I/O pins

9

+ one I/O if boot0 is based on option bit

- PH3 pin can be used either as BOOT0 pin or as standard GPIO
 - It depends on the nSWBOOT0 option bit
 - nSWBOOT0 = 0: Boot0 taken from the option bit nBOOT0, so PH3 is available as GPIO
 - nSWBOOT0 = 1: Boot0 taken from PH3/BOOT0 pin.
 - PH3/BOOT0 GPIO is configured in:
 - Input mode during the complete reset phase if the option bit nSWBOOT0 is set. It then switches automatically in analog mode after reset is released (BOOT0 pin).
 - Input mode from the reset phase to the completion of the option byte loading if the bit nSWBOOT0 is cleared (BOOT0 value coming from the option bit). It switches then automatically to the analog mode just after the reset.



PH3 may be used either as a boot pin (BOOT0) or as a GPIO.

Depending on the nSWBOOT0 bit in the user option byte, it switches from the input mode to the analog input mode:

- After the option byte loading phase if nSWBOOT0 = 1,
- After reset if nSWBOOT0 = 0.

So PH3 pin is not a dedicated pin. It can be used during reset time to select the boot mode and can become a general purpose I/O during the run-time.

TrustZone Security

10

- Each I/O pin of GPIO port can be individually configured as secure through the GPIOx_SECCFGR register when the TrustZone security is active
- TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register (TZEN = 1)
- When TZEN=1
 - The configuration bits of a secure I/O are secure against any non-secure access
 - Secure I/O data can not be redirected to a non-secure I/O
 - Non-secure I/O data can not be redirected to a secure peripheral
 - If an I/O is secure, it can be accessed by non-secure and secure digital peripheral and only by secure analog peripheral.
 - If an I/O is non-secure, it can only be accessed by a non-secure digital peripheral and by a non-secure analog peripheral.



After reset, all GPIO ports are secure

Each I/O pin of GPIO port can be individually configured as secure when the TrustZone security is active

TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register.

When the TrustZone security is active:

- The configuration bits of a secure I/O are secure against any non-secure access
- Secure I/O data can not be redirected to a non-secure I/O
- Non-secure I/O data can not be redirected to a secure peripheral
- If an I/O is secure, it can be accessed by non-secure and secure digital peripheral and only by secure analog peripheral.
- If an I/O is non-secure, it can only be accessed by a non-secure digital peripheral and by a non-secure

analog peripheral.

After reset, all GPIO ports are secure.

Low-power modes

11

Mode	I/O Description
Run	Active
Sleep	
Low-power run	
Low-power sleep	
Stop 0/1/2	
Standby	I/Os can be configured with internal pull-up, pull-down or floating in Standby mode
Shutdown	I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode
Reset	Forced to analog input mode when the MCU is under reset



I/O pins remain active in all modes except Standby and Shutdown, where the only available configuration is input with internal pull-up, pull-down resistor or floating input. When exiting Shutdown mode, the I/O configuration is lost. When the MCU is under reset, I/O pins are forced into an analog input mode.