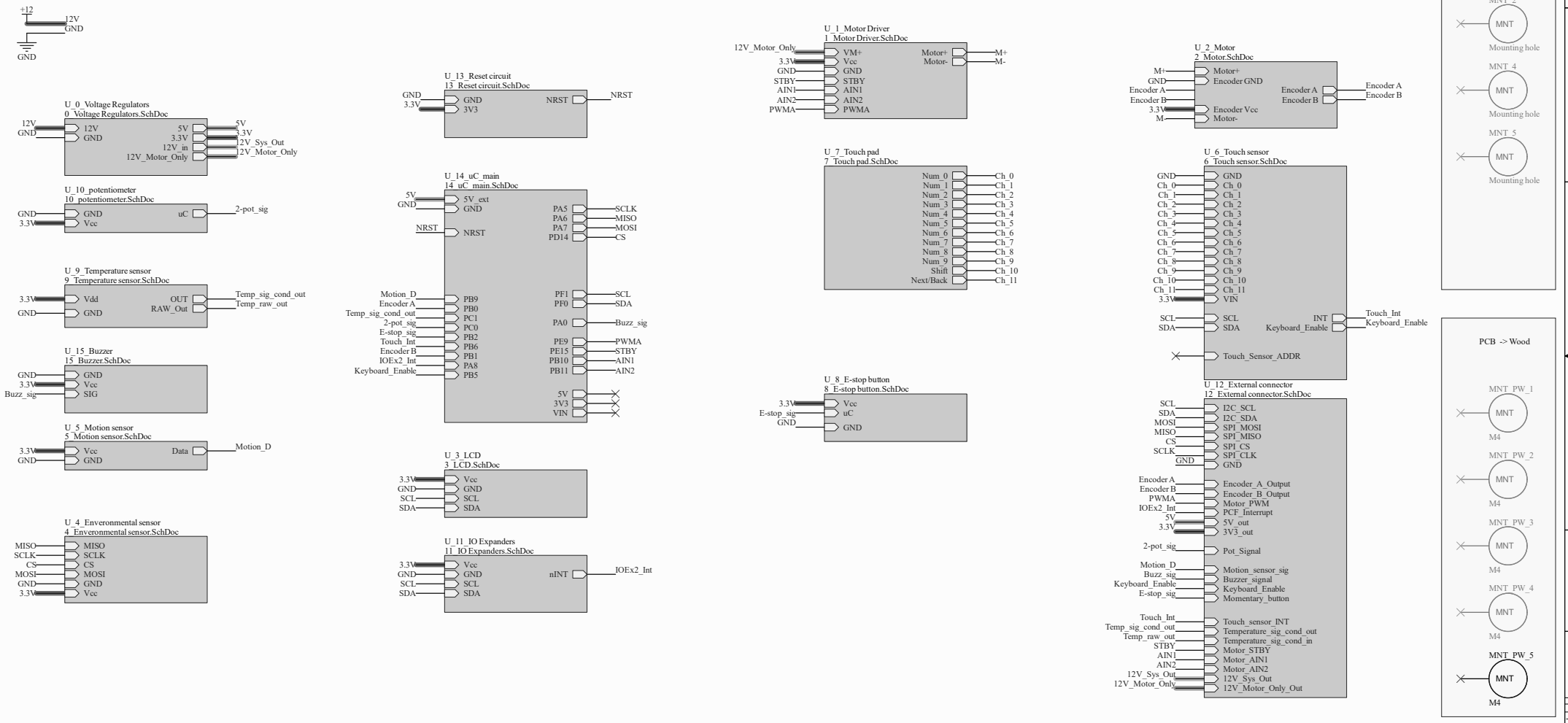
DWG. NO. | REV. | SHT. 1

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: D! - Puranjan Gaur	--/--/--
DSN: D! - Puranjan Gaur	--/--/--
CHK: Pierre Adam & Miodrag Bolic	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: CEG 3136

uOttawa

TITLE: Embedded systems lab

SIZE: B | DWG NO.

SCALE: | FILE NAME: 00_Block diagram.SchDoc | SHEET 1 OF 17