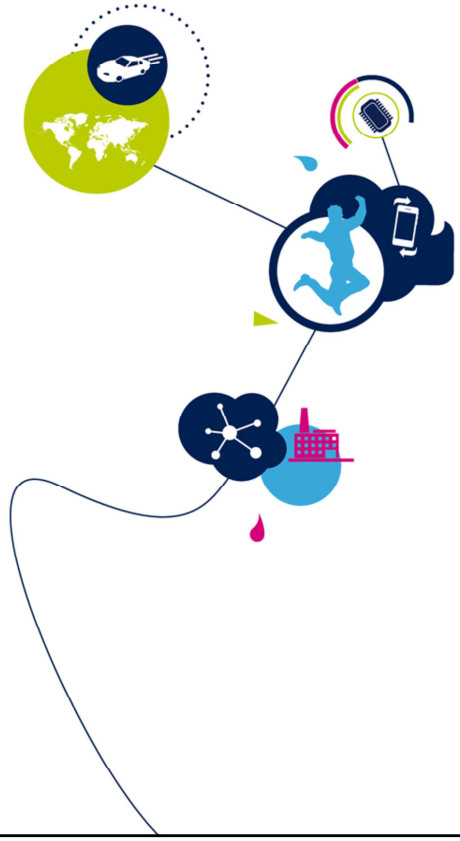
STM32L5 - CRS

Clock Recovery System (CRS)
Revision 1.0



life.augmented

Welcome to this presentation of the STM32L5 clock recovery system. It covers the main features of this module used to control the precision of the USB clock frequency.

Overview

- CRS purpose
  - The goal is to get a precise-enough clock signal for USB communication without the need for an external resonator component.
  - The USB traffic is used as timing reference and more precisely the Start Of Frame (SOF) generated every 1 ms.
- CRS functions
  - Trimming of the HSI 48-MHz clock on the fly
  - Fine granularity to meet USB device requirements with HSI only
  - Flexible warning and error control
    - Interrupts or events can be generated to take corrective actions

Application benefits

- Possible to have crystal-less USB device applications
- Simpler BOM, application firmware and PCB layout.

life.augmented

The goal of the Clock Recovery System is to obtain a precise-enough clock signal for use by the USB module without the need for an external resonator component, just by simply using the USB traffic as a timing reference.
The peripheral's main functions are its ability to trim the internal oscillator on the fly, to benefit from its fine granularity in order to meet the USB protocol requirements and have enough information available for the user to track in early phases any potential issues.

Key features

- Selectable synchronization source with programmable prescaler and polarity:
  - External pin, LSE oscillator output or USB SOF packet reception
- Possibility to generate synchronization pulses by software
- Automatic oscillator trimming capability with no need for CPU action
- Manual control option for faster start-up convergence
- 16-bit frequency error counter with automatic error value capture and reload
- Programmable limit for automatic frequency error value evaluation and status reporting
- Maskable interrupts/events:
  - Expected synchronization (ESYNC), Synchronization OK (SYNCOK), Synchronization warning (SYNCWARN) and Synchronization or trimming error (ERR)

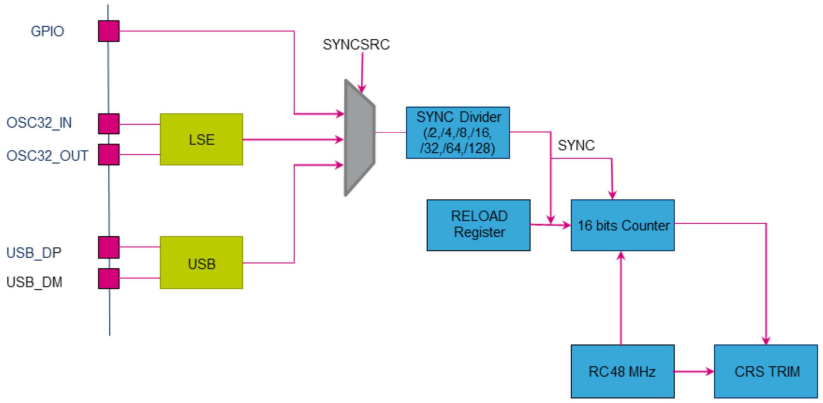
life.augmented

The Key features are:
A selectable synchronization source with programmable prescaler and polarity: External pin, LSE oscillator output or USB SOF packet reception,
The possibility to generate synchronization pulses by software,
An automatic oscillator trimming capability with no need for CPU action,
A manual control option for faster start-up convergence,
A 16-bit frequency error counter with automatic error value capture and reload,
A programmable limit for automatic frequency error value evaluation and status reporting,
Maskable interrupts/events: Expected synchronization (ESYNC), Synchronization OK (SYNCOK), Synchronization warning (SYNCWARN) or Synchronization or trimming error (ERR).

CRS block diagram

- The reference signal for the HSI 48-MHz clock can be selected from different sources.
- This reference (SYNC) is used to reload the 16-bit counter and capture the previous countdown value. Depending on the value, the HSI 48-MHz clock is fine-tuned to reach the most accurate frequency possible.

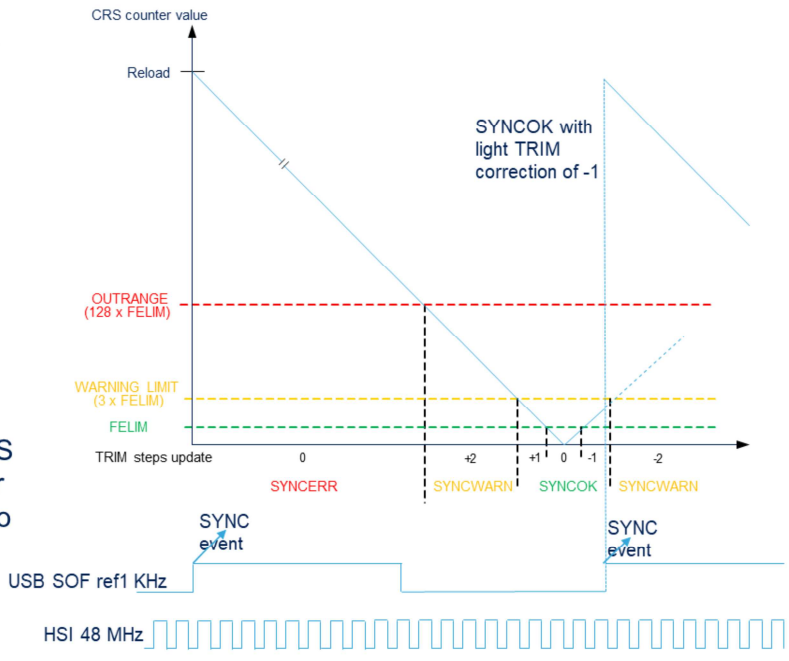
- 4 possible inputs:
  - An external signal on a GPIO
  - The 32-kHz crystal oscillator
  - The USB Start of Frame signal



4 different sources can be selected for the Clock Recovery System:
• an external signal on a GPIO,
• the 32-kHz crystal, or
• the USB start of frame signal can be used as a clock source to create a reference signal to calibrate the HSI 48MHz oscillator.
This reference signal (called SYNC) is used to reload the 16-bit counter and capture the value of the actual countdown. Depending on this value, the HSI 48-MHz clock frequency (HSI48) is fine-tuned to reach the most accurate frequency.

CRS behavior on the USB Start of Frame

- CRS counter value is reloaded with the RELOAD value on each SYNC event. It starts counting down till it reaches zero and starts counting up to the OUTRANGE limit where it eventually stops (if no SYNC event is received) and generates a SYNCMISS event.
- When a SYNC event is received, the CRS generates an error if the counter is above OUTRANGE limit, a warning if the counter is above the warning limit or the SYNCOK if below the Frequency Error Limit (FELIM)
- FELIM is the Frequency Error Limit. If the CRS counter value is above this threshold, the user trim bit field called TRIM, is updated in order to fine-tune the HSI 48-MHz clock frequency.



The CRS counter value is reloaded with the RELOAD value on each SYNC event. It starts counting down till it reaches zero.
Then it starts counting up to the OUTRANGE limit where it eventually stops (if no SYNC event is received before) and generates a SYNCMISS event.
A SYNC event received when the counter is below the outrange will eventually fine TRIM the HSI48, depending on the FELIM[7:0] value.
If the CRS counter value is below the FELIM limit, no TRIM actions are taken.
If it is between 3 times FELIM and FELIM, the TRIM bit field is incremented or decremented by 1, depending on the counter direction.
If the CRS counter is between 128 times FELIM and 3 times FELIM, the TRIM bit field is incremented or decremented by 2 TRIM steps.

Interrupts & Low Power modes

- Interrupt events for each channel

Interrupt event	Description
Expected synchronization	Set when the counter reach zero and start counting up
Synchronization OK	Set when the SYNC event has been received within the expected time window
Synchronization warning	Set when the SYNC event has been receive in margin of the OK window but not yet in the error range.
Synchronization or trimming error	**(TRIMOVF, SYNCMISS, SYNCERR)** Set when the SYNC event has been received too early, not received at all, or in case the TRIM bit field overflow after update.

- The CRS works in Run and Sleep modes. In other modes, the HSI48 is stopped.

life.augmented

The following interrupts can be activated by the Clock Recovery System :
The Expected synchronization is set when the counter reaches zero and starts counting up.
The Synchronization OK is set when the SYNC event has been received within the expected time window.
The Synchronization warning is set when the SYNC event has been received within the margins of the OK window but not yet in the error range.
The Synchronization or trimming error (TRIMOVF, SYNCMISS, SYNCERR) is set when the SYNC event has been received too early, not received at all, or if the TRIM bit field overflows after an update.

Related peripherals

- Refer to these trainings linked to this peripheral for more information:
  - Universal serial bus full-speed device interface (USB)
  - Reset and clock control (RCC)

life.augmented

You can refer to peripheral training slides related to the USB and RCC modules for additional information.