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FACULTY OF INTERNATIONAL EDUCATION

HCMUTE

REPORT ON VLSI Integrated Circuit Design

Topic: DESIGN OF 6T, 4T, 8T AND LOW POWER SRAM

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I. ABSTRACT

This research investigates the performance characteristics of SRAM (Static Random Access Memory) cells with varying transistor configurations, specifically 4T, 6T, and 8T designs, alongside an exploration of Low-Power SRAM architectures. The study focuses on evaluating power consumption and delay metrics to understand the trade-offs associated with different SRAM configurations. The SRAM cells are analyzed for their potential in memory applications, considering the increasing demand for energy-efficient and high-performance memory solutions. The investigation involves a comprehensive assessment of power efficiency and delay characteristics in order to provide valuable insights into the comparative advantages and limitations of 4T, 6T, and 8T SRAM designs, as well as low-power SRAM alternatives. The findings from this research contribute to the ongoing efforts to optimize memory architectures for diverse applications in modern integrated circuits.

We conducted simulations using Cadence software for the 90nm technology node and demonstrated a power saving of approximately 37%.

II. INTRODUCTION

A complete industrial 90-nm process was first introduced by Intel in 2003 [Ghani]. With transistor channels around 50 nm in size (50 billionths of a meter), comparable to the smallest micro- organisms, this technology is truly a nanotechnology.

Strained Silicon

The main novelty related to the 90 nm technology is the introduction of strained silicon to speed-up the carrier mobility, which boosts both the n-channel and p-channel transistor performances. It has been known for decades that stretching the silicon lattice improves the carrier mobility, and consequently the device current.

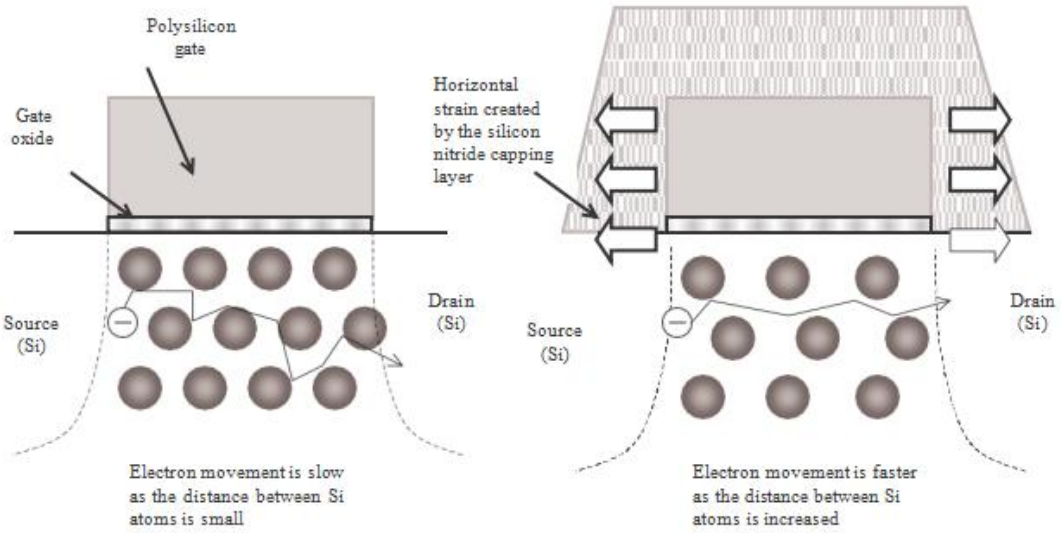

Figure 1: Strain generated by a silicon-nitride capping layer which increases the distance between atoms underneath the gate, which speeds up the electron mobility of n-channel MOS devices

SRAM

Figure 2: Static Random Access Memory (SRAM)

Static random-access memory (static RAM or SRAM) is a type of random-access memory (RAM) that uses latching circuitry (flip-flop) to store each bit. SRAM is volatile memory; data is lost when power is removed.

The term static differentiates SRAM from DRAM (dynamic random-access memory):

- SRAM will hold its data permanently in the presence of power, while data in DRAM decays in seconds and thus must be periodically refreshed.
- SRAM is faster than DRAM but it is more expensive in terms of silicon area and cost.
- SRAM is typically used for the cache and internal registers of a CPU while DRAM is used for a computer's main memory.

Uses of SRAM Memory

SRAM memory can be used in many different places, and this part will tell you the uses of SRAM memory.

Contemporary SRAM Devices

You can find SRAM on general purpose products and chips.

General Purpose Products

- With an asynchronous interface.
- With a synchronous interface.

Integrated on Chip

- As RAM or cache in microcontrollers (usually from 32 bytes to 128 KB).
- As the main cache in powerful microprocessors (from 8 KB to several megabytes).
- To store registers and parts of the state-machines used in some microprocessors (see register file).

- On a dedicated IC or ASIC (usually in the order of kilobytes).
- In Field Programmable Gate Array and Complex Programmable Logic Device.

Embedded Use

You can find static RAM in many categories of industrial and scientific subsystems, automotive electronics and similar products. Almost all modern devices, toys and so on that implement electronic user interfaces also embed a certain amount of data (kilobytes or less). Gigabytes can be used for complex products such as digital cameras, mobile phones, synthesizers, etc.

Dual-port SRAM is sometimes used in real-time digital signal processing circuits.

In Computers

SRAM is also used in personal computers, workstations, routers, and peripherals: CPU register files, internal CPU caches, and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also typically hold the image displayed (or to be printed) by using static RAM. Some early personal computers (such as ZX80, TRS-80 Model

Hobbyists

Due to the ease of interfacing, hobbyists, especially home-built processor enthusiasts, usually prefer SRAM. Compared to DRAM, it is easier to use because there are no refresh cycles and the address and data buses are directly accessible. In addition to buses and power connections, SRAM typically requires only three controls: Chip Enable (CE), Write Enable (WE) and Output Enable (OE). In synchronous SRAM, Clock (CLK) is also included.

Types of SRAM Memory

+ Non-Volatile SRAM (NV-SRAM)

Non-volatile SRAM (nvSRAM) possesses standard SRAM functionality, but saves data when power is off, thereby ensuring the preservation of critical information. nvSRAM is widely used in many occasions such as networking, aerospace and medical, where the preservation of data is very important and where the battery is impractical.

+ Pseudo SRAM (P-SRAM)

PSRAM features a DRAM memory core and incorporates a self-refresh circuit. They appear externally as a slower SRAM. Compared to true SRAM, they have density/cost advantages without the access complexity of DRAM.

States of SRAM

SRAM cells have three different states: standby (the circuit is in idle state), read (data requested) or write (update content). SRAM operating in read mode and write mode should have “readability” and “write stability”, respectively.

III. SPECIFICATION

In the process of optimizing the performance of SRAM, the careful selection of threshold voltage and frequency plays a pivotal role in ensuring stability and efficiency in static random-access memory. However, to ensure that our designs operate flexibly in various environmental conditions, we also integrate technical specifications related to temperature into the design process.

We carefully choose the threshold voltage to achieve stability in the operation of SRAM. This includes optimizing the threshold voltage not only to control standby current but also to maintain the stability of the cell under various operating conditions.

Moreover, the operating frequency not only influences the data access speed and latency of SRAM but is also closely related to the threshold voltage. To ensure synchronization between performance and energy consumption, we pay special attention to this interaction. Thus, we not only ensure stable performance under specific threshold voltage and frequency settings but also consider the impact of temperature to ensure the reliability and flexibility of SRAM in various environmental conditions.

Below are the detailed specifications of the various SRAM designs in our project.

Table 1: Controllable Parameter of SRAM

Parameters	Values
Supply Voltage	1V
Frequency	0.1Ghz-10Ghz
Temperature	27 Degree(s) Celsius

The tools for the design, implementation and testing is:

Table 2: Tools for the design

Tool/Simulator	Cadence
Technology	CMOS 90nm

IV. DESIGN

4.1. I/O

4.1.1. Pre-charge

A precharge system of the divided bit line types for a SRAM (Static Random Access Memory) reduces the active current consumption and bit line peak current by decreasing the number of bit lines to be precharged at any one time during a precharge cycle.

Circuit pre-charge helps align the voltage levels of two bit lines before latching the address. The structure of the Precharge circuit is depicted in the diagram below:

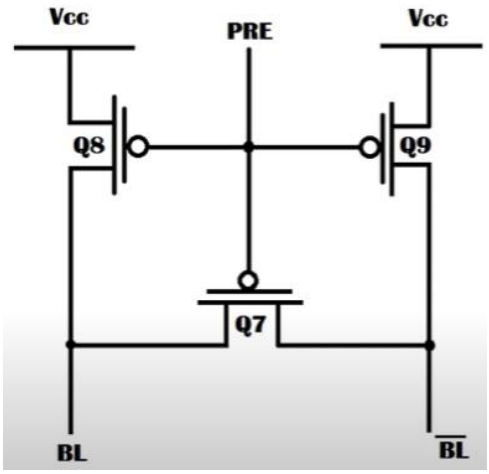

Figure 3: Precharge Architecture

The simplest pre-charge circuit consists of 3 transistors:

- Q8 is connected to the Bit-line along with Vcc.
- Q9 is connected to the Bit-line-bar along with Vcc.
- Q7 is used for voltage balancing.

→ In summary, Q8 and Q9 are used for charging, and Q7 is used for voltage balancing. All three transistors, Q7, Q8, and Q9, function as a switch

For the Pre-charge circuit to operate, the Pre signal should receive a logic 0 for the P-MOS. Vcc will be connected to both BL and BLB, and the voltage between these two bit lines will be balanced through Q7.

The operating principle Precharge Circuit:

When PRE is active, Q8 and Q9 are responsible for charging the bit lines, while Q7 balances the voltage.

If either voltage on Q8 or Q9 is different, that voltage will flow through Q7. Q7 will discharge the side with higher voltage and charge the side with lower voltage. This process continues until both sides balance in voltage.

The duration of this process is called the Pre-charge time. When this process is finished, it will be performed during the memory access process.

The pre-charge circuit helps improve SRAM memory access speed by preparing the memory cell with a stable voltage level before reading or writing, thereby increasing access performance.

Waveform of Precharge Circuit:

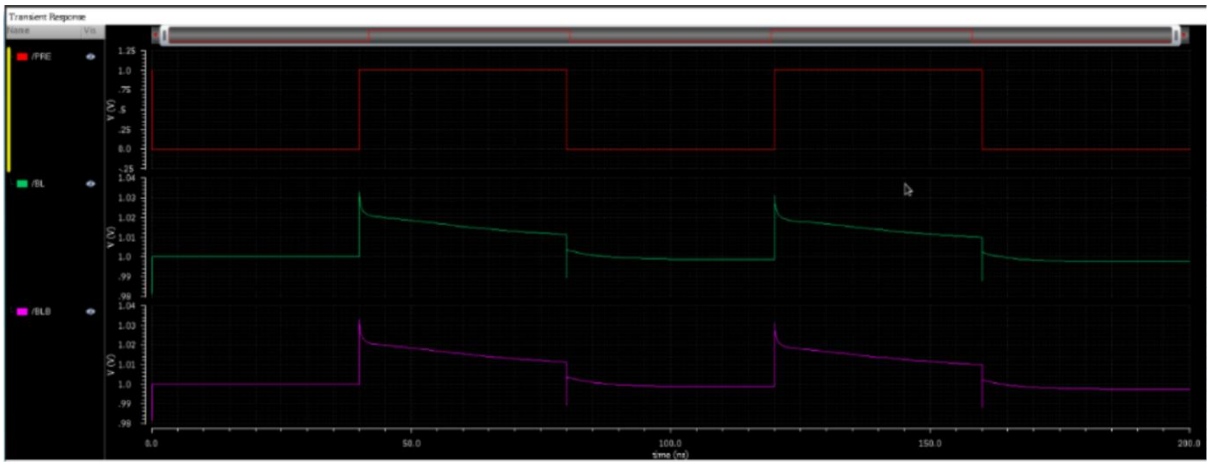

Figure 4: Waveform of Precharge circuit

We simulate the waveform of the Precharge circuit with a voltage level of 1V and a frequency of 1GHz.

We observe a state referred to as "Floating". The "floating" state in a precharge circuit often occurs when the output of the circuit is not held at a specific value but is instead "loose" to accept a new value. The floating state is commonly implemented in logic circuits to optimize speed and energy consumption.

The precharge gate no longer holds the output high; instead, it is "loose" to accept a new value from registers or other logic elements. During this phase, the output may change depending on the circuit conditions and the newly input data.

The "floating" state ensures that the circuit can quickly accept a new value and smoothly transition between different states.

4.1.2. Write driver

The Write driver circuit is to provide sufficient energy to perform the write operation in the SRAM cell. When a write request is activated, the Write Driver circuit enhances the dynamic energy on the data lines to ensure that the new value can be written to the cell accurately and completely.

This process consists of two main stages:

+ Precharge: Before performing a write, the Write Driver circuit typically needs to precharge, setting the voltage to a certain level (which can be either high or low) to prepare for energy transfer when the write is activated.

+ Drive: When a write request is present, the Write Driver circuit will stimulate and provide sufficient energy to change the state of the SRAM cell, transitioning from holding the old value to the newly requested value.

The structure of the Write driver is depicted in the diagram below:

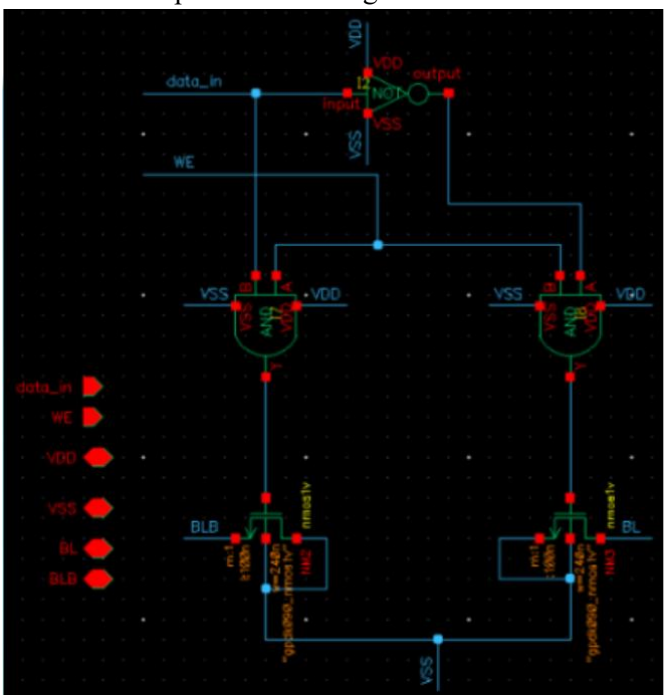

Figure 5: Schematic of Write driver

The operating principle of the Write Driver circuit

1. When the data_in signal is X (don't care), and the Write Enable signal (WE) is 0, both outputs of the AND gate will be 0. The N-MOS will not operate at this time and will take the value from the Bitline (BL) and Bitline Bar (BLB).

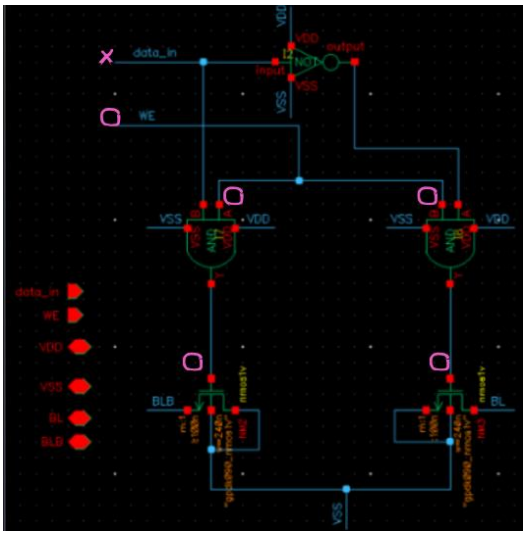

Figure 6: Write enable has the value of 0

2. When the data_in signal is 0 and the Write Enable signal is 1, the output of the first AND gate (on the left) will be at a logic level 0, causing the N-MOS connected to the first AND gate to turn off. Meanwhile, the output of the second AND gate (on the right) will be at

a logic level 1, turning on the corresponding N-MOS. When the N-MOS is ON, BL will have a value of 0 and will be transmitted to the SRAM cell. The SRAM will then produce the corresponding output value on BLB.

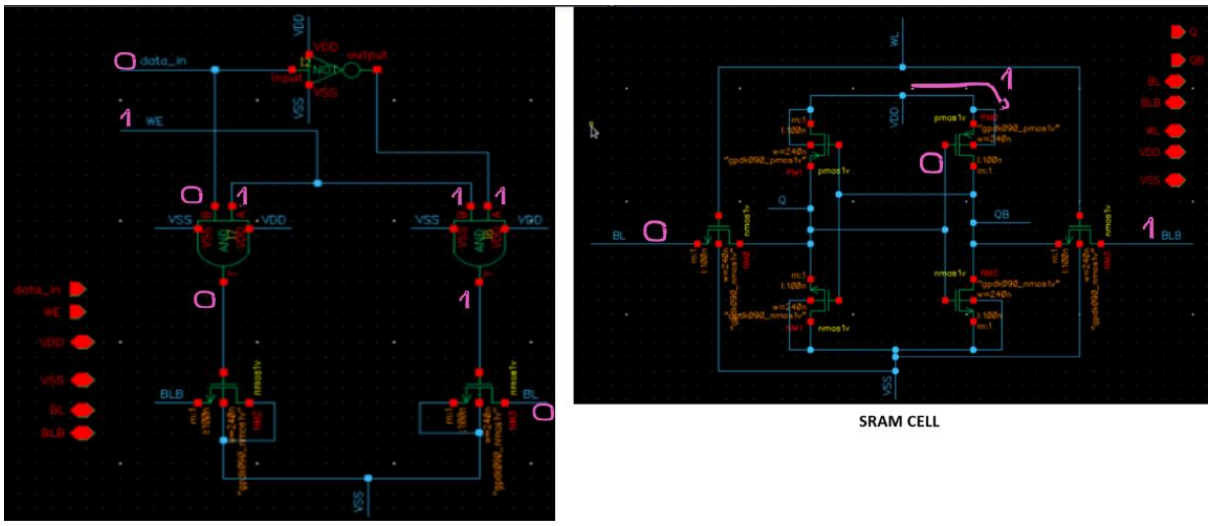

Figure 7+8: Write enable has the value of 1, data = 0

3. When the data_in signal is 1, and the Write Enable signal is also 1, the output of the first AND gate (on the left) is 1, and the output of the second AND gate (on the right) is 0. At this point, the N-MOS connected to the first AND gate (on the left) is ON, and the N-MOS connected to the second AND gate (on the right) is OFF. Now, BLB will have a value of 0 and will be transmitted to the SRAM cell. The SRAM cell will then produce the corresponding output value on BL.

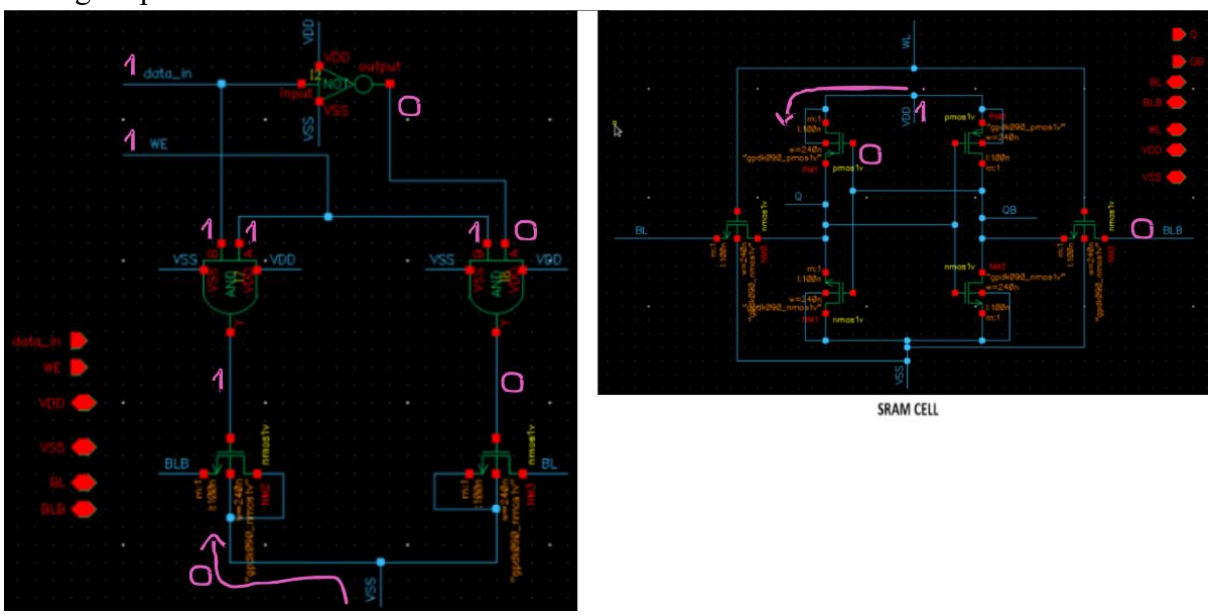

Figure 9+10: Write enable has the value of 1, data = 1

Waveform of Write driver:

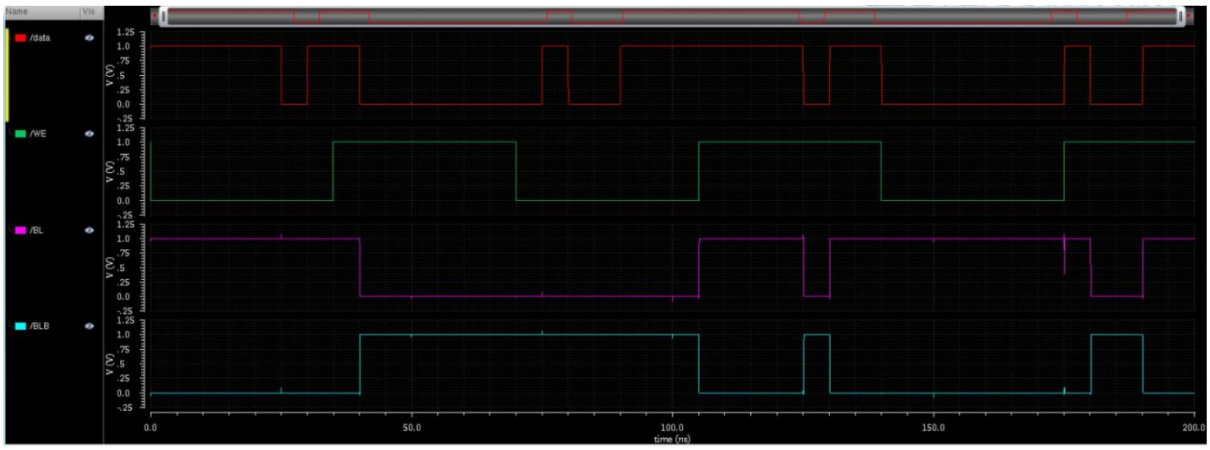

Figure 11: Waveform of Write driver

When Write Enable (WE) is set to 1, it allows data to be written to the bitline (BL) of the memory cell. For data equal to 1 with WE equal to 1, BL is set to 1, and BLB is set to 0. Similarly, for data equal to 0 with WE equal to 1, BL is set to 1, and BLB is set to 0.

When Write Enable (WE) is set to 0, it prohibits data from being written to BL of the memory cell. BL retains its previous state.

Truth table of Write driver:

Table 3: Truth table of Write Driver

WE	DataIn	BL	BLB
0	X	Q	Q_Bar
1	0	0	1
1	1	1	0

Some additional uses of Write driver

The Write Driver circuit in the design of SRAM (Static Random-Access Memory) serves important functions in the process of writing data into SRAM cells. Some key purposes of the Write Driver circuit:

- Data Writing:

The primary function of the Write Driver circuit is to perform the data writing process into the SRAM cells. When a specific address is selected for writing, the Write Driver circuit stimulates the write process to store the new data.

- Generate Write Signal:

The Write Driver circuit generates a write signal (write enable signal) to control the data writing process. This signal can be generated using input signals from the system.

- Ensure Stabilization:

After the data is written, the Write Driver circuit ensures that the new value has stabilized sufficiently and is stored in the SRAM cells. This ensures the integrity and reliability of the data.

- Voltage Control:

The Write Driver circuit may also be involved in controlling the voltage applied during the writing process to ensure the stability of this process.

- Application in SRAM Architecture:

In the SRAM architecture, the Write Driver circuit is an essential part of the Write Circuitry. It, along with other elements like Read Circuitry, plays a role in ensuring the proper operation of the SRAM memory.

4.1.3. Sense Amplifier

Sense amplifier in SRAM is a switching circuit used to amplify and clarify the read signal from SRAM cells. When a specific SRAM cell is selected for reading, the data from the bitline is transmitted to the sense amplifier to boost the signal level and convert the data from the standby current form into a readable signal. The sense amplifier enhances and clarifies the logic state of the data, playing a crucial role in accelerating the readout process from SRAM cells, ensuring performance, and maintaining accuracy in memory operations.

To read the value in Sram memory cells, an AMPLIFIER circuit is needed to SENSE (sense) the value in the memory cell.

The input of a sense amplifier circuit is the bit lines of the SRAM memory cell column with an output voltage of 0 or 1.

The bitline must be loaded before each read cycle to ensure that the difference between the two bitlines is correct. Ensuring that there is a difference between the two bitlines is important. For example, if bit line 0 is loaded first, the reading circuit is likely to read incorrectly and vice versa.

The structure of the Sense amplifier is depicted in the diagram below:

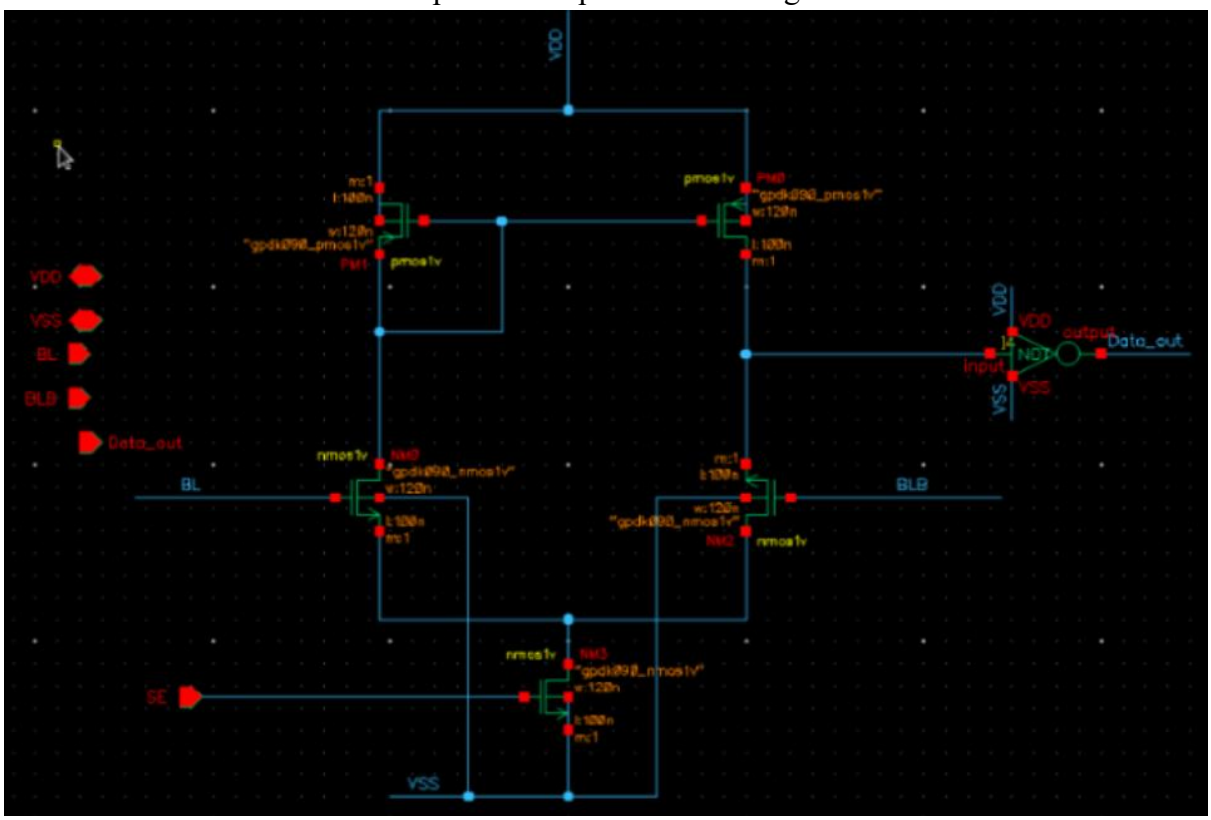

Figure 12: Schematic of Sense amplifier

The operating principle of the Sense amplifier

The sense amplifier circuit in SRAM plays an important role in the process of reading data from SRAM memory cells. Below is a description of how the sense amplifier circuit works:

- Preparation (Precharge): Before the read process, the Sense Amplifier typically needs preparation. This involves setting the initial state and preparing the components of the circuit to receive and process signals from SRAM cells.

- Signal Conversion: When a specific SRAM cell is selected for reading, the data from the bitline is transmitted to the Sense Amplifier. The Sense Amplifier amplifies this signal, making it large enough for use in subsequent read stages.

- Logic Level Determination: The Sense Amplifier helps determine the logic level of the data from the SRAM cell. Based on the amplified signal, the Sense Amplifier determines whether the data is logic 0 or logic 1.

- Generating Accurate Read Output: The output of the Sense Amplifier represents the logic level of the data from the SRAM cell and is used to generate accurate read output from the SRAM memory.

Waveform of Sense amplifier:

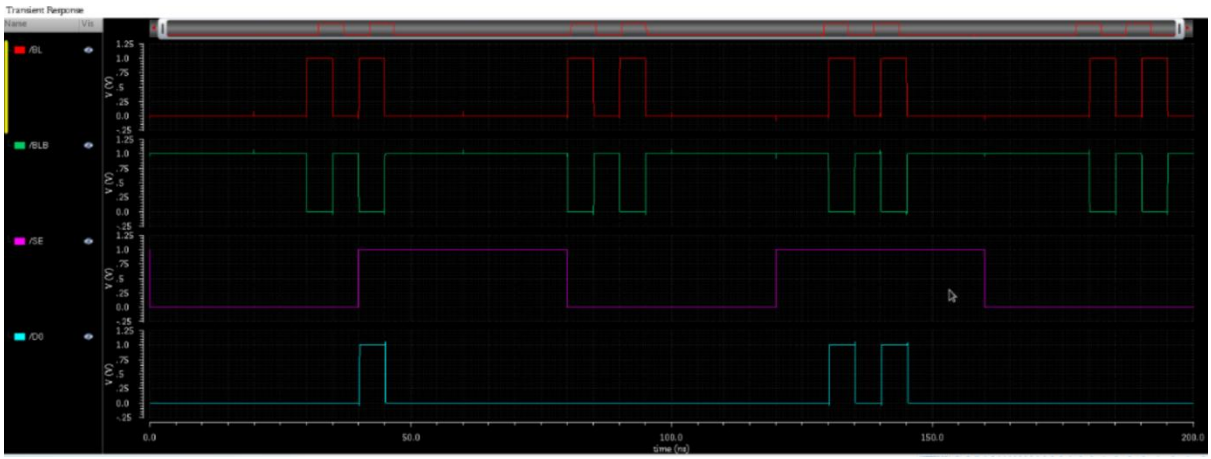

Figure 13: Waveform of Sense amplifier

When Sense Enable (SE) is set to 1, the output D0 receives the value of BL.
When Sense Enable (SE) is set to 0, the output D0 will not read and will have no value.

4.1.4. Row/Column Decoder

Row Decoder (Decoder 2 to 4):

A 2-to-4 Decoder is a type of digital circuit designed to convert a 2-bit binary input into one of four corresponding output lines. The main goal of a decoder circuit is to reduce the number of output lines compared to the number of input lines, thereby reducing system complexity and increasing efficiency.

Decoder circuits are commonly used in applications where it is necessary to determine one of several choices or data paths based on a binary input signal. Common applications of a 2-to-4 decoder include controlling 7-segment displays, selecting input lines for a latch, or determining the address of a memory register.

Features:

+ Number of Inputs and Outputs: A 2 to 4 Decoder has 2 binary inputs (A0 and A1), 1 Enable Signal and 4 outputs (Y0, Y1, Y2, Y3)
+ Input and Output Pin Configuration:

Input (A and B): The circuit can accept binary input signals 00, 01, 10, or 11.

Output (Y0, Y1, Y2, Y3): Each output corresponds to a binary value of the input

The structure of the Row Decoder is depicted in the diagram below:

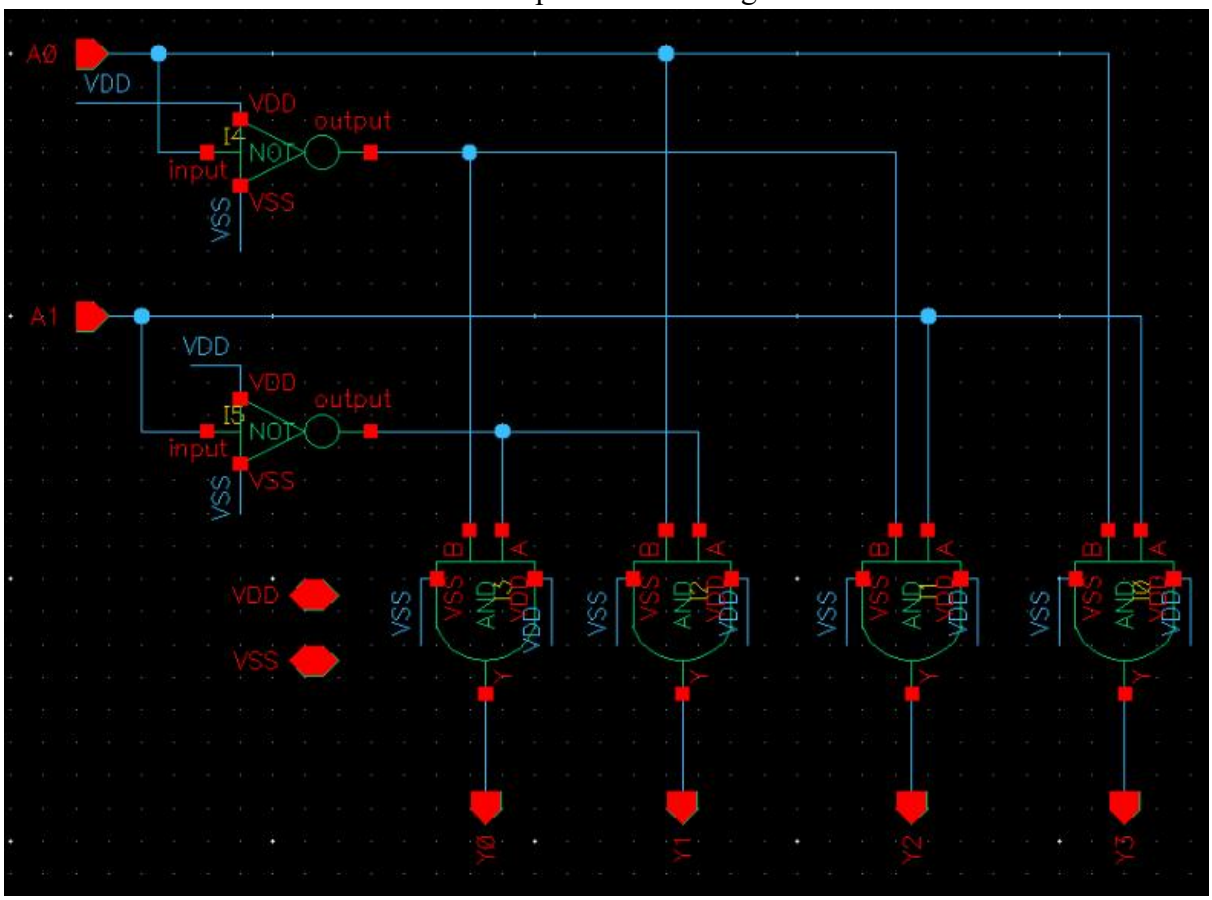

Figure 14: Schematic of Row Decoder

Waveform of Row Decoder

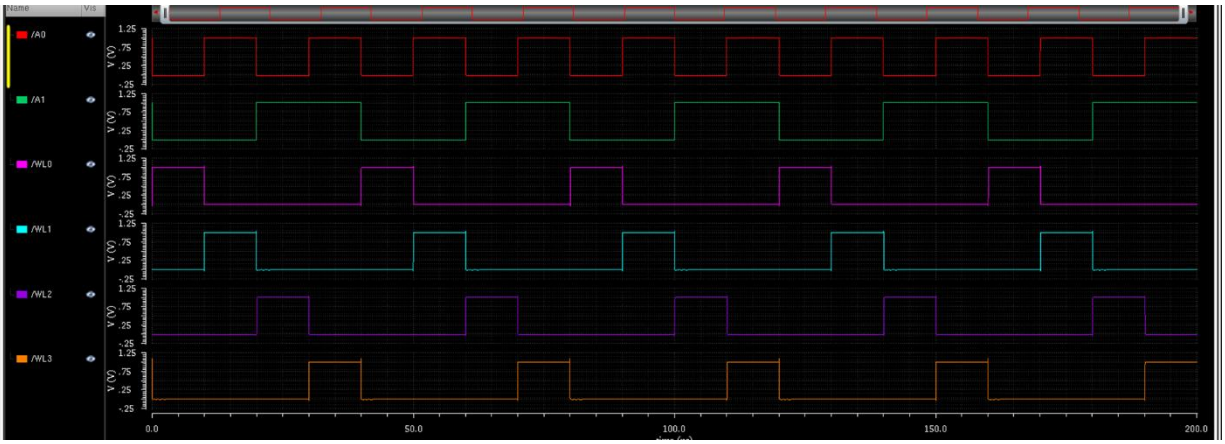

Figure 15: Waveform of Row Decoder

The truth table of Row Decoder:

Table 4: Truth table of Row decoder

Inputs			Outputs			
EN	A0	A1	Y3	Y2	Y1	Y0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

The operating principle of the Row Decoder circuit

The state of the input determines which output is activated. One of the outputs becomes active (logic high), while the remaining outputs are in an inactive state (logic low).

When the EN (Enable) signal is 0, the inputs (A0, A1) are undefined, and during this time, the outputs (Y3, Y2, Y1, and Y0) are set to 0.

When the EN signal is 1:

For input (A0, A1) = "00," output Y0 is activated.

For input (A0, A1) = "01," output Y1 is activated.

For input (A0, A1) = "10," output Y2 is activated.

For input (A0, A1) = "11," output Y3 is activated.

Column Decoder:

A 3-to-8 column decoder is a type of column decoding circuit designed to convert a 3-bit column address into one of eight corresponding output lines. This is commonly used in applications such as SRAM or word line decoders, where it helps determine the specific column to be activated or selected.

The role of the column decoder in SRAM (Static Random-Access Memory) is crucial in the read and write operations of memory. SRAM is organized into a matrix, and both the row and column decoders are essential in determining a specific location in that matrix.

Features:

+ Number of Inputs and Outputs: This decoder has 3 binary inputs (A, B and C), 1 Enable Signal and 8 outputs (Y0 to Y7).

+ Output Pin Configuration: Each 3-bit column address value maps to one of the eight corresponding outputs

The structure of the Column Decoder is depicted in the diagram below:

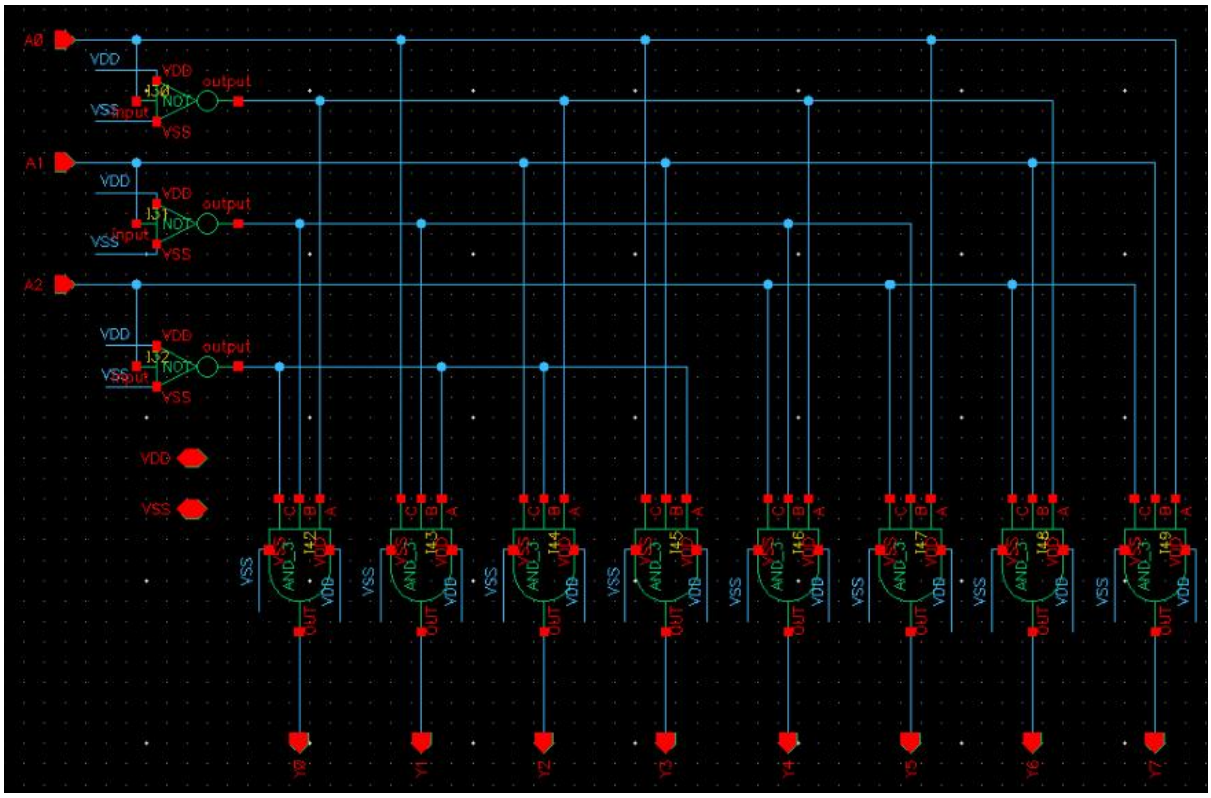

Figure 16: Schematic of Column Decoder

Waveform of Column Decoder

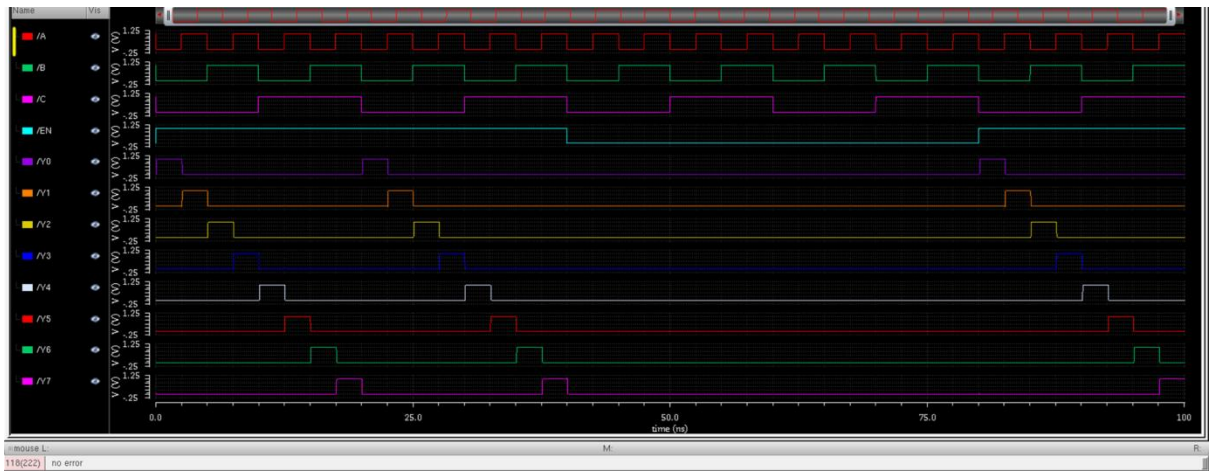

Figure 17: Waveform of Column Decoder

The truth table of Column Decoder:

Table 5: Truth table of Column decoder

	Inputs			Outputs							
EN	**A**	**B**	**C**	**Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

The operating principle of the Row Decoder circuit

The state of the input determines which output is activated. One of the outputs becomes active (logic high), while the remaining outputs are in an inactive state (logic low).

When the EN (Enable) signal is 0, the inputs (A, B, C) are undefined, and during this time, the outputs (Y0 to Y7) are set to 0.

When the EN signal is 1:

For input (A, B, C) = "000," output Y0 is activated.

For input (A, B, C) = "001," output Y1 is activated.

For input (A, B, C) = "010," output Y2 is activated.

For input (A, B, C) = "011," output Y3 is activated.

For input (A, B, C) = "100," output Y4 is activated.

For input (A, B, C) = "101," output Y5 is activated.

For input (A, B, C) = "110," output Y6 is activated.

For input (A, B, C) = "111," output Y7 is activated.

4.2. SRAM CELL

4.2.1. 6T-SRAM

A 6T SRAM cell refers to a type of Static Random-Access Memory (SRAM) cell that consists of six transistors. The 6T-SRAM cell consists of two cross-coupled inverters and two access transistors. SRAM is a type of volatile semiconductor memory that stores binary information as long as power is supplied. The 6T SRAM cell is commonly used in integrated circuits (ICs) such as microprocessors and cache memories.

The structure of the 6T-SRAM is depicted in the diagram below:

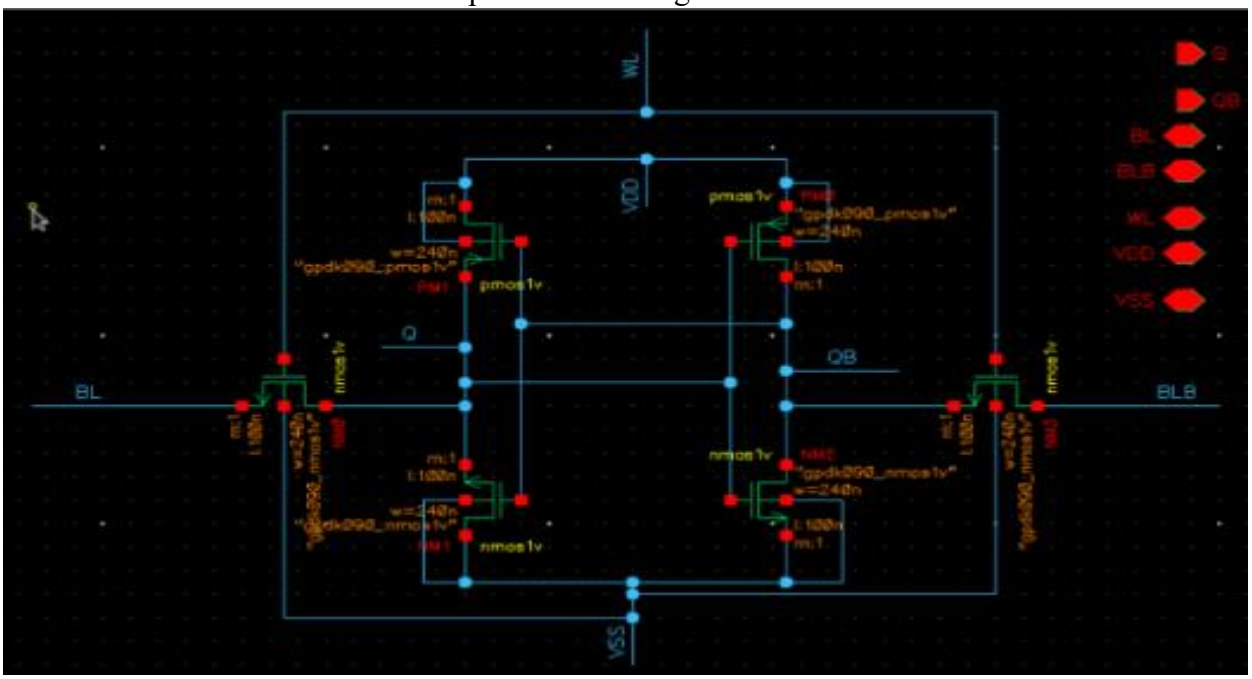

Figure 18: Schematic of 6T-SRAM cell

The operating principle of 6T SRAM

- Initialization (Write Operation):

Initially, the two access transistors (usually NMOS transistors) connecting the storage node (bitline) to the bitlines are turned off, isolating the cell from external influences.

The bitlines are precharged to a certain voltage level.

- Writing a '0' or '1':

To write a '0' to the cell, the write driver forces one of the bitlines (BL or BLB) to a low voltage while the other is kept high.

This causes one of the pull-up transistors in the cross-coupled latch to conduct, establishing a low voltage at one side of the latch.

The low voltage propagates through the latch due to the feedback provided by the cross-coupled inverters, reinforcing the '0' state.

To write a '1' to the cell, the operation is reversed. The other bitline is pulled low while the opposite is kept high, causing the opposite pull-up transistor to conduct and establish a high voltage in the latch.

- Read Operation:

During a read operation, the access transistors are turned on, allowing the contents of the cell to be read onto the bitlines.

The voltage levels on the bitlines are sensed to determine the stored bit. If the voltage on one bitline is higher than the other, it indicates a '1,' and if the voltage on the other bitline is higher, it indicates a '0.'

- Storage and Stability:

The cross-coupled inverters store the binary state (0 or 1) by maintaining a stable voltage difference between them.

The latch will retain its state until a write operation is performed, or power is removed.

The two access transistors are used to read and write data to the cell. When a read operation is performed, the bit line is precharged to a high voltage level. If the cell contains a logic high, the bit line is discharged through the access transistor, causing a voltage drop. This voltage drop is detected by a sense amplifier, which amplifies the signal and outputs the data1. During a write operation, the bit line is driven to the desired voltage level, and the access transistor is turned on to write the data to the cell1.

Waveform of 6T-SRAM

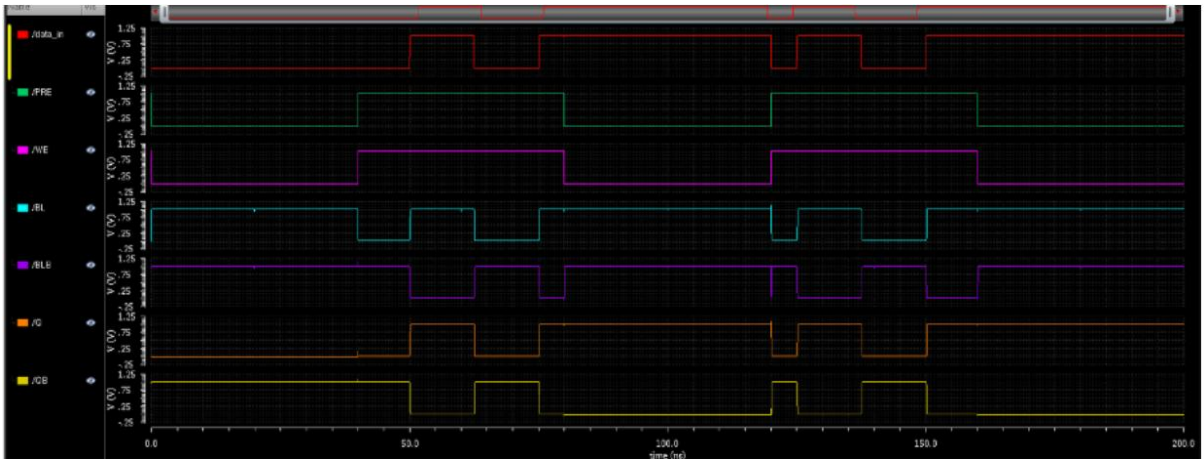

Figure 19: Waveform of 6T-SRAM cell

Data lines and Pre-charge signals. When the Pre-charge signal is 0, it pulls BL and BLB lines up to VDD=1V to establish the appropriate voltage level for the memory cell. When the Pre-charge signal is 1, and the Write Enable signal (allowing writing) is also 1, data can be written to the memory cell.

Upon introducing data to the memory cell, it writes the data using the Bitline and Bitline-bar, and the written data is stored at the memory latch points (Q and QB). If the data is 1, BL writes 1, and Q stores 1.

When the Pre-charge signal is set to 0, BL and BLB are pulled up to VDD=1V again. If the Write Enable signal is 0, indicating that the memory is not allowed to write data, Q retains its previous state. This means if Q was storing 1 when WE=1, then when WE=0, Q will maintain its previous state of 1, and vice versa.

4.2.2. 4T-SRAM

A 4T SRAM (Static Random-Access Memory) cell is an alternative design to the more commonly used 6T SRAM cell. As the name suggests, the 4T SRAM cell consists of four transistors. It sacrifices some of the stability of the 6T SRAM cell in favor of reduced size and power consumption.

The structure of the 4T-SRAM is depicted in the diagram below:

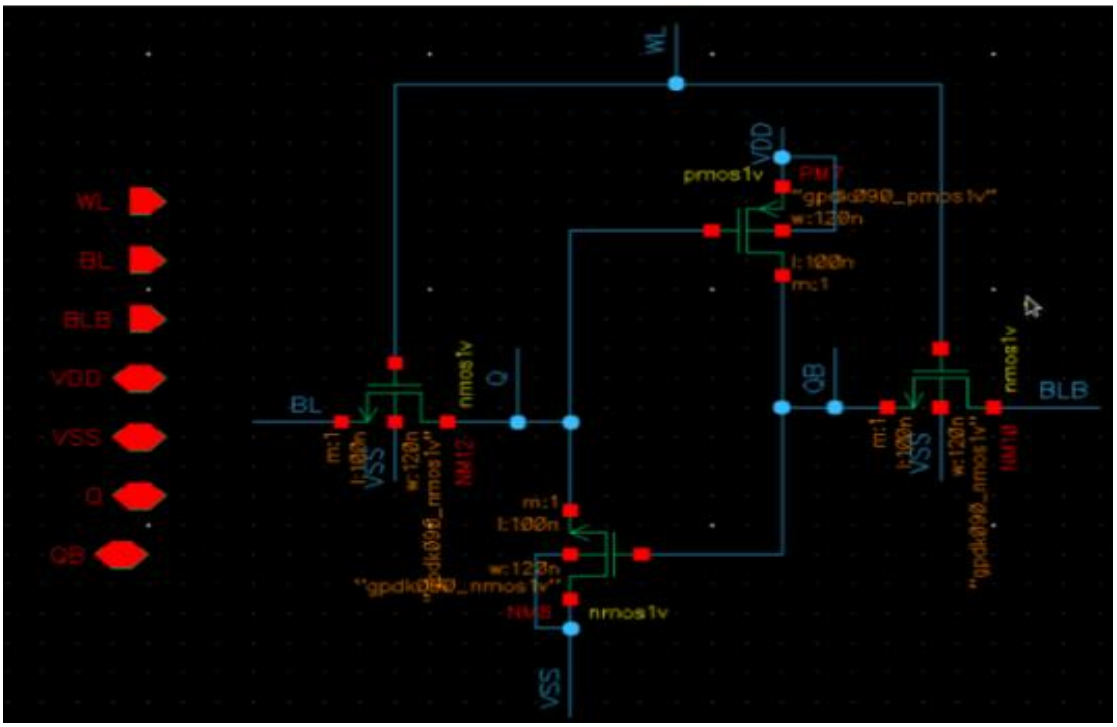

Figure 20: Schematic of 4T-SRAM cell

The operating principle of 4T SRAM

Access transistors (2 transistors): These transistors are responsible for connecting the storage node (bitline) to the internal nodes of the cell during read and write operations. They control the access to the memory cell.

Cross-coupled inverters (2 transistors): These transistors form a latch that stores the binary information. The cross-coupled inverters function similarly to the ones in the 6T SRAM cell but with one pair of pull-up/pull-down transistors instead of two pairs.

Write Operation:

During a write operation, the access transistors are turned on, connecting the storage node to the bitlines.

The values to be written are then driven onto the internal nodes of the cell.

Read Operation:

During a read operation, the access transistors are turned on, connecting the storage node to the bitlines.

The voltage on the bitlines is then sensed to determine the stored bit. If one bitline has a higher voltage than the other, it indicates a '1,' and vice versa.

Waveform of 4T-SRAM

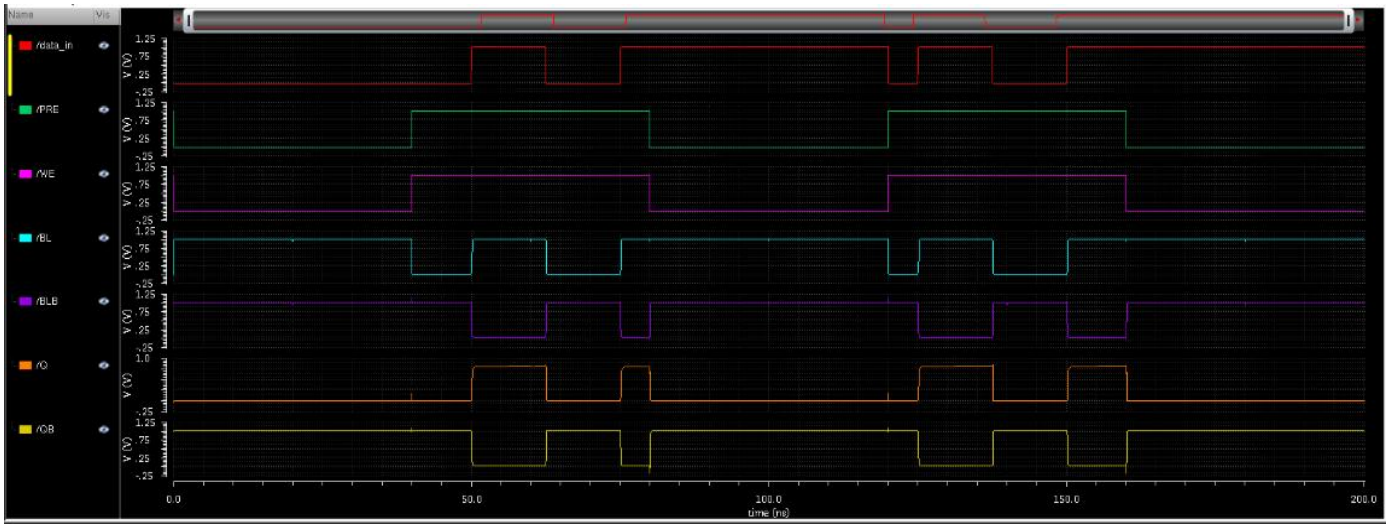

Figure 21:Waveform of 4T-SRAM cell

Data lines and Pre-charge signals. When the Pre-charge signal is 0, it pulls BL and BLB lines up to VDD=1V to establish the appropriate voltage level for the memory cell. When the Pre-charge signal is 1, and the Write Enable signal (allowing writing) is also 1, data can be written to the memory cell.

Upon introducing data to the memory cell, it writes the data using the Bitline and Bitline-bar, and the written data is stored at the memory latch points (Q and QB). If the data is 1, BL writes 1, and Q stores 1.

When the Pre-charge signal is set to 0, BL and BLB are pulled up to VDD=1V again. If the Write Enable signal is 0, indicating that the memory is not allowed to write data, Q retains its previous state. This means if Q was storing 1 when WE=1, then when WE=0, Q will maintain its previous state of 1, and vice versa.

4.2.3. 8T-SRAM

To improve the SRAM cell functionality, several solutions have been proposed from device to architecture level. For instance, the use of new devices such as FinFETs leads to a significant performance improvement. At the cell level, new cells such as 7T, 8T, 9T, 10T, and 11T have been proposed with the focus on improving read static noise margin (RSNM) or write margin (WM). At the architecture level, proposed read and write assist techniques in literature can improve SRAM robustness and performance while occupying less area compared to the cell techniques (e.g. 8T and 10T) and can be used with any type of SRAM. To understand the existing challenges in SRAM design let us explain the operation of standard 6T-SRAM cells.

To overcome this issue, different cell techniques such as 8T-SRAM cell ameliorates the degraded robustness of the standard 6T-SRAM cell by separating read and write bitlines leading to a significant improvement in read static noise margin (RSNM) while the write margin is not affected. The standard 8T-SRAM as it is seen, read and write cycles use different wordlines and bitlines.

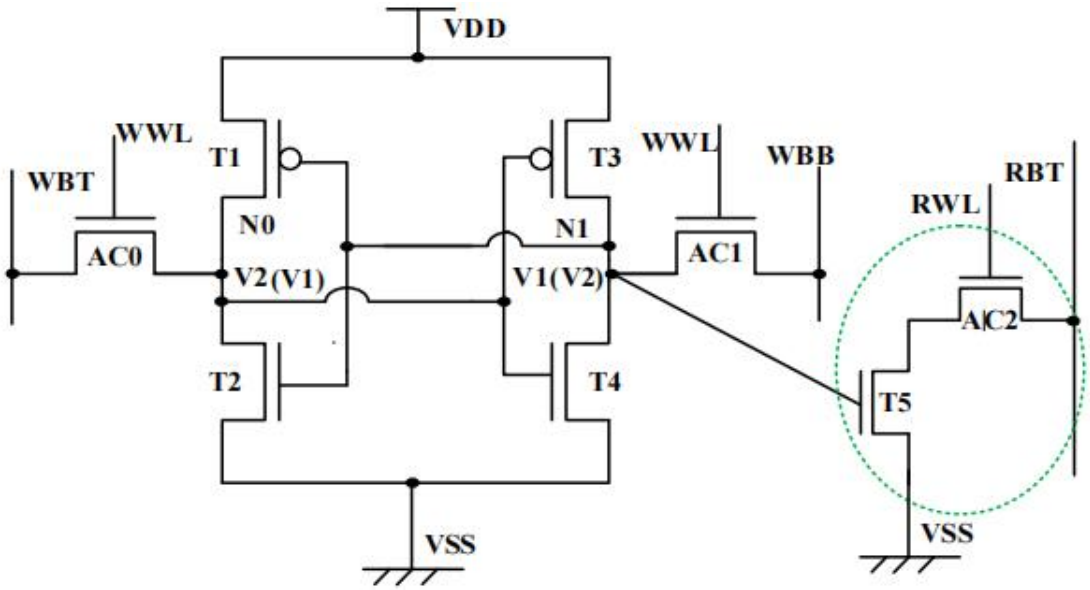

Figure 22: Schematic of 8T-SRAM cell

The operating principle of 8T SRAM

The basic design of 8T is based on the standard SRAM design with a 6-transistor memory cell. In this design, the 8T separates the two parts of writing and reading data into the SRAM cell, as illustrated by the dashed circle in Figure 4. The transistors AC0 and AC1 are controlled by the write wordline signal (WWL), while AC2 is controlled by the read wordline signal (RWL). The write bitlines (WBT) and write bitline bar (WBB) are used to write data into the SRAM cell. On the other hand, the read bitline signal (RBT) is used to read data from the SRAM cell.

The advantage of separating the write and read parts in the 8T design significantly improves the Read Static Noise Margin (SNM) without affecting the write operation or previously stored data in the memory cell. Compared to the 6T design, the new design is considered asymmetric because it only uses the RBT line to read data. During the read operation, the RBT line is first pulled up to the VDD voltage level. Then, depending on the stored bit value in the memory cell, the RBT line will be pulled down to 0 or remain in the high state.

The structure of the 8T-SRAM is depicted in the diagram below:

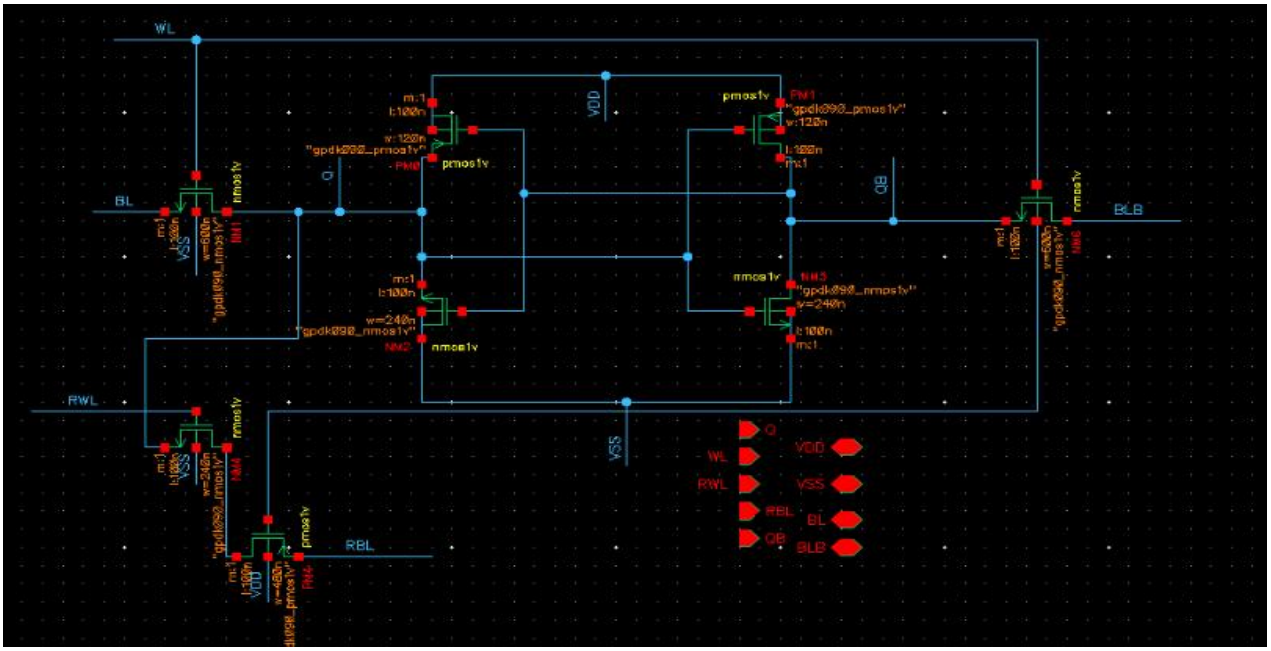

Figure 23: Schematic of 8T-SRAM cell

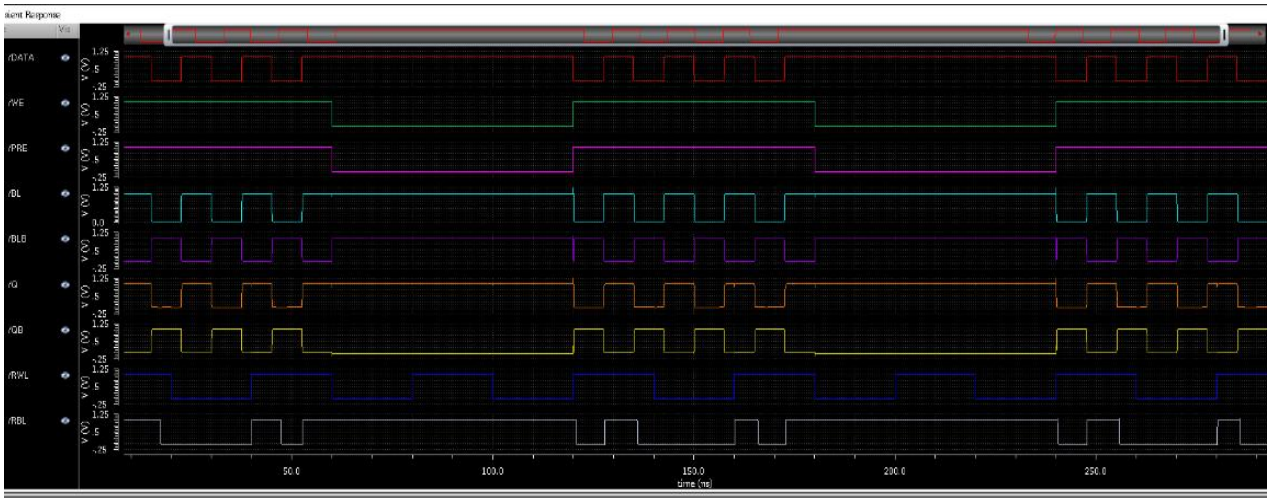

Figure 24: Waveform of 8T-SRAM cell

Firstly, we have a data line, which is the information we want to store in the SRAM cell. Next is the WE (Write Enable) line, indicating that when WE is set to one, the data on the data line will be written to BL (Bitline). If WE is set to zero, it means that the data won't be written. When the PRE (Precharge) line is set to zero, both BL and BLB (Bitline Bar) are pulled up to a high level (VDD=1). If PRE is set to one while WE is also set to one, the data will be written to both BL and BLB. If the WWL (Write Wordline) is set to one, the value from BL will be written to the Q line. Specifically, in this case, we assume WWL is set equal to WE. Conversely, if WWL is set to zero, Q will be set to zero. To read the value from the memory cell, we need to rely on the RWL (Read Worldline) line. When RWL is set to one, the data value will be read into the RBL (Read Bitline). If RWL is set to zero, RBL will be set to zero as well.

4.2.4. LP 6T-SRAM

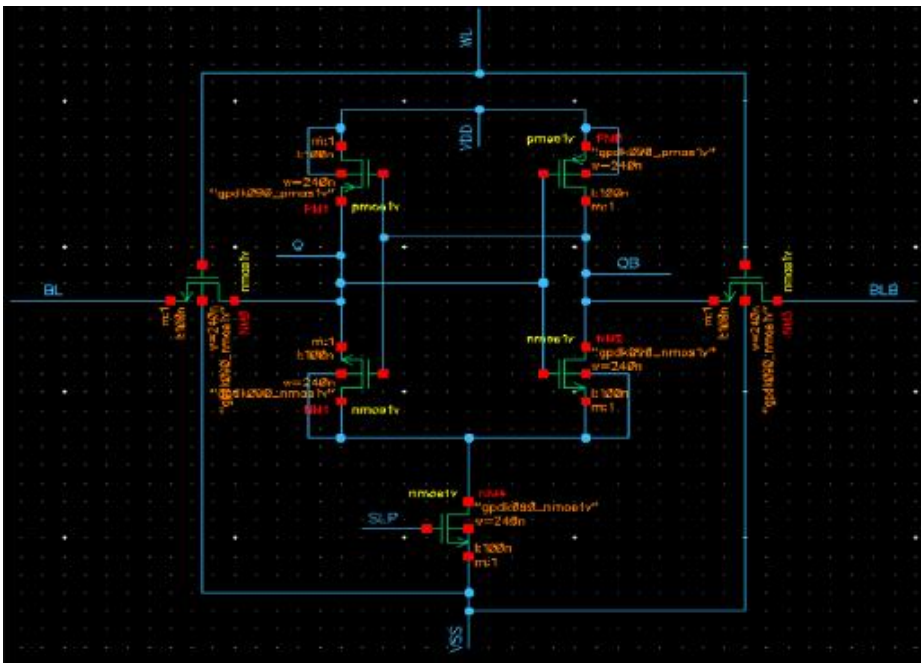

Figure 25: Schematic of Low-power 6T-SRAM cell

4.3. 32-BIT SRAM

4.3.1. 32-bit 6T-SRAM

This is an SRAM with a capacity of 32 bits. The internal structure consists of 4 rows and 8 columns, the memory cell address is the position of that memory cell based on rows and columns, for example, the first memory cell will have the address of row 1 and column 1 (R1, C1), the second memory cell will have the address of row 1 and column 2 (R1, C2),...

Each column will consist of a Pre-charge circuit at the top connected to the bottom 4 memory cells, the Bitline (BL) and Bitline-bar of the memory cells will be connected to the BL and BLB outputs of the Write Driver circuit. At the bottom is a Sense-amplifier that allows SRAM to read data from the memory cell.

Row-decoder is Decoder 2-4 connected to the WL pin of memory cells in horizontal rows. The column-decoder is the Decoder 3-8 connected to the WE pin of the Write Driver circuits.

The structure of the 32-bit 6T-SRAM is depicted in the figure below:

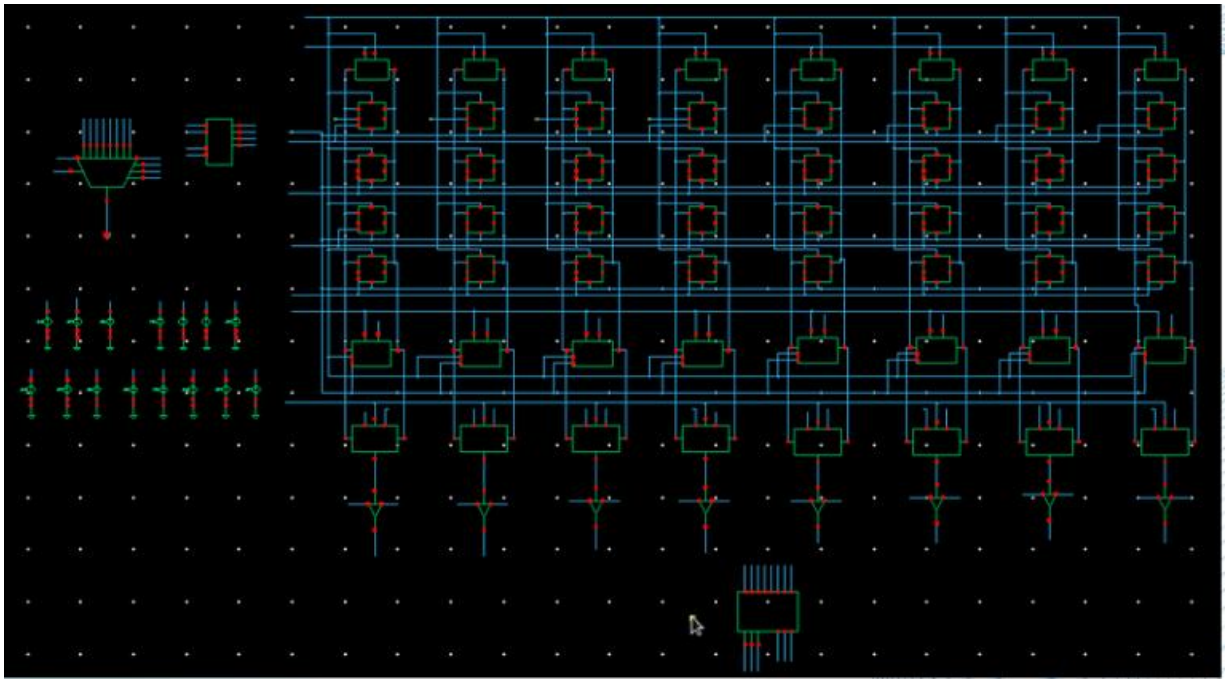

Figure 26: Structure of the 32-bit 6T-SRAM

Waveform of the 32-bit 6T-SRAM:

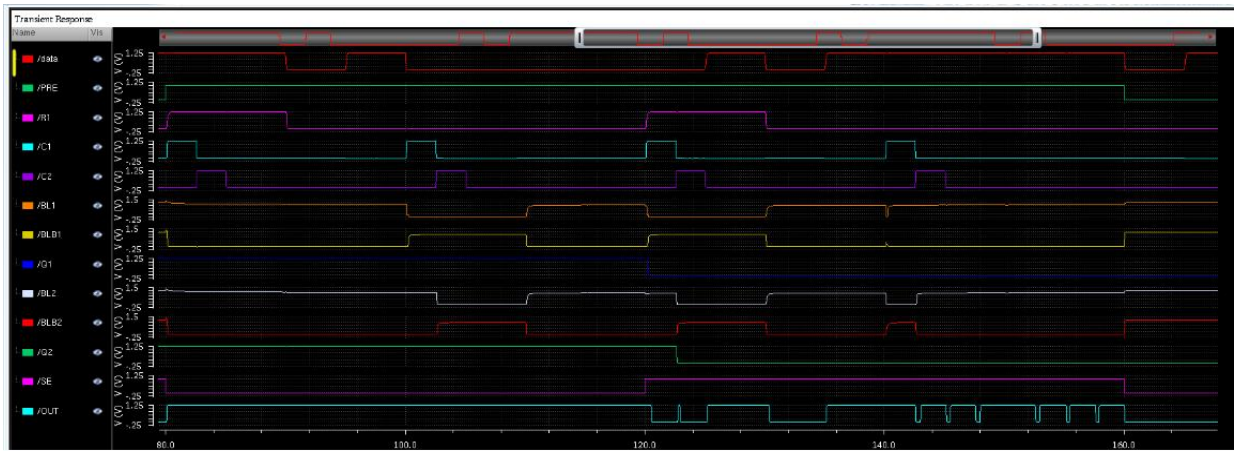

Figure 27: Waveform of the 32-bit 6T-SRAM

The operating principle of 32-bit 6T-SRAM

Write operation.

When the Pre-charge (PRE) signal reaches 0, the Bitline and Bitline-bar lines of all memory cells are pulled up to VDD=1V to set the appropriate voltage level for the memory cells. When the Pre-charge signal has a value of 1, Row-decoder (Rn), Column-decoder (Cn) select the memory cell according to row position and column position. Data =0, PRE=1, R1=1, C1=1 – the first memory cell is selected and written to Bitline 1 (BL1) and Bitline-bar 1 (BLB1) – BL1=0, BLB1=1 and the data will be written to Storage-point (Q1=BL1=0). Then C1=0 and C2=1, the second memory cell (row 1 – column 2) is selected, BL2=0, BLB2=1, Q2=0.

Read operation

When the Sense Enable (SE) signal has a value of 0, memory will not read the written data. When SE has a value of 1, allowing the memory to read data from the written memory

cells, the output data (OUT) will have the same value as the value of Storage-point (Q), SE=1, Q=0, OUT=0

4.3.2. 32-bit 4T-SRAM

This SRAM has a 32-bit capacity, organized internally into 4 rows and 8 columns. The memory cell address is determined by the row and column positions. For instance, the first memory cell is located at row 1, column 1 (R1, C1), the second memory cell at row 1, column 2 (R1, C2), and so on.

In each column, there is a Pre-charge circuit positioned at the top, linked to the bottom 4 memory cells. The Bitline (BL) and Bitline-bar of these memory cells are connected to the BL and BLB outputs of the Write Driver circuit. At the lower part, a Sense-amplifier facilitates data reading from the memory cells in the SRAM.

The row-decoder, specifically the Decoder 2-4, is connected to the WL pin of memory cells arranged in horizontal rows. As for the column-decoder, it is the Decoder 3-8 linked to the WE pin of the Write Driver circuits.

The structure of the 32-bit 4T-SRAM is depicted in the diagram below:

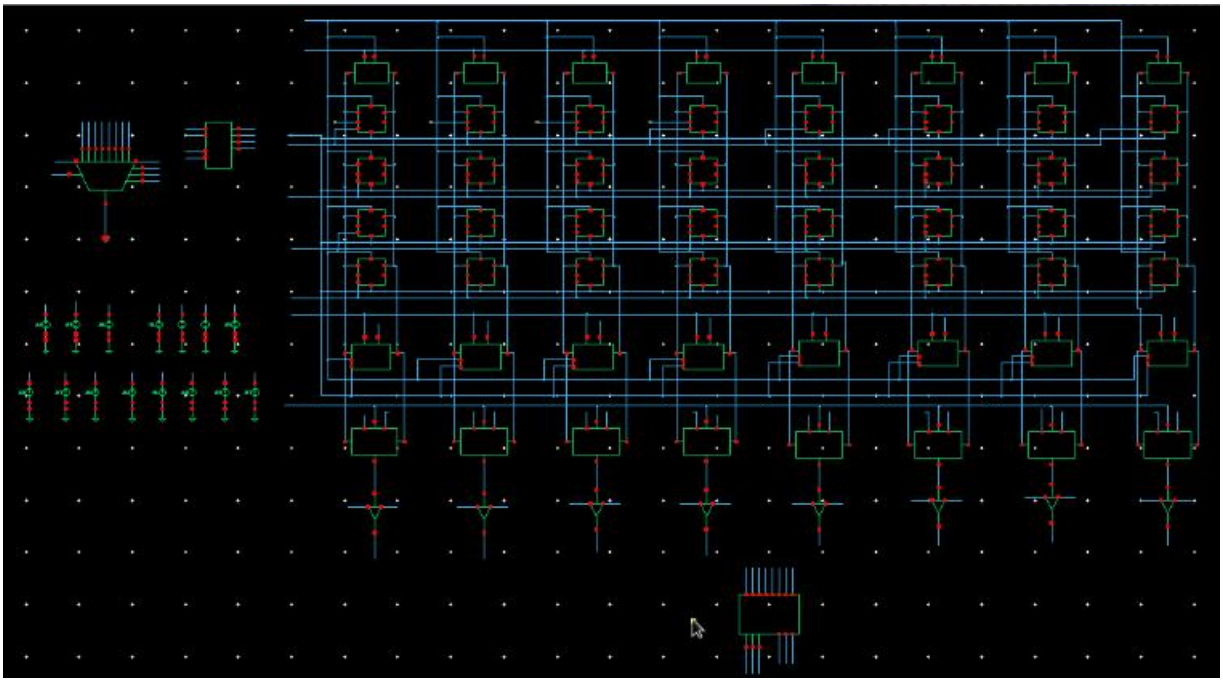

Figure 28: Structure of the 32-bit 4T-SRAM

Waveform of the 32-bit 4T-SRAM:

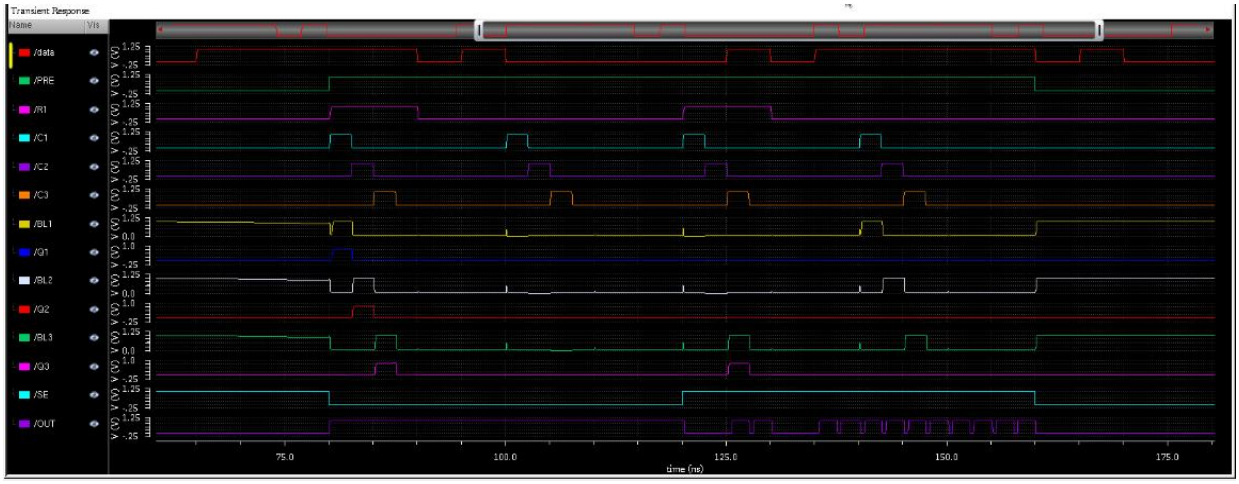

Figure 29: Waveform of the 32-bit 4T-SRAM

The operating principle of 32-bit 4T-SRAM:

Write Operation:

During the write operation, when the Pre-charge (PRE) signal drops to 0, the Bitline and Bitline-bar lines of all memory cells are raised to VDD=1V, establishing the appropriate voltage level. With a Pre-charge signal of 1, the Row-decoder (Rn) and Column-decoder (Cn) select the memory cell based on the row and column positions. For instance, with Data=0, PRE=1, R1=1, C1=1, the first memory cell is chosen and written to Bitline 1 (BL1) and Bitline-bar 1 (BLB1). This results in BL1=0, BLB1=1, and the data is written to the Storage-point (Q1=BL1=0). Subsequently, when C1=0 and C2=1, the second memory cell (row 1–column 2) is selected, BL2=0, BLB2=1, and Q2=0.

Read Operation:

For the read operation, when the Sense Enable (SE) signal is 0, the memory does not read the written data. On the other hand, with SE having a value of 1, enabling the memory to read data from the written memory cells, the output data (OUT) will match the value of the Storage-point (Q). Therefore, when SE=1, Q=0, OUT=0

4.3.3. 32-bit 8T-SRAM

This represents an SRAM module featuring a 32-bit capacity. Its internal arrangement encompasses 4 rows and 8 columns, where the memory cell's address is determined by its position in terms of rows and columns. For instance, the initial memory cell is addressed as (R1, C1), the second one as (R1, C2), and so forth. In each column, a pre-charge circuit is positioned at the top, linking to the lower 4 memory cells. The Bitline (BL) and Bitline-bar of these memory cells are connected to the BL and BLB outputs of the Write Driver circuit.

The row-decoder, identified as Decoder 2-4, is linked to the Word Line (WL) pin of memory cells in horizontal rows. Simultaneously, the column-decoder, recognized as Decoder 3-8, is connected to the Write Enable (WE) pin of the Write Driver circuits. This setup facilitates systematic addressing and access to the 32-bit data stored in the SRAM. The pre-charge circuit, along with Bitline connections and decoders, plays a crucial role in ensuring proper functionality during read and write operations.

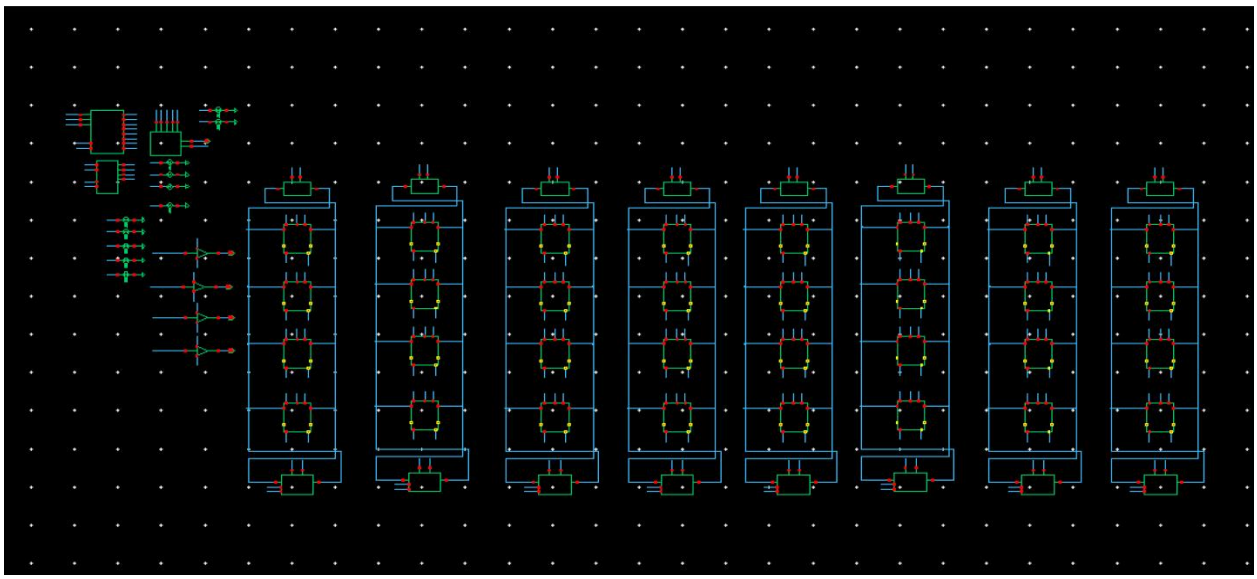

Figure 30: Structure of the 32-bit 8T-SRAM

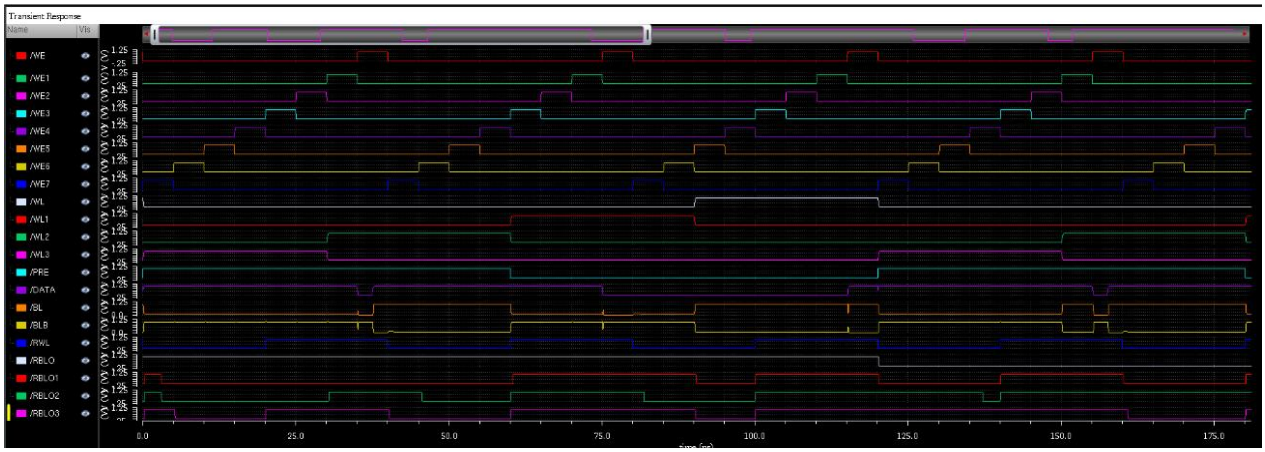

Figure 31: Waveform of the 32-bit 8T-SRAM

The operating principle of 32-bit 8T-SRAM:

Write operation.

When the Pre-charge (PRE) signal reaches 0, the Bitline and Bitline-bar lines of all memory cells are pulled up to VDD=1V to set the appropriate voltage level for the memory cells. When the Pre-charge signal has a value of 1, Row-decoder (Rn), Column-decoder (Cn) select the memory cell according to row position and column position. Data =0, PRE=1, R1=1, C1=1 – the first memory cell is selected and written to Bitline 1 (BL1) and Bitline-bar 1 (BLB1) – BL1=0, BLB1=1 and the data will be written to Storage-point (Q1=BL1=0). Then C1=0 and C2=1, the second memory cell (row 1 – column 2) is selected, BL2=0, BLB2=1, Q2=0.

Read operation

When the Real Bitline (RBL) signal has a value of 0, memory will not read the written data. When RBL has a value of 1, allowing the memory to read data from the written memory cells, the Read Wordline (RWL) will have the same value as the value of Storage-point (Q), RBL=1, Q=0, RWL=0

4.4. Delay & Power

4.4.1. Delay

4.4.1.1.Definitions

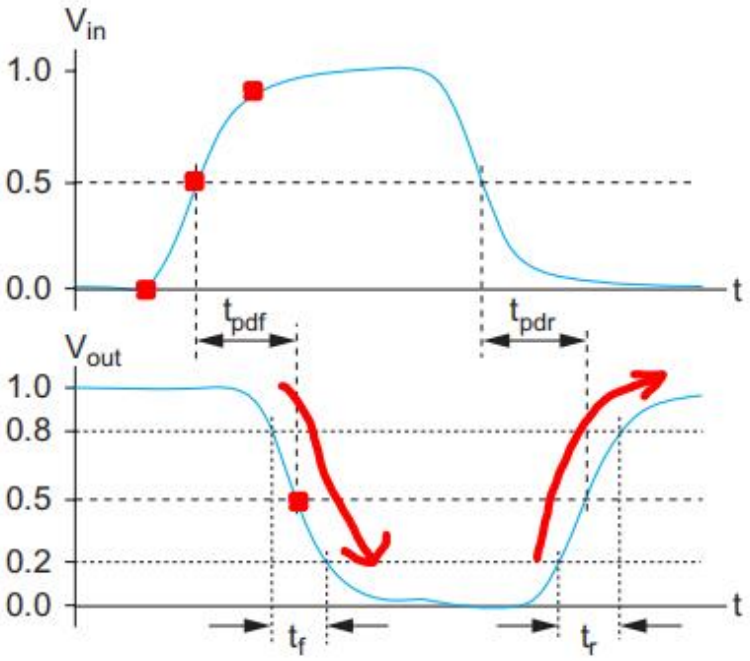

Figure 32: Propagation delay and rise/fall times

- Propagation delay time, tpd = maximum time from the input crossing 50% to the output crossing 50%.
- Contamination delay time, tcd = minimum time from the input crossing 50% to the output crossing 50%.
- Rise time, tr = time for a waveform to rise from 20% to 80% of its steady-state value.
- Fall time, tf = time for a waveform to fall from 80% to 20% of its steady-state value.
- Edge rate, trf = (tr + tf)/2.

Propagation delay is usually the most relevant value of interest, and is often simply called delay.

A timing analyzer computes the arrival times, i.e., the latest time at which each node in a block of logic will switch. The nodes are classified as inputs, outputs, and internal nodes. The user must specify the arrival time of inputs and the time data is required at theoutputs. The arrival time ai at internal node i depends on the propagation delay of the gate driving i and the arrival times of the inputs to the gate:

$$a_i = \max_{j \in fanin(i)} \{a_j\} + t_{pd_i}$$

The timing analyzer computes the arrival times at each node and checks that the outputs arrive by their required time. The *slack* is the difference between the required and arrival

times. *Positive slack* means that the circuit meets timing. *Negative slack* means that the circuit is not fast enough.

4.4.1.2. Timing Optimization

Timing optimization is the process of adjusting the design of an electronic circuit to ensure that control and data signal paths operate synchronously and meet the specified timing requirements within a system. The primary goal of timing optimization is to reduce the delay in the electronic circuit, especially in digital and processing circuits, to ensure performance, meet timing constraints, and enhance the system's operating speed.

In the majority of designs, numerous logic paths operate at a speed that doesn't necessitate deliberate intervention. These paths already meet the timing objectives of the system, being sufficiently fast. Nonetheless, there exist critical paths that impose restrictions on the operational speed of the system, demanding careful consideration of timing intricacies. These critical paths may undergo influences at four primary levels:

- The architectural/microarchitectural level.
- The logic level.
- The circuit level.
- The layout level.

4.4.2. Power

4.4.2.1. Definitions

The *instantaneous power* $P(t)$ consumed or supplied by a circuit element is the product of the current through the element and the voltage across the element

$$P(t) = I(t)V(t)$$

The *energy* consumed or supplied over some time interval T is the integral of the instantaneous power

$$E = \int_0^T P(t)dt$$

The *average power* over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt$$

Power is expressed in units of Watts (W). Energy in circuits is usually expressed in Joules (J), where 1 W = 1 J/s. Energy in batteries is often given in W-hr, where 1 W-hr = (1 J/s)(3600 s/hr)(1 hr) = 3600 J

4.4.2.2. Sources of Power Dissipation

Power dissipation in CMOS circuits comes from two components:

Dynamic dissipation due to

○ Charging and discharging load capacitances as gates switch

○ “Short-circuit” current while both pMOS and nMOS stacks are partially ON Static dissipation due to

○ Subthreshold leakage through OFF transistors

○ Gate leakage through gate dielectric

○ Junction leakage from source/drain diffusions
○ Contention current in ratioed circuits
Putting this together gives the total power of a circuit

$$P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{short circuit}}$$

$$P_{\text{static}} = \left(I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}}\right)V_{DD}$$

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$$

4.4.2.3. Dynamic power

Dynamic power consists mostly of the switching power. The supply voltage VDD and frequency f are readily known by the designer. To estimate this power, one can consider each node of the circuit. The capacitance of the node is the sum of the gate, diffusion, and wire capacitances on the node. The effective capacitance of the node is its true capacitance multiplied by the activity factor. The switching power depends on the sum of the effective capacitances of all the nodes.

Dynamic power also includes a short-circuit power component caused by power rushing from VDD to GND when both the pullup and pulldown networks are partially ON while a transistor switches. This is normally less than 15% of the whole, so it can be conservatively estimated by adding 15% to the switching power. Switching power is consumed by delivering energy to charge a load capacitance, then dumping this energy to GND. Intuitively, one might expect that power could be saved by shuffling the energy around to where it is needed rather than just dumping it. Resonant circuits, and adiabatic charge-recovering circuits seek to achieve such a goal. Unfortunately, all of these techniques add complexity that detracts from the potential energy savings, and none have found more than niche application

4.4.2.4. Static power

Static power is consumed even when a chip is not switching. CMOS has replaced nMOS processes because contention current inherent to nMOS logic limited the number of transistors that could be integrated on one chip. Static CMOS gates have no contention current. Prior to the 90 nm node, leakage power was of concern primarily during sleep mode because it was negligible compared to dynamic power. In nanometer processes with low threshold voltages and thin gate oxides, leakage can account for as much as a third of total active power

4.5. Low Power SRAM

4.5.1. Power Gating technique:

Optimizing power in SRAM involves a multifaceted approach addressing capacitance, voltage, current, frequency, temperature, operational modes, transistor sizes, and leakage current. Achieving low-power SRAM designs is essential for applications demanding energy efficiency, extended battery life, and reduced heat dissipation.

Low-power SRAM designs often employ advanced techniques such as voltage scaling, adaptive body biasing, power gating, and dynamic voltage and frequency scaling. For

example, utilizing multi-threshold voltage transistors and implementing advanced power management strategies can significantly enhance the power efficiency of SRAM, ensuring its viability in energy-sensitive applications such as mobile devices and IoT devices. These techniques strike a balance between performance and power efficiency, making them instrumental in the design of modern, power-efficient SRAM architectures.

Integrating power gating techniques into the design of SRAM with a 6T architecture is a crucial step to reduce energy consumption in idle states. By diminishing energy consumption during inactive states, power gating not only optimizes performance but also extends battery life in energy-efficient applications.

Incorporating power gating transistors into specific blocks within SRAM, such as read and write circuits, helps disconnect power when they are not in use. This presents a significant opportunity to substantially reduce static power consumption, particularly in applications demanding extremely low energy consumption.

While integrating this technique requires careful design considerations and control, the results can strike an ideal balance between performance and energy consumption. This enhances the feasibility and appeal of 6T SRAM in systems with stringent energy requirements, ranging from mobile devices to IoT applications. Precisely controlling the timing of operation and inactivity of circuit blocks through power gating not only minimizes energy consumption but also ensures the safety and stability of data, enhancing the overall reliability of the global system.

Why do we need Power Gating?

A majority of the devices in the market nowadays have low power dissipation requirements, whether it is a battery-operated device or a device sensitive to heat dissipation.

In older technology nodes, the dynamic power dissipation used to be quite high compared to leakage power, but at lower technology nodes, the subthreshold leakage power is becoming quite comparable to dynamic power dissipation. Hence focusing on reducing leakage power in the design is as important as dynamic power reduction.

Reducing the supply voltage for the whole design or some subsystems helps to save dynamic power, while leakage power can be drastically reduced by turning off the power supply to the inactive parts of the design.

Power gating is very efficient at reducing the leakage power in the design and it is gaining a lot of popularity in mobile devices.

Since we are integrating a lot of functionality in modern-day System on Chip (SoC), there is a very high possibility that some of these functional blocks are inactive for long times during operation. This provides a lot of opportunities for power gating the design.

4.5.2. LP 6T-SRAM

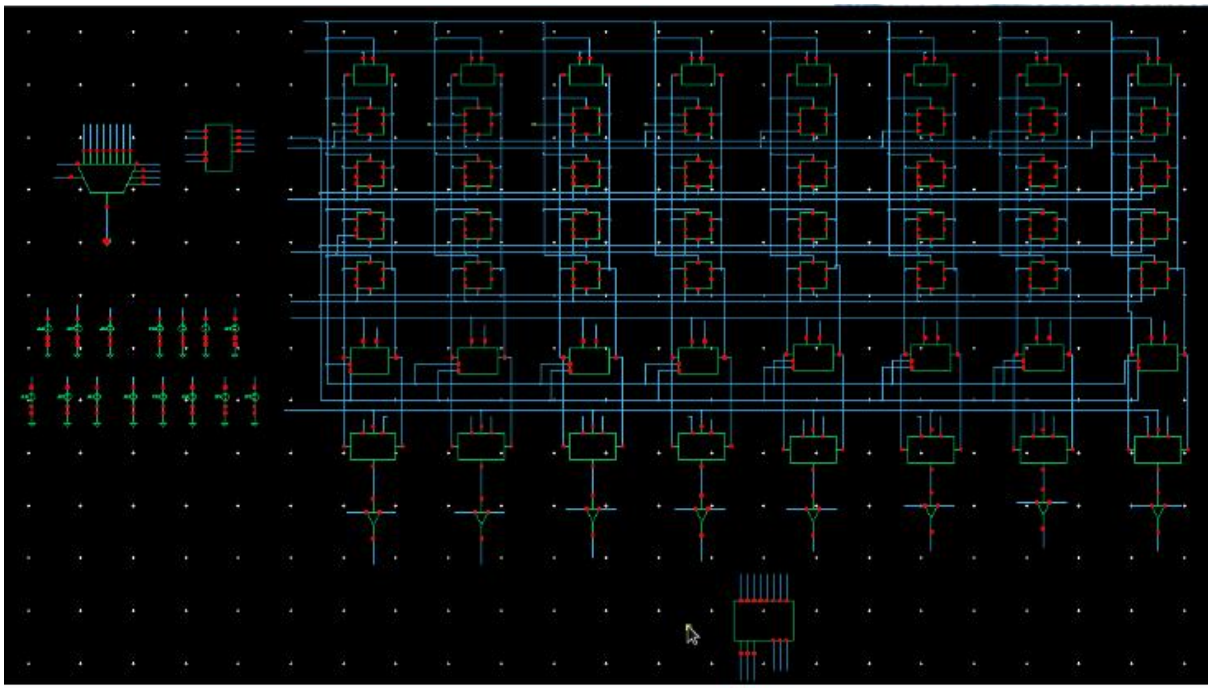

Figure 33: Schematic of 32-bit LP 6T-SRAM

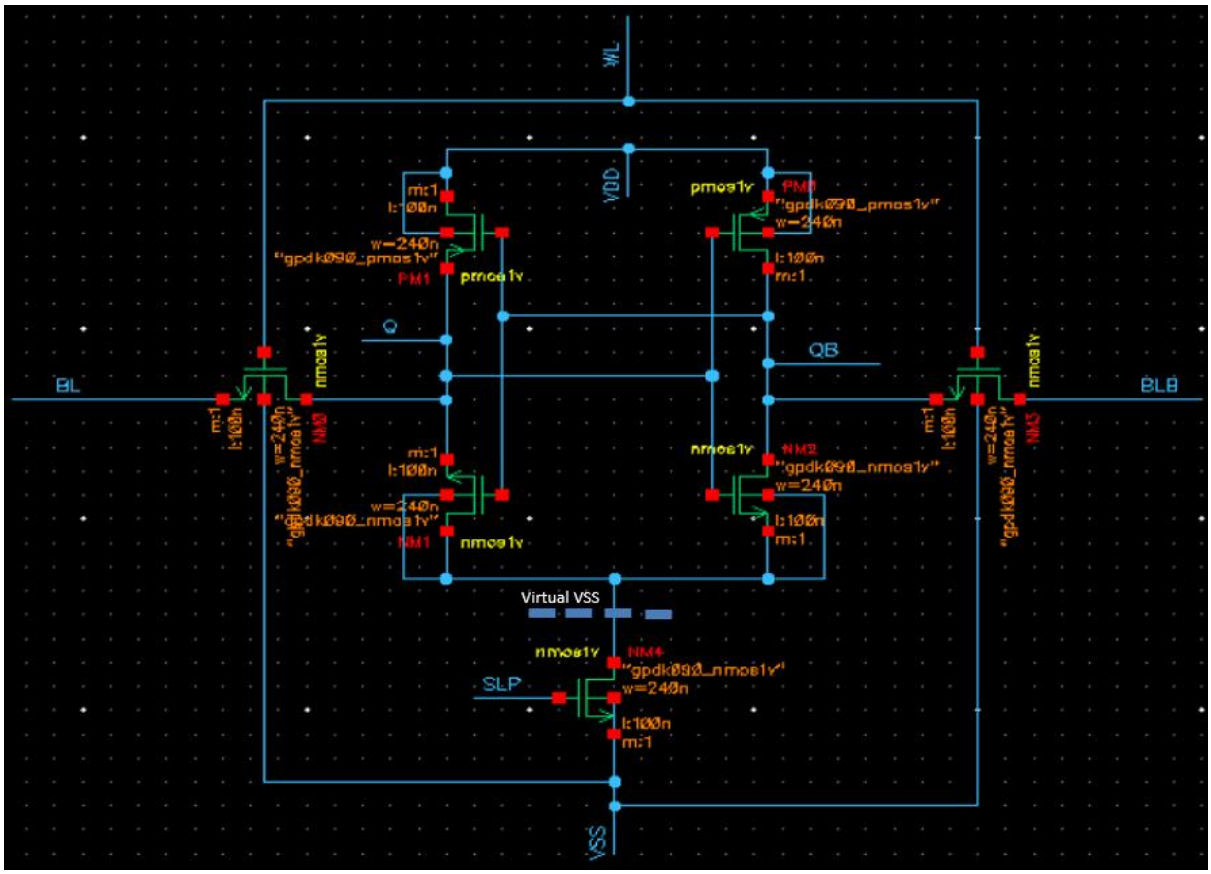

Figure 34: Schematic of LP 6T-SRAM

The operating principle of 32-bit LP 6T-SRAM:

Write operation:

When the Pre-charge (PRE) signal reaches 0, the Bitline and Bitline-bar lines of all memory cells are pulled up to VDD=1V to set the appropriate voltage level for the memory cells. When the Pre-charge signal has a value of 1, Row-decoder (Rn), Column-decoder (Cn) select the memory cell according to row position and column position. Data =0, PRE=1, R1=1, C1=1 – the first memory cell is selected and written to Bitline 1 (BL1) and Bitline-bar 1 (BLB1) – BL1=0, BLB1=1 and the data will be written to Storage-point (Q1=BL1=0). Then C1=0 and C2=1, the second memory cell (row 1 – column 2) is selected, BL2=0, BLB2=1, Q2=0.

Read operation:

When the Sense Enable (SE) signal has a value of 0, memory will not read the written data. When SE has a value of 1, allowing the memory to read data from the written memory cells, the output data (OUT) will have the same value as the value of Storage-point (Q), SE=1, Q=0, OUT=0

When the system is in an idle state and doesn't need SRAM operations, the power gating NMOS transistor is turned off.

This disconnects the SRAM cell from the power supply, isolating it and reducing power consumption. The additional NMOS transistor helps create a virtual ground when power gating is activated. This isolates the SRAM cell from the power supply and reduces leakage current, contributing to power savings.

V. THE MEASUREMENT RESULTS AND COMPARISONS.

5.1. Results

- Delay of I/O

In the scope of this research, we conducted delay measurements for I/O circuits, encompassing the Write Driver and Sense Amplifier, across different frequencies while maintaining a constant input voltage of 1V.The specific parameters are illustrated in the figure below:

Table 6: I/O Delay

I/O DELAY			
Voltage supply	**Frequency**	**Write Driver**	**Sense amplifier**
1 (V)	100M (Hz)	Tp= 75.51 (pS)	Tp = 138.55 (pS)
1 (V)	1G (Hz)	Tp = 82.487 (pS)	Tp = 140.8975 (pS)

A general observation is that the delay values are within an acceptable range. The delay time increases proportionally with its corresponding frequency.

The factors that can influence the delay may arise from efforts to meet timing constraints, capacitance effects, transistor switching times, the accurate operating frequency range of the circuit,...

- Power of I/O

In this section, we select several increasing frequencies ranging from 0.1 GHz to 10 GHz, with an operating voltage of 1V. The measured power corresponding to each case is presented in the table below:

Table 7: Voltage supply, Frequencies and power of I/O devices

Frequency	Voltage	Pre-charge	Write	Sense Amplifier
0.1 GHz	1V	0.017 μW	0.373 μW	6.75 μW
1 GHz	1V	0.1412 μW	3.335 μW	8.20 μW
10 GHz	1V	1.003 μW	30.25 μW	21.39 μW

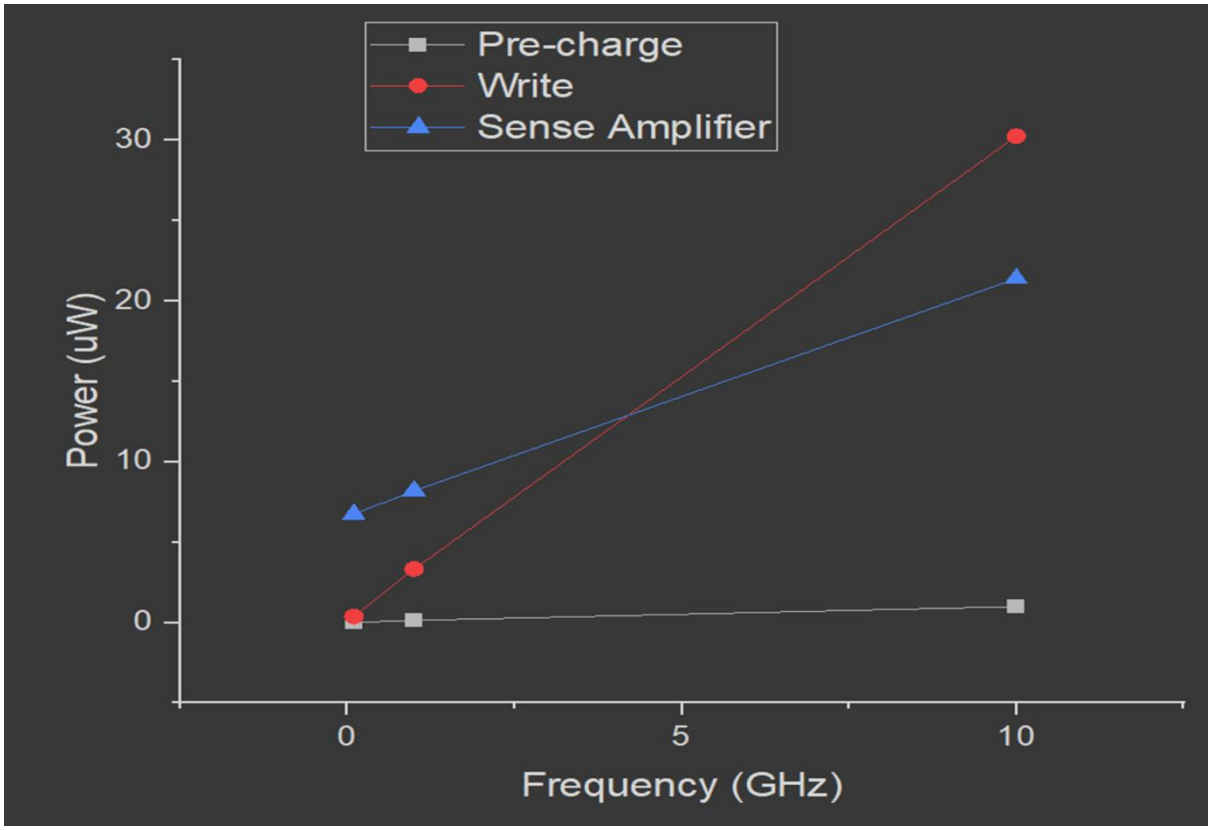

Figure 35: The comparison chart among I/O's power consumption

With a fixed input voltage and variations across different frequencies, discernible differences in power consumption emerge.

A notable observation is the higher power demand of the Sense Amplifier in comparison to the Write Driver & Precharge modules. This divergence may be attributed to increased power consumption within the logic gates of the Sense Amplifier circuit, surpassing that of the Write Driver & Precharge. Additionally, environmental factors such as temperature play a role in influencing both their operational efficiency and power requirements.

- **Delay of SRAM cell:**

Table 8: SRAM cells Delay

SRAM CELL DELAY				
Voltage supply	**Frequency**	**4T-SRAM cell**	**6T-SRAM cell**	**8T-SRAM cell**
1 (V)	100M (Hz)	Tp = 102.462 (pS)	Tp = 109.4777 (pS)	Tp(write): 89.4128 (pS) Tp(read): 58.23506 (pS)
1 (V)	1G (Hz)	Tp = 99.901 (pS)	Tp = 116.287 (pS)	Tp(write) = 116.1861 (pS) Tp(read): 10.68265 (pS)

Above is a table comparing the latency of SRAM memory cells with voltage levels of 1 (V) and at different frequencies (100MHz, 1GHz). Latency also affects a significant part of the working speed (write – read) of the memory cell.

- **Power of SRAM cell**

To measure the power of SRAM cells, we selected frequency milestones with progressively increasing values of 0.1 GHz, 1 GHz, and 10 GHz. The measured power corresponding to each case is listed in the table below:

Table 9: Voltage supply, Frequencies and power of SRAM cells

Frequency	Voltage	6T-SRAM cell	4T-SRAM cell	8T-SRAM cell	LP 6T-SRAM cell
0.1 GHz	1V	0.45 μW	0.423 μW	0.36 μW	0.302 μW
1 GHz	1V	4.01 μW	3.65 μW	3.54 μW	3.36 μW
10 GHz	1V	37.69 μW	32.39 μW	30.78 μW	29.62 μW

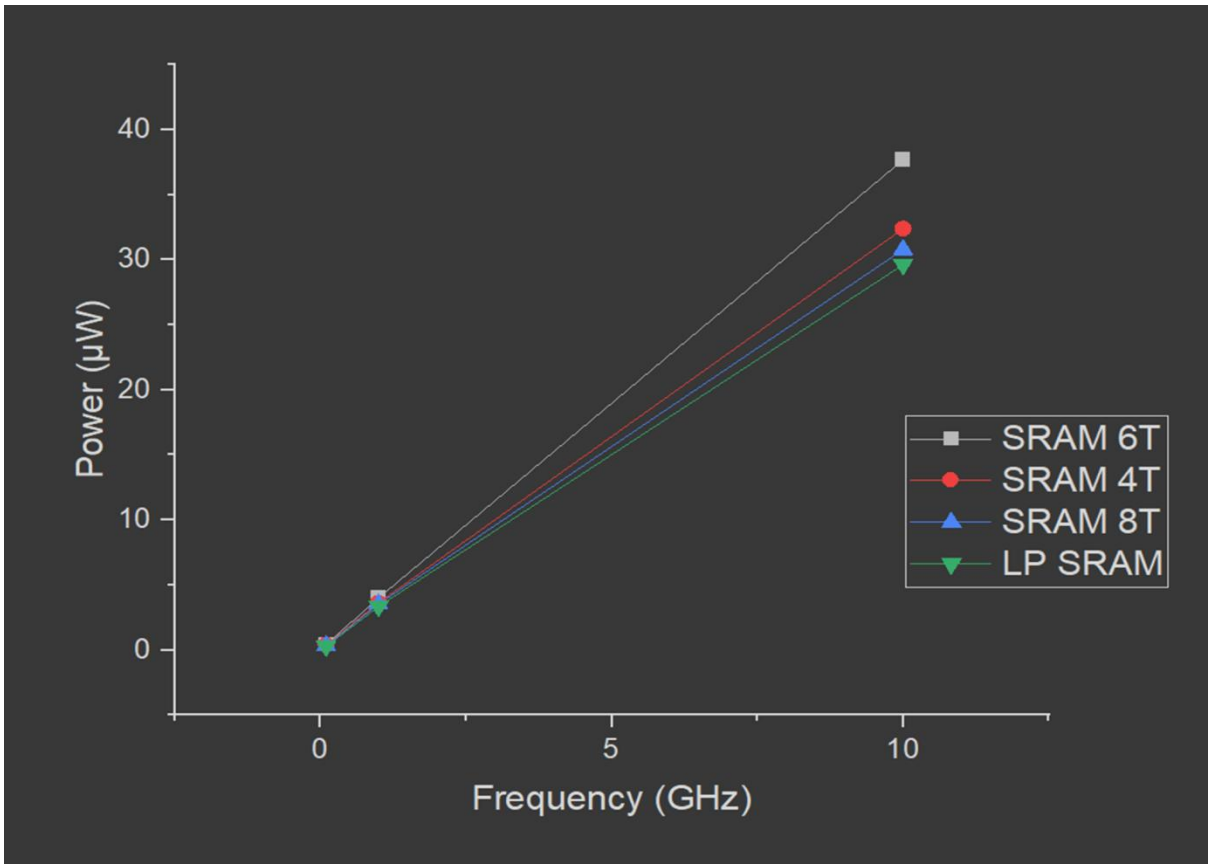

Figure 36: The comparison chart among SRAM cells power consumption

- **Power of 32-bit - SRAMs cell**

To assess the power characteristics of 32-bit SRAMs, we opted for incremental frequency benchmarks at 0.1 GHz, 1 GHz, and 10 GHz. The recorded power values for each scenario are detailed in the following table:

Table 10: Voltage supply, Frequencies and power of 32-bit SRAMs

Frequency	Voltage	6T-SRAM	4T-SRAM	8T-SRAM	LP 6T-SRAM
0.1 GHz	1V	113.7 μW	95.93 μW	76.73 μW	71.64 μW
1 GHz	1V	270 μW	224.4 μW	157.3 μW	127.6 μW
10 GHz	1V	798 μW	705 μW	493.5 μW	450.3 μW

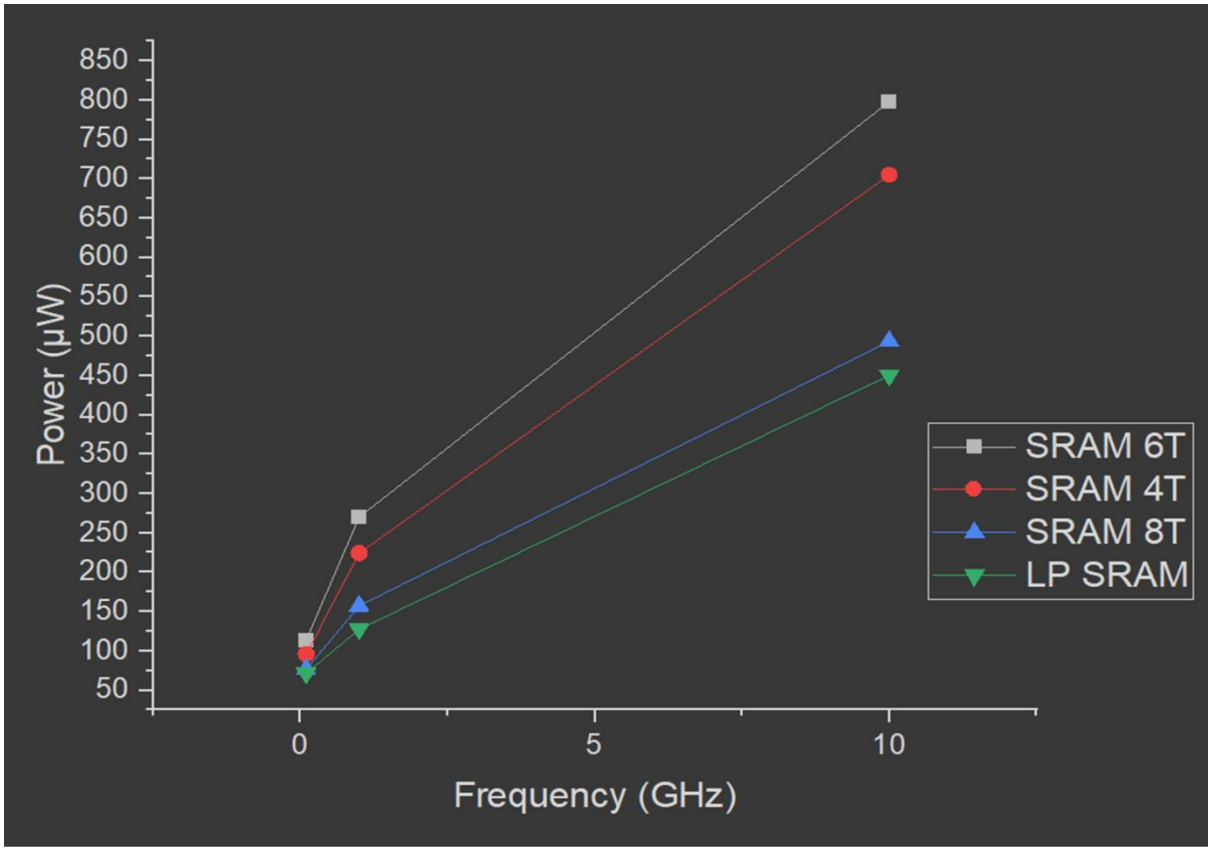

Figure 37: The comparison chart among 32-bit SRAMs power consumption

5.2. Comparison of power and delay between SRAM 8T and 6T.

In *Table 8*, we can see that with each increment in frequency values, the power of each type of SRAM increases. Particularly noteworthy is that, at each frequency level, the measured power of the 8T SRAM appears to be more optimized compared to the 6T SRAM.

Designing an 8T SRAM utilizing separate write and read data paths introduces a power dissimilarity, primarily observed during read operations in the 8T design. Prior to initiating a read operation, the bitlines are precharged to a high logic level. The parasitic capacitance discharge on the bitlines depends on the stored value in the SRAM cell being read. This contributes to a reduction in power consumption in the 8T design compared to the 6T design, particularly in terms of static power.

Signal Noise Margin (SNM):

In 8T SRAM, the separate read and write paths can enhance SNM by minimizing interference between the two operations, leading to improved stability during read cycles.

In contrast, 6T SRAM may experience more significant SNM challenges due to the shared read and write path s, potentially leading to higher susceptibility to noise-induced errors.

Design Area:

The 8T SRAM typically requires a larger design area compared to 6T SRAM due to the additional transistors and complexity introduced by the separate read and write paths. Larger design areas in 8T SRAM can contribute to higher dynamic and static power consumption, affecting the overall power efficiency.

Summary:

In summary, the overall power consumption of the 8T design is optimized compared to the 6T design due to the separate write/read path structure.The separate read and write paths in 8T SRAM, while potentially increasing design area, offer advantages in terms of SNM and stability during read operations.

Despite the larger design area, the optimized SNM and reduced susceptibility to noise in 8T SRAM can result in more efficient power utilization compared to 6T SRAM, especially in scenarios where noise considerations and stability are critical.

The overall power efficiency of 8T SRAM, taking into account SNM and design area trade-offs, can make it a favorable choice in applications prioritizing stability and reliability over a smaller footprint.

5.3. Comparison of power and delay between 6T-SRAM and LP 6T-SRAM.

As in Table 8, we can observe a significant difference in power consumption between 6T-SRAM and LP (Low-Power) 6T-SRAM. This discrepancy lies in their designs.

For LP 6T-SRAM, we employed power gating techniques with the aim of substantially reducing energy consumption during idle states. However, in terms of performance, LP 6T-SRAM may have lower efficiency compared to 6T-SRAM due to potential delays introduced by the activation and deactivation of power gating.

In the case of 6T-SRAM, it excels in high-performance operations for reading and writing data. Nevertheless, given the contemporary demand for low power consumption in devices, the substantial energy consumption during both active and idle states can pose a significant obstacle to meeting user requirements.

Summary:

In the context of increasing demands for both performance and energy efficiency, the comparison between LP (Low-Power) 6T-SRAM and 6T-SRAM becomes crucial. Upon examining Table 8, a notable difference in power consumption between these two SRAM types is evident.

LP 6T-SRAM is designed with the primary goal of reducing energy consumption, especially during idle states, through the use of power gating techniques. Despite potential delays associated with activating and deactivating this technique, LP 6T-SRAM remains a reliable choice for applications prioritizing energy efficiency.

However, 6T-SRAM maintains its advantage with high operational performance. Its ability to meet speed and performance requirements makes it a preferred choice for applications demanding robustness and flexibility.

By utilizing power gating and similar methods, we can develop devices with low power consumption while ensuring stable performance, presenting an opportunity to address diverse user needs in the future.

VI. USER DOCUMENT

A. TITLE

32-bit 6T, 4T, 8T, LP-SRAM: 4 rows, 8 columns

B. GENERAL DESCRIPTION

+ **Technical Specifications (Datasheet):**

Capacity: 32 bits

Bit Organization: 32-bit

+ **Basic Signals:**

Power Supply Voltage (VDD)

Ground (VSS)

Data Input Line (data)

Data Output Line (OUT)

Control Signals (Read/Write, Enable,...)

+ **User Guide:**

- **Read Data:**

Activate the read signal and wait for the access time.

Data is returned on the DOUT[0] line.

- **Write Data:**

Activate the write signal and provide data on the DIN[0] line.

Wait for the necessary write time.

+ **Adjustment Tables and Operating Conditions:**

Supply Voltage: 1 V

Operating Temperature: 27°C

+ **Power Gating Technology:**

Adding NMOS to VSS (Power GND):

When not in use, the NMOS is activated to create a virtual ground, cutting off the power supply to the SRAM, reducing energy consumption.

VII. REFERENCE

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VIII. APPENDIX fr4

IX. MEMBER CONTRIBUTIONS

We would like to thank Doctor Pham Van Khoa for his support on the group's project.
The distribution of credit for each part of group is given below:

Hardware Simulation

+ I/O:

- Pre-charge: Đỗ Mạnh Dũng
- Write driver: Phạm Trần Minh
- Sense Amplifier: Trần long
- Row/Column decoder: Đặng Trung Nghĩa

+ SRAM:

- SRAM 4T: Phạm Trần Minh
- SRAM 6T: Trần long
- SRAM 8T: Đỗ Mạnh Dũng
- LP SRAM: Đặng Trung Nghĩa

PROJECT

ABSTRACT:

Trần Long: 100%

INTRODUCTION

Đỗ Mạnh Dũng: 100%

SPECIFICATION

Phạm Trần Minh: 100%

DESIGN

Trần Long: 25%
Phạm Trần Minh: 25%
Đặng Trung Nghĩa: 25%
Đỗ Mạnh Dũng: 25%

THE MEASUREMENT RESULTS AND COMPARISONS.

Trần Long: 25%
Phạm Trần Minh: 25%
Đặng Trung Nghĩa: 25%
Đỗ Mạnh Dũng: 25%

USER DOCUMENT

Đặng Trung Nghĩa: 100%