# **Dylan-Matthew Garza**

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# **Objective**

Computer Engineering student graduating in December 2024 seeking an engineering role in embedded Linux development, and Linux systems development.

## **Skills Summary**

with Yocto Project

o Toolchains, SDKs, BSPs • Systems Programming: C/C++, Assembly, Rust

Scripting: POSIX/bash/python

o Git and command line interface

Intel's PinTool

• Full-stack development: Web • Linux server administration

Arm

development for  $\circ \mu C$ 

Cortex-M4

•μC peripheral: CAN-FD, DRAM, I2C, UART, STM32MP1, SPI

• Embedded Linux development • Dynamic binary analysis with • Object-Oriented Programming

Security: PKI, SSL/TLS

### **Experience**

#### **ZF Group, Research and Development Intern**

August 2024 - Present

- · Design and implement a device with capabilities to test different vehicle components to determine if specifications are met
- · Streamline device testing and test data handling and interpretation
- · Using Yocto Project to build a custom embedded linux image for the Arm Cortex-A7 architecture
- · Designing an interactive web application for testers implemented fully in Web Assembly with the Yew framework in Rust
- · Designing a Rust backend application to handle HTTP request and communicate to an onboard microcontroller (Arm Cortex M4) using interprocess communication (IPC) through the OpenAMP framework

#### Resideo, Embedded Linux Engineer Intern

May 2022 - August 2022

- · Successfully integrated debuginfod, a file server, into CI/CD pipeline in order to make the debugging workflow and analyzing core files of embedded Linux images simpler and more efficient.
- · Developed shell/bash scripts to automate tasks
- · Learned about the Yocto Project to develop custom reproduceable embedded Linux images
- · Wrote technical documentation and gave a presentation on how to utilize tools
- · Learned the principles of agile develop to improve software velocity, reduce bug count and decrease time to market

#### eMatrix Energy Systems, Assembly Technician

May 2021 - August 2021

- Constructed and tested various components of battery packs and battery cells
- Worked with engineers on prototyping new designs of battery packs
- · Followed safetey procedures to ensure a safe working environment

### **Projects**

#### **Custom Status Bar Development for Linux Desktop Environment**

July 2024 - Present

- $\cdot \ Developed\ a\ fully\ custom\ status\ bar\ utilizing\ Eww\ Widgets\ (standalone\ widget\ system\ implemented\ in\ Rust)$  for the Hyprland Wayland\ Compositor
- $\cdot \ Dynamic\ workspace\ display\ implemented\ using\ C\ through\ UNIX\ sockets, interprocess\ communication\ and\ signal\ handling$
- · System statuses fetched real-time using compiled C and Rust binaries include SSID, Wi-Fi connectivity, IPv4 address, RAM usage, battery capacity, and time/date
- · Styled in GTK SCSS
- · Link to Project Github Repository

#### Simulation of Fixed-length Vector Architecture Superpipline

November 2023 - December 2023

- · Simulated a pipeline for a vector processor in fully Object-Oriented C++
- · Utilized Intel's PinTool to dynamically profile binary for vector instructions (AVX/AVX2) instructions to generate a custom trace file
- · Supported Variable single-instruction multiple-data (SIMD) lanes
- · Implemented 6-stage pipeline (fetch, decode, issue, execute, commit)
- · Out-of-order execution through Tomasulo's algorithm (method of dynamic instruction scheduling and out-of-order execution) with a fixed issue width

## **Dynamic Conveyor Belt Positioning System**

April 2023

- · Designed and implemented a system utilizing an STM32 microcontroller
- · Move an object on a conveyor belt from start to end position
- · Using peripherals such as LED indicator, IR emitter, Ohm speaker, and relay switch
- · H-Bridge motor driver module, and motor encoder module
- · With specific operations and frequency/duty cycle adjustments based on input signals

#### **Custom 10-bit CPU**

January 2023 - April 2023

- · Designed a custom 10-bit ISA and simulated a 5 stage pipelined CPU using the Verilog HDL
- · CPU was implemented with two-level memory hierarchy with cache and RAM.
- $\cdot \ Branch\ predictor\ was\ also\ implemented\ as\ a\ 2-bit\ predictor\ with\ a\ branch\ history\ register\ and\ pattern\ history\ table$
- · Wrote machine code for bubble sort, string copy, and multiply programs

#### **Certifications**

#### LFD 460:Embedded Linux Developement with Yocto Project

August 2022

Expected: December 2024

Gained expertise in developing custom embedded Linux systems through the Yocto Project, encompassing advanced tool usage and IDE integration for efficient embedded product development.

Credly Badge | Linux Foundation Certificate

#### Education

## B.S. in Computer Engineering and Minor in Mathematics

Western Michigan University - Kalamazoo, Michigan