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Three dimensional memristor-based neuromorphic computing system and its application to cloud robotics☆

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ABSTRACT

Neuromorphic computing based on three-dimensional inetgraed circuits (3D-NCs) offers a novel hardware implementation of neuromorphic computing, and provides high device density, massively parallel signal processing capability, low power consumption, and direct analog signal processing capability. In this paper, by replacing conventional CPUs based on Von Neumann architecture with 3D-NCs, a novel neuromorphic computing based cloud robotics (NC-robotics) system is proposed, which is constructed by 1) cloud server center using 3D-NCs as computing units, 2) neuromorphic robotics based on neural network control technology. Besides the benefits of normal Cloud Robotics platform, this NC- Robotics system has more advantages on massive parallel-computing, analog signals processing, and lower power consumption. In order to implement this NC––Robotics system, a novel 3D-NCs architecture combining vertical RRAM structure is investigated and its concise equivalent circuit model is created, evaluated, and analyzed through SPICE simulations.

1. Introduction

The concept of cloud robotics has been conducted for many years in various applications, such as unmanned aerial vehicles (UAVs), warehouse robotics, home automation systems, self-driving vehicle [1], etc. Unlike traditional off-network robotics with isolated data processing that cannot communicate with each other, the robotics in cloud possess the capability of sensing real world data/signals and updating them to cloud side server for further processing and computing. The topology of cloud robotics system is illustrated in Fig. 1. With the assistance of powerful computational resources on the server side, robotics in the cloud can share knowledge/information, learn from each other, access global library of images, maps and object data centers, and accomplish tasks collaboratively.

For now, the computing units in both server and robotic sides are designed in conversational CPUs, which is based on Von Neumann architecture. This type of architecture separates central process unit (CPU) and memory, as exemplified in Fig. 2. The data communication between the CPU and memory is through the parallel data bus whereby the speed of the data bus dictates the system achievable data rate. As the data rate keeps elevating, the parallel bus ultimately becomes the energetic and speed bottleneck. The robotics created by using this type of CPU as computing unit has been improving the productivity and quality of our society for many years. However, the abilities of these robotics pales comparing with the animals and

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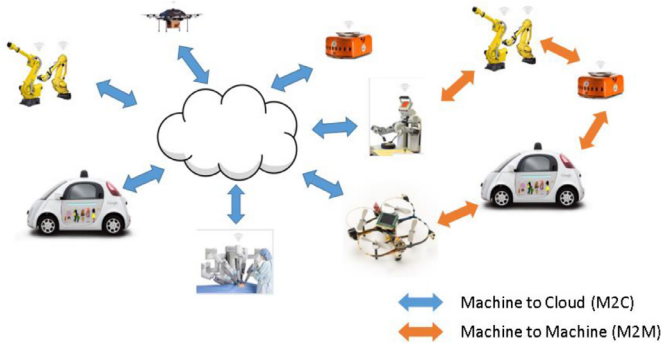

Fig. 1. Cloud robotics concept diagram.

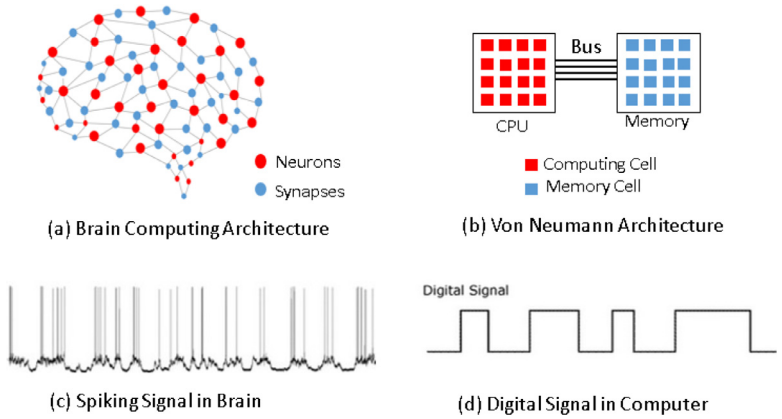

Fig. 2. Comparison between brains computing system with conventional Von Neumann computing system. The bus in traditional Von Neumann is energetic and speed bottleneck.

insects, which processes signals using neurons as the biological computing units. These biological organisms survive in dynamic environments for centuries and display extraordinary flexibility and adaptability that all artificial intelligent system lack for now. Moreover, the computing system based on the neural network also can efficiently control the body to make rapid and coordinated response corresponding to the changes from the physical world. For example, birds can constantly adjust the flying height and direction to avoid obstacles through visionary signals captured by their eyes. These visionary analogic signals are processed and analyzed in their several grams brain with extremely low power consumption.

These impressive capabilities of computing and controlling capabilities come from the unique nervous system structure macroscopically and the signal encoding methodology microscopically. The nervous system does not only exist within the brain, but also extends throughout the whole body as illustrated in Fig. 3. This neural network based response/control system inspired the dedicated researchers to develop robotics with the neural network control system [2] and to propose the neuromorphic computing concept [3], as demonstrated in Fig. 4.

Although many neuromorphic ICs have been applied to robotics field, there is still a lack of cloud server assembled by neuromorphic ICs connecting another neuromorphic robotics. In this paper, a new purely neuromorphic computing based cloud robotics system is proposed, as illustrated in Fig. 5. This novel Neuromorphic Cloud Robotics (NC-Robotics) system replaces conventional computing units (CPU + Memory) with neuromorphic ICs on both robotics and server sides. Each neuromorphic robot in the cloud network can seamlessly connect to the neuromorphic server for further analog signal processing.

In order to build neuromorphic cloud server, more powerful and efficient neuromorphic IC architecture and technology need to be investigated. Table 1 summarizes the existing state-of-art fabricated “analog” and “digital” neuromorphic computing chips. To the best of our knowledge, all reported fabricated neuromorphic chips employ traditional two-dimensional integrated circuit (2D-ICs) design methodology and complementary metal–oxide–semiconductor (CMOS) technology.

Although the 2D-ICs listed in Table 1 offer more neuromorphic computational capabilities than the conventional ICs using Von Neumann architecture, their inevitably inherent limitations hinder them to have a compelling performance close to the human brain. To be more specific, with the number of neurons increasing, 2D neuron placement becomes incapable due to its routing density increasing linearly with the number of the connections. In order to satisfy the desired connections, longer routing and larger die area are the inevitable consequences, hence larger power and cost consumptions as a result. Furthermore, to a certain extent, 2D connections become prohibitive longer, which counterpoises the benefit offered by neuromorphic computing. For example, in Table 1, each neuron of TrueNorth chip only connects 244 synapses. The same

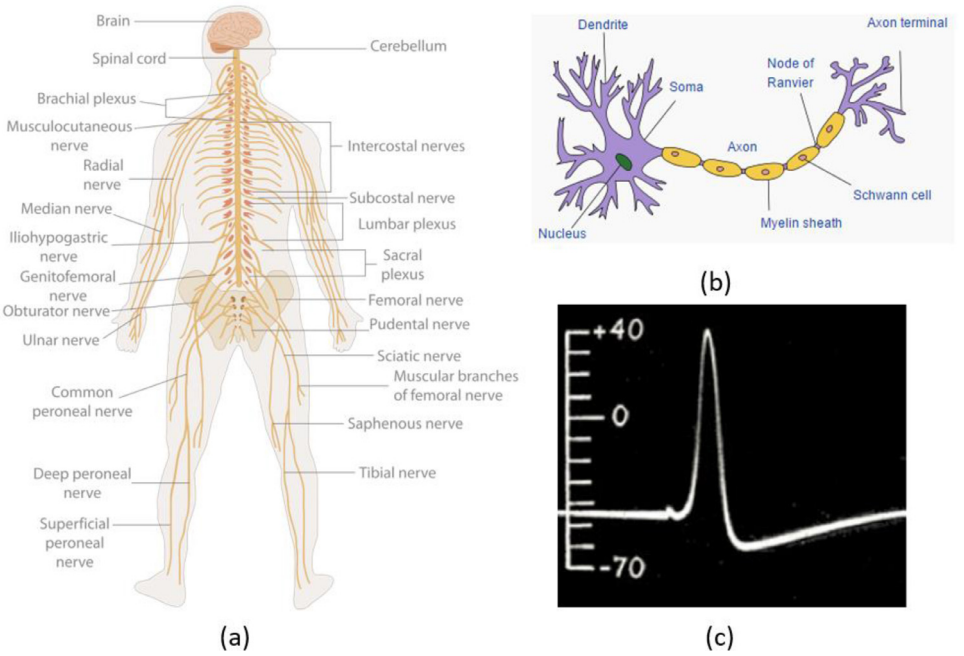

Fig. 3. (a) Human neuron system; (b) neuron structure; (c) action neural potential recorded by Hodgkin and Huxley from a squid axon [4].

Table 1
Comparison of power density, neuron density, synapse density, and neuron connection degree.

	TrueNorth [6]	ROLLs [7]	Neurogrid [7,8]	HICANN Chip/ BrainScaleS [7,9]	SpiNNaker [7,10,11]	Human brain [7]
Neurons	1048,576	256	65,535	511	20,833	20 Billion
Synapses	256 million	128,000	N/A	113,636	20,833,333	200 Trillion
Area/Volume	430 mm^2	51.4 mm^2	168 mm^2	50 mm^2	102 mm^2	1130 cm3
Neuron Density	2438.55 per mm^2	5 mm^2	390 per mm^2	10 per mm^2	204 per mm^2	17,699 per mm^3
Synapses Density	0.595 million per mm^2	2490	N/A	2272 per mm^2	204,248 per mm^2	177 million per mm^3
Ratio of synapses to neurons	244	500	N/A	222	1000	10,000
Power density	0.15 mW/ mm^2	0.078 mW/ mm^2	18 mW/ mm^2	57 mW/ mm^2	0.012 mW/ mm^2	0.0177 mW/ mm^3

parameter in HICANN chip is 222. The lower connectivity of system would further reduce its parallel-processing capability. A traditional SRAM [6] is used in the synapse implementation, which is volatile and large device, typically at 100–150 F^2 level, where F is the minimum feature size.

To overcome the limitations in 2D neuromorphic computing ICs, we propose a 3D Neuromorphic IC architecture with less connection wiring length and lower power consumption, which uses the vertical monolithic interlayer vias (MIVs) and nanowires to form resistive random access memory (V-RRAM) serving as a vertical synaptic array. An equivalent circuit model of the vertical synaptic array using V-RRAM is created whereby the parameters in the model have calculated analytically. The electrical characteristics of the vertical synaptic array are evaluated using the equivalent circuit model in SPICE simulation.

This paper is organized as follows, Section 2 introduces the Analog-to-Spiking Converter (ASC) design, Section 3 discusses the 3D neuromorphic IC architecture we proposed, Section 4 illustrates 3D synaptic array structure, Section 5 describes 3D synaptic array modeling, Section 6 presents some results and discussions, and Section 7 draws some conclusions.

2. Analog-to-Spiking converter design

In the nervous system, the analog information received from the physical world is encoded into spiking sequence signals by sensory neurons. After this encoding process, the spiking signals are computed by more complex and powerful nervous system (brain or spine). In order to mimic the capability of sensing analog signals, an Analog-to-Spiking Converter, which can convert analog signals to spiking signals directly, is proposed. The spiking firing rate highly corresponds to the input analog signal magnitude. The diagram of ASC and schematic design are shown in Figs. 6 and 7, respectively.

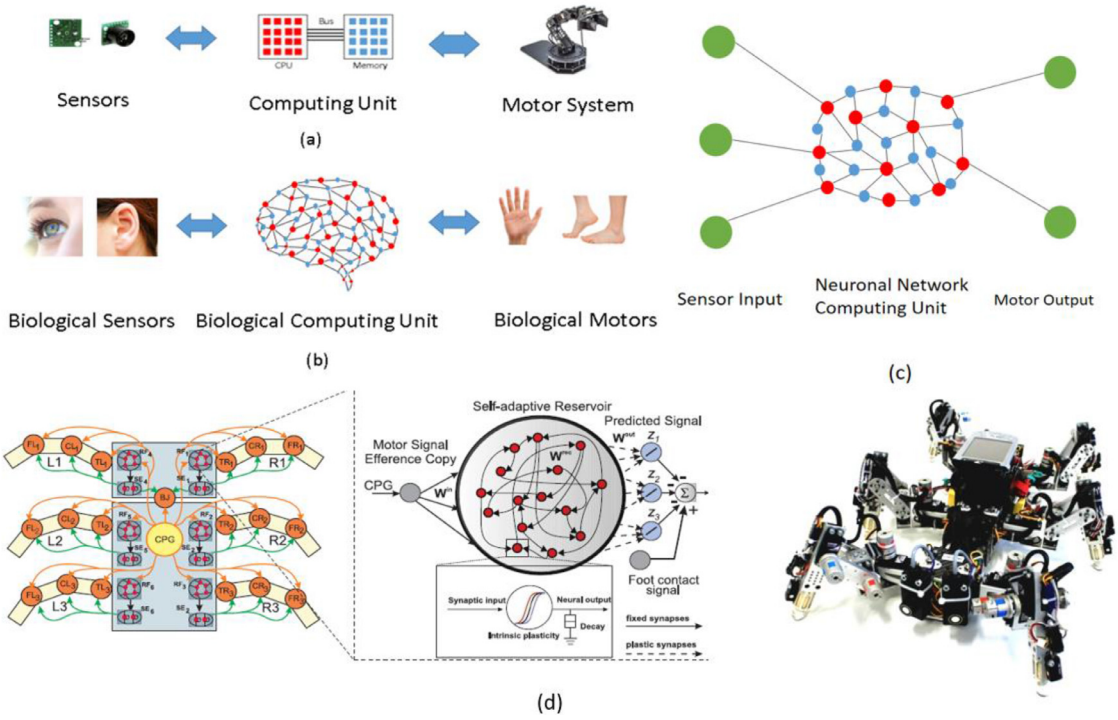

Fig. 4. (a) Conventional robot system including sensors, center computing units (CPUs), and motor system; (b) biology body system including biological sensors, biological computing unit and biological motors; (c) neural network robot control system; (d) neural mechanisms implemented on the bio-inspired hexapod robot AMOS2 [5].

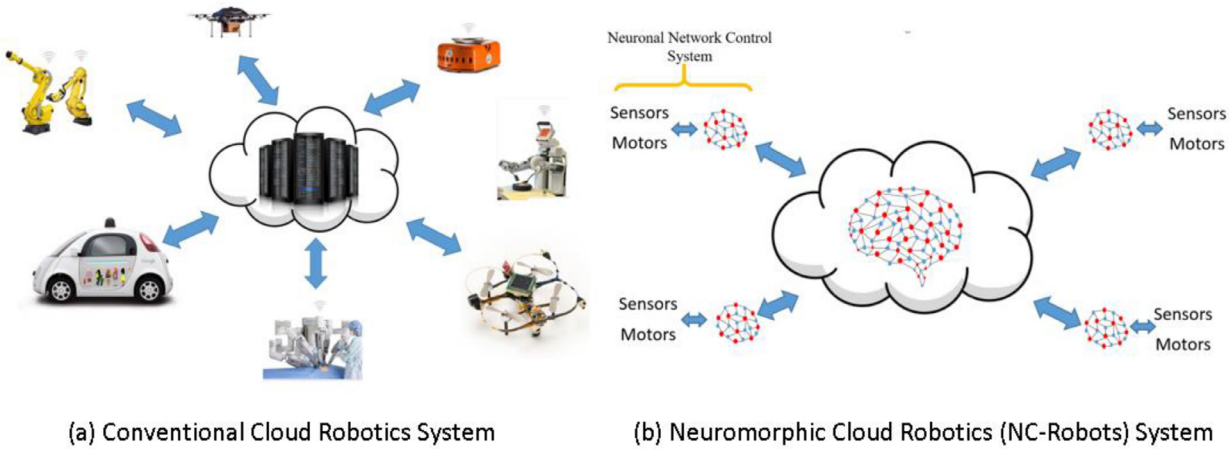

Fig. 5. Evolution from conventional cloud robotics system to neural network based cloud robotics system.

This design comprises three parts:

- Five stage current starved ring voltage-controlled oscillator (VCO)
- Controller
- Integrate and fire neuron circuit model [12]

In this design, an analog input signal is used to control the oscillating frequency of a current starved VCO as illustrated in Fig. 7. The output oscillating signals will input to an out-of-phase switcher implemented by a POMS and an NMOS as controlling signal. The out-of-phase switcher will control the charging and discharging behaviors of in Integrate and fire neuron model. The simulation result of spiking signal is shown in Figs. 9 and 10.

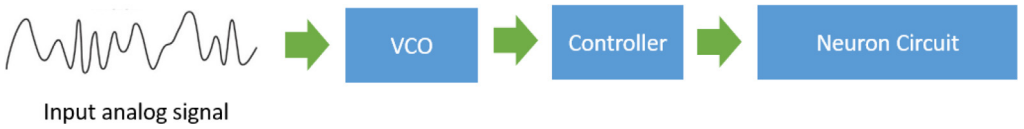

Fig. 6. Diagram of ASC design.

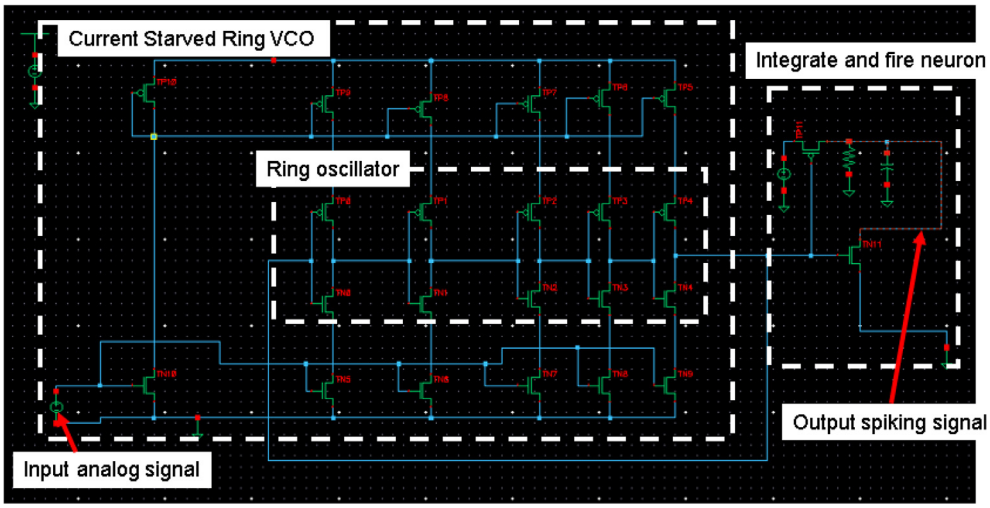

Fig. 7. Analog-to-Spiking converter schematic design.

3. 3D neuromorphic computing IC architecture

Fig. 11 depicts the novel 3D Neuromorphic IC (3D-NC) architecture that we propose. In this structure, neurons and memristor-based (RRAM) synaptic array are stacked vertically.

By enabling the third-dimension interconnection [13], monolithic 3D integration and RRAM in neuromorphic ICs offer the following benefits:

1. Increase the interconnection density, reduce the critical path length by 3× [14], provide scalability, and decrease power consumption by 50% and minify the die area by 35% [15];
2. Provide a high-complexity, high-connectivity, and massively parallel-processing circuital system that can accommodate highly demanding computational tasks [16];
3. RRAM is a new two-terminal nanoscale nonvolatile device with the conductance can be gradually modified by controlling charge or flux through it. Moreover, as a nonvolatile device, it does not need the power to maintain the weight value;
4. Address the 2D neuron routing congestion problem, thereby increasing interconnectivity and scalability of the NC network and reducing the critical-path lengths;
5. Reproduce the biophysical processes occurring in the human brain. The proposed design will use a layered 3D structure that employs analogs for biological components to emulate the layered structure used for information processing in the human retina and visual cortex;
6. Provide a high-complexity, high-connectivity, and massively parallel-processing circuital system that can accommodate highly demanding computational tasks [17].

4. 3D synaptic array structure

In general, there are two types of 3D RRAM structures that can be used as 3D synaptic arrays: Horizontal RRAM (H-RRAM) and vertical RRAM (V-RRAM) [18-21], as shown in Figs. 12 and 13, respectively.

In both structures, the device sizes can be $4F^2/n$, where n is the number of the stacked layers and F is the minimal lithographic feather size dictated by technology node. The number of critical lithography masks for H-RRAM structure increases linearly with increasing number of stacked layers while the number of masks for V-RRAM is relatively independent of the stacking number [19,20]. The cost-per-bit comparison between V-RRAM and H-RRAM is shown in Fig. 14. Apparently, V-RRAM is more appealing than H-RRAM is in term of cost. With increasing number of stacked layers, V-RRAM becomes even more cost-efficient [18].

Due to its bit-cost advantage, we select V-RRAM as synaptic array implementation structure. The specific 3D-NC architecture diagram is illustrated in both Figs. 15 and 16. Note the TEM figure in Fig. 15 is cited from [22].

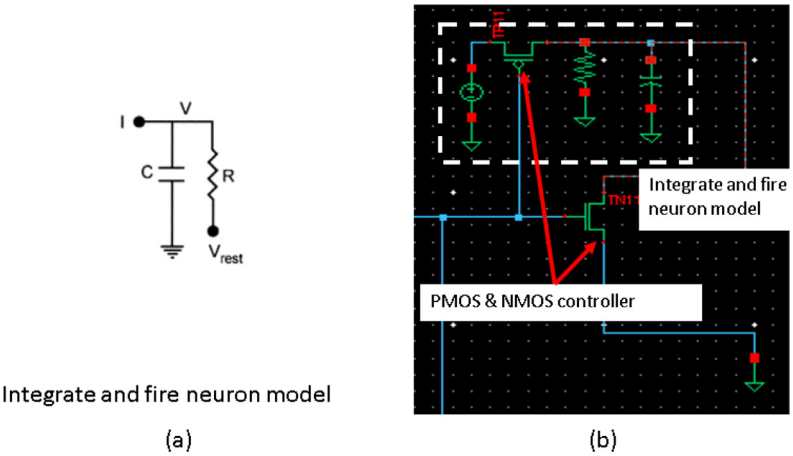

Fig. 8. (a) Integrate and fire neuron model [12]. (b) I&F neuron model implementation: a PMOS & NMOS is used for controlling neuron firing event.

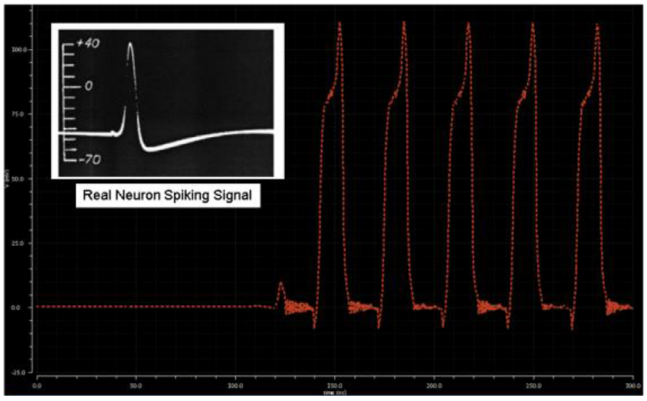

Fig. 9. Spiking signal simulation result. The real neuron spiking signal image comes from [4].

In this architecture, each synapse cell is defined by the intersection between the horizontal nanowire and a vertical metal electrode. The selective device connecting neuron and pillar electrode can be vertical transistor. This architecture uses analog spiking signal as the coding format. The spiking signal received by each neuron through the vertical pillar electrodes is the sum of voltage/current spiking signals from nanowires in different layers as shown in Fig. 17, where R_1 to R_n represent resistances of nanowires and R_{via}represents the resistance of the vertical electrode.

The controller is used for Address Event Representation communication protocol implementation, which also can be employed into NC-Robotics system. The cloud robotics system with chips based on this novel architecture potentially can process analog signal directly without Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC), resulting in lower power consumption and faster response time.

Another benefit of neural network robot is that it potentially can directly process analog signal without transforming them to digital format, resulting in a fast response time. Additionally, weights of synapses have been proven to relate to memory storage and learning process. The dynamic synaptic weight value in neuromorphic computing system could form an adaptive network with respect to real environment thereby creating a cognitive robot [2].

5. 3D vertical synaptic array structure modeling

In order to analyze the electrical characteristics of the 3D synaptic array with the proposed architecture, a 3D circuit physical structure shown in Figs. 8 and 9 is created. The structure includes eight RRAM synapse cells, four nanowires and four MIVs, which serve as both the pillar electrodes and the vertical connections between controller and synapses in different layers as illustrated in Fig. 16. The synaptic cell is defined at the intersection between nanowire and MIV.

For simplicity, The RRAM cells in the circuit are treated as resistors: the lower resistance state (LRS) is 2 kΩ, and the high resistance state (HRS) is 3 MΩ. The pillar electrode and nanowire materials are modeled as platinum.

Due to the low operating frequency of neuromorphic IC [6], only the resistance and capacitance in the model are considered in this study. The model parameters are listed in Table 2.

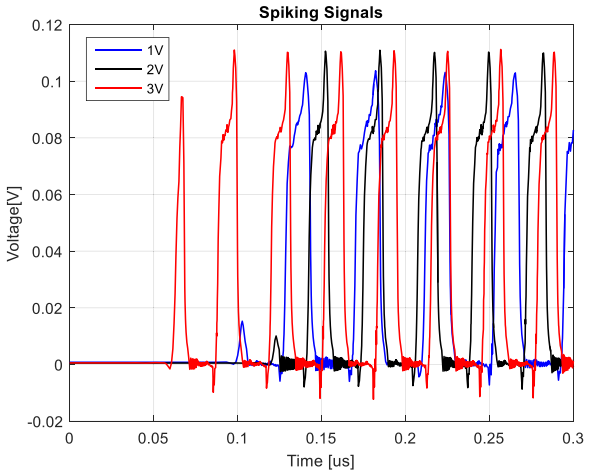

Fig. 10. Spiking signals with respect to the various stimulus voltage levels.

Table 2
Model parameters.

Parameters	Description	Explored values
H	Horizontal distance of nanowires	30 nm
MIV_s	Distance between MIVs	70 nm
MIV_d	MIV diameter	30 nm
w_w	Nanowire width	50 nm
w_h	Nanowire height	20 nm
w_s	Vertical distance of nanowires	20 nm
t_{ox}	Thickness of RRAM material	5 nm

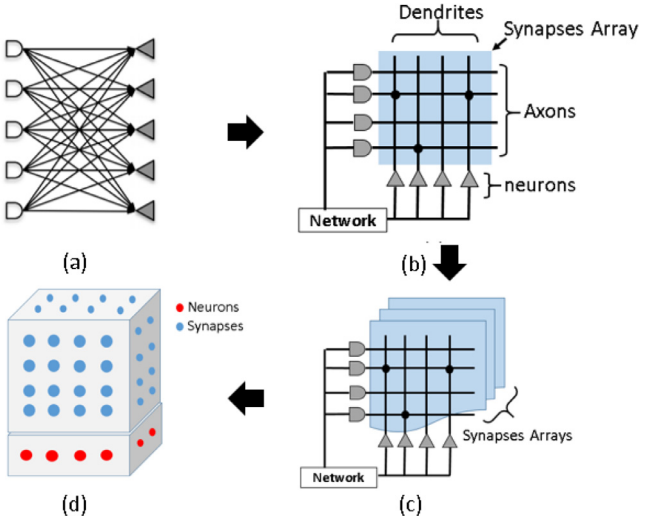

Fig. 11. Evolution of neuromorphic IC architecture: from 2D flatly to 3D vertically. (a) Neuron network; (b) 2D neuromorphic IC architecture; (c) 3D Neuromorphic IC architecture; (d) 3D Neuromorphic IC architecture Diagram.

The equivalent circuit model shown in Fig. 20 describes the electrical connections of the proposed structure. In this equivalent circuit model, the connection of the neurons on the CMOS substrate are designated as Port 1 to Port 4 while the link realized by the nanowire are represented by the path from Port 5 to Port 12.

5.1. Resistance calculation

In the SPICE model, there are two resistances need to be calculated:

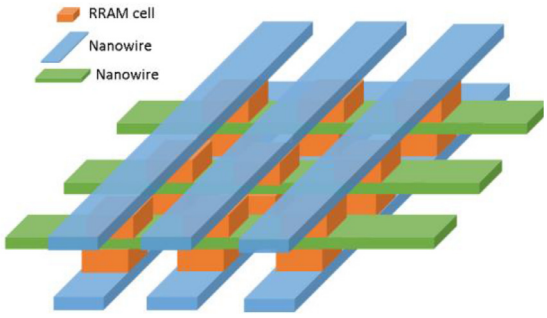

Fig. 12. Horizontal RRAM structure.

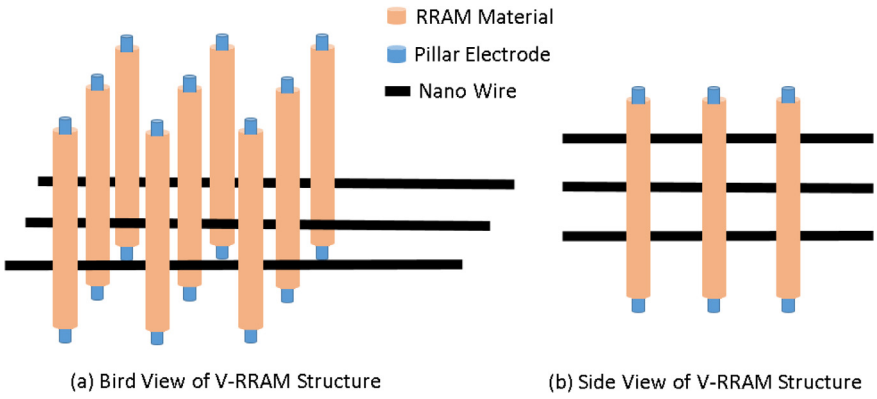

Fig. 13. Vertical RRAM structure.

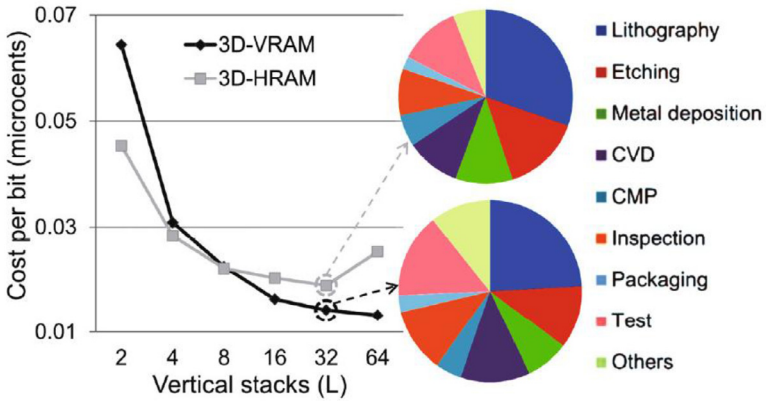

Fig. 14. Cost breakdown for per bit projections.

(a) MIV (pillar electrode) resistance, MIV is short for monolithic inter-layer via, a new 3D-IC stacking technology can further decrease the package area;
(b) Nanowire resistance.

First, the MIVs is modeled as cylinder geometry and its resistance can be calculated using $R = \rho \times l/A$. The calculated value is 4.49 Ω.

Secondly, for the nanowire calculation, it is partitioned into two parts: Region A and Region B as shown in Fig. 19. In Region A, the resistance of the nanowire is 6.17 Ω. In the Region B, the current mainly flows in the platinum part due to the relatively low conductivity of RRAM even at low resistance state (2kΩ). The outer two resistors R2_1 and R2_2 represent the Platinum portion of the nanowire in Region B as presented in Fig. 21. The resistance R_x of the Shape X illustrated in Fig. 11 is calculated using Eq. (1), where h is the nanowire height. The result of R_x is 12 Ω.

$$R_x = \int_0^L \rho \frac{1}{h(s - \sqrt{r^2 - x^2})} dx \tag{1}$$

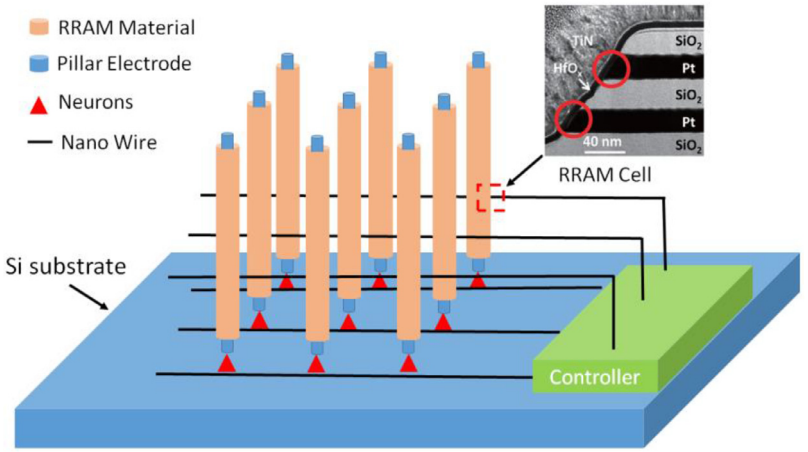

Fig. 15. Proposed new 3D neuromorphic IC (3D-NC) architecture using vertical RRAM as synaptic array.

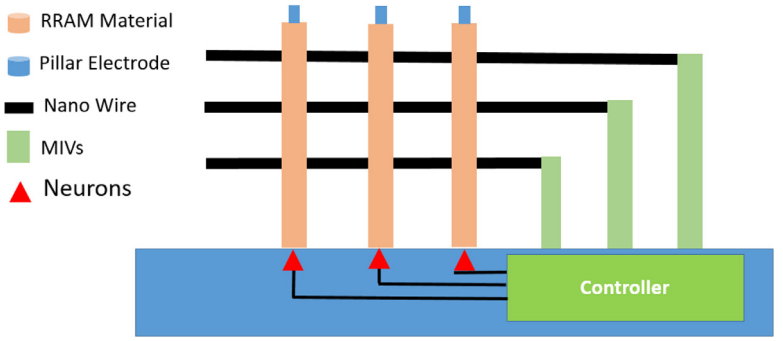

Fig. 16. Side view of new 3D neuromorphic IC architecture.

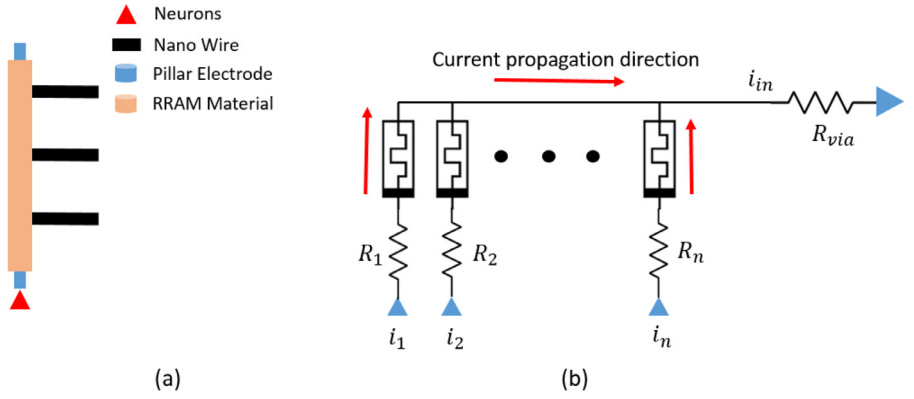

Fig. 17. Neuron receives current from different layers.

5.2. Capacitances calculation

In this study, all eight RRAM synapse cells are modeled at LRS. The Wire 1 and Wire 2 are electrically connected, so are Wire 3 and Wire 4. Totally, there are four capacitances under this state. Two capacitors are formed by the nanowire pairs while other two are induced by MIVs pairs.

The capacitances between nanowires are calculated using the parallel-plate capacitance equation. The capacitance of each nanowire pair is 1.84e−5 pF.

The capacitance between MIVs is calculated using Eq. (2) [23]:

$$\frac{\pi \epsilon}{\cosh^{-1}(D/2a)} \tag{2}$$

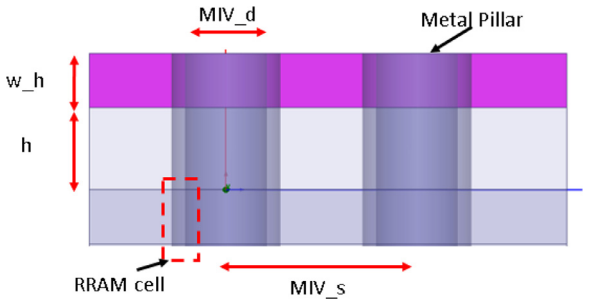

Fig. 18. Side view of model.

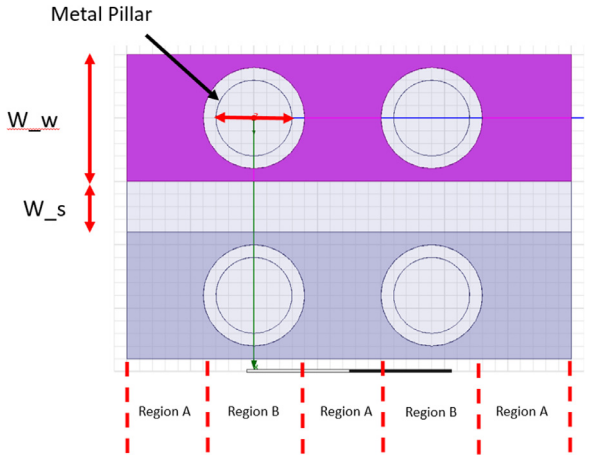

Fig. 19. Top view of the model.

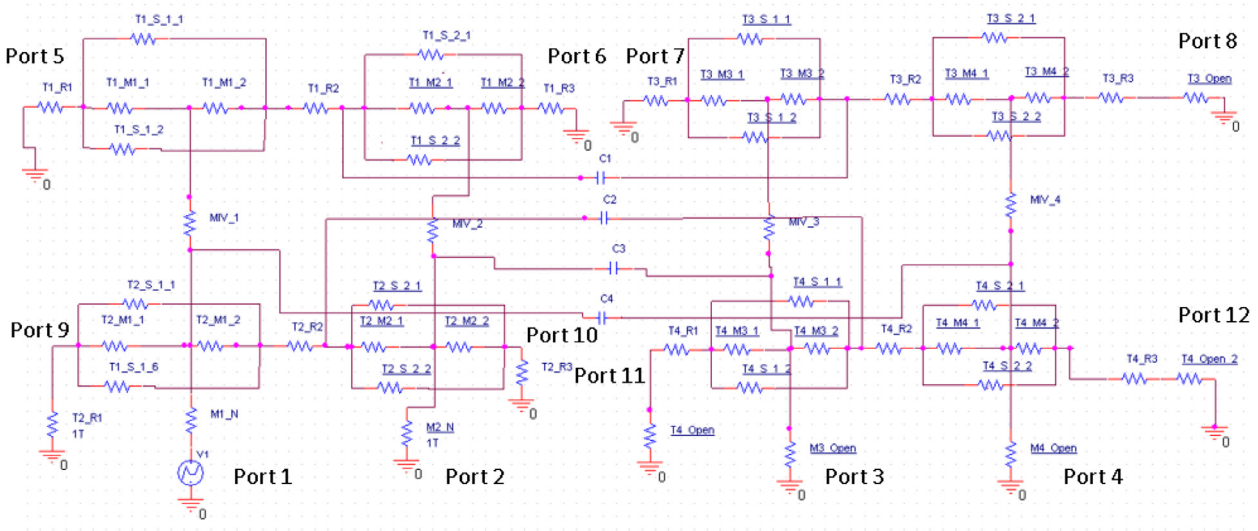

Fig. 20. SPICE model of vertical RRAM synaptic array that includes four nanowires and four MIVs. The synaptic cell is defined at the intersection between nanowire and MIV. From Port 1 to Port 4 are designed for connecting neurons at CMOS substrate. From Port 5 to Port 12 are used for nanowire connection.

The capacitance of each MIV pair is 1.52e−5 pF. Adding all capacitances together, the total capacitance between two electrically separated structures is 6.72e−5 pF, which is in good agreement with the ANSYS Q3D Extractor simulation result of 6.19e−5 pF.

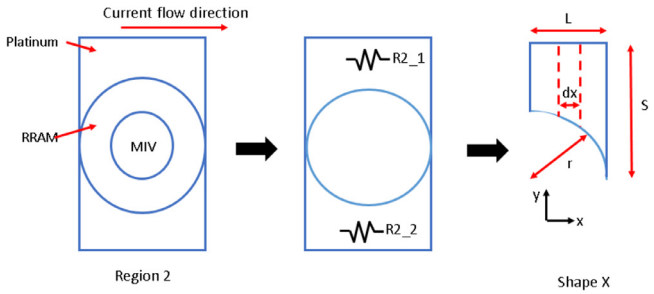

Fig. 21. Region 2 partition for resistance calculation.

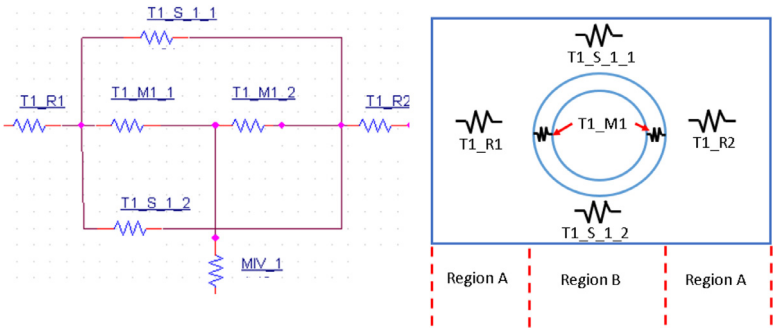

Fig. 22. The SPICE model of intersection region between nanowire and MIVs.

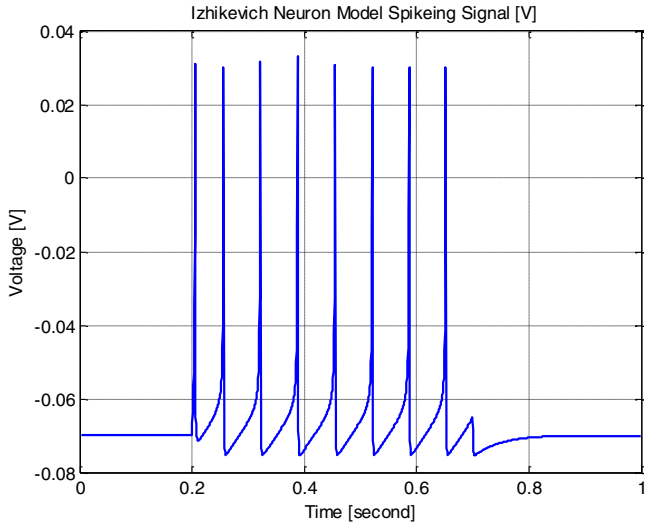

Fig. 23. Izhikevich neuron model spiking signal.

6. Simulation results and discuss

6.1. SPICE model

Based on the calculated parameter values, the intersection region between nanowire and MIV is modeled by an equivalent circuit as shown in Fig. 22.

An Izhikevich Neuron Model Spiking Signal [24] as demonstrated in Fig. 23 is used as a voltage stimulus at Port 1. The Izhikevich neuron spiking model is widely used in navigation control as shown in Fig. 24.

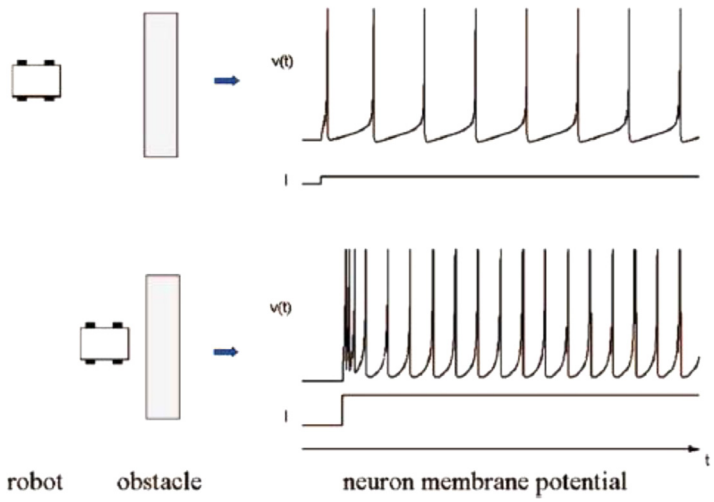

Fig. 24. The Izhikevich neuron model spiking rate is proportional to the amplitude of the distance to the obstacle [25].

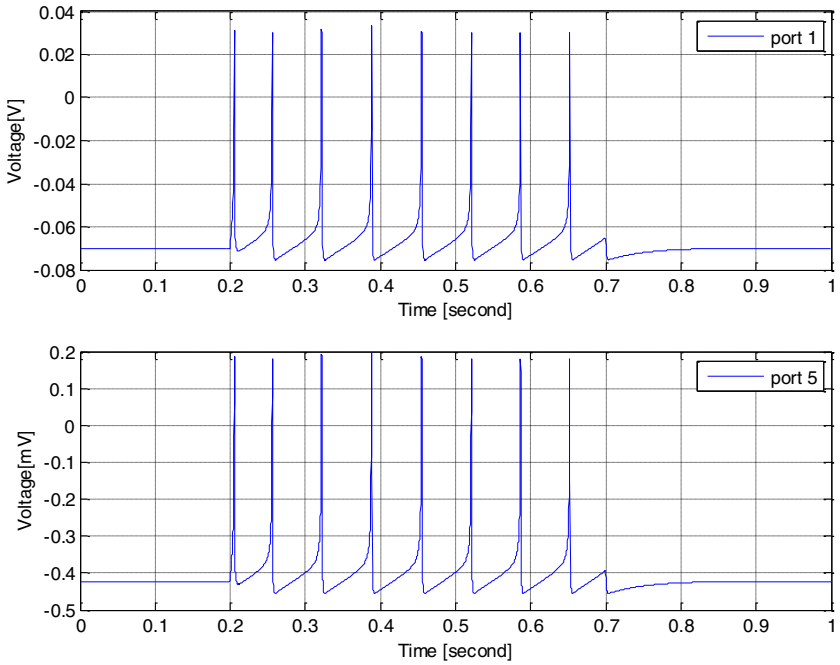

Fig. 25. The spiking signals at Port 1 and Port 5.

6.2. RRAM resistance range analysis

The main drawback of analog spiking coding method is its high sensitivity to noise, especially when the spiking signal is extremely weak. As illustrated in Fig. 25, the spiking signal at port 5 is attenuated to 0.2 mV due to the high resistance of synapse. Moreover, the high resistance of synapse could also increase power consumption in a very large-scale neuromorphic IC.

6.3. Signal integrity analysis

In this V-RRAM synaptic array structure, the nanowires separation introduces a mutual capacitance between them. The coupling noise in the victim MIVs is generated by spiking stimulus rising and falling edge as shown in Fig. 26.

Even the noise signal coupled from Port 1 to Port 3 through mutual capacitance is relatively small (at pV scale), the accumulated noised cannot be neglected when massive neurons drive multiple synapses simultaneously.

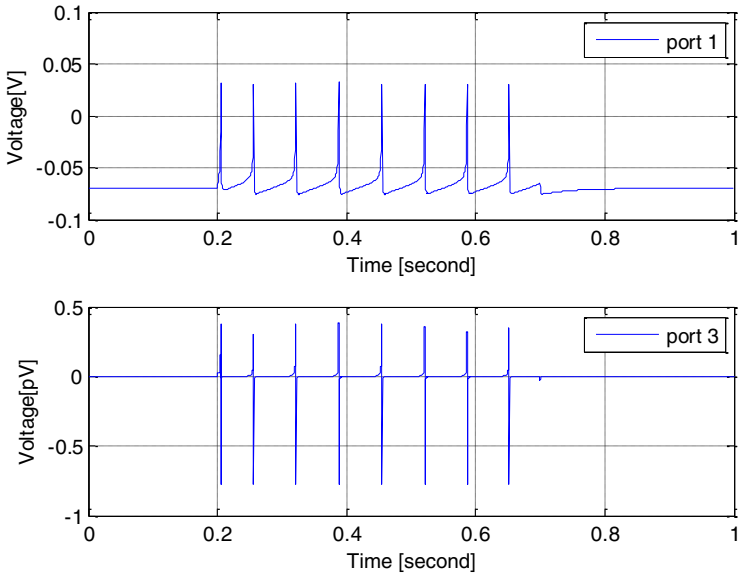

Fig. 26. The spiking signals at Port 1 and Port 3.

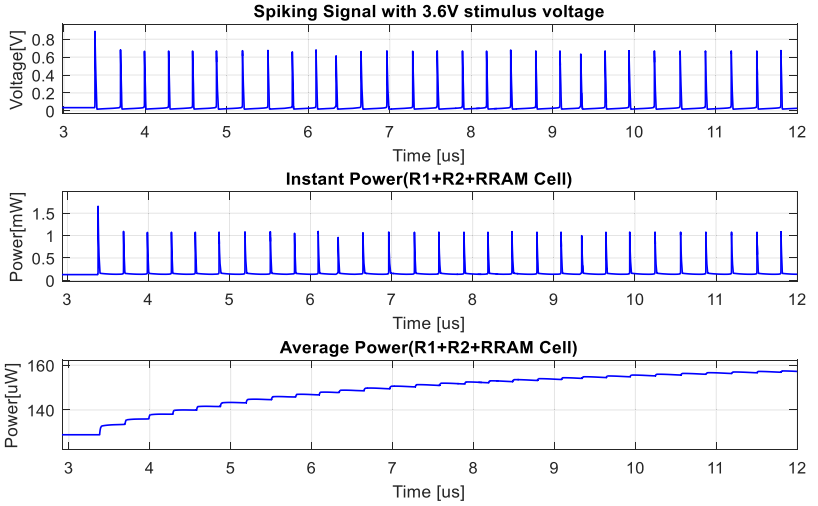

Fig. 27. Instant and average power corresponding to spiking signal under 3.6 V voltage stimulus.

6.4. Power consumption analysis

At last, we would like to demonstrate the power efficiency of our proposed structure. The power consumption of a spiking neuron per spiking event can be estimated by multiplying the pulse amplitude with the current through vertical RRAM array and the spiking width. To calculate the average power consumption in our design, we also need to consider the internal between spiking, which is equivalent to neuron firing rate. The instant and average power under 3.6 V stimulus voltage are shown in Fig. 27.

As shown in Fig. 27, the timing of each firing event is approximate 0.02 μs. The total energy of each spiking event of our design is approximate 3.2 pJ.

7. Conclusion

In this paper, we proposed and discussed a novel cloud robotics platform based on the neuromorphic chips as the core computing and memory units. Neuromorphic computing as a non-Von Neumann architecture is developed by mimicking human brain neural network structure and computing methodology. In human brain, neurons (computing units) interconnect with each other through synapses (memory units) to construct a network-based computing architecture. In this architecture,

the signals are processed in various regions of the network simultaneously, which consequently accelerate the information processing capacity of brain on massive data. Moreover, the network-based architecture emplaces the computing units (neuron) and the memory units (synapse) in close proximity, which eliminates the time and power consumption in the signal propagation. By mimicking these unique features of human brain, neuromorphic chips are potentially the next generation of computing platform with faster response time, less power consumption, and smaller chip area compared to conventional digital computer. Unlike other state-of-the-art neuromorphic chips with SRAM as memory unit and two-dimensional placement design methodology, we applied a nanoscale three-dimensional vertical RRAM structure as memory unit in neuromorphic chip design. This emerging nanoscale device can further shrink the memory unit size and signal propagation distance by stacking the individual memory unit and offering a vertical signal transfer path. A physical-based model of the proposed vertical RRAM structure is developed. Through the simulations, the resistance effect of individual RRAM cell, power consumption and crosstalk of the structure are analytical analyzed. Though the resistance of RRAM cell can be modified gradually like synapse in human brain, the high resistance value of individual RRAM cell (even at low resistance state) significantly attenuates the amplitude of signals propagating in the structure. This signal attenuation effect limits the size of vertical RRAM structure to implement large scale synapse array.

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