TDT4295 Computer Design Project

Assignment Text

2015

Graphic processing and processors specially designed to boost graphic processing power is a sub-field of processor design that is in high demand for enabling rich, visual user experiences in different products. GPUs (Graphics Processing Unit) and GP-GPUs (General Purpose computation on GPU) are industry products that have pushed the limit of semiconductor technology and given us highly parallel processors. not only for graphic processing but also for high performance computing (HPC).

The project will look into two different specialized architectures that are aimed at graphics. The two traditional ways of representing and processing digital graphics, which are pixel/raster-based and vector-based, will be explored. We are open for two different types of processors, and each of this year's two groups gets to choose what kind of processor they would like to make.

Task 1: A Convolution Engine-like processor.

Image processing (and GPUs) are typically constructed around the SIMD (single instruction multiple data) paradigm [1] where the same operations are performed on different data simultaneously. This project will look at a sub-set of such processors inspired by the Convolution Engine [2]. Figure 1 illustrates a 2D convolution operation, which takes in an input matrix (e.g. the source image) and a convolution kernel, then produces an output image. This can be thought of as a series of map-reduce operations: the kernel matrix is “placed” on top of the source matrix at each position, a *map* operator (e.g multiplication) is used to combine the source and kernel, then a *reduce* operator (e.g addition) is used to generate a single output value from the mapped values.

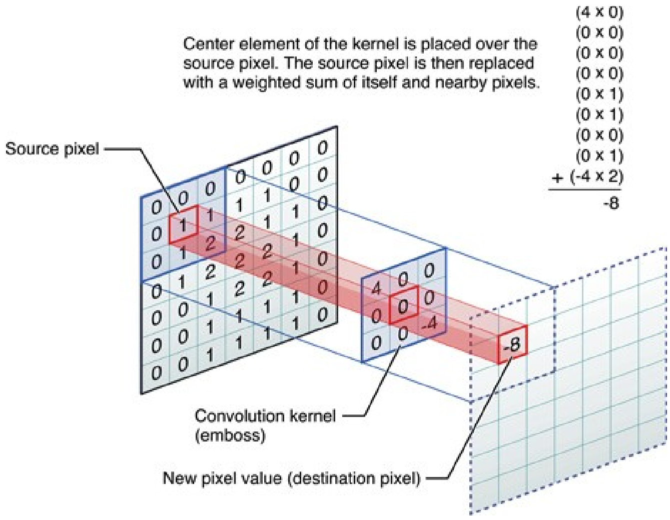
Center element of the kernel is placed over the source pixel. The source pixel is then replaced with a weighted sum of itself and nearby pixels.

Figure 1: Example of 2D convolution for emboss, reproduced from [8].

The task is to design and implement a processor that is optimized to perform convolution operation on data with two-dimensional structure (e.g. images).

Task 2: A Vector Graphics processor.

Image generation using vector graphics as the core method is a powerful and scalable way of generating image data. Vector graphics represents images at a higher abstraction level than single-pixels. A vector graphics processor can make use of drawing instructions to produce images, which is a task well suited for hardware acceleration [3]. Parallelization with multiple cores and/or at the instruction level are architectural possibilities that can be exploited to design a specialized processor. The task is to design and implement a processor for producing vector graphics. Figure 2 illustrates a vector display which takes in vector drawing commands (instead of a stream of pixels) as input.

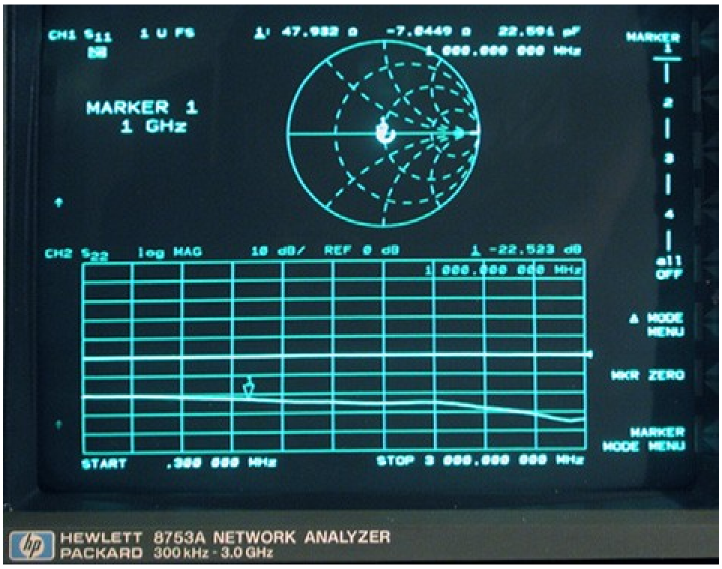

Figure 2: A vector graphics display on a network analyzer, reproduced from [9].

Additional requirements

Your processor will be implemented on an FPGA, and you are free to choose how to realize your computer architecture. Studying the architecture of general multi-core processors [6], and parallel machines options [4, 5, 6, 7] can be a good starting point.

The task should also include a suitable application that can process/produce graphical data. The output is to be displayed in order to demonstrate the processor.

The unit must utilize a Silicon Labs EFM32 series microcontroller (to act as an I/O processor) and a Xilinx FPGA (to implement your architecture on). The budget is 10.000 NOK per group, which must cover components and PCB production. The unit design must adhere to the limits set by the course staff at any given time. Deadlines are given in a separate time schedule.

And a final tip; ***Keep it simple, as simple as possible, but not simpler.***

Evaluation

The project is evaluated based on the project report and an oral presentation of the work as well as a prototype demonstration. One grade will be given to the group as a whole, unless there are significant variations in the amount of effort put into the project.

References

1. M Flynn; Some Computer Organizations and Their Effectiveness; IEEE Transactions on Computers. Volume:C-21 , Issue: 9. 1972
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3. Open VG: https://www.khronos.org/openvg/
4. Bell et al.; TILE64 - Processor: A 64-Core SoC with Mesh Interconnect; ISSCC; 20M Flynn; Some Computer Organizations and Their Effectiveness; IEEE Transactions on Computers. Volume:C-21 , Issue: 9. 1972
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6. Wikipedia; Goodyear MPP; http://en.wikipedia.org/wiki/Goodyear_MPP
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8. http://www.westworld.be/convolution-kernels/
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