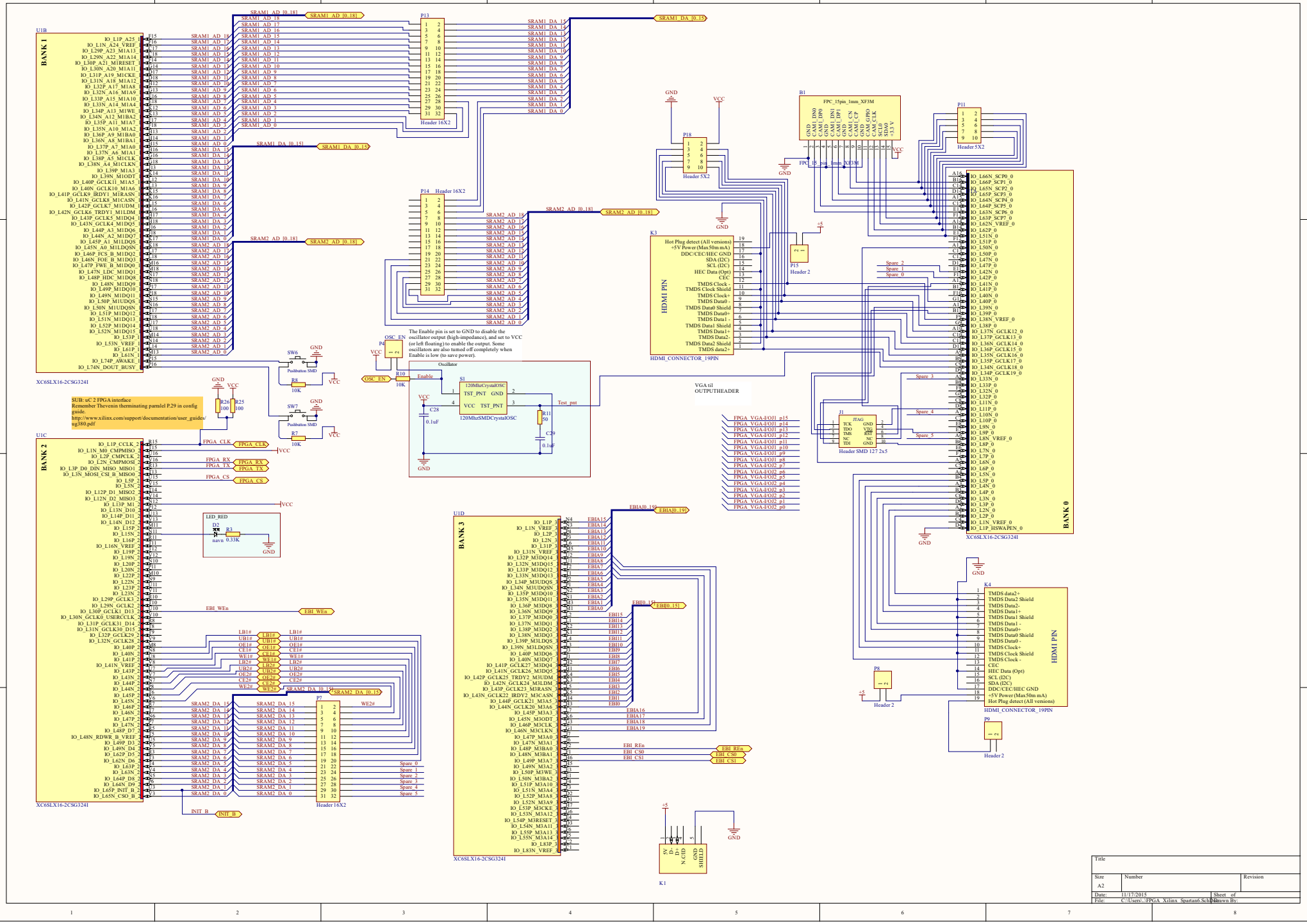
U1B
BANK 1
XC6SLX16-2CSG324I
P13
Header 16X2
P14 Header 16X2
P18
Header 5X2
B1
FPC_15pin_1mm_XF3M
P11
Header 5X2
K3
HDMI1 PIN
HDMI_CONNECTOR_19PIN
P15
Header 2
OSC_EN
P4
Oscillator
The Enable pin is set to GND to disable the oscillator output (high-impedance), and set to VCC (or left floating) to enable the output. Some oscillators are also tumed off completely when Enable is low (to save power).
S1
120MhzCrystalOSC
VGA til OUTPUTHEADER
SW6
SW7
Pushbutton SMD
R8
R7
10K
R26
R25
100
SUB: uC 2 FPGA interface
Remember Thevenin therminating parralel P.29 in config guide.
http://www.xilinx.com/support/documentation/user_guides/ug380.pdf
U1C
BANK 2
XC6SLX16-2CSG324I
LED_RED
D2
R3
0.33K
J1
JTAG
Header SMD 127 2x5
U1D
BANK 3
XC6SLX16-2CSG324I
P7
Header 16X2
K1
K4
HDMI1 PIN
HDMI_CONNECTOR_19PIN
P8
Header 2
P9
Header 2
BANK 0
XC6SLX16-2CSG324I
Title
Size
A2
Number
Revision
Date: 11/17/2015
Sheet of
File: C:\Users\...\FPGA_Xilinx_Spartan6.SchDoc
Drawn By: