

# Update of the register size used in the NeXtRad Synchronization Controller

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## 1 Introduction

### 1.1 Subject and Motivation of Report

The author was requested to make modifications to the NeXtRad Synchronization Controller developed by Johann Burger. In particular, the register size of the Synchronization Controller needed to be increased from 16 bits to 32 bits.

### 1.2 Background of the NeXtRad Synchronization Controller

### 1.3 Methodology

## 2 Modifications of the Synchronization Controller

## 3 Experimental setup

The experimental setup used to test the modified controller can be seen in figure 1. A signal generator operating at 100MHz with an amplitude of +550mV was used as the input clock. This clock signal was passed through a diode then fed into the rhino. An oscilloscope was used to measure the Main bang offset and Digitisation signals coming out of the rhino.

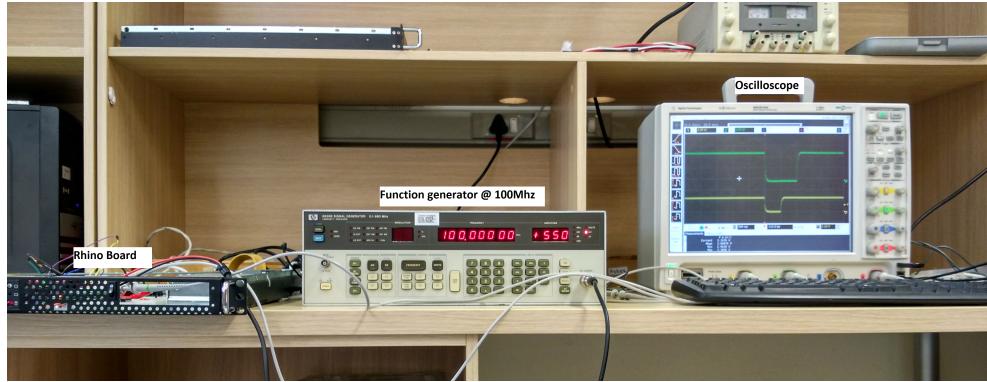


Figure 1: Picture of the equipment used to test the 32 bit version of the synchronization controller

## 4 Results of the Experiment

### 4.1 Using the Rhino Board Internal 100MHz clock

Testing of the modified synchronization controller began with using the internal clock of the Rhino board. Using the internal clock, 1kHz, 2kHz, 3kHz and 4kHz signals were produced.

Figure 2 shows the output of the main bang and the digitisation signals measured from the Rhino board. A time division of 1.0 ms was used to display the output.

### 4.2 Using an External 100MHz Clock Signal

## 5 Conclusions

## 6 Recommendations

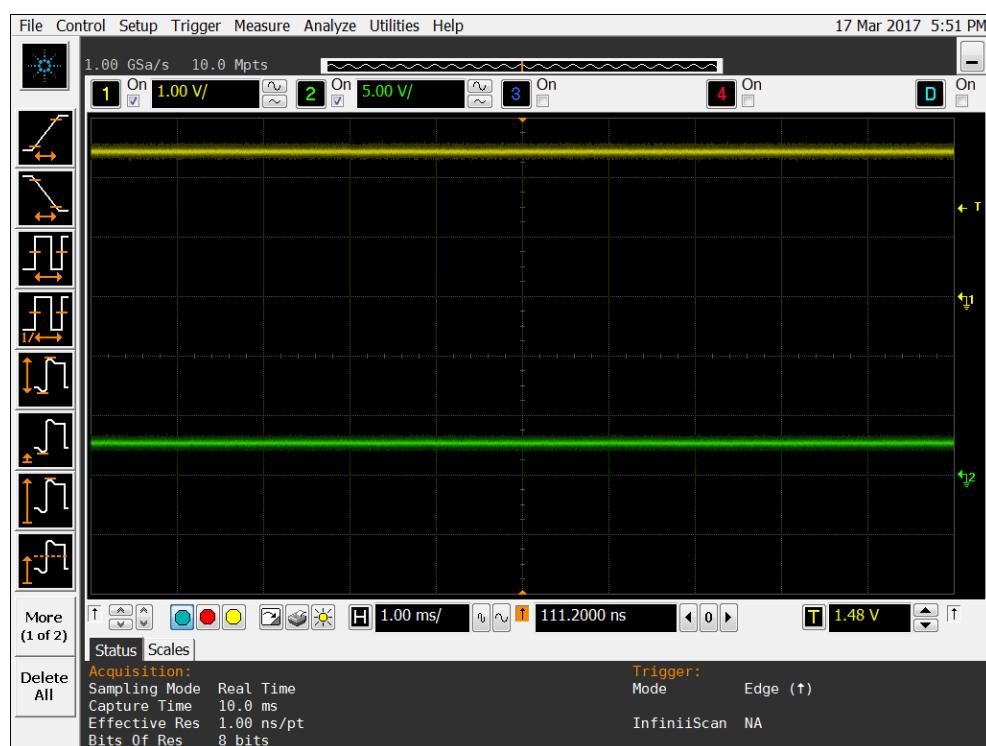


Figure 2: 1khz signal produced using the internal clock of the rhino