Faculty:	Computing	**Page:**	1 of 4
Program name:	Master of Computer Science		
Course code:	MCSS2313	**Academic Session/Semester:**	2024/25/1
Course name:	Advanced Computer System and Architecture	**Pre/co requisite (course name and code, if applicable):**	
Credit hours:	3		

Course synopsis	This course focuses on advanced topics in the design and analysis of computer architectures. Topics covered include instruction set design, pipelining, instruction- level parallelism, high-speed memory systems, storage systems, interconnection networks, and multiprocessor architectures. Students will have an opportunity to perform research in these and other areas in the field of computer architecture. An undergraduate course in computer architecture (or equivalent) is the prerequisite
Course coordinator (if applicable)	

Course lecturer(s)	**Name**	**Office**	**Contact no.**	**E-mail**
	A.P. Dr. Mohd Shahizan Othman	N28A	0127363269	shahizan@utm.my

Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:

No.	CLO	PLO (Code)	*Taxonomies and **generic skills	T&L methods	***Assessment methods
CLO1	Differentiate the organizational paradigms that determine the capabilities and performance of computer systems;	PLO1 [P1,A2]	C2	Lecture, active learning	T, Asg
CLO2	Analyze the interactions between the computer's architecture and its software;	PO1 [P2,A2]	C3	Project-based learning	T, F, PR
CLO3	Ability to apply the advanced design features on modern processors that boost the performance;	PO2 [P2,A2]	C3	Lecture, Project-based learning	T, Asg, F
CLO4	Design and analyze a simple high-performance computer architecture;	PO2 [P2,A2]	C3	Lecture, active learning	Asg, F

Refer
*Taxonomies of Learning and
**UTM's Graduate Attributes, where applicable for measurement of outcomes achievement

Prepared by: Name: Signature: Date:	Certified by: Name: Signature: Date:

***T – Test; Q – Quiz; HW – Homework; Asg – Assignment; PR – Project; Pr – Presentation; F – Final Exam etc.

Details on Innovative T&L practices:

No.	Type	Implementation
1.	Active learning	Conducted through in-class activities
2.	Project-based learning	Conducted through design assignments. Students in an individual projects that require advanced computer system and architecture solutions involving the design. Compliance to the design specifications need to be given in the form of written reports.

Weekly Schedule:

Week 1	**Chapter 1: Fundamental of Quantitative Design and Analysis** Classes of Computers, Defining Computer Architecture, Trends in Technology, Trends in Power and Energy in Integrated Circuits, Trends in Cost, Dependability
Week 2	**Benchmark** Desktop Benchmarks, Server Benchmarks, Putting It All Together: Performance, Price and Power
Week 3	**Chapter 2. Memory Hierarchy Design** Basic of Memory Hierarchy, Memory Technology and Optimizations, Reducing Power Consumption in SDRAMs
Week 4	**Reducing Power Consumption in SDRAMs**
Week 5	**Chapter 3: Instruction-Level Parallelism and Its Exploitation** Data Dependences, Name Dependences, Data Hazards, Branch-Target Buffers, Integrated Instruction Fetch Units, Speculation Support: Register Renaming Versus Reorder Buffers, Speculation Support: Register Renaming Versus Reorder Buffers, The Challenge of More Issues Per Clock
Week 6	**Instruction-Level Parallelism and Its Exploitation** Speculating Through Multiple Branches, Speculation and The Challenge of Energy Efficiency, Performance of A53 Pipeline The Intel Core i7, Performance of i7
Week 7	**Chapter 4: Data-Level Parallelism in Vector, SIMD, and GPU Architecture** Vector Architecture, SIMD Instruction Set Extensions For Multimedia, Graphics Processing Units, NVIDIA GPU Computational Structures, NVIDIA GPU Instruction Set Architecture, NVIDIA GPU Memory Structure

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Week 8	Mid-Semester Break
Week 9	**Chapter 5: Thread-Level Parallelism** Multiprocessor Architecture, Centralized Shared Memory Architecture, Performance of Symmetric Shared-Memory Multiprocessors
Week 10	**Thread-Level Parallelism - Multi-core Processor** Multicore-Based Processor on Multiprogrammed Workload
Week 11	**Chapter 6 : Warehouse Scale Computers to Exploit Request-Level and Data Level Parallelism** Warehouse-Scale Computer Programming models and workload, Warehouse-Scale Computer Architecture, Warehouse-Scale Computer Memory Hierarchy, Warehouse-Scale Computer Efficiency and Cost, Cloud Computing, Amazon Web Services
Week 12	**Warehouse Scale Computers Putting it All Together** Google Warehouse-Scale Computer
Week 13	**Chapter 7: Domain Specific Architecture** Google Tensor Processing Unit, an Interference Data Centre Accelerator
Week 14	**Microsoft Catapult and Intel Crest** Microsoft Catapult, a Flexible Data Centre Accelerator, Intel Crest, a Data Centre Accelerator For Training
Week 15	**Pixel Visual Core** Pixel Visual Core, A Personal Mobile Device Image Processing Unit, Pixel Visual Core Software, Pixel Visual Core Architecture Philosophy

Transferable skills (generic skills learned in course of study which can be useful and utilised in other settings):

Team working
Written communication

Student learning time (SLT) details:

Distribution of student Learning Time (SLT) Course content outline	**Guided Learning (Face to Face)**				**Teaching and Learning Activities**		**TOTAL SLT**
					Guided Learning Non-Face to Face	**Independent Learning Non-Face to face**	
CLO	**L**	**T**	**P**	**O**			
CLO 1	8h			2h	2h	21h	33h
CLO 2	8h			3h	3h	21h	35h

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CLO 3	8h			2h	2h	11h	23h
CLO 4	8h			3h	2h	10h	23h
Total SLT	**32h**			**10h**	**9h**	**63h**	**114h**

	Continuous Assessment	**PLO**	**Percentage**	**Total SLT**
1	Quiz		5	30m
2	Assignment 1		5	1h
3	Assignment 2		5	1h
4	Assignment 3		5	1h
5	Individual Project 1		15	As in CLO 2 (7h30m)
6	Individual Project 2		15	As in CLO2 (7h30m)
	Final Assessment		**Percentage**	**Total SLT**
1	Final Examination		50	2h 30m
	Grand Total		**100**	**120h**

L: Lecture, T: Tutorial, P: Practical, O: Others

Special requirement to deliver the course (e.g: software, nursery, computer lab, simulation room):

Learning resources:

Text book (if applicable)

John Hennessy, David Patterson, Computer Architecture 6th Edition, Morgan Kaufmann, 2017.

Academic honesty and plagiarism: *(Below is just a sample)*

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES)

Copying of work (texts, simulation results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of **zero** for the assignment and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

Other additional information (Course policy, any specific instruction etc.):

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Disclaimer:

Prepared by:	Certified by:
Name:	Name:
Signature:	Signature:
Date:	Date: