Computer Organization & Architecture

Chapter 8 – Semiconductor Memories

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Contents of this lecture

- 8.2 Semiconductor RAM Memories
  - Static RAM
  - Dynamic RAM
  - Structure of Larger Memories

Static RAM

- Implementation of a SRAM cell
- CMOS SRAM
- Internal Organization of Static RAM
- Static RAM chips
- Summary of Static RAM

Semiconductor RAM Memories (1)

- Semiconductor RAM Memory
  - The most common type of semiconductor memory is referred to as *random-access memory* (RAM).
  - Characteristic
    - It is possible both to read data from the memory and to write new data into the memory easily and rapidly
    - It is volatile.
    - Access time is of just a few nanoseconds (10^{-9} seconds).

Main Memory Technology

- Static RAM (SRAM)
  - Binary values are stored using traditional flip-flop logic-gate configurations.
  - Densities ¼ to 1/8 of DRAM
  - Speeds 8-16x faster than DRAM
  - Cost 8-16x more per bit
  - Optimized for speed ->caches
- Dynamic RAM (DRAM)
  - Made with cells that store data as charge on capacitors.
  - Highest densities
  - Optimized for cost/bit ->main memory
- Note
  - Both static RAMs and dynamic RAMs are volatile.

Implementation of a SRAM Cell (1)

- A Static RAM Cell (SRAM)
  - Figure

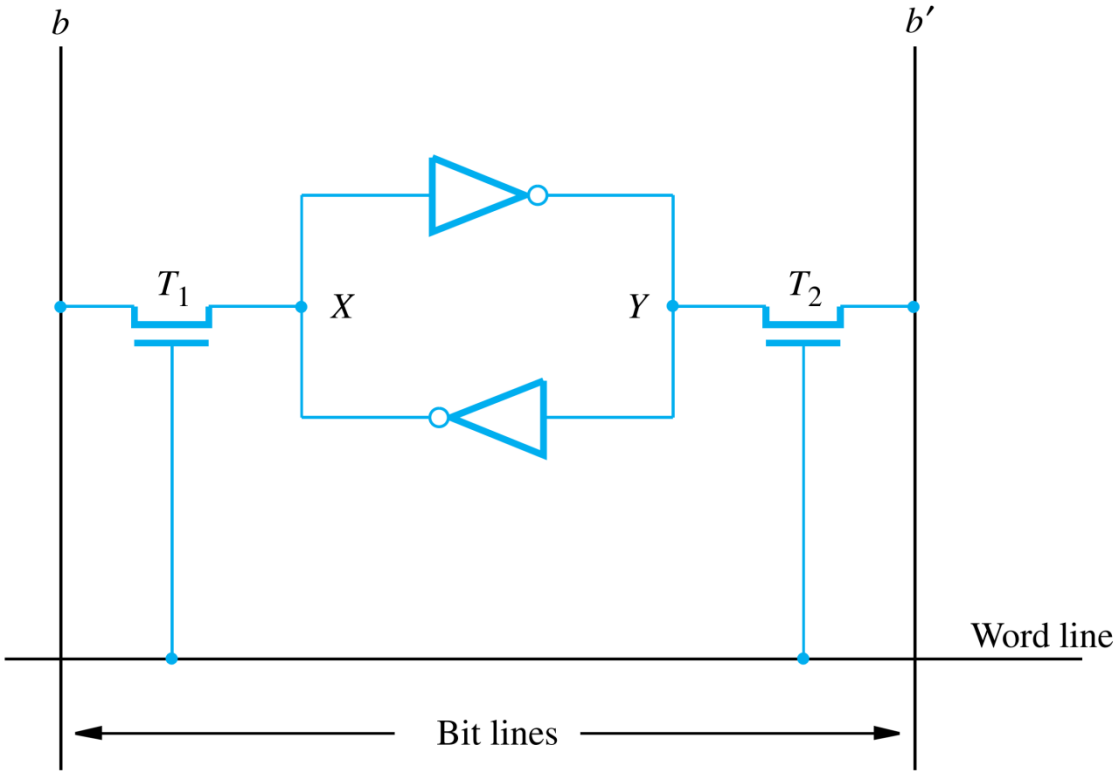


Figure 8.4 A static RAM cell.

Implementation of a SRAM Cell (2)

- A Static RAM Cell (ctd.)
  - State “1”
    - Assume that the cell is in state 1 if the logic value at point X is 1 and at point Y is 0.
  - State “0”
    - Assume that the cell is in state 0 if the logic value at point X is 0 and at point Y is 1.
    - State “1”

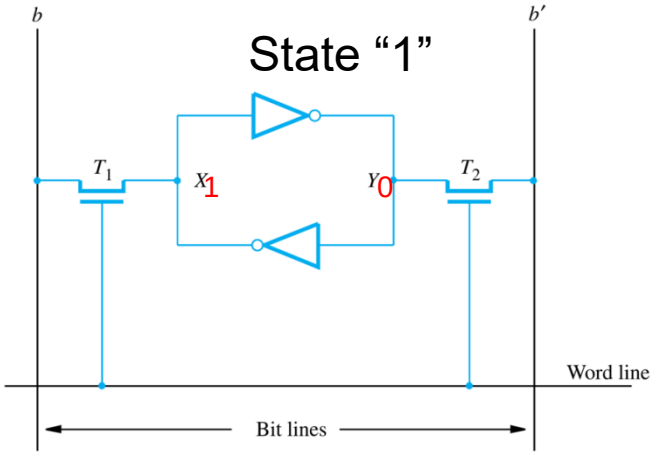


Figure 8.4 A static RAM cell.

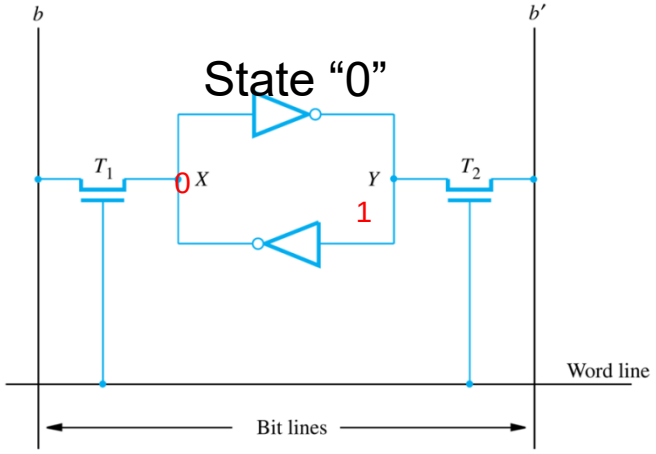


Figure 8.4 A static RAM cell.

Implementation of a SRAM Cell (3)

- A Static RAM Cell (ctd.)
  - Read Operation
    - The word line is at high level.
    - Read “1”: The signal on the bit line b is high and the signal on the bit line b’ is low.
    - Read “0”: The signal on the bit line b is low and the signal on the bit line b’ is high.
    - Note: Sense/write circuits at the end of the bit lines monitor the state of b and b’ and set the output accordingly.

Implementation of a SRAM Cell (4)

- A Static RAM Cell (ctd.)
  - Write Operation
    - The word line is at high level.
    - Write “1” : Place high level signal on bit line b and place low level signal on bit line b’.
    - Write “0” : Place high level signal on bit line b and place low level signal on bit line b’.
    - Note: The required signals on the bit lines are generated by the Sense/Write circuit.
  - Maintain State
    - The word line is at ground level.

CMOS SRAM (1)

- CMOS Realization of a SRAM Cell
  - MOS IC
    - NMOS
    - PMOS
    - CMOS: Complementary Metal-Oxide Semiconductor (互补金属氧化物半导体)

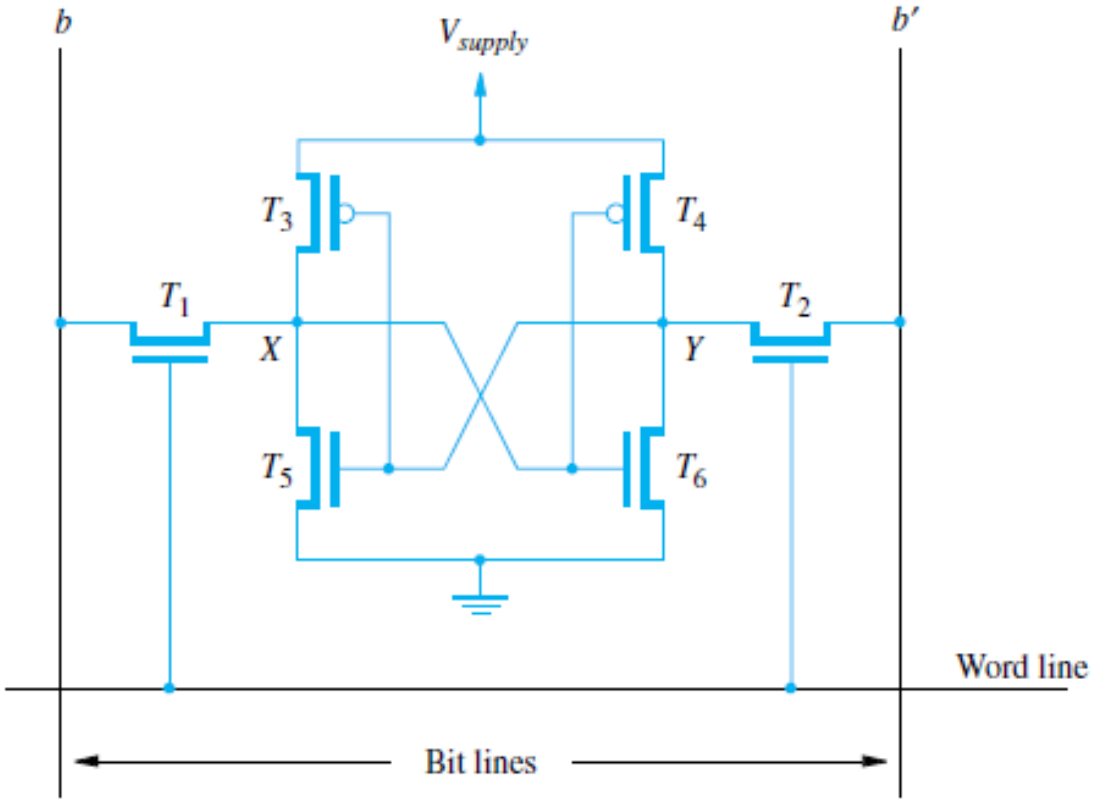


Figure 8.5 An example of a CMOS memory cell.

CMOS SRAM (2)

- CMOS Realization of a SRAM Cell (ctd.)
  - Note: If power is interrupted and then it is restored, the latch will settle into a stable state, but it will not necessarily be the same state the cell was in before the interruption.
  - The power supply voltage is 5V in older CMOS SRAMs or 3.3V in new low-voltage versions.
  - CMOS SRAMs' power consumption is very low.

Internal Organization of Static RAM (1)

- Organization of 128 Bit Cells (16 × 8)
  - Figure 8.2: a matrix of 16 row × 8 column

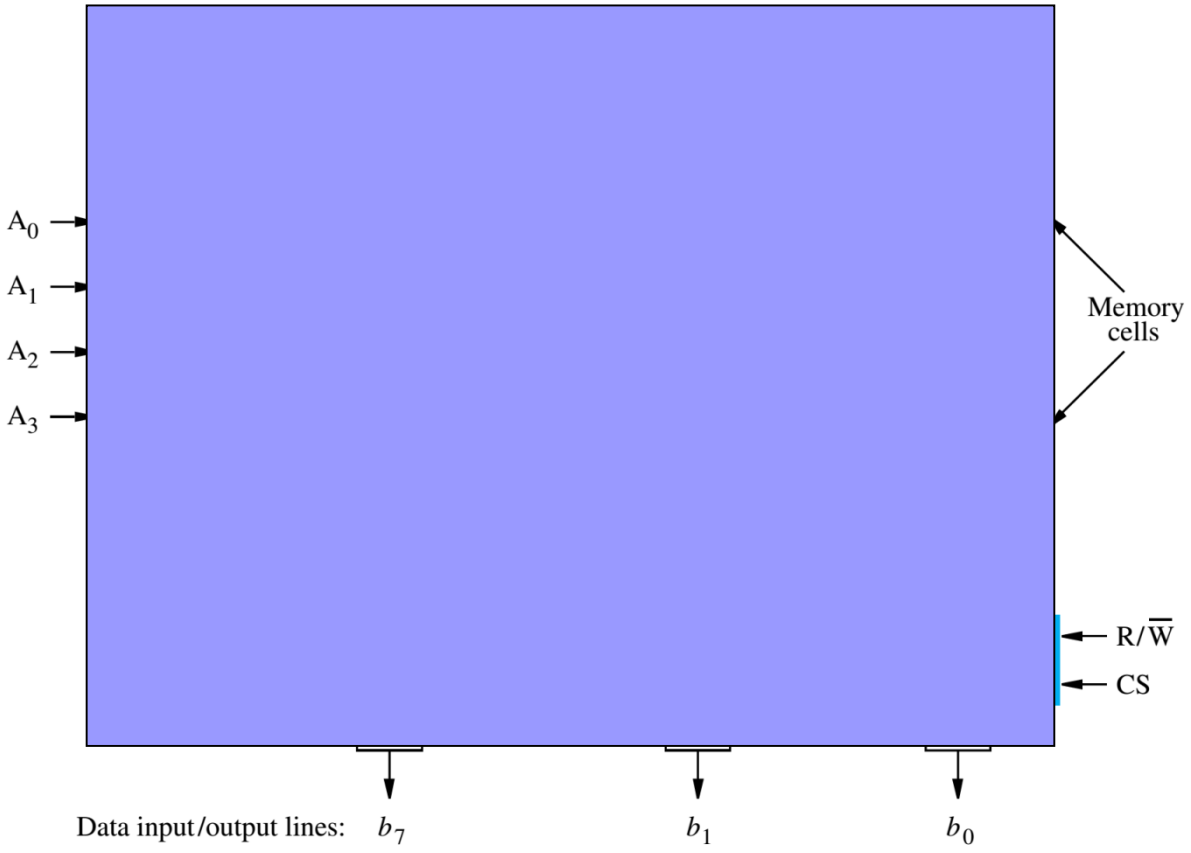


Figure 8.2 Organization of bit cells in a memory chip.

Internal Organization of Static RAM (2)

- Organization of 128 Bit Cells (ctd.)
  - Internal Organization
    - Word line: driven by the address decoder.
    - Bit lines
    - Sense/Write circuits
  - External Connections
    - Address lines(Input): $A_0 – A_3$
    - Data lines(Input/Output): $b_0 – b_7$
    - Control lines(Input)
      - R/$\overline{W}$ (Read/Write): Specify the required Read or Write operation.
      - CS(Chip Select): Select a given chip in a multi-chip memory system.

Internal Organization of Static RAM (3)

- Organization of 128 Bit Cells (ctd.)
  - External Connections (ctd.)
    - Power Supply line
    - Ground line
    - Total Connections = 4 + 8 + 2 + 1 + 1 = 16

Internal Organization of Static RAM (4)

- Organization of 1024 (1K) Bit Cells
  - 128 × 8 Organization
    - Internal Organization
      - A matrix of 128 row × 8 column
    - External Connections
      - Address lines(Input): $A_0 – A_6$
      - Data lines(Input/Output): $b_0 – b_7$
      - Control lines(Input): R/$\overline{W}$, CS
      - Power supply line
      - Ground line
      - Total Connections = 7 + 8 + 2 + 1 + 1 = 19

Internal Organization of Static RAM (5)

- Organization of 1024 (1K) Bit Cells (ctd.)
  - 1K × 1 Organization
    - Figure

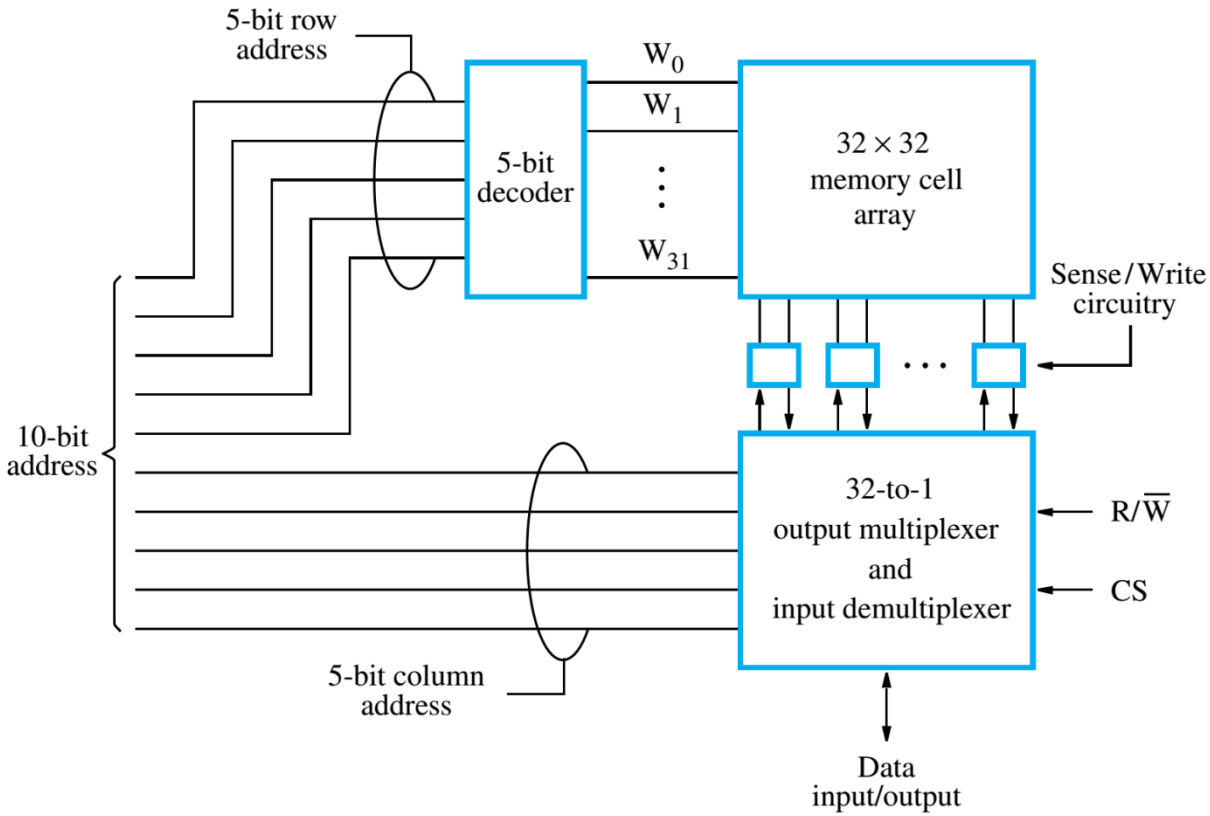


Figure 8.3 Organization of a 1K × 1 memory chip.

Internal Organization of Static RAM (6)

- Organization of 1024 (1K) Bit Cells (ctd.)
  - 1K × 1 Organization (ctd.)
    - External Connections
      - Address lines(Input): $A_0 – A_9$
      - Data lines(Input/Output): b_0
      - Control lines(Input): R/$\overline{W}$, CS
      - Power supply line
      - Ground line
      - Total Connections= 10 + 1 + 2 + 1 + 1 = 15
    - Large chips have essentially the same organization as Figure 5.3 but use a larger memory cell array and have more external connections.

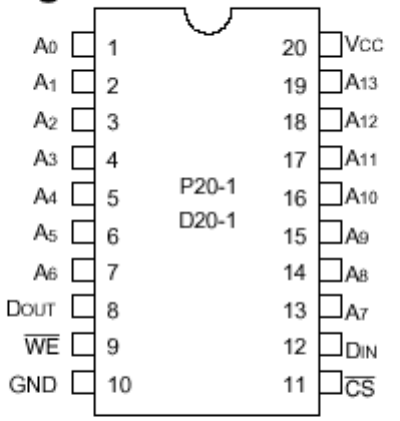
Static RAM Chips (1)

- Example: IDT616
  - DIP: Dual In-line Packages

双列直插封装（中小规模集成电路均采用这种封装形式，其引脚数一般不超过100）

IDT6167SA/LA
CMOS Static RAM 16K (16K x 1-Bit)

Pin Configurations



DIP
Top View

Pin Descriptions

Name	Description
A_0 - A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
D_{IN}	$DATA_{IN}$
D_{OUT}	$DATA_{OUT}$
GND	Ground

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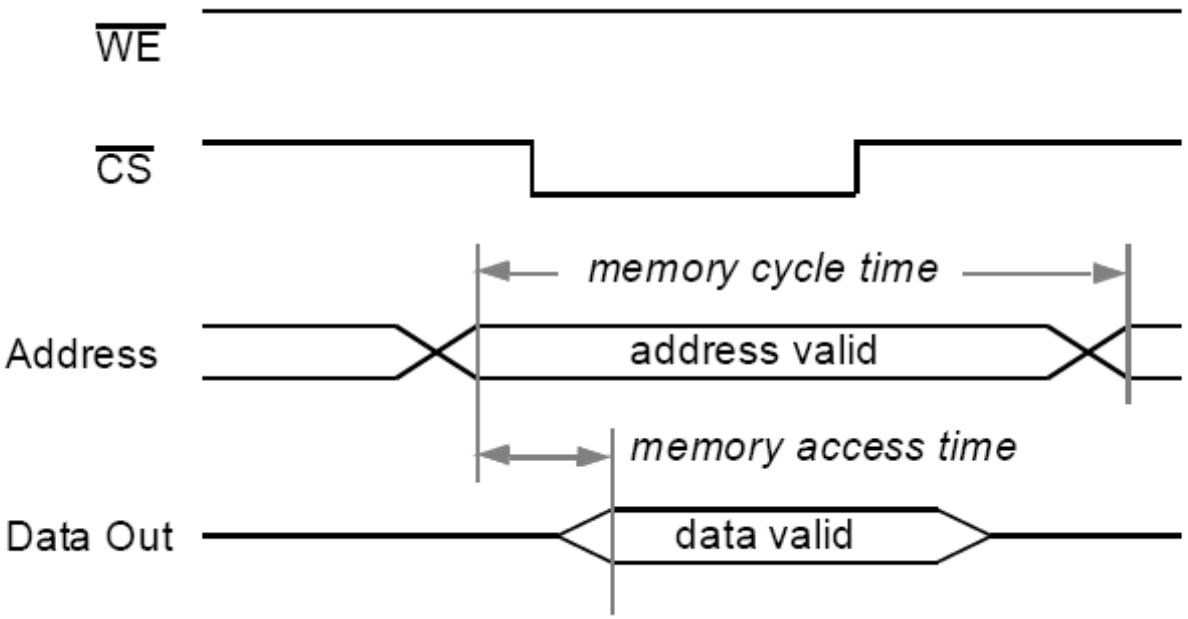
Static RAM Chips (2)

- Example: Read Sequencing



  - Memory access time = time from address valid to data out valid
  - Memory cycle time = time between subsequent memory accesses

Advantage and Disadvantage

- Advantage of Static RAM
  - Fast
- Disadvantages of Static RAM
  - Low density
  - High cost

Summary of Static RAM

- 知识点: Static RAM
  - SRAM Cell
  - Internal Organization of SRAM
  - SRAM Chip
- 掌握程度
  - 了解SRAM Cell的存储原理和读写操作原理
  - 了解SRAM内部存储元的组织方式
  - 掌握SRAM芯片的外部引脚

Exercise (1)

1. Assume that the capacity of a kind of SRAM chip is 8K×16, so the address lines and data lines of this chip are _____ respectively.

- A. 8, 16
- B. 13, 16
- C. 13, 4
- D. 8, 4

Exercise (2)

2. Assume that the capacity of a kind of SRAM chip is 32K×32, so the sum of address lines and data lines of this chip is _____.
   - A. 47
   - B. 64
   - C. 46
   - D. 74

Contents of this lecture

- 8.2 Semiconductor RAM Memories
  - Static RAM
  - Dynamic RAM
  - Structure of Larger Memories

Dynamic RAM

- Single-Transistor DRAM Cell
- Internal Organization of Asynchronous DRAM Chip
- DRAM Refresh
- DRAM Chips
- Asynchronous DRAM
- Enhanced DRAM
- Synchronous DRAM
- Summary of Dynamic RAM

Single-Transistor DRAM Cell (1)

- Figure

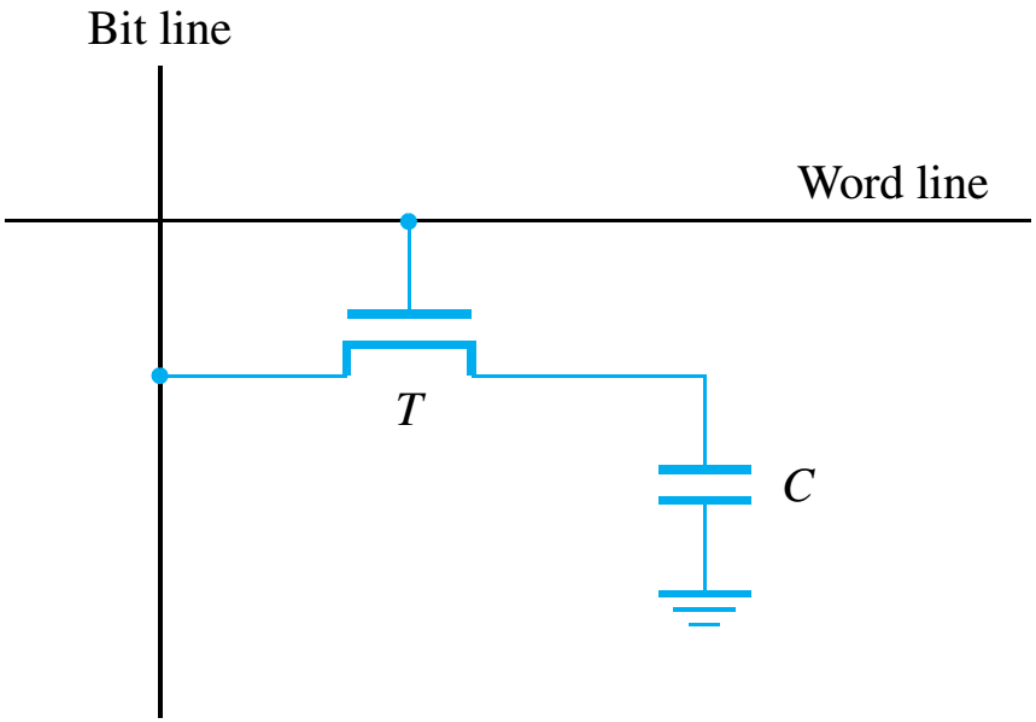


Figure 8.6 A single-transistor dynamic memory cell.

Single-Transistor DRAM Cell (2)

- Read “1”
  - Take the word line HIGH.
  - If the charge stored on the capacitor is above the threshold value, the sense amplifier drives the bit line to a full voltage that represents “1”. This voltage recharges the capacitor to the full charge that correspond to “1”.

Single-Transistor DRAM Cell (3)

- Read “0”
  - Take the word line HIGH.
  - If the charge stored on the capacitor is below the threshold value, the sense amplifier pulls the bit line to ground level, which ensures that the capacitor will have no charge, representing “0”.

Single-Transistor DRAM Cell (4)

- Write Operation
  - Take the word line HIGH.
  - Set the bit line LOW or HIGH to store 0 or 1.
  - Take the word line LOW.
  - Note: The stored charge for a 1 will eventually leak off.
- Maintain State
  - The word line is low.

Internal Organization of Asynchronous DRAM Chip (1)

- Example: A 32M × 8 DRAM chip
  - Figure

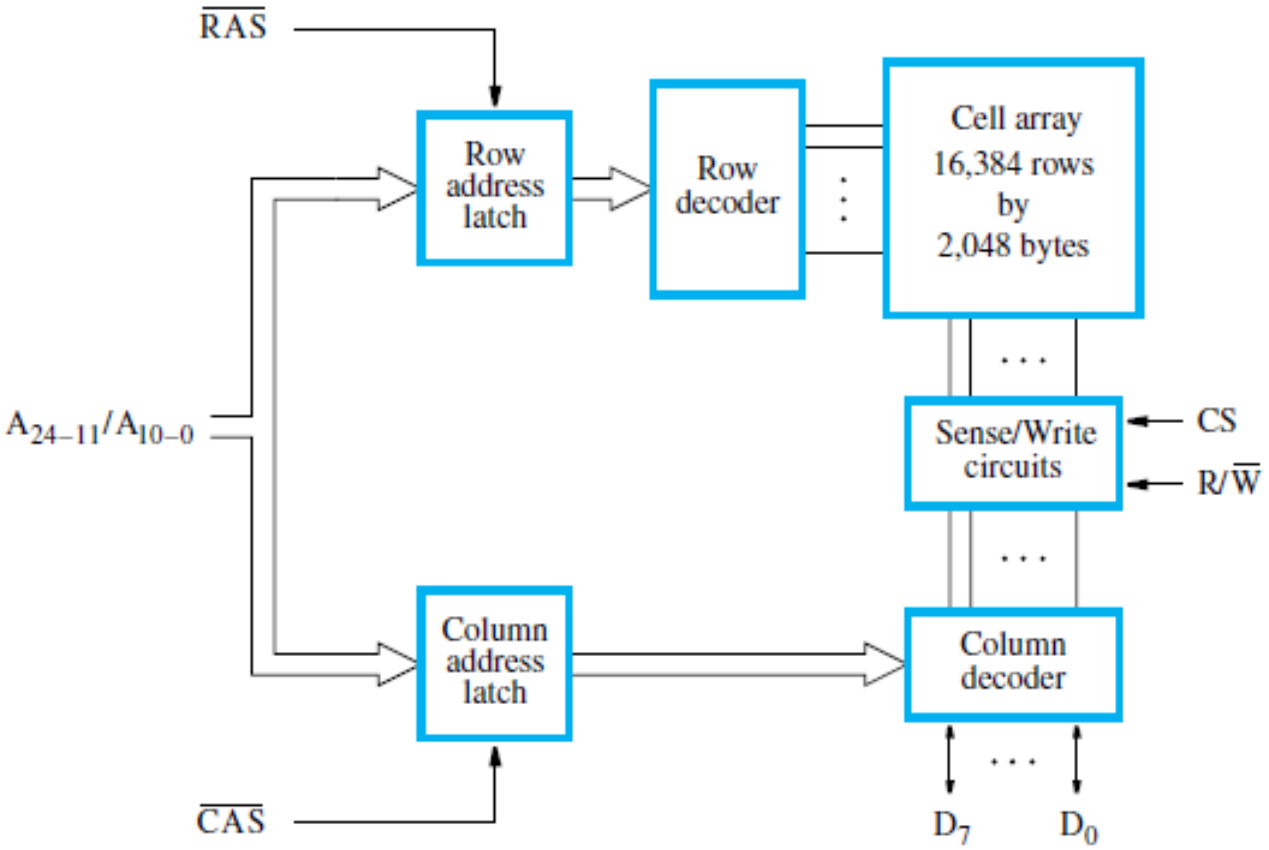


Figure 8.7 Internal organization of a 32M × 8 dynamic memory chip.

Internal Organization of Asynchronous DRAM Chip (2)

- Example: A 32M × 8 DRAM chip (ctd.)
  - External Connections
    - 14 bit address bits are needed to select a row.
    - Another 11 bits are needed to specify a group of 8 bits in the selected row.
    - Total: 25-bit address
    - To reduce the number of pins needed for external connections, the row and column addresses are multiplexed on 14 pins.
    - Row Address Strobe ($\overline{RAS}$)
    - Column Address Strobe ($\overline{CAS}$)

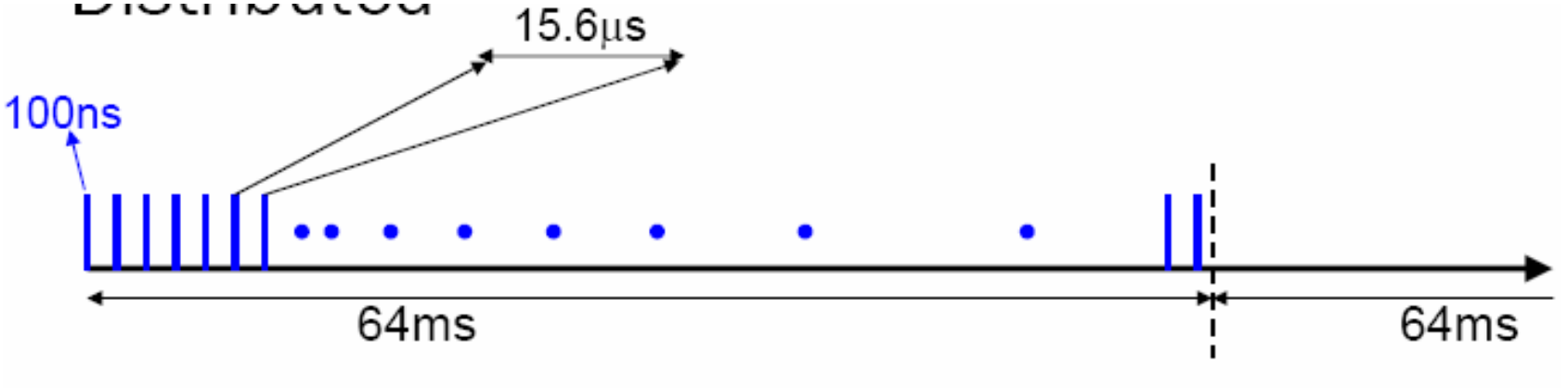
DRAM Refresh (1)

- Leaky storage
- Periodic refresh across DRAM rows.
- Un-accessible when refreshing.
- Read, and write the same data back.
- Example: 4K rows in a DRAM, 100ns read cycle, Decay in 64ms
  - 4096*100ns = 410μs to refresh once
  - 410μs / 64ms = 0.64% unavailability

DRAM Refresh (2)

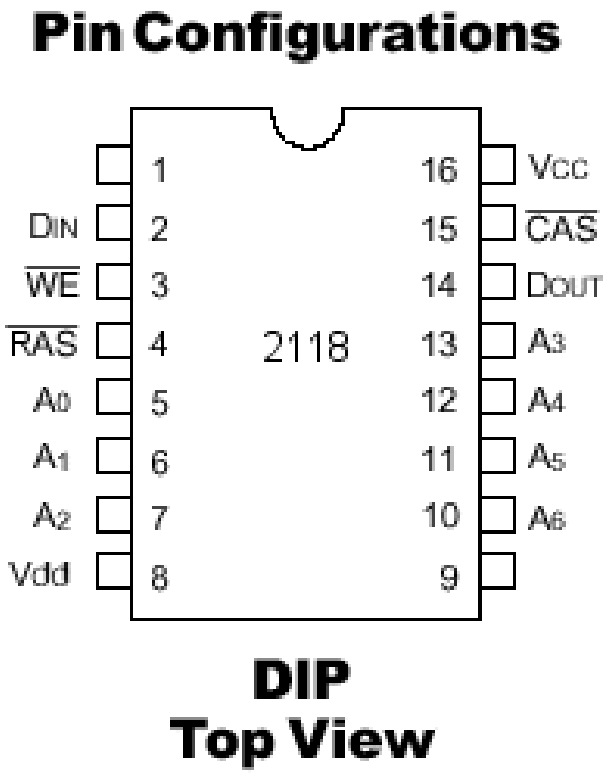
- Refresh Styles
  - Burst

  - Distributed



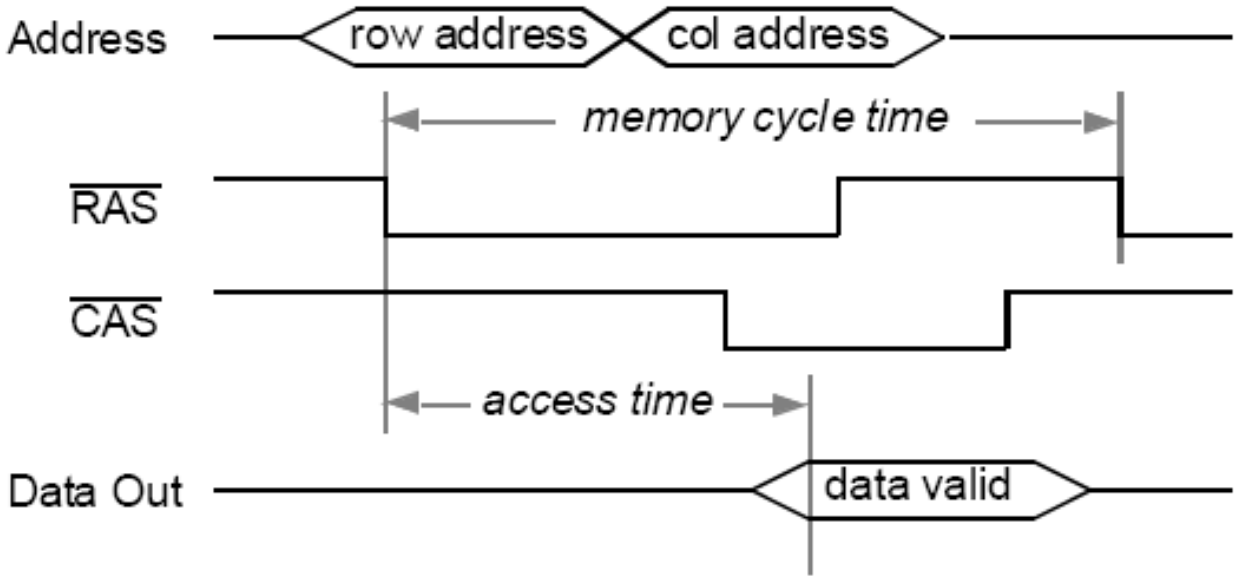
DRAM Chips (1)

- Example: Intel 2118
  - 16K × 1
  - Different control signals than SRAM chips.
    - Requires only 1/2 number of input address lines.
    - Replaced CS by RAS and CAS (very strict timing constraints)
    - Separates data inputs and outputs (typically)



DRAM Chips (2)

- Example: Intel 2118 (ctd.)
  - Read Sequencing



Asynchronous DRAM (1)

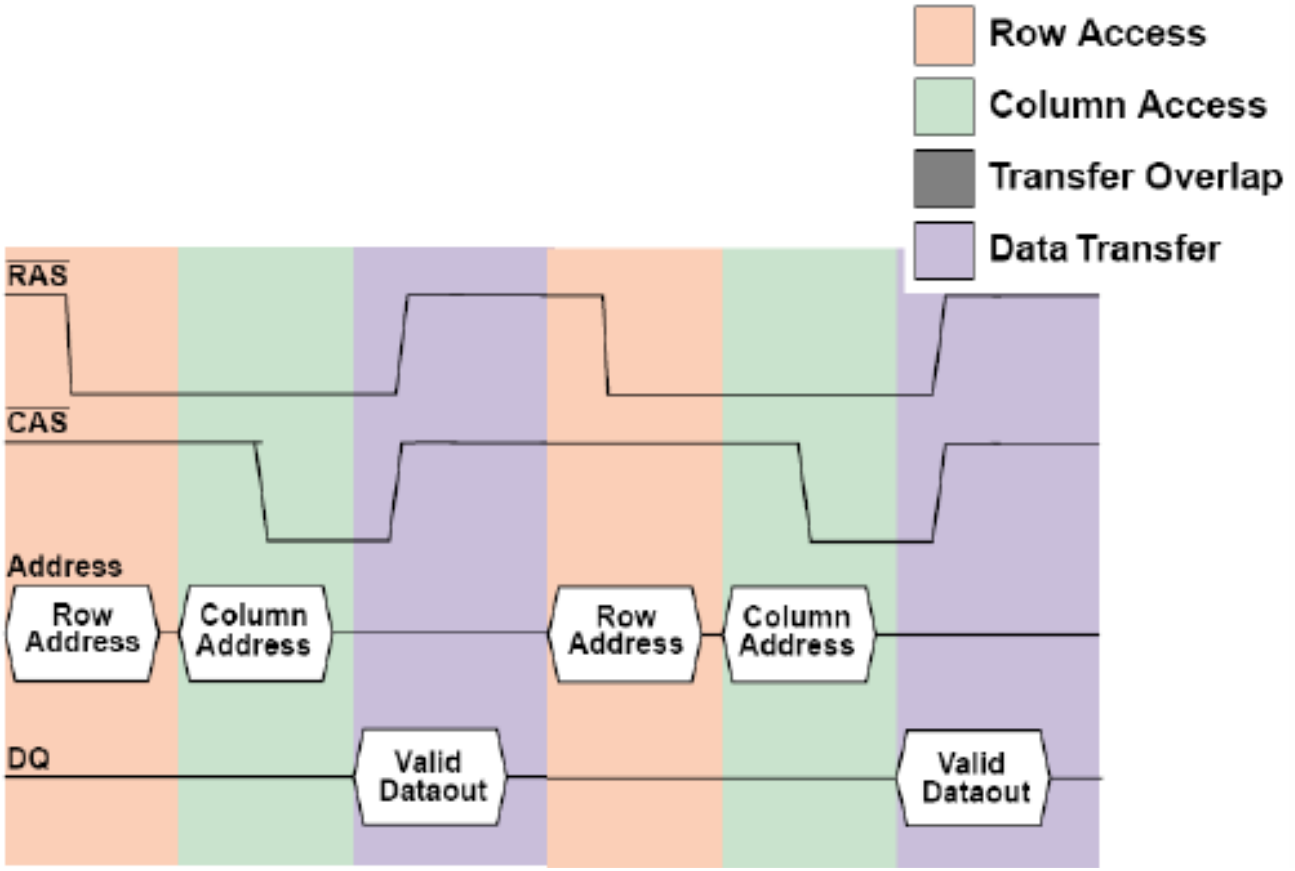
- The memory is not synchronized to the system clock. A memory access is begun, and a certain period of time later the memory value appears on the bus. The signals are not coordinated with the system clock at all.
- The timing of the memory is controlled asynchronously.
  - Normal: Responds to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals (no clock)
  - A specialized memory controller circuit provides the necessary control signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ that govern the timing.

Asynchronous DRAM (2)

- Question: How to access the other bytes in the same row of a DRAM chip?
- Fast Page Mode (FPM)
  - Row remains open after RAS for multiple CAS commands.
  - It allows transferring a block of data at a much faster rate than can be achieved for transfers involving random addresses.

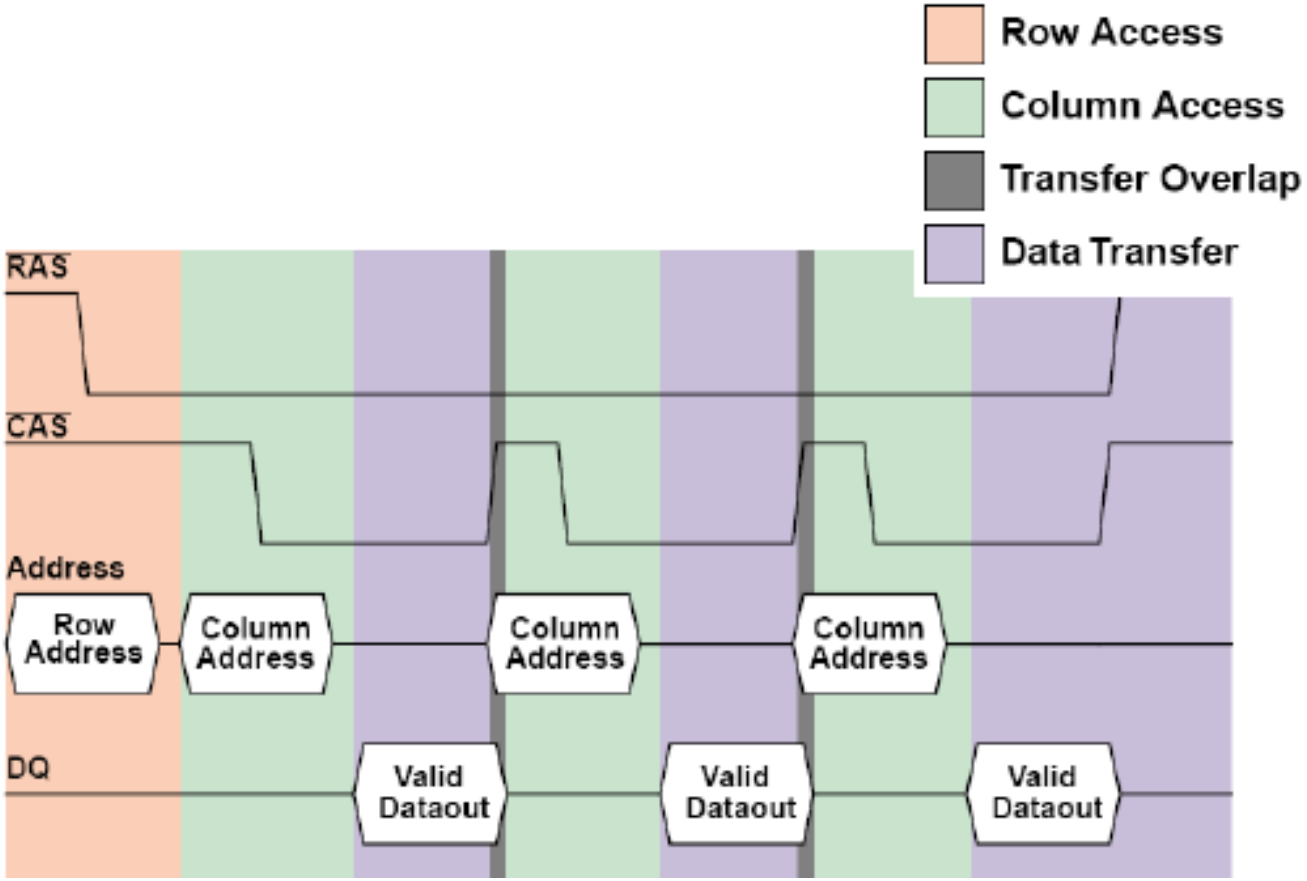
Asynchronous DRAM (3)

- Conventional Memory Read Timing
  - Figure



Asynchronous DRAM (4)

- FPM Memory Read Timing



Evolution of the DRAM (1)

- DRAM Architecture

Figure 7: Evolution of the DRAM Architecture

Each step along DRAM's evolution has been incremental. Original designs were clocked; in the mid-1970's the clock disappeared; fast page mode (FPM) kept the sense amplifiers active; extended data-out (EDO) added a latch; burst EDO (BEDO) added an internal counter; SDRAM came full circle by reinstating a clock signal.

Evolution of the DRAM (2)

- Obsolete Technologies
  - Fast page mode DRAM (FPM DRAM)
    - Allowed re-use of row-addresses
  - Extended data out DRAM (EDO DRAM)
    - Enhanced FPM DRAM with more closely spaced CAS signals.
  - Burst EDO DRAM (BEDO DRAM)
    - A faster type of EDO

Evolution of the DRAM (3)

- DRAM Cores with better interface logic and faster I/O.
  - Synchronous DRAM (SDRAM): Uses a conventional clock signal instead of asynchronous control.
  - Double Data Rate Synchronous DRAM (DDR SDRAM): Double edge clocking sends two bits per cycle per pin.
  - Rambus™ DRAM (RDRAM):Uses faster signalling over fewer wires (source directed clocking) with a transaction oriented interface protocol.

Synchronous DRAM (1)

- Their operation is directly synchronized with a clock signal.
- Structure of a SDRAM Chip

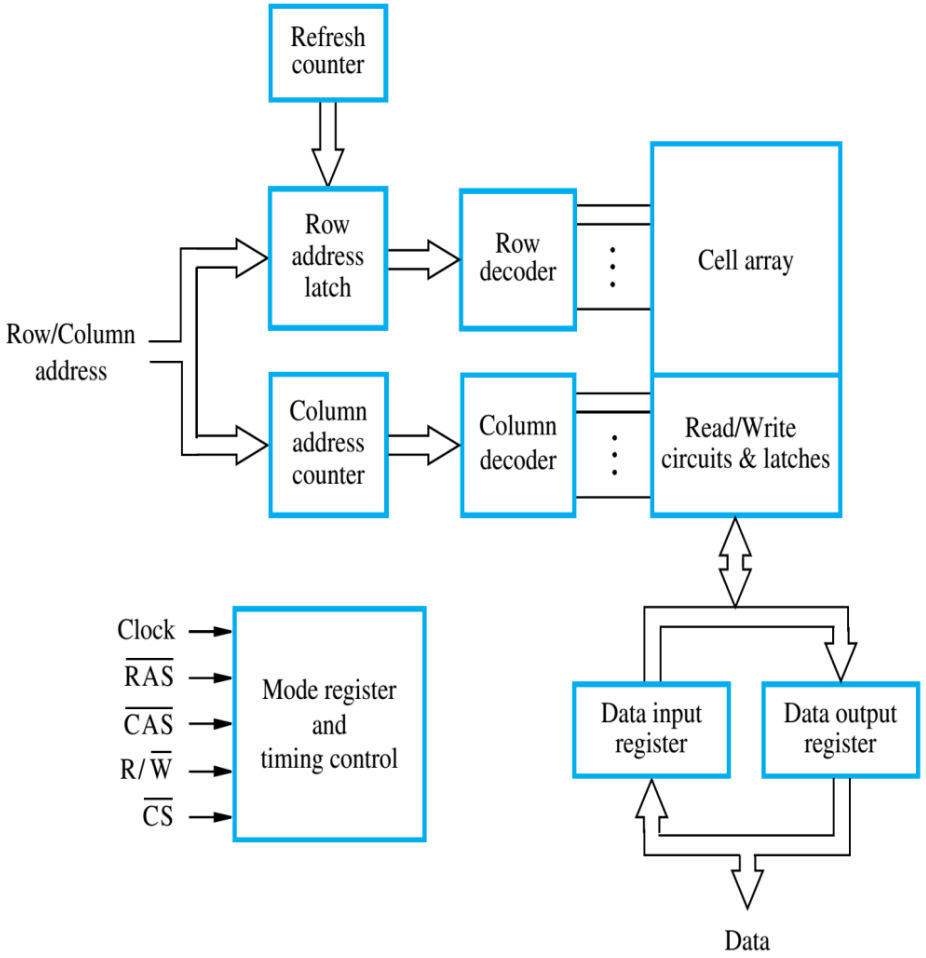


Figure 8.8 Synchronous DRAM.

Synchronous DRAM (2)

- Structure of a SDRAM Chip (ctd.)
  - If an access is made for refreshing purpose only, it will merely refresh the contents of the cells, not changing the contents of the latches.
  - It is not necessary to provide externally generated pulses on the CAS line to select successive columns. The necessary control signals are provided internally using a column counter and the clock signal.
  - SDRAMs have built-in refresh circuitry. A refresh counter is a part of built-in refresh circuitry.

Synchronous DRAM (3)

- Burst Operation
  - Example: Burst read of length 4 in an SDRAM.

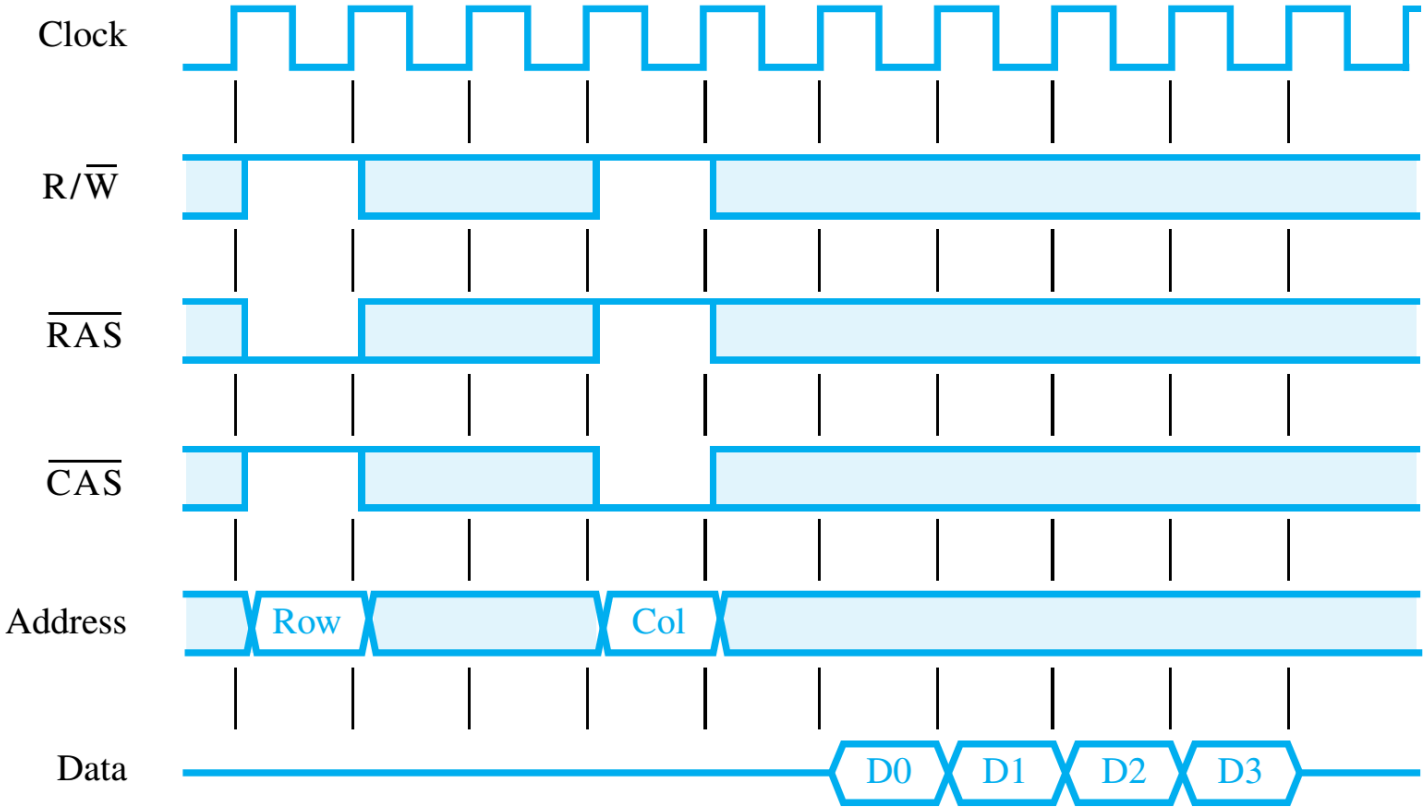
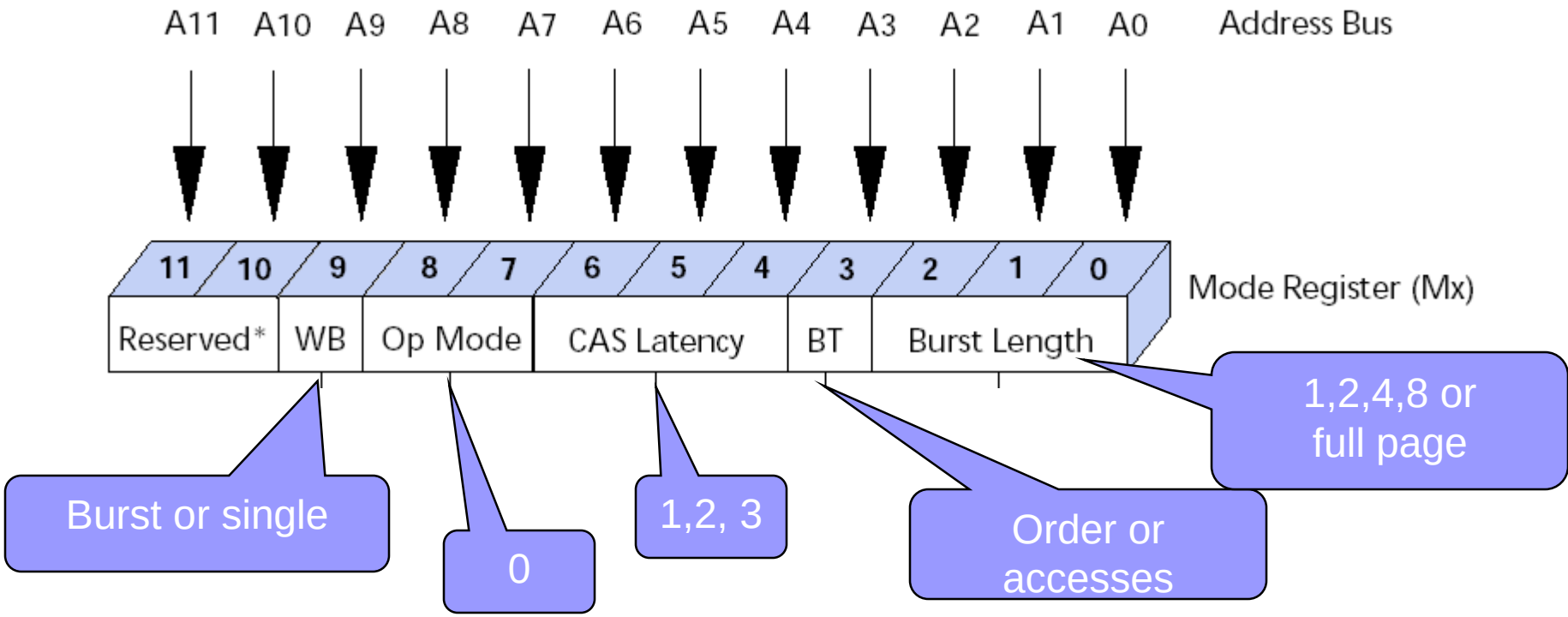


Figure 8.9 A burst read of length 4 in an SDRAM.

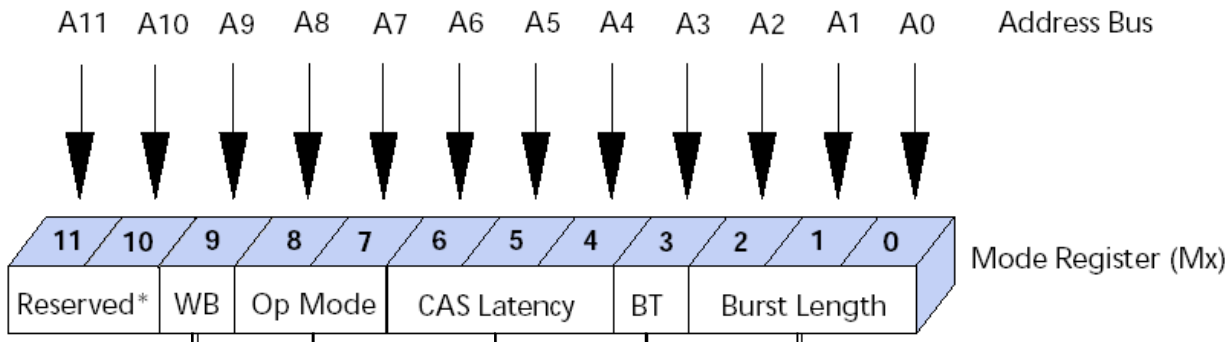
Synchronous DRAM (4)

- Mode Register Example



Synchronous DRAM (5)

- Mode Register Example(ctd.)



M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
			All other reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6M5M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 x x	Reserved

M2M1M0	Burst Length	
	M3=0	M3=1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

Synchronous DRAM (6)

- Mode Register Example (ctd.)

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0-A7 (location 0-255)			Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

IntoZGC hbs.intozgc.com

Synchronous DRAM (7)

- Speed of SDRAM
  - The speed of SDRAM is rated in MHz rather than in nanoseconds (ns).
  - Advantage
    - This makes it easier to compare the bus speed and the SDRAM chip speed.
  - Example
    - Intel has defined PC100 and PC133 bus specifications in which the system bus is controlled by a 100 or 133 MHz clock respectively. Therefore, major manufacturers of memory chips produce 100 and 133 MHz SDRAM chips.
  - Note
    - Convert the SDRAM clock speed to nanoseconds by dividing the chip speed into 1 billion ns.

Synchronous DRAM (8)

- Latency and Bandwidth are two parameters indicating the performance of a memory system.
- Latency
  - Refers to the amount of time it takes to transfer a word of data to or from the memory.
  - Note
    - In block transfers, latency is used to denote the time it takes to transfer the first word of data.
  - When buying DRAM, the latency rating that you see most often is the memory access time.

Synchronous DRAM (9)

- Latency (ctd.)
  - Example: The first word of data is transferred 5 clock cycles later.The latency is 5 clock cycles.

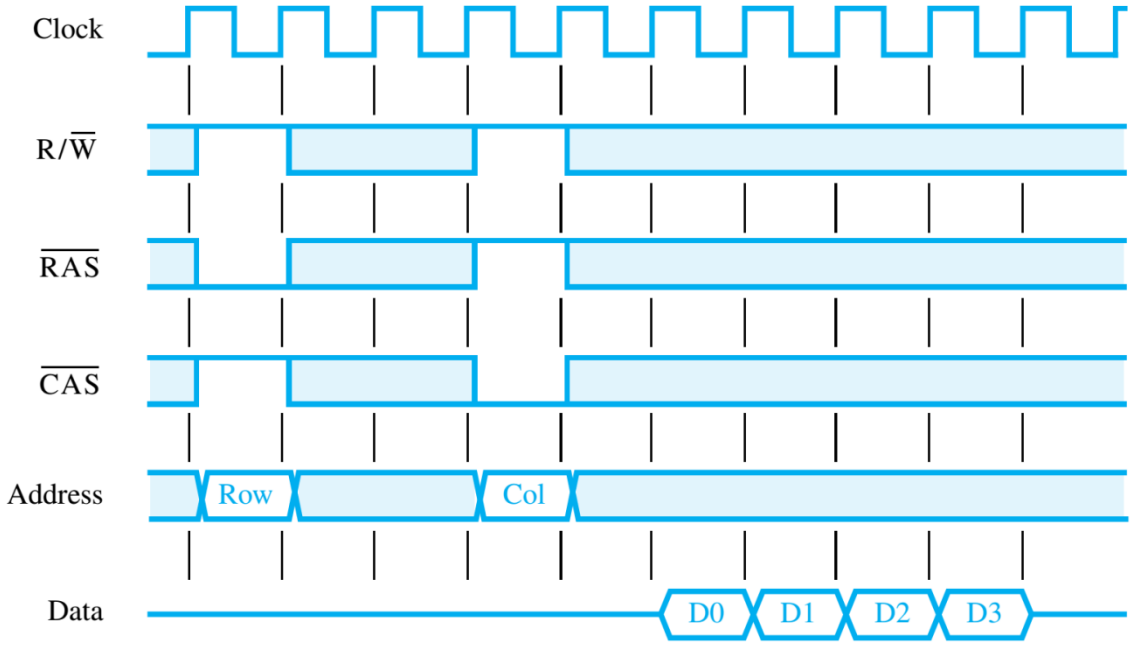


Figure 8.9 A burst read of length 4 in an SDRAM.

Synchronous DRAM (10)

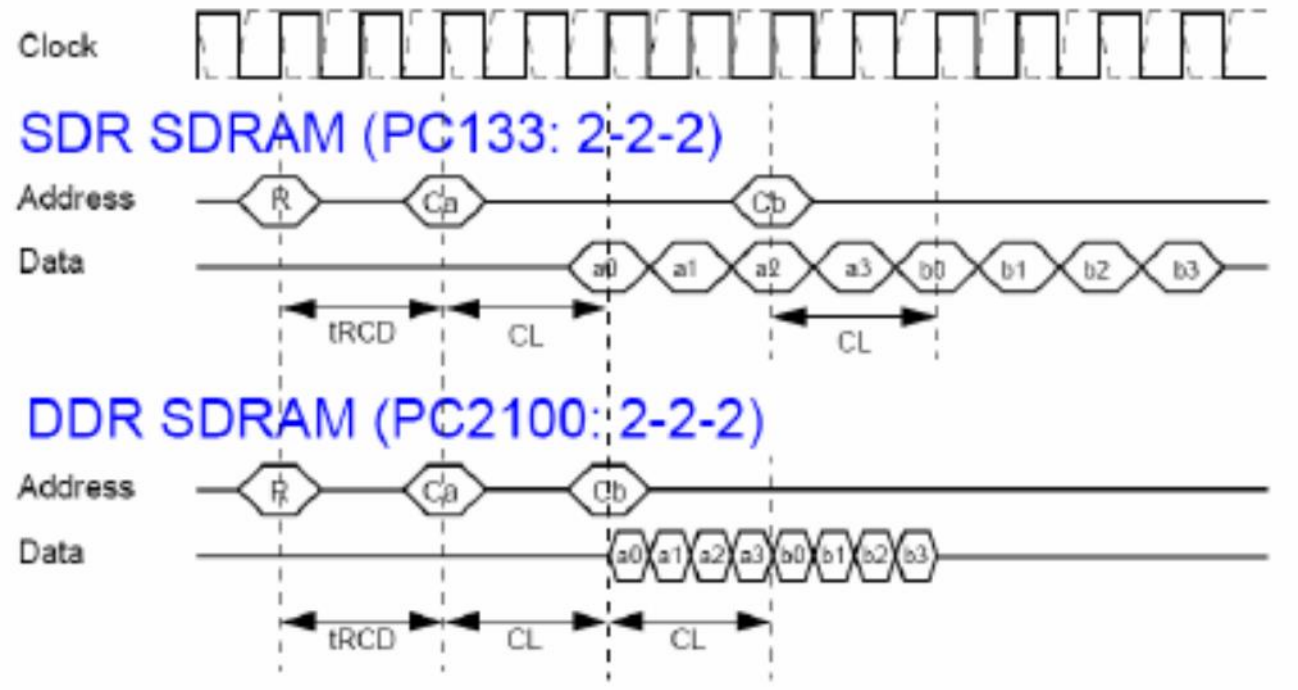
- Bandwidth
  - The number of bits or bytes that can be transferred in one second is referred to as *bandwidth*.
  - Unit :bit per second or byte per second
  - The bandwidth of a memory unit depends on the speed of access to the stored data and on the number of bits that can be accessed in parallel.
  - The effective bandwidth also depends on the transfer capability of the links that connect the memory and the processor, typically the speed of the bus.
  - Effective Bandwidth = Bus Speed $\times$ Bus Width

DDR SDRAM (1)

- In 2000, JEDEC released DDR Specification.
- DDR: double data rate
  - The latency is the same as for standard SDRAMs.
  - Uses both rising (positive) and falling (negative) edge of clock for data transfer. (typical 100MHz clock with 200 MHz transfer). (bandwidth ×2) (SDRAM only carries information on the rising edge of a signal.)
- DDR SDRAM also consumes less power, which makes it ideal for notebook computers.

DDR SDRAM (2)

- Example Timing Diagram



PC2100是指DDR的存取速度 2100MB/s, 即DDR266

DDR SDRAM (3)

- DDR Terminology

Name	Clock Freq.	Data Rate	Module Name
DDR200	100 MHz	200 MHz	PC1600
DDR266	133 MHz	266 MHz	PC2100
DDR333	167 MHz	333 MHz	PC2700
DDR400	200 MHz	400 MHz	PC3200

DDR2 SDRAM

- 2003 The first DDR2 memory module was released.
- By the end of 2004, DDR2 was surpassing DDR.
- 基于DDR技术，并在关键领域有所提升
  - FBGA package (更为良好的电气性能与散热性), 1.8V
  - 4-bit prefetch buffer, burst length = 4
  - Higher latency

	DDR	DDR II
数据传输率	200/266/333/400 MHz	400/533/667 MHz
总线频率	100/133/166/200 MHz	200/266/333 MHz
内存频率	100/133/166/200 MHz	100/133/166 MHz
Batch reading size	2/4/8	4/8
Data Strobe	Single DQS	Differential Strobe:DQS
CAS Latency	1.5, 2, 2.5	3+, 4, 5
Write Latency	1T	Read Latency-1
封装	TSOP	FBGA
发热量	大	小
针脚模组	184PIN	240PIN

DDR3 SDRAM

- 2007 DDR3 first introduced.
- DDR3 SDRAM
  - Comes with a promise of a power consumption reduction of 30%, 1.5V
  - "Dual-gate" transistors to reduce leakage of current.
  - 8 bit pre-fetch buffer, burst length = 8

Name	Clock Freq.	Data Rate	Module Name
DDR3-800	100 MHz	800 MHz	PC3-6400
DDR3-1066	133 MHz	1066 MHz	PC3-8500
DDR3-1333	166 MHz	1333 MHz	PC3-10600
DDR3-1600	200 MHz	1600 MHz	PC3-12800

DDR4 SDRAM

- 2005 JEDEC began developing DDR4.
- Scheduled to reach market by 2012.
  - Failed to do so.
  - Estimated to reach mass production by end of 2014.
- DDR4 Improvement
  - Transfer Rate
  - Data Integrity
  - Power Consumption
  - Memory Size
  - Command Encoding

DDR SDRAM Comparison

- Table

Feature/Option	DDR	DDR2	DDR3	DDR4	DDR4 Advantage
Voltage (core and I/O)	2.5V-2.6V	1.8V	1.5V	1.2V	Reduces memory power demand
Low voltage standard	No	Yes 1.55V	Yes (DDR3L at 1.35V)	Anticipated (likely 1.05V)	Memory power reductions
Data rate (Mb/s)	333, 400, 667, 800	533, 667, 800, 1066	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667, 3200	Migration to higher-speed I/O
Densities	256Mb to 1Gb	256Mb to 4Gb	512Mb–8Gb	2Gb–16Gb	Better enablement for large-capacity memory subsystems
Internal banks	4	4	8	16	More banks
Bank groups (BG)	0	0	0	4	Faster burst accesses

DDR5 SDRAM

- July 14, 2020, JEDEC published the final specification of DDR5.

Features	DDR4	DDR5	DDR5 Advantages
Speed	1.6 to 3.2 Gbps data rate 0.8 to 1.6 GHz clock rate	4.8 to 6.4 Gbps data rate 1.6 to 3.2 GHz clock rate	Higher bandwidth DDDR5-4800 initial designs
IO Voltage	1.2 V	1.1 V	Lower power
Power Management	On motherboard	On DIMM PMIC	Better power efficiency Better scalability
Channel Architecture	72-bit data channel (64 data + 8 ECC) 1 channel per DIMM	40-bit data channel (32 data + 8 ECC) 2 channels per DIMM	Higher memory efficiency Lower latency
Burst Length	BC4, BL8	BC8, BL16	Higher memory efficiency
Max. Die Density	16Gb	64Gb	Higher capacity DIMMs

Rambus

Advantages and Disadvantages

- Advantages of Dynamic RAM
  - High density
  - Low cost
- Disadvantages of Dynamic RAM
  - Longer memory access time
  - Leaky, needs to be refreshed
  - Cannot be easily integrated with CMOS

Summary of DRAM (1)

- 知识点DRAM
  - DRAM cell
  - DRAM Refresh
  - DRAM Chip
  - SDRAM
  - Burst Operation
  - Latency
  - Bandwidth

Summary of DRAM (2)

- 掌握程度
  - 了解DRAM Cell的存储原理和读写操作原理
  - 了解DRAM内部存储元的组织方式
  - 掌握DRAM芯片的外部引脚
  - 了解DRAM芯片Refresh
  - 掌握SDRAM的Burst Operation
  - 掌握latency特别是SDRAM的latency概念，掌握bandwidth的概念。

Exercises (1)

- Comparing to SRAM, the main advantage of DRAM is ( ).
  - A. high speed；
  - B. non-volatile stored data；
  - C. high density；
  - D. easily controlled；
- Solution:
  - C. high density；

Exercises (2)

- 简答: What are advantages and disadvantages of DRAM?
- Solution:
  - Advantages
    - High density
    - Low cost
  - Disadvantages
    - Longer memory access time
    - Leaky, needs to be refreshed
    - Cannot be easily integrated with CMOS

Contents of this lecture

- 8.2 Semiconductor RAM Memories
  - Static RAM
  - Dynamic RAM
  - Structure of Larger Memories

Structure of Larger Memories

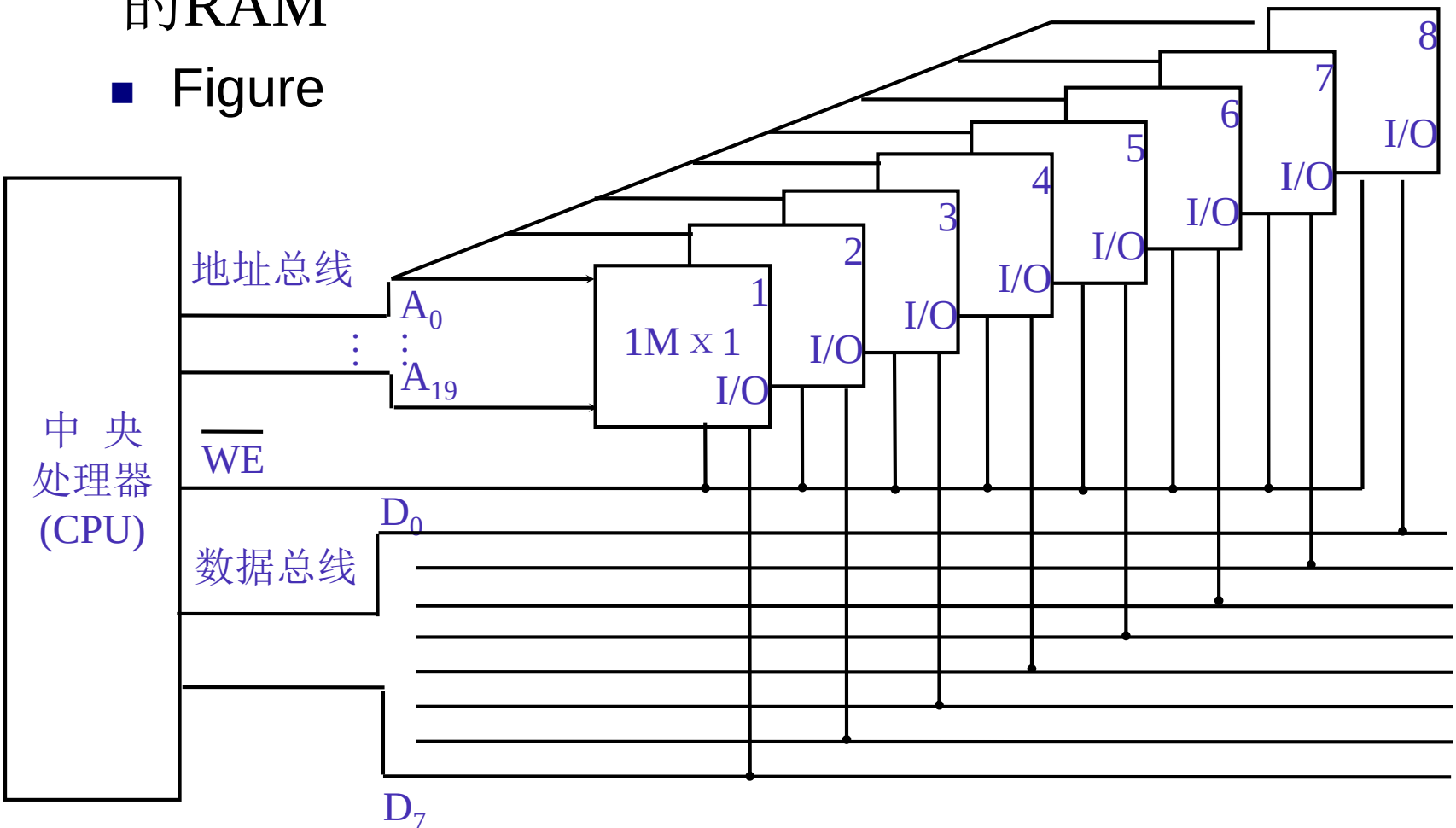
- Static Memory Systems
  - How to connect a number of static memory chips to form a much larger memory?
    - 位扩展法
    - 字扩展法
    - 字位同时扩展法
- Dynamic Memory Systems
  - How to connect a number of dynamic memory chips to form a much larger memory?

Static Memory Systems (1)

- 位扩展法
  - 芯片每个存储单元的位数小于存储器字长，需进行位扩展。
  - 例：用1M×1位存储芯片组成1M×8位（1MB）的RAM
    - 共需要8片1M×1位存储芯片，每片存储同一位权的一位数据（片的I/O端接D_i）
    - 访问芯片需20位地址码：A_{19}~A_0
    - $\overline{WE}$:写读控制信号

Static Memory Systems (2)

- 位扩展法 (ctd.)
  - 例：用1M×1位存储芯片组成1M×8位（1MB）的RAM
    - Figure

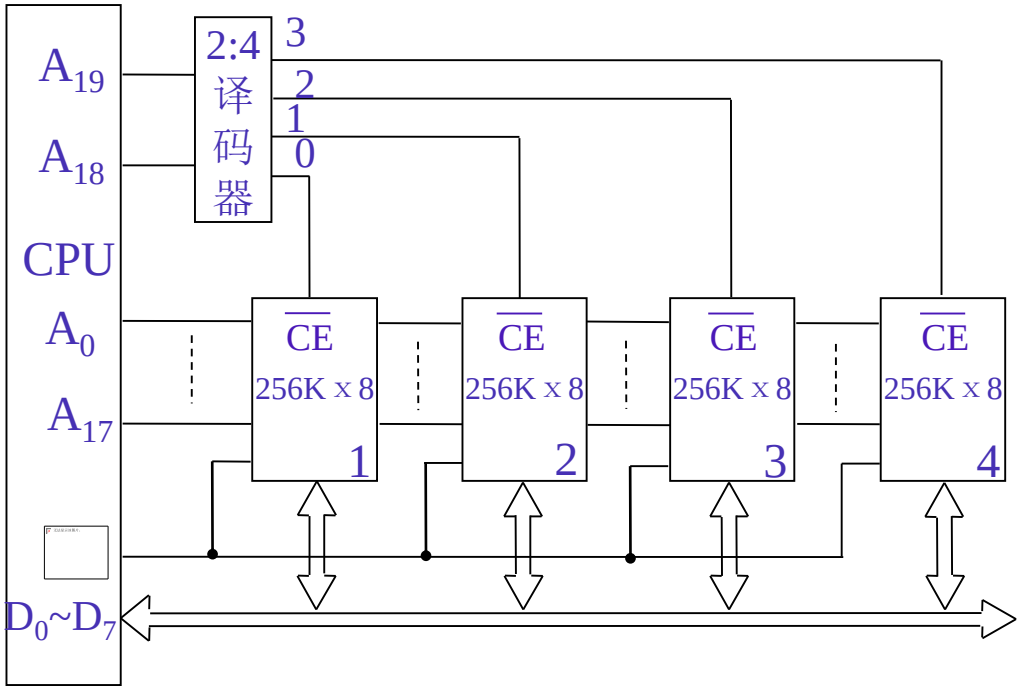


Static Memory Systems (3)

- 字扩展法
  - 芯片每个存储单元的位数等于存储器字长，但容量(字数)不够，需进行字扩展。
  - 例：用256K×8位芯片组成1MB的RAM
    - 1MB容量需20位地址码(A_{19}~A_0)
    - 256KB芯片需18位片内地址码(A_{17}~A_0)
    - 用高二位地址$A_{19}A_{18}$经2:4译码器（74139）选择芯片读/写
    - 每片8条I/O线分别接D_7~D_0

Static Memory Systems (4)

- 字扩展法 (ctd.)
  - 例：用256K×8位芯片组成1MB的RAM
    - Figure

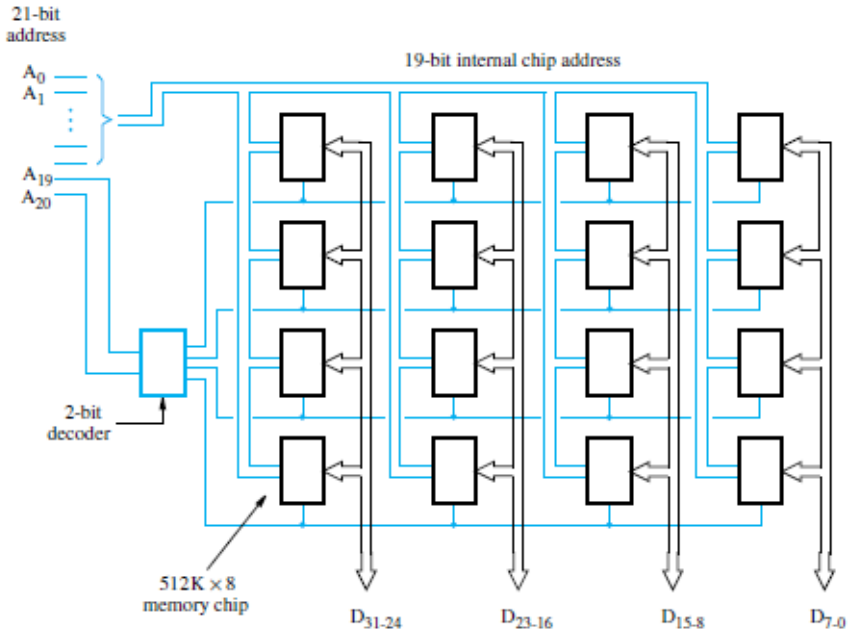


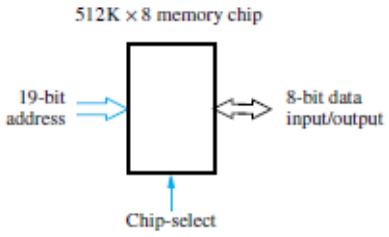
Static Memory Systems (5)

- 字位同时扩展法 (ctd.)
  - Assume that the capacity of a memory unit is M × N bit, if constituted of using l × k bit chips, the number of total chips needed is (M/l) × (N/k).
  - Example: Using 512K × 8 static memory chips to implement a memory of 2M × 32.
    - Total chips = $\frac{2\times 1024}{512}\times\frac{32}{8} = 4\times 4 = 16$

Static Memory Systems (6)

- 字位同时扩展法 (ctd.)
  - Example: Using 512K × 8 static memory chips to implement a memory of 2M × 32 .
    - Figure





Static Memory Systems (7)

- 补充例题：

用8K×8位的ROM芯片和8K×4位的RAM芯片组成存储器，按字节编址，其中RAM的地址为0000H-5FFFH，ROM的地址为C000-FFFFH，画出此存储器组成结构图及与CPU的连接图。

Static Memory Systems (8)

- 解答：

RAM的地址范围展开为：

000 0000000000000 ~

010 1111111111111

A_{12} ~ A_0从0000H ~ 1FFFH，容量为8K，高位地址$A_{15}A_{14}A_{13}$从000 ~ 010，所以RAM的总容量为：8K×3=24K。

RAM用8K×4的芯片组成，需8K × 4的芯片6片。

Static Memory Systems (9)

- 解答：

ROM的末地址 – 首地址=FFFFH – C000H= 3FFFH，所以ROM的容量为2^{14}=16K。

ROM用8K×8的芯片组成，需8K×8的芯片两片。

ROM的地址范围展开为：

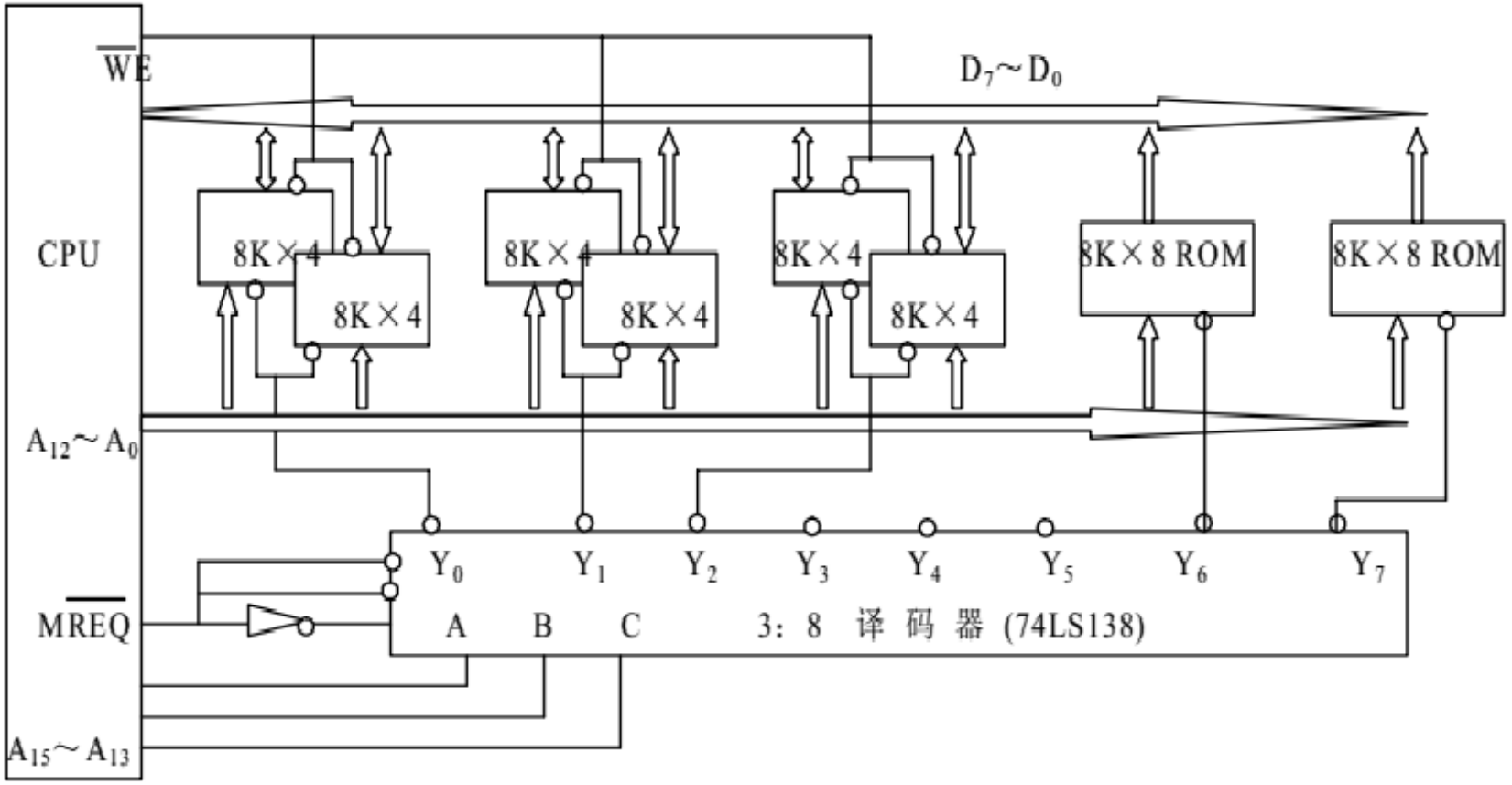
1100 0000 0000 0000 ~

1111 1111 1111 1111

高位地址从110 ~ 111。

Static Memory Systems (10)

- 解答：



Dynamic Memory Systems (1)

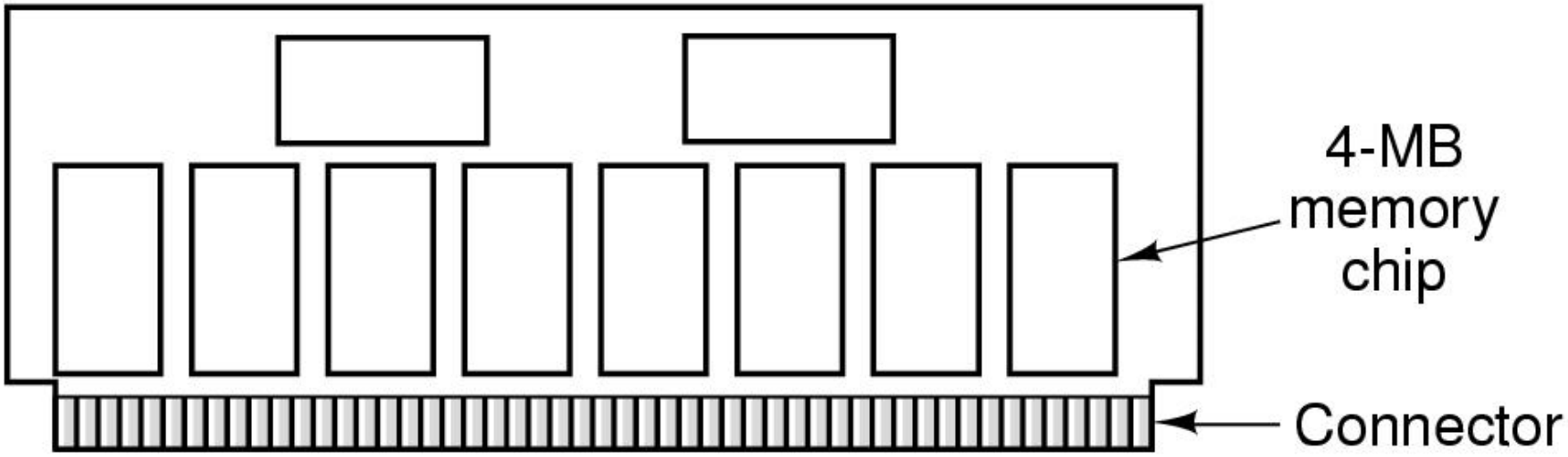
- Dynamic Memory Systems
  - The organization of large dynamic memory systems is essentially the same as the above static memory system.
  - Packaging: Memory Module
    - SIMM (Single In-line Memory Modules)
    - DIMM (Double In-line Memory Modules)

Dynamic Memory Systems (2)

- SIMM (Single In-line Memory Modules)
  - A SIMM is a basic DRAM packaging type that fits most older systems.
  - Single-sided: RAM chips on one side only
  - Double-sided: RAM chips on both sides
  - 30-pin SIMM: 256KB,1MB,4MB,16MB;8 bits; plus 1bit for parity; single-sided
  - 72-pin SIMM: 1MB, 4MB, 16MB (single-sided); 2MB, 8MB, 32MB (double-sided); 32 bits, plus 4 bits for parity/ECC.

Dynamic Memory Systems (3)

- SIMM (ctd.)
  - Example: A single inline memory module (SIMM) holding 32MB. Two of the chips control the SIMM.

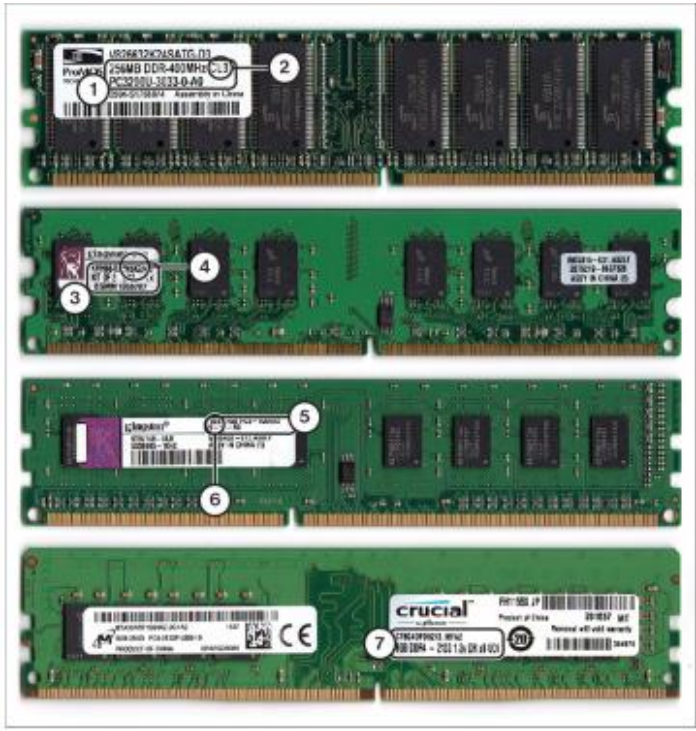


Dynamic Memory Systems (4)

- DIMM (Double In-line Memory Modules)
  - At present, DIMMs are the standard way for memory to be packaged.
  - A DIMM is capable of delivering 64 data bits at once.
  - Differences between SIMM and DIMM
    - DIMMs have separate electrical contacts on each side of the module, while the contacts on SIMMs on both sides are redundant.
    - Standard SIMMs have a 32-bit data path, while standard DIMMs have a 64-bit data path.

Dynamic Memory Systems (5)

- DIMM (Double In-line Memory Modules)
  - Figure: From top to bottom, DDR, DDR2, DDR3, and DDR4 DIMM desktop memory modules.
    - 1: 256MB DDR module,
    - PC3200 (DDR400)
    - 2: CL3 latency
    - 3: 2GB DDR2 module (from
    - matched set), DDR2-667 (PC2-530(
    - 4: CL5 latency
    - 5: 2GB DDR3 module,
    - PC3-10600 (DDR3-1333)
    - 6: CL9 latency
    - 7: 8GB DDR4 module, DDR4-2133 (PC4-17000)

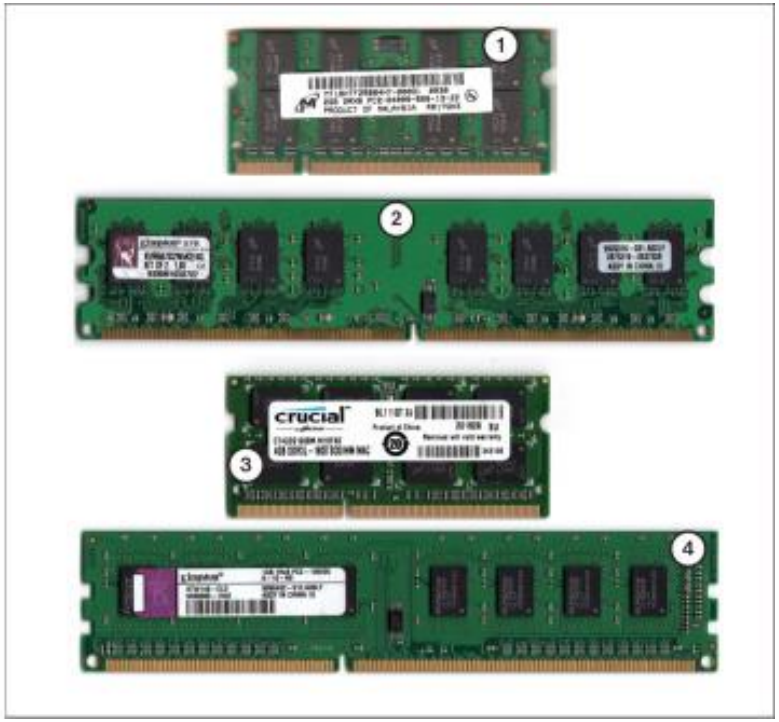


Dynamic Memory Systems (6)

- SO-DIMM
  - Most desktop computers use full-sized memory modules known as DIMMs.
  - Laptop computers and some small-footprint mini-ITX motherboards and systems use reduced-size memory modules known as small outline DIMMs (SO-DIMMs).

Dynamic Memory Systems (7)

- SO-DIMM (ctd.)
  - Figure: DDR2 SODIMM and DIMM modules compared to DDR3 SODIMM and DIMM modules.
    - 1: DDR2 SO-DIMM
    - 2: DDR2 DIMM
    - 3: DDR3 SO-DIMM
    - 4: DDR3 DIMM



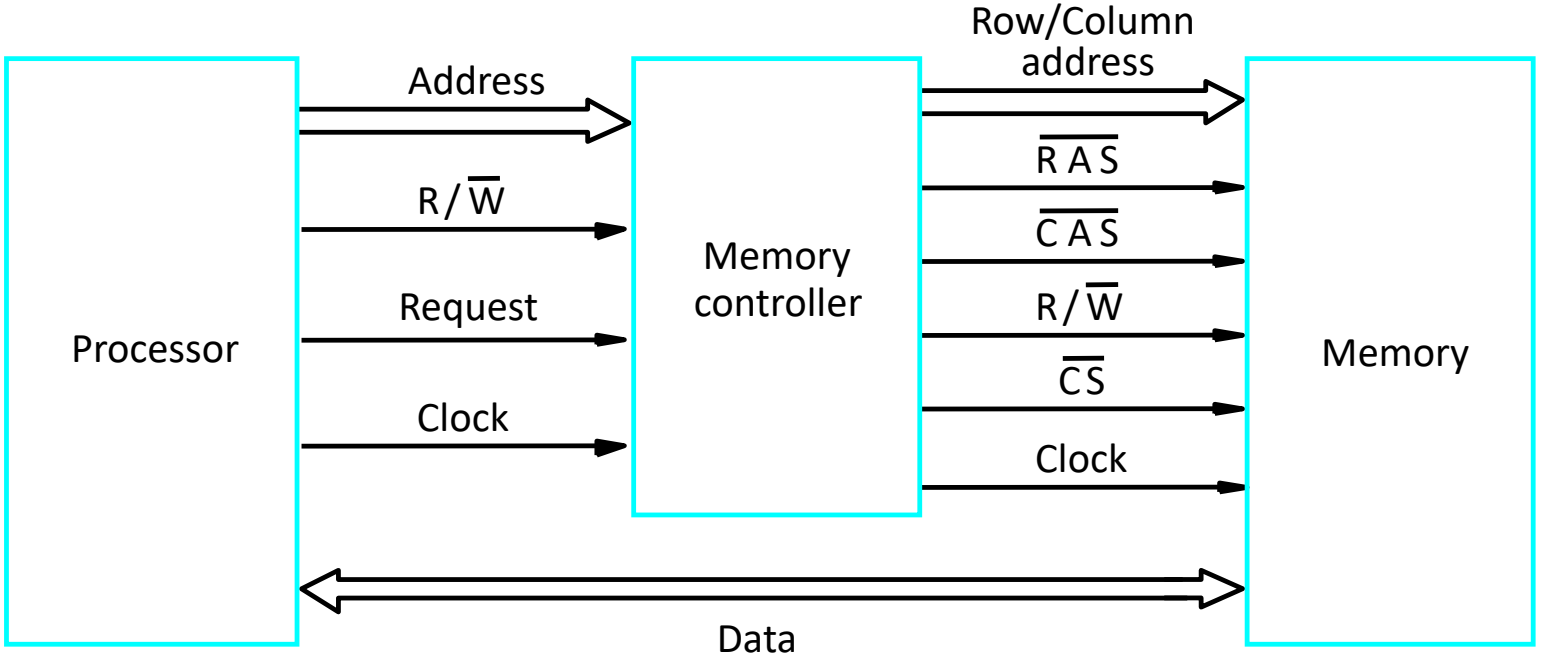
Dynamic Memory Systems (8)

- DIMM (ctd.)
  - Table: DDR SDRAM Comparisons

RAM Type	Pins(DIMM)	Pins(SODIMM)	Common Type and Speed
DDR	184	200	PC3200=400MHz/3200 Mbps
DDR2	240	200	DDR2-800(PC2-6400)=800MHz/6400Mbps
DDR3	240	204	DDR3-1333(PC3-10600)=1333MHz/10600 Mbps
DDR4	288	260	DDR4-2400(PC4-19200)=2400MHz/19200 Mbps

Memory Controller (1)

- A typical processor issues all bits of an address at the same time, a multiplexer is required.



Memory Controller (2)

- Request Signal
  - Indicate a memory access operation is needed.
- When used with DRAM chips which do not have self-refreshing capability, the memory controller has to provide all the information needed to control the refreshing process.

Choice of Technology

- The choice of a RAM chip for a given application depends on
  - Cost
  - Speed
  - Power dissipation
  - Size of the chip
- Static RAMs
  - Cache
- Dynamic RAMs
  - Synchronous DRAMs: main memory

Types of Semiconductor Memory

- Semiconductor RAM and ROM

<table>
<tr><th>Memory Type</th><th>Category</th><th>Erasure</th><th>Volatility</th></tr>
<tr><td>RAM</td><td>Read-Write</td><td>Electrically</td><td>Volatile</td></tr>
<tr><td>ROM</td><td rowspan="2">Read-only Memory</td><td rowspan="2">Not possible</td><td rowspan="5">Nonvolatile</td></tr>
<tr><td>PROM</td></tr>
<tr><td>EPROM</td><td rowspan="3">Read-mostly Memory</td><td>UV light</td></tr>
<tr><td>EEPROM</td><td>Electrically</td></tr>
<tr><td>Flash memory</td><td>Electrically</td></tr>
</table>

Uses for Nonvolatile Memories

- Firmware programs stored in a ROM (BIOS, controllers for disks, network cards, graphics accelerators, security subsystems,…)
- Solid state disks (flash cards, memory sticks, etc.)
- Smart cards, embedded systems, appliances
- Disk caches

Summary

- 知识点: Structure of Larger Memories
  - Static Memory Systems
    - 位扩展法
    - 字扩展法
    - 字位同时扩展法
- 掌握程度
  - 使用指定的芯片构造大容量存储器，能够分析出使用多少片芯片，画出芯片排列情况，数据线、地址线、片选线连接正确。

Exercises (1)

- Consider a 64M×16 memory built by using 512K×8 memory chips. How many memory chips are needed?
  - A. 32;
  - B. 64;
  - C. 128;
  - D. 256;
- Solution:
  - D.256

Exercises (2)

- Consider a 16M×128 memory built by using 512K×16 memory chips. How many rows of memory chips are needed?
  - A. 8;
  - B. 16;
  - C. 32;
  - D. 64;
- Solution:
  - C.32

Homework

- P328　8.2, 8.3
- 补充题：

2.　Assume that there are two types of static memory chips: 128×8 bit (total 4 chips) and 512×4 bit (total 2 chips). Please use these memory chips to implement a 512×16 bit memory. Draw the figure of the memory organization.