

Chapter2补充题

1. Consider a processor with 64 registers and an instruction set of size 15. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a 12-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, what is the amount of memory (in bytes) consumed by the program text?

Solution:

Number of registers=64

Number of bits to address register= $\lceil \log_2 64 \rceil = 6$ bits

Number of instructions=15

Opcode size= $\lceil \log_2 15 \rceil = 4$

Opcode(4)	Reg1(6)	Reg2(6)	Reg3(6)	Immediate(12)
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Chapter2补充题

1. (ctd.)

Solution: (ctd.)

Total bits per instruction = $4 + 6 \times 3 + 12 = 34$ bits

Total bytes per instruction = 4.25 bytes

Due to byte alignment we can not store 4.25 bytes, without wasting 0.75 bytes.

So, total bytes per instruction = 5

Total number of instructions = 100

Total size = number of instructions \times Size of an instruction
= $100 \times 5 = 500$ bytes

Chapter 2 补充题

2. Design a 16-bit instruction format using expanding opcode for the following: 14 three-address instructions, 30 two-address instructions, 30 one-address instructions, 32 zero-address instructions. Assume that there are 16 registers and operands are placed in register.

Solution:

16 registers → 4-bit address field for one operand in the instruction

(1) 3-address instruction format

4-bit opcode 0000-1101, 12-bit address field for 3 register address.

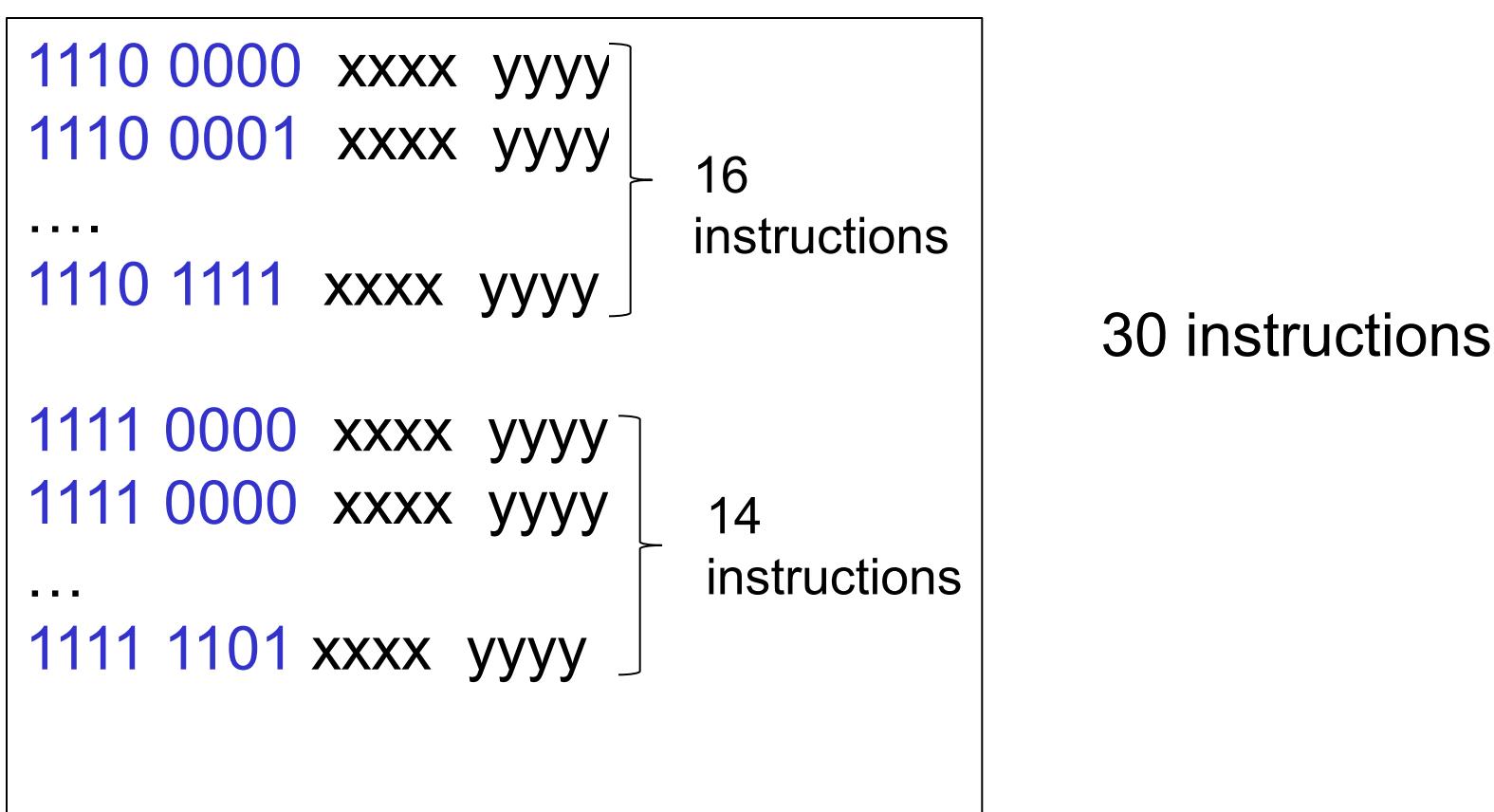
0000	xxxx	yyyy	zzzz
0001	xxxx	yyyy	zzzz
...			
1101	xxxx	yyyy	zzzz

14 instructions

Chapter 2 补充题

(2) 2-address instruction format:

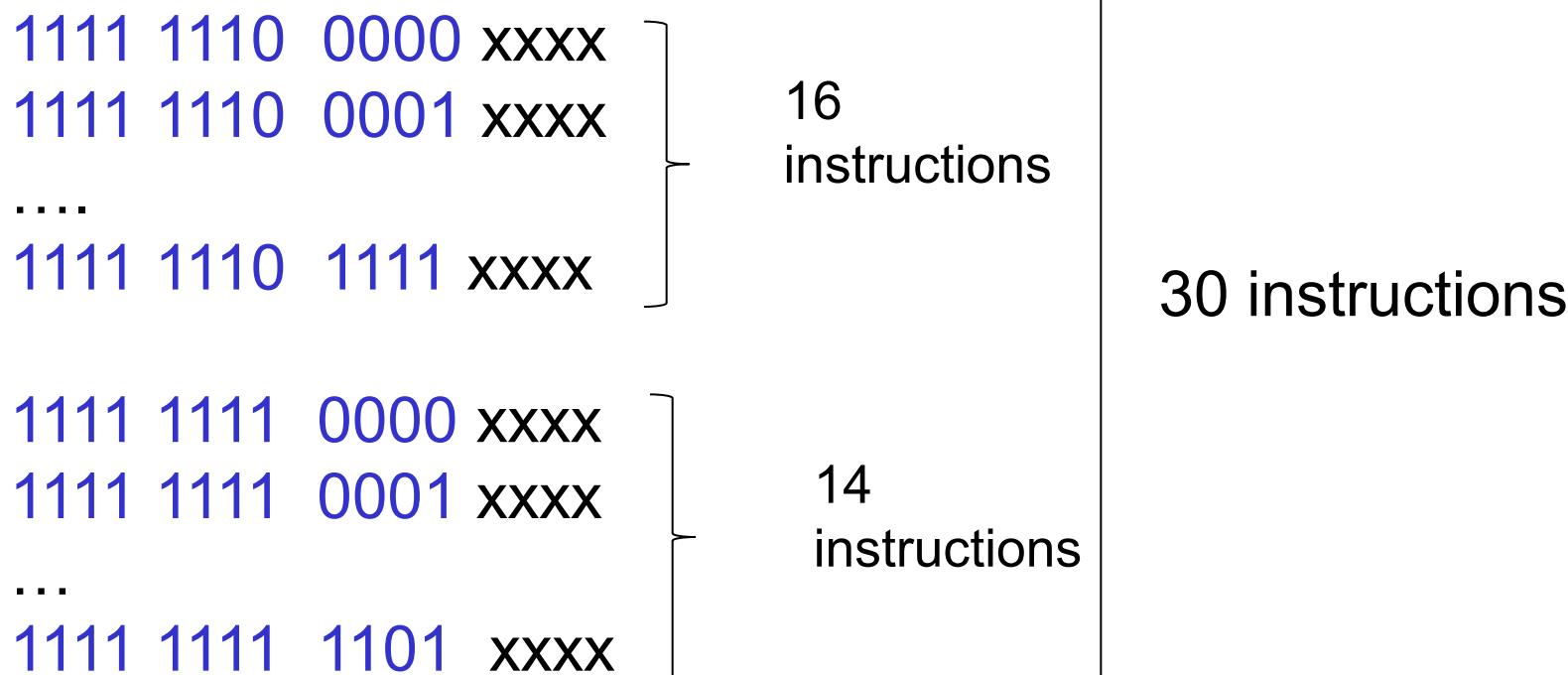
8-bit opcode 11100000-11101111(16条), 11110000-11111101(14条), 8-bit address field for 2 register address.



Chapter 2 补充题

(3) 1-address instruction format:

12-bit opcode 111111100000-111111101111(16条),
111111110000-111111111101(14条), 4-bit address field for 1
register address.



Chapter 2 补充题

(4) 0-address instruction format:

16-bit opcode 111111111100000-111111111101111(16条),
111111111110000-111111111111111(16条)

1111 1111 1110 0000
1111 1111 1110 0001
....
1111 1111 1110 1111

16
instructions

32 instructions

1111 1111 1111 0000
1111 1111 1111 0001
....
1111 1111 1111 1111

16
instructions

Chapter 5 5.4 Solution

Register contents are read in step 2 and loaded into the inter-stage registers at the end of that clock period.

下表列出的是每个周期开始时的各寄存器值

Step	RA	RB	RZ	RY	R6
3	1000	2500	*	*	7500
4	1000	2500	-1500	*	7500
5	1000	2500	-1500	-1500	7500
1	1000	2500	-1500	-1500	-1500

* These values are determined by the previous instruction.

5.4 Solution (ctd.)

下表列出的是每个周期结束时的各寄存器值

Step	RA	RB	RZ	RY	R6
3	1000	2500	-1500	*	7500
4	1000	2500	-1500	-1500	7500
5	1000	2500	-1500	-1500	-1500
1	1000	2500	-1500	-1500	-1500