Soft IP cores

RISC-V Processors and More

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Background

Processor Evolution

- Hardcore processors enjoyed dominance in the field of IC design.
- These processors, physically constructed on silicon at the transistor level, provided a specialized and efficient solution.
- Challenges emerged like customization, prototyping inefficiencies and customizability.
- This resulted in the development of soft processors. Softcore processors have a critical advantage which is configurability.

Intel i7 hardcore processor

Microblaze Soft-Processor

Soft Cores

Significance in IC Design

- A soft core is a pre-defined HDL model of a microprocessor or digital logic, typically tailored for a specific application.
- Designed using Tools like Xilinx Vivado, Intel Quartus Prime, Lattice Diamond, and Altium Designer.
- Synthesizable for Different Target.
- The design process can be complex but made easier by reusable Intellectual properties.

Benefits of Soft Cores

Significance in IC Design

- Reduced PCB footprint.
- Rapid Prototyping.
- Cost Savings: Softcores eliminate expensive manufacturing and customization processes inherent in hardcore design.
- Faster Time to Market: HDL based nature streamlines design to market deployment process.

Types of Soft Core

- Microblaze by Xilinx
- Picoblaze by Xilinx
- Open RISC by OpenCores

Softcore Vs Hardcore

- Performance trade-off
- Memory
- System Complexity

	MICROBLAZE ON ARTY	ARDUINO UNO REV 3	RASPBERRY PI 3
Processor Speed	100 MHz	16 MHz	1.2 GHz
RAM	256 MB DDR3L	2K SRAM	1 GB LPDDR2
Operating System	No	No	Yes

A comparison of a few of the capabilities of the most popular hardware microcontroller development boards with that of the ARTY, a development board for the Artix 7 FPGA. The Raspberry Pi has a higher clock speed and more RAM than either the Arduino or ARTY, but it requires an operating system to run more than one thread, which may not permit timing-critical applications, such as data acquisition, that are intolerant of jitter.

- *Hardcore: High performance, more memory.*
- *Softcore: Flexibility for rapid prototyping, leading to finalized hardcore designs.*

RISC-V Architecture

ISA (Instruction set architecture)

- CISC dominance.

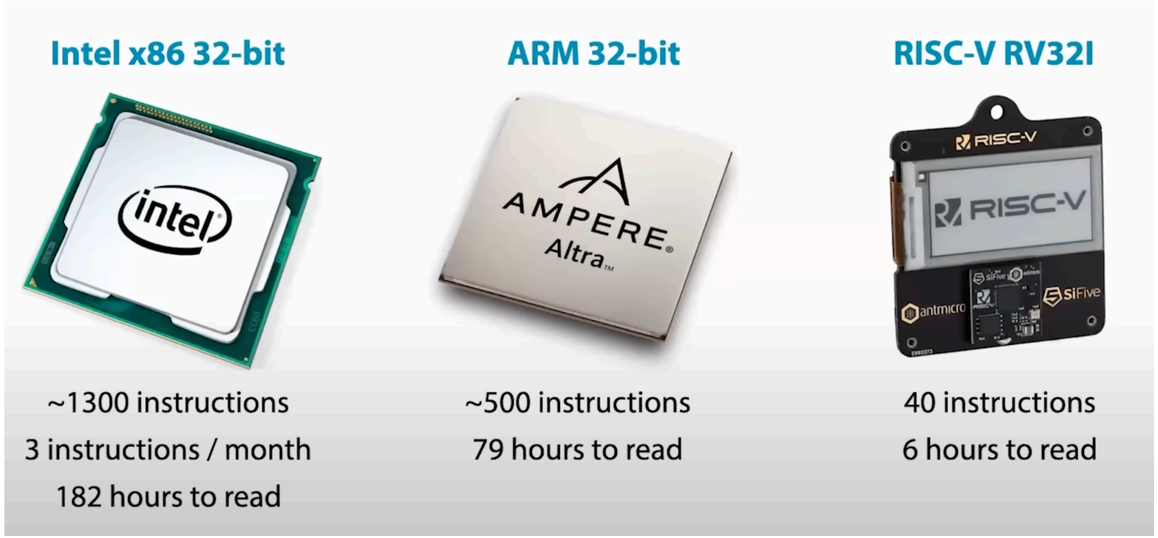
- A Desire for more efficiency and Customizability in Industry 4.0 applications.

- Reduced instruction set computer architecture (RISC), Known for simplicity, open source and modularity.

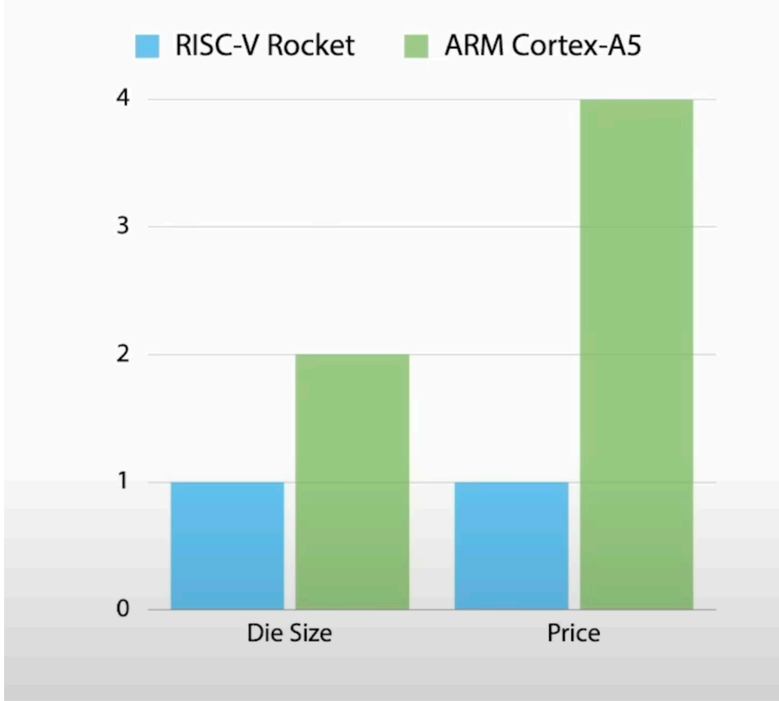
- RISC-V ISA defines processor operations using RISC principles for efficient functionality.

RISC-V logo

RISC-V Comparisons



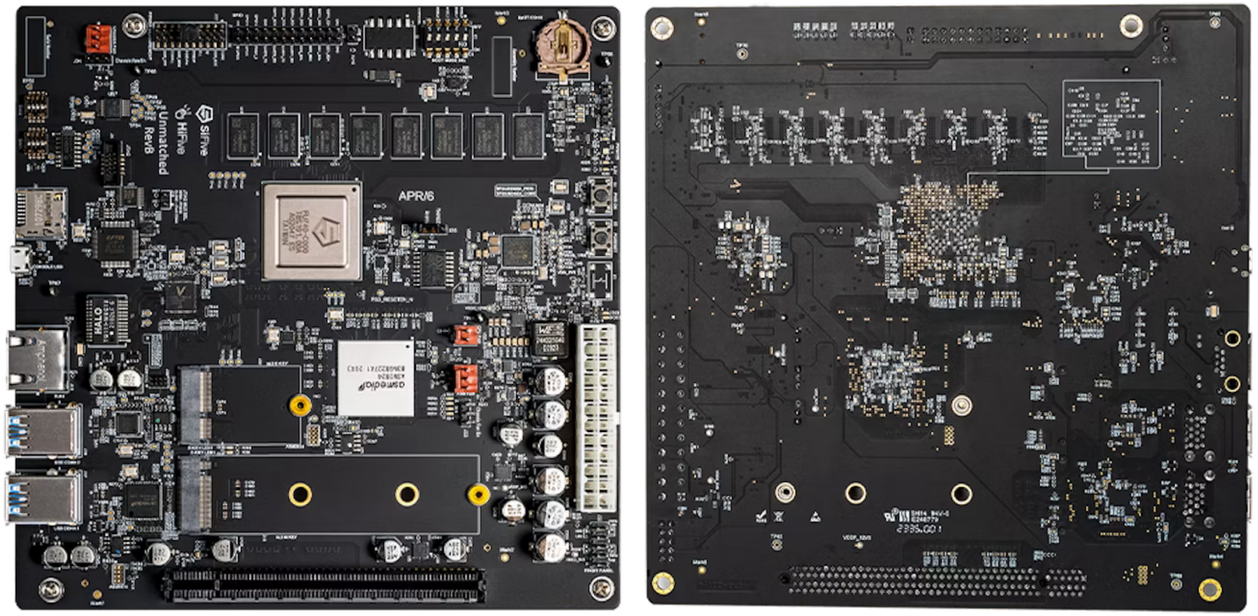
Instructions Comparison



Rocket vs Cortex A5

- Despite similar performance, Risc-v is half the die size meaning half the price.
- In microcontrollers we can get a significantly smaller chip based on this.

Available RISC-V solutions



Hi Five Unmatched by Sifive

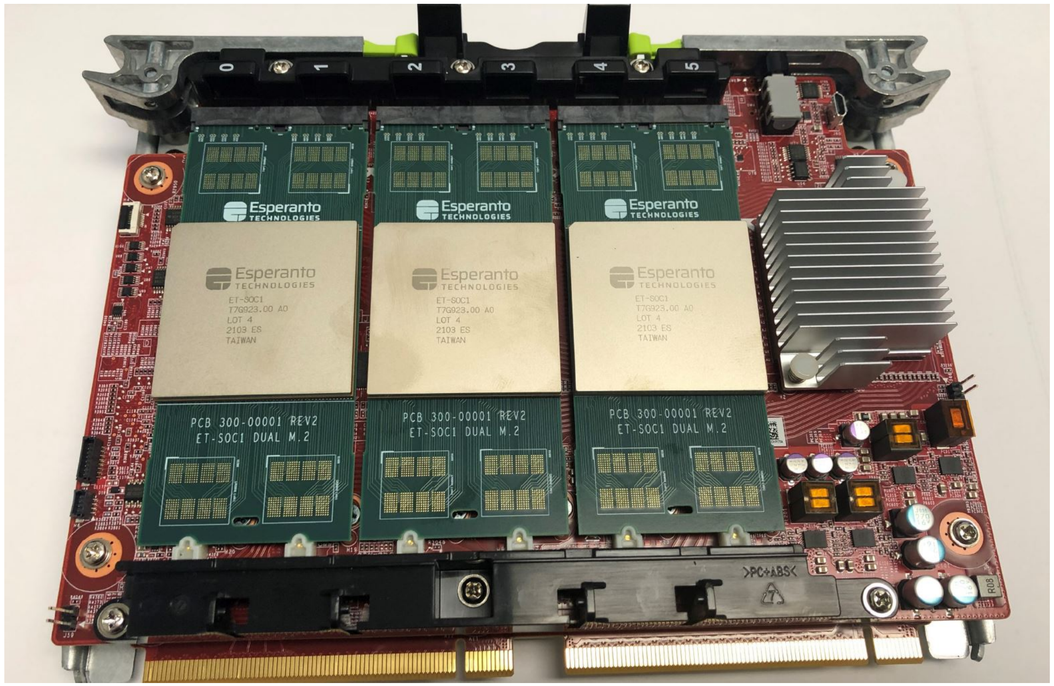
- Personal Computer
- Multi-core, Linux-capable RISC-V hardware

Sipeed MaixDuino

IoT- RISC-V

- Dual Core 64-bit RISC-V CPU
- Neural network processor
- Tensorflow for Deep learning

Available RISC-V solutions



ESPERANTO ET-SOC-1

- Most advanced RISC based Chip.
- Competes with advanced machine learning chips like NVIDIA H100.
- 1088 ET-minion RISC-V cores with Vector Processing Unit.

Advantage

- < 20 watts for machine learning.
- NVIDIA H100 uses up to 700 watts.

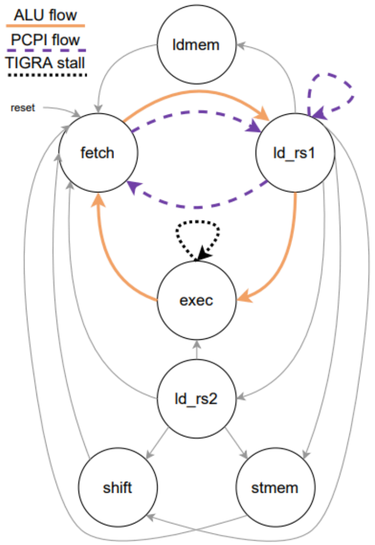
Importance of RISC-V in Soft Processors

- Open Source: Unrestricted access, inclusive option for soft core developers.
- Pipelining: Effective pipelining compared to CISC.
- Modular Design: Selective implementation of features.
- Load-Store Architecture: Simplifies memory access patterns.
- Acceleration: The optimized instruction set in RISC-V reduces compute overhead when deployed on a power optimized hardware platform, particularly on an FPGA.

RISC-V logo

Examples of RISC-V Soft Processors

- PicoRV32: Minimalistic but efficient!
- NeoRV32: User-friendly and configurable, offers more performance than the PicoRV32.
- SiFive Intelligence Family: Optimized for machine learning
- SiFive Performance Family: For Intensive Computations.



State machine for PICO RV32

Case Study

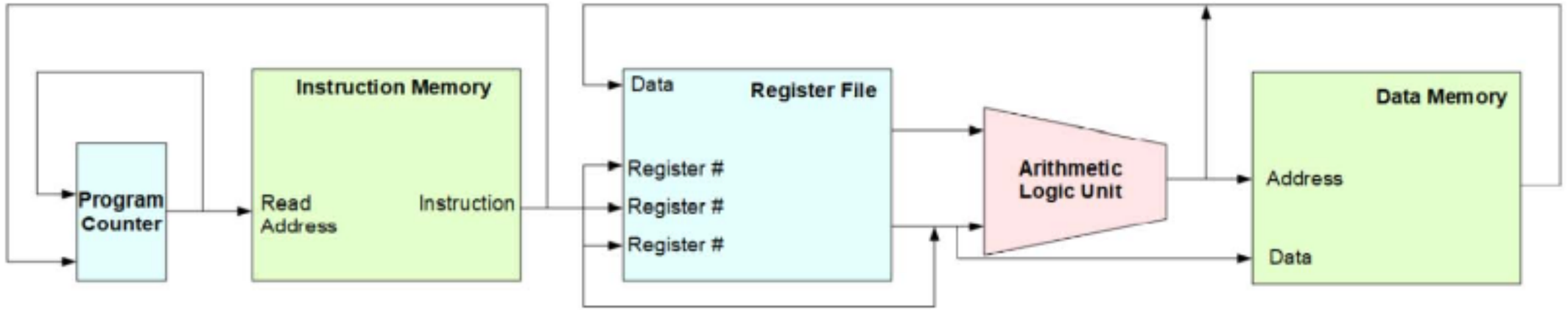
Implementing a RISC-V Soft core

- Simple design, No Pipelining, Havard architecture.

Case Study

Process Architecture

All Blocks are first Implemented at RTL level in System Verilog



Processor Architecture

Implementing a RISC-V Soft core

Actual Implementation

- Typically at this stage designs are sent to the manufacturer to be fabricated onto an ASIC.

- However, for softcore processors, instead of fabrication, we generate a bitstream to configure an FPGA.

Results

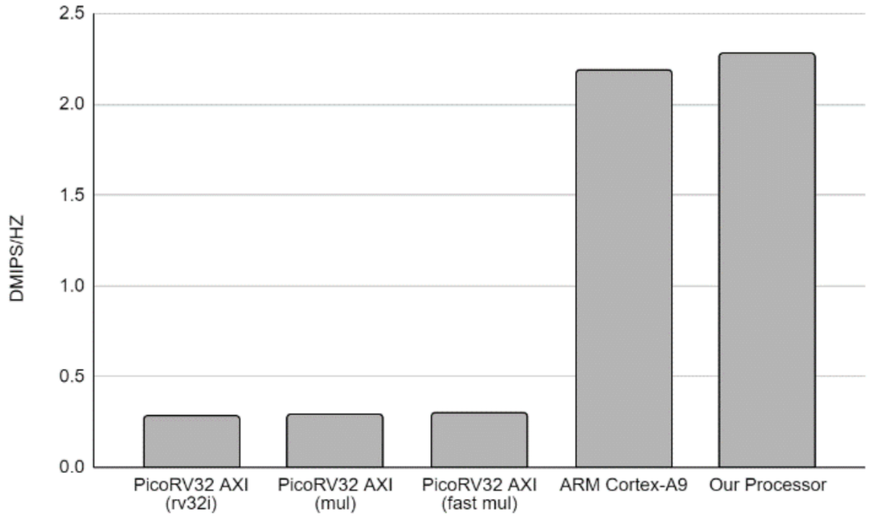
- *Each instruction is executed in one cycle.*
- *Commendable Resource efficiency*
- *Performance on Par with well known processors like ARM cortex- A9*

```
ld r0, 33, r1
add r1, r2, r31
add r2, r0, r1
add r31, r0, r2
add r31, r0, r2
beq r0, r0, -2
```

Instruction For Fibonacci sequence

Resource	Utilization	Utilization %
Look-up tables	322	1.55
Flip-Flops	229	0.55
IO	18	16.98

Resource Utilization



Benchmark Using Dhrystone test.

Challenges

- Vulnerable to Single event Upsets(SEUs).
- Performance: Cannot match Hardware.
- Clock Speeds: Hardware is superior.

Conclusion

In conclusion, while hardcore processors offer the pinnacle of performance and speed due to their custom-tailored fabrication, softcore processors stand out for their flexibility and adaptability, thanks to their FPGA-based design. This makes softcores ideal for specialized applications where customization and rapid prototyping are key. As technology advances, the gap between softcore and hardcore processors continues to close, making softcore processors an increasingly viable option for a wide range of applications.

Thanks For Listening!