Proceedings of the 8th International Conference on Communication and Electronics Systems (ICCES 2023)
IEEE Xplore Part Number: CFP23AWO-ART; ISBN: 979-8-3503-9663-8

Design and Implementation of RISC-V based Pacemaker

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2023 8th International Conference on Communication and Electronics Systems (ICCES) | 979-8-3503-9663-8/23/$31.00 ©2023 IEEE | DOI: 10.1109/ICCES57224.2023.10192752

***Abstract*— Heart failures are highly increasing in modern times, regardless of patients' age or genders. Arrhythmia is a severe cardiac condition that affects roughly 5% of the world's population and causes severe damage to patients and may result in death. There is just one solution to this problem that is to regulate your heart rate. A pacemaker is an implanted medical device, which is already available on the market. However, the existing device consumes more power, ranging from 60 micro watts to 100 micro watts. Here, this research work suggests using RISC-V CPU to minimize power and area. The proposed design of RISC-V based pacemaker is implemented using 90nm technology node. The proposed RISC-V model consumes 4.053223 microwatts when compared with existing pacemaker.**

***Index Terms*—Arrhythmia, ASIC-Application specific integrated circuit, RISC-V ('RISC' means Reduced instruction set computer and 'V' means fifth generation), Pacemaker.**

I. INTRODUCTION

Modern society is experiencing an alarming rise in heart failure, independent of the age or gender of the patient. Arrhythmia is one of the main heart conditions that affects about 5 percentage of the world's population, causes severe harm to patients, and may even result in death. Arrhythmia is a medical condition that affects the electrical impulses that control the heart's rhythm. The heart is controlled by an electrical system that sends signals to the heart muscle, causing it to contract and pump blood. When this system is disrupted, it can lead to abnormal heart rhythms or Arrhythmia. There are various types of arrhythmia. Bradycardia, Tachycardia, Atrial fibrillation, Ventricular fibrillation are the most common types of arrhythmia, affecting millions of people worldwide. It occurs when the heart's upper chambers (atria) [1] beat irregularly and out of sync with the lower chambers (ventricles), leading to a range of symptoms, including palpitations, dizziness, fainting, chest pain, and shortness of breath. To overcome this situation, we are providing solution to this problem, there is an implantable medical device called a pacemaker. There are various types of pacemakers like single chamber, dual chamber, bi ventricular pacemaker, etc are available on the market and most of the pacemaker apparatuses are not quite efficient. In order to improve the power efficiency of the pacemaker RISC-V processor architecture and be used for their unique requirements, the ISA can be modified. Because of this, RISC-V is especially well suited for usage in embedded devices and other niche applications where customization is crucial. The use of RISC-V in the creation of medical devices, particularly pacemakers, has gained popularity in recent years. Manufacturers of medical devices may gain from RISC-V's improved performance, reduced power consumption, and heightened security [2]. RISC-V's modular architecture enables the development of unique processor architectures that may be tailored for a variety of jobs, which improves performance. Improved performance in pacemakers and other medical devices that depend on accurate and effective processing of electrical impulses can result from this. The modular structure of RISC-V also enables the development of CPU designs with low power consumption.

II. LITERATURE SURVEY

Millions of people globally are afflicted by arrhythmias, which are abnormal heart rhythms. Genetics, advanced age, underlying cardiac illness, electrolyte imbalances, and drug side effects are just a few of the causes of arrhythmias. Atrial fibrillation, ventricular tachycardia, and supra ventricular tachycardia [3] are a few examples of prevalent arrhythmias. About 2.7 million people experience rhythms each year, according to the American Heart Association. Arrhythmias are more common in older people than in younger adults, and their incidence rises with age [4]. Arrhythmias are slightly more common in males than in women, but both genders experience them at roughly the same rates. However, some rhythms, like atrial fibrillation, may affect women more frequently. It's crucial to remember that not all arrhythmias need to be treated, but some of them can be severe and demand medical attention.

Arrhythmias can cause palpitations, fainting, dizziness, loss of breath, and chest discomfort. It's crucial to consult a healthcare professional if you experience any of these signs.

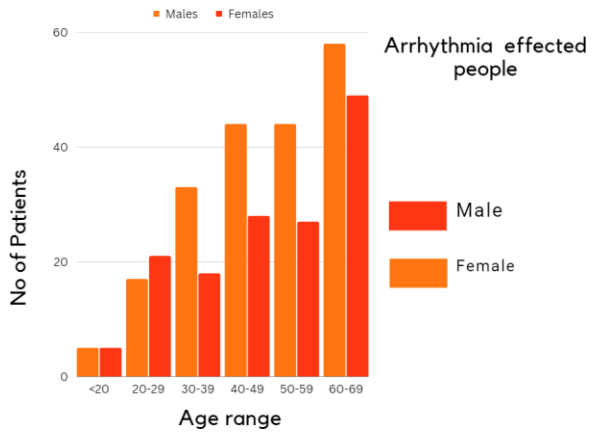

Fig. 1. Patients suffering from Arrhythmia

Figure 1 makes it abundantly evident that men are more prone than women to experience arrythmia and other health problems between the ages of 40 and 60 [5]. As a result of seeing this, we had the idea to take action that would actually assist individuals in getting rid of their pacemakers. However, there is a problem these pacemakers are already available on the market. So, we looked at various pacemaker manufacturing companies. We discovered that the device had a drawback in that it used more power and took up more space. Fig 2 Table gives an example of how much power it uses. We therefore developed a solution using a RISC- V-based architecture. This architecture is an existing one,

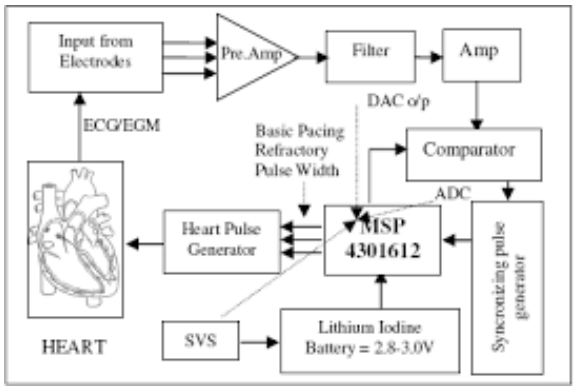

Fig. 2. Existing Architecture

and as a result, it is obvious that there is a flaw in it. It is a comparator, and additional unnecessary blocks are present that consume more power and take up more space, directly increasing delay. In addition, the system as a whole is not application-specific, so it is not, by definition, optimized. In the following chapter, we therefore suggest a new design with the aid of RISC-V. Depending on the model and features,

Name of the Manufacturing company	Power consumption (mw)
Medtronic	1.5-2.5
Abbott Laboratories	1-3
Boston Scientific	1-3
LivaNova	1-3
Biotronik	1-3

Fig. 3. Survey on Pacemakers

the power consumption of Liva Nova's, Abbott Laboratories, Boston Scientific's, Biotronik pacemakers might vary, but on average, they use 1-3 milliwatts (mW) per hour. The power consumed by the Medtronic pacemaker is about around 1.5 to 2.5 mW per hour. specific power consumption of these pacemakers would depend on the model and settings.

III. DESIGN METHODOLOGY

The design methodology of semi-custom ASIC is as shown in figure. we have used the following steps to design the proposed architecture of RISC-V based Pacemaker [4].

A. MARKET SURVEY

The main goal is to finalize the chip's specification and architecture, and in order to do that, market study is crucial. We must be knowledgeable about the items, including their capabilities, speeds, powers, and areas, as well as their user interfaces and electrical properties

B. DESIGN PLANNING

Architecture and micro-architecture design, often known as design planning, are the terms used to describe the process. Design planning involves understanding the needs for storage and memory as well as timing and top-level interface information.

C. LOGIC DESIGN

Since the quality of the RTL design and chip verification are based on the logic design phase of an ASIC, it is essential. The following activities, which were covered in RTL design, must be carried out during the logic design phase: (a) RTL verification; (b) synthesis; (c) DFT and scan insertion; and (d) equivalence checking.

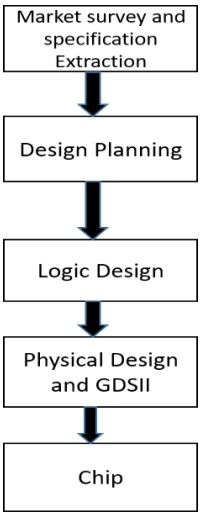

Fig. 4. Design flow of ASIC

D. PHYSICAL DESIGN

The physical design of an Application Specific Integrated Circuit (ASIC) requires the use of various data sets or standard cell libraries, input-out pads which contain different components such as physical layout, abstract views, timing models, simulation or functional models, and transistor level circuit descriptions. These libraries provide a collection of necessary resources that aid in the design process of the ASIC.

E. CHIP

There are a number of production and packaging steps involved in getting the chip from the foundry. Test houses will be given the sample chips to conduct the testing.

IV. IMPLEMENTATION

We implemented a RISC-V based pacemaker by using cadence software from front design to back-end design [6]. There are three tools used in cadence software for implementing a RISC-V based pacemaker.

1) INCISIVE: It is a simulation and verification tool used in the creation of integrated circuits (ICs) and other electronic systems it is known as the Incisive Enterprise Simulator in the field of electronic design automation (EDA). The simulation had done in incisive tool.

2) GENUS: This is a tool for RTL synthesis, which translates the design from the high-level description to a gate-level netlist. The simulation and RTL synthesis are front end design.

3) INNOVUS: This is a tool for physical design of digital circuits. The floor planning, placement, routing, and optimization had done in innovus after generating a netlist file.

a) FLOOR PLANNING: After importing the design, the first step in physical design is Floor planning. An ASIC design with improved performance and optimal area results can be achieved by the perfect floor planning. Floor layout involves deciding where to put I/O pads, macros, power, and ground structures [7].

b) POWER PLANNING: The next step is power planning. The distribution of power throughout the chip is a key component it involves adding of VDD, VSS, stripes and metallayers. [8].

c) PLACEMENT: Standard cell placement's objective is to map ASIC components. To decrease the chip's area and adhere to timing requirements, the placement tool optimizes the placement. The cells may need to be moved to various positions [9], altered in size or shape, or rearranged at this step.

d) CLOCK TREE SYNTHESIS: After the placement, next step is clock tree synthesis. The clock tree is made to reduce clock. The first step in clock tree synthesis is to identify the clock source, which is typically an oscillator or a PLL (Phase-Locked Loop) [10]. The clock signal produced by the source is then transmitted to the clock tree's main inputs. The next stage is to build a clock distribution network that distributes the clock signal to all of the sequential chip components [11]. In order to minimize clock skew and ensure that all consecutive elements receive the clock signal within the necessary timing limits, the clock tree was devised. The chip can run dependably and at peak performance with proper clock tree synthesis.

e) ROUTING: In order to connect the various chip parts in a way that matches the specified performance and power requirements, a physical layout is created through the routing process. Routing refers to the process of connecting the different components or modules of the chip using metal wires [12]. At this step nano route had done by using minimum wire length, minimum spacing between wires, and maximum number of vias.

f) GRAPHCIAL DESIGN SYSTEM: The last step in the physical design process is GDSII (Graphical Design System II) The GDSII format is a binary format that makes it simple to store and transport huge amounts of data by storing the layout information in a highly compressed form. GDSII files are used to exchange data about the chip's physical layout between various design flow software tools. Transistors, wires, and contacts, among other chip components, are routed and placed according to information in the GDSII file format.

A. PROPOSED DESIGN

The working of our proposed architecture is enable when the reset is zero, the system starts up. The processor chooses the type of operation based on the Program Counter value [13]. The Instruction Memory, which holds the opcodes for the instruction to be performed, receives the PC value. The instruction memory sends the opcode to the IFU (Instruction Fetch Unit), which then processes it and sends it to the control unit based on the PC value. The control unit chooses the kind of operation to be carried out and provides the input to the comparator and ALU. The input data set is used for retrieving historical data and the current data are kept in the registers. If the pulse rate levels are above or below the threshold level,

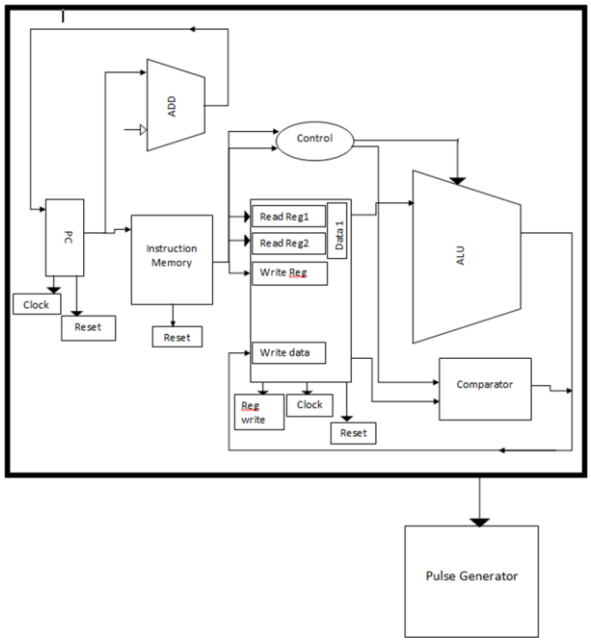

Fig. 5. Proposed Architecture for RISC-V Based Pacemaker

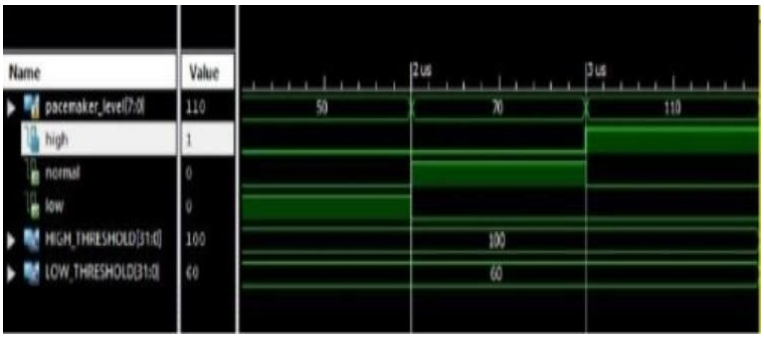

Fig. 6. Results of RISC-V Based Pacemaker

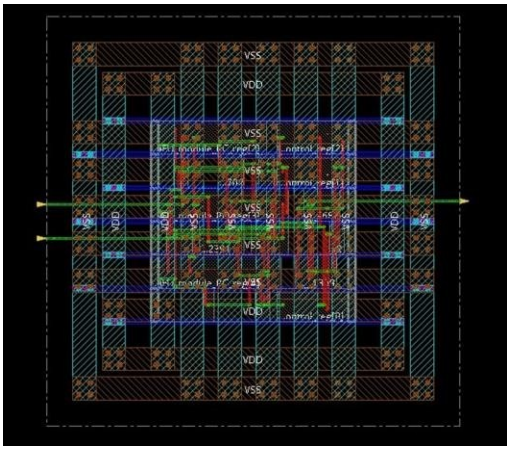

Fig. 7. Physical Layout of the RISC-V based Pacemaker

an interrupt signal is generated by the comparator when this data is provided to it, which compares the heart rate with the threshold value. The processor and pulse generator are connected. The CPU drives the pulse signal based on the interrupt signal to keep the heart rate normal.

When the heartbeat rate rises or falls above or below the threshold value, the proposed block diagram employs the RISC V processor to detect the heartbeat rate. Because of this, we employed the comparator block to signal any time the heart-beat exceeded or fell below the threshold value. Continuous heart rate monitoring is performed. The average heartbeat is between 60 and 100 beats per minute. An interrupt signal is issued to the processor if the heartbeat rate rises or falls above the threshold value the pulse generator will be signalled to turn on whenever the processor receives an interrupt, providing a steady heartbeat in accordance. When the reset is turned on, the CPU begins to function. The instruction memory delivers the instruction opcodes based on the Program counter value. The control unit chooses the operation that needs to be carried out based on the instruction opcodes. The registers are used to store data, and they are also used to handle the output. The PC value will increase by 4.

V. RESULTS

The heart beat rate for a normal person is ranges from 60 to 100 beats per minute. The proposed design has two threshold values, one threshold value for the heat beat rate below the normal rate and the another is for the heart beat rate is above the normal rate. when input is 110, which is above the threshold value then high is activated. It detects the heart beat rate is high and sends to processor.

TABLE I
AVERAGE POWER CONSUMPTION

Type of Design	Power in microwatts
Traditional Design	77.7
Proposed Design	4.053223

TABLE II
TOTAL AREA AND CELLS REQUIRED

Cell count	21
Area	174.087

The result after physical design has been completed is shown in figure.

table I shows the difference in the power consumption of Pacemaker with Traditional design and Proposed Design.

table II shows the total no of Cells and Area required for RISC-V based pacemaker

Routing is used for designing physical connections between signal pins with the help of metals is known as routing and with the help of routing we can able to reduce the wire length, minimize the path delay (Critical), minimize the various noises like cross-talk noise and there are various tasks that are performed in this stage like Global routing, Track assignment, Detailed Routing it places a crucial role in design in order to avoid few constraints.

CONCLUSION AND FUTURE SCOPE

In this project RISC-V based Pacemaker has been proposed to get more accurate information about heart, to regulate heart rhythm in critical circumstances The proposed design requires 4.053223 of power. Using RISC V processor, the response time is reduced as it has only 47 base instructions compared to otherprocessors and controllers.

A. FUTURE SCOPE

Future pacemakers might have artificial intelligence algorithms that can change the device's settings in response to information about the patient's level of activity, heart rate variability, and other physiological factors. This may enhance the device's functionality while lowering the possibility of issues.

Multi-Functionality: Future pacemakers might include further characteristics like defibrillation or the ability to distribute drugs, which could offer more thorough therapy of heart rhythm issues.

Personalization: As personalized medicine develops, pacemakers may one day be created to meet the particular cardiac anatomy and physiology of each patient. This might result in more efficient medical care and better patient outcomes.

Remote Tracking: Pacemakers with this feature could become more common in the future, enabling medical professionals to track patients' heartbeats and pacemaker performance in real-time. This might result in earlier identificationof possible problems and quicker intervention.

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