ABSTRACT

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EXTRACTION AND RECOGNITION OF OPTICAL CHARACTERS BASED ON HARDWARE AND SOFTWARE CO-DESIGN OVER RECONFIGURABLE PLATFORM

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This work presents the implementation and analysis of a system devoted to the extraction and recognition of optical characters which is based on the hardware and software co-design methodology and built over a reconfigurable platform. Since vision is a very important sense, the research in the field of artificial vision systems has been carried out since the very beginning of the digital era, in the early 60's. Taking into account the recent evolution experienced by the configurable computing area, a new tendency of research and development of heterogeneous artificial vision systems emerges. Among the main benefits provided by the so called systems on chip are the reduction of power dissipation, financial costs and physical area. In this sense, taking a License Plate Recognition System (LPRS) as a case study, the focus of this work is the implementation of the character localization and recognition steps, while the partitioning of hardware and software resources is based in cost-benefit heuristics. Initially, a software-only version of the system is build over an x86 platform. More than to allow the evaluation of several character localization related methods, this software-only version is also intended to be used as parameter of comparison for the embedded version of the system. Regarding the character recognition step, it is performed by the means of an Artificial Neural Network. Based on the results provided by the software-only evaluation system, the implementation of the embedded version is performed, considering an FPGA as platform. In this embedded version, the character localization step consists of a dedicated hardware block, while the character recognition step comprises a piece of software executed in a microprocessor that is physically implemented inside the FPGA. Taking into account a 10 times higher frequency of operation for the processor of the x86 platform, as well as the fact that most of the embedded hardware block employs a clock frequency smaller or equal to 25 MHz, the most noticeable result is the 2.25 times faster speed of processing achieved by the embedded version. Regarding the plate recognition capability, both systems have the same performance, being able to successfully recognize plates in 51.62 % of the cases (considering the best case). Beyond LPRSs, the system developed here could also be employed to build other applications that require optical character recognition features, such as automatic traffic signs recognition and serial number reading of items in a production line.

Keywords: *computer vision*; *hardware and software co-design*; FPGA, *artificial neural networks, embedded systems*.