

74LVC125A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Rev. 7 — 11 April 2013

Product data sheet

1. General description

The 74LVC125A consists of four non-inverting buffers/line drivers with 3-state outputs (\overline{nY}) that are controlled by the output enable input (\overline{nOE}). A HIGH at \overline{nOE} causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC125AD	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm	SOT108-1
74LVC125ADB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC125APW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC125ABQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

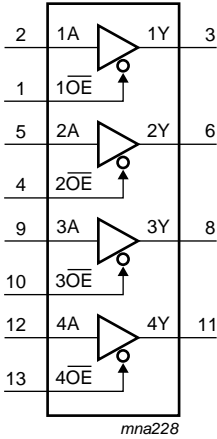


Fig 1. Logic symbol

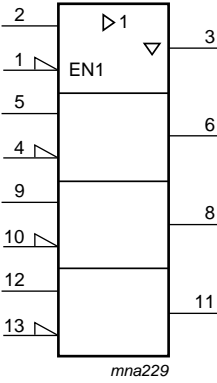


Fig 2. IEC logic symbol

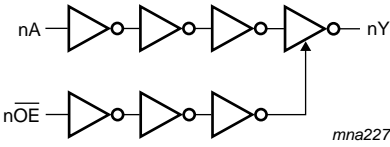
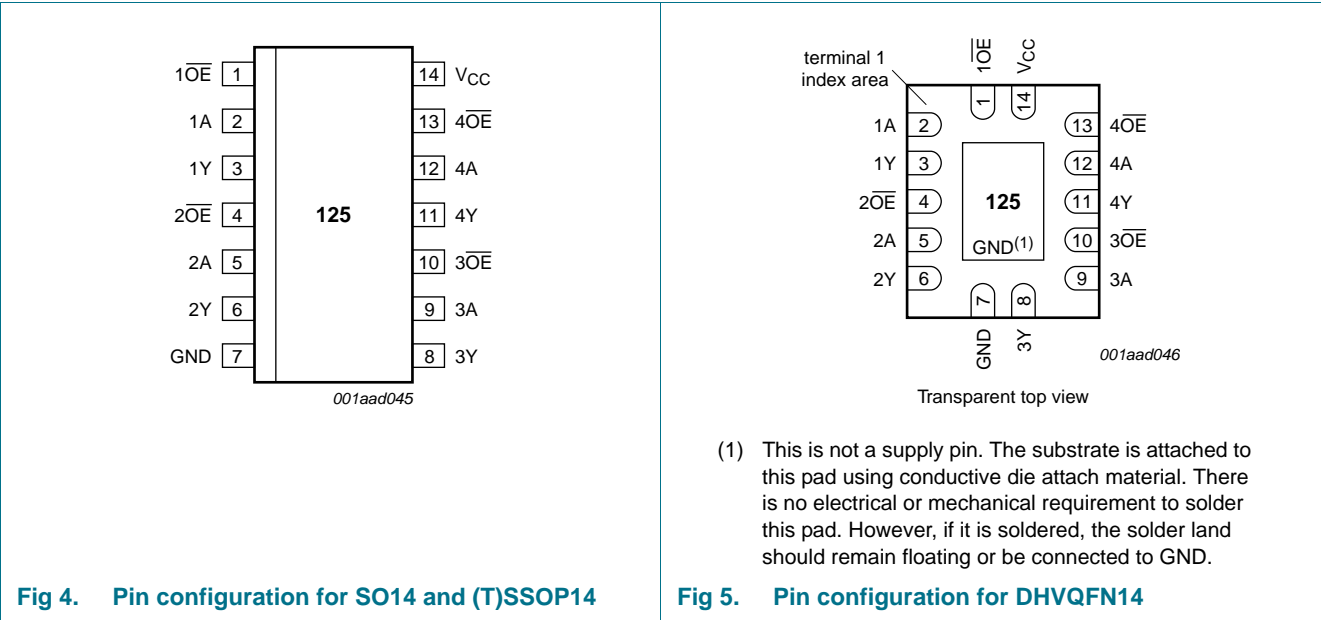


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$, $\overline{4OE}$	1, 4, 10, 13	data enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Inputs		Output
\overline{nOE}	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW-state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	500	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For (T)SSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = –100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} – 0.2	-	-	V _{CC} – 0.3	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = –18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0.0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	12.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	5.4	11.0	1.5	12.8	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.9	5.7	1.0	6.7	ns
		$V_{CC} = 2.7\text{ V}$	1.5	2.8	5.5	1.5	7.0	ns
t_{en}	enable time	\overline{nOE} to nY; see Figure 7 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	16.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.0	5.0	12.2	1.0	14.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	2.9	6.8	0.5	7.9	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.1	6.6	1.5	8.5	ns
t_{dis}	disable time	\overline{nOE} to nY; see Figure 7 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	7.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.2	4.6	7.5	2.2	8.7	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	2.6	4.2	0.5	5.0	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.1	5.0	1.5	6.5	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to }V_{CC}$ ^[4]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	6.0	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	9.4	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	12.4	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}$, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

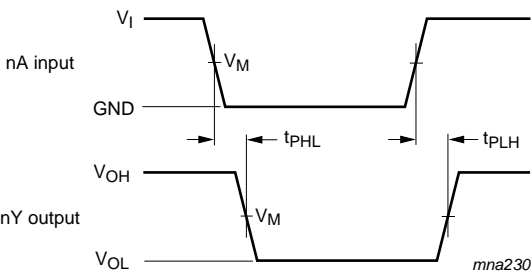
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

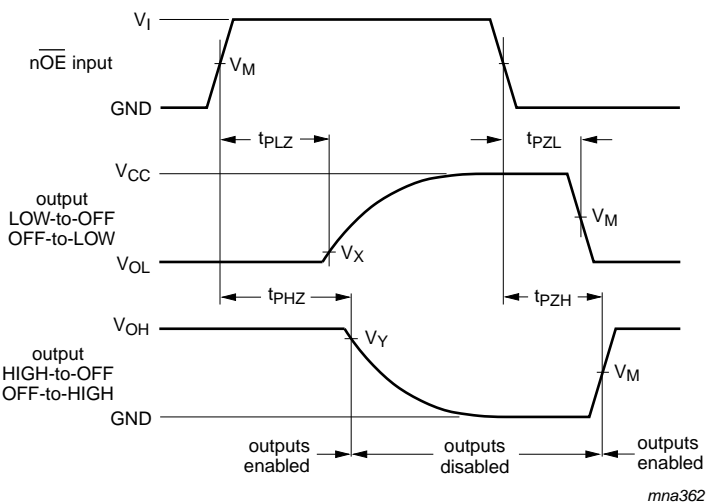
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. AC waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The input nA to output nY propagation delays

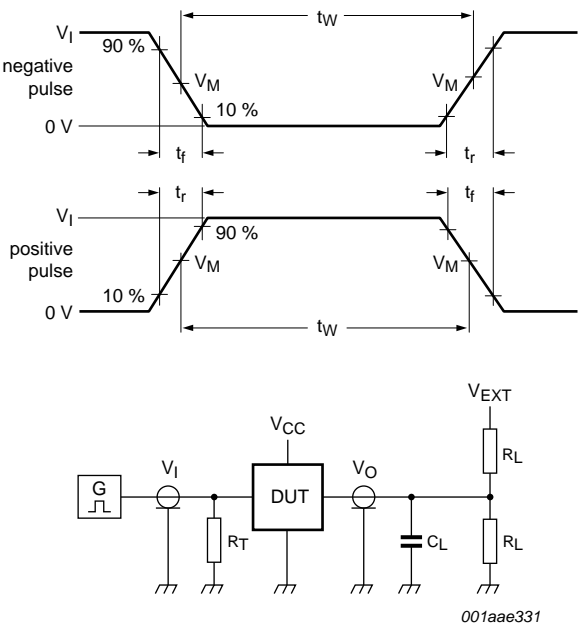


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

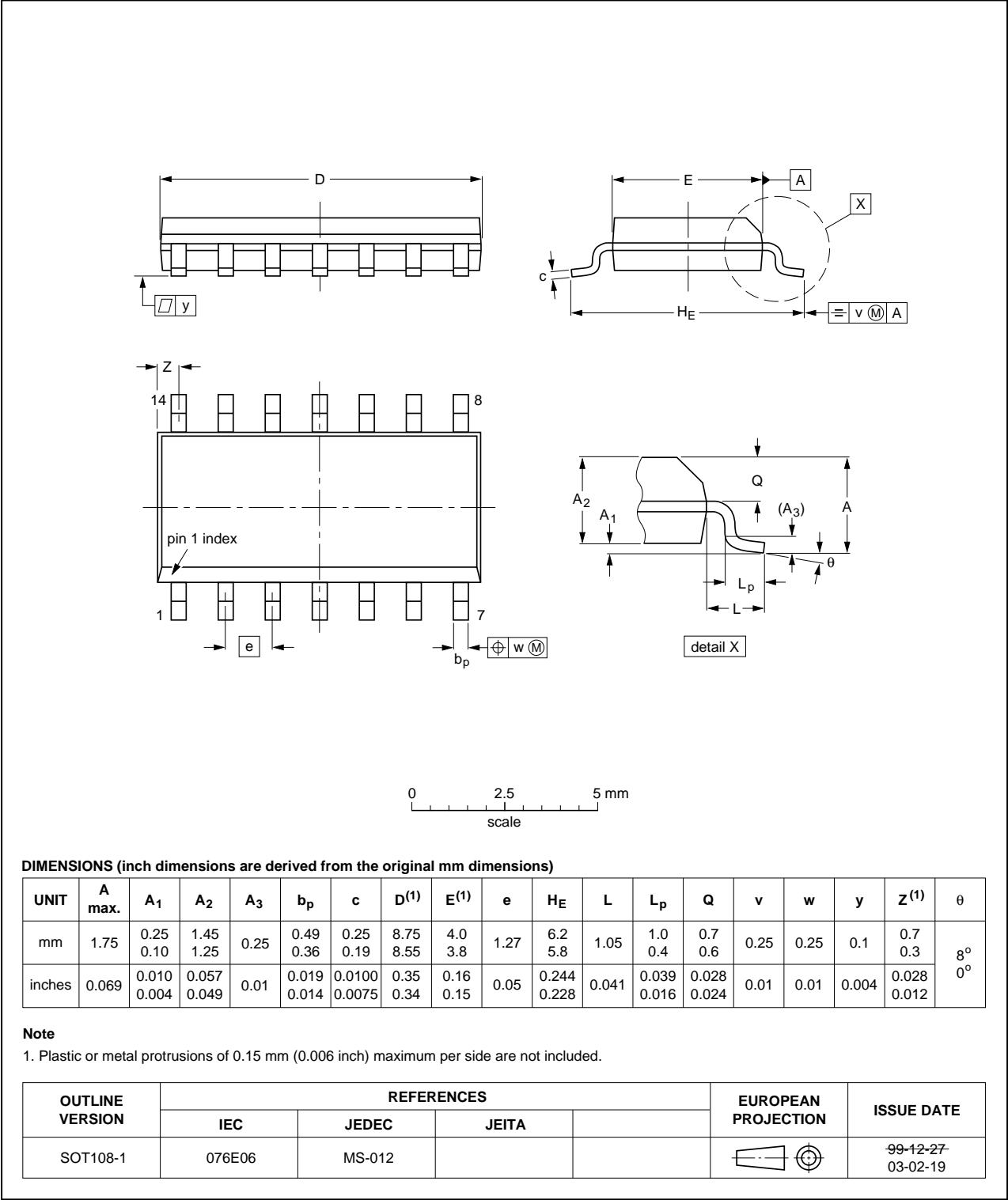


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

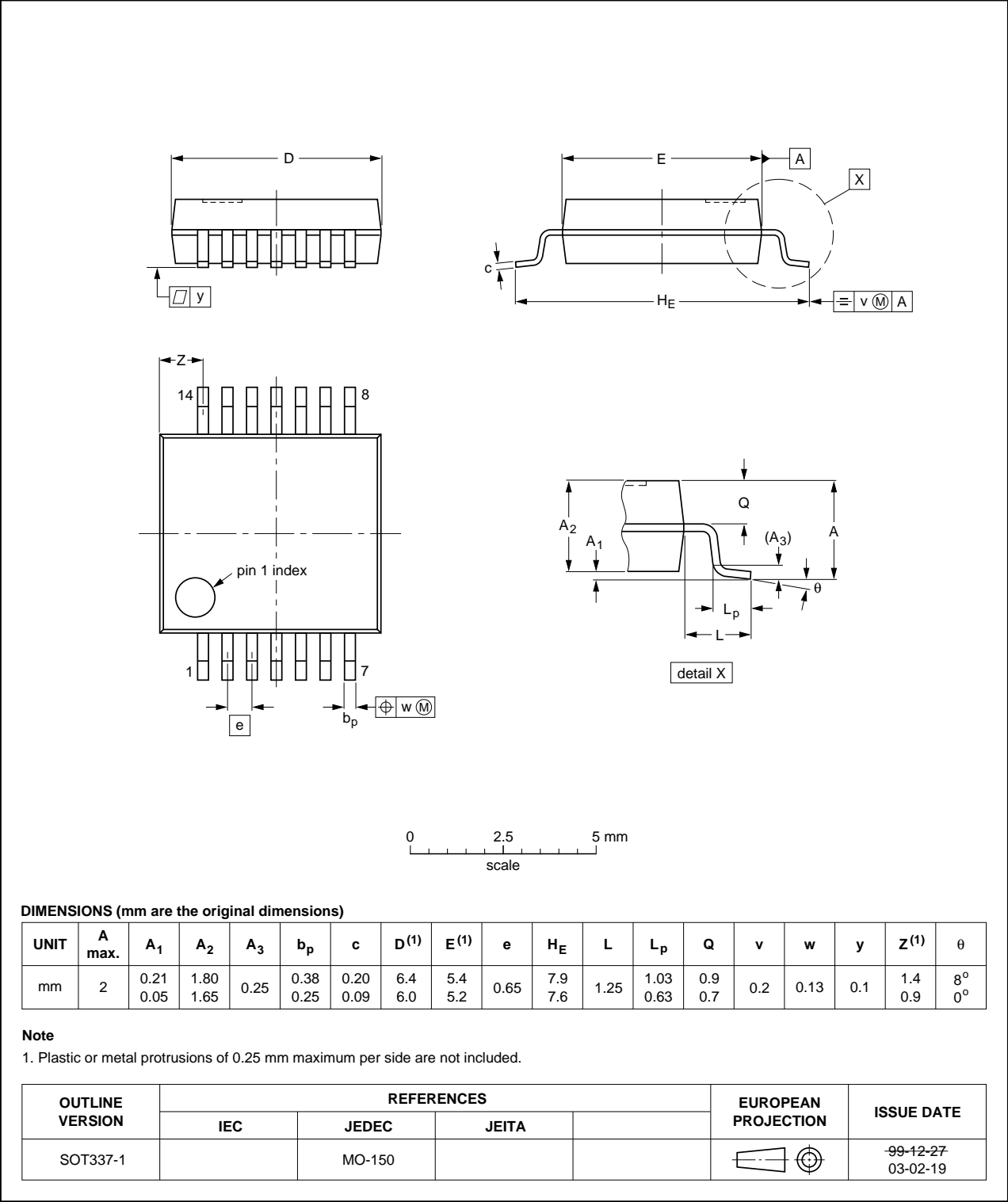


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

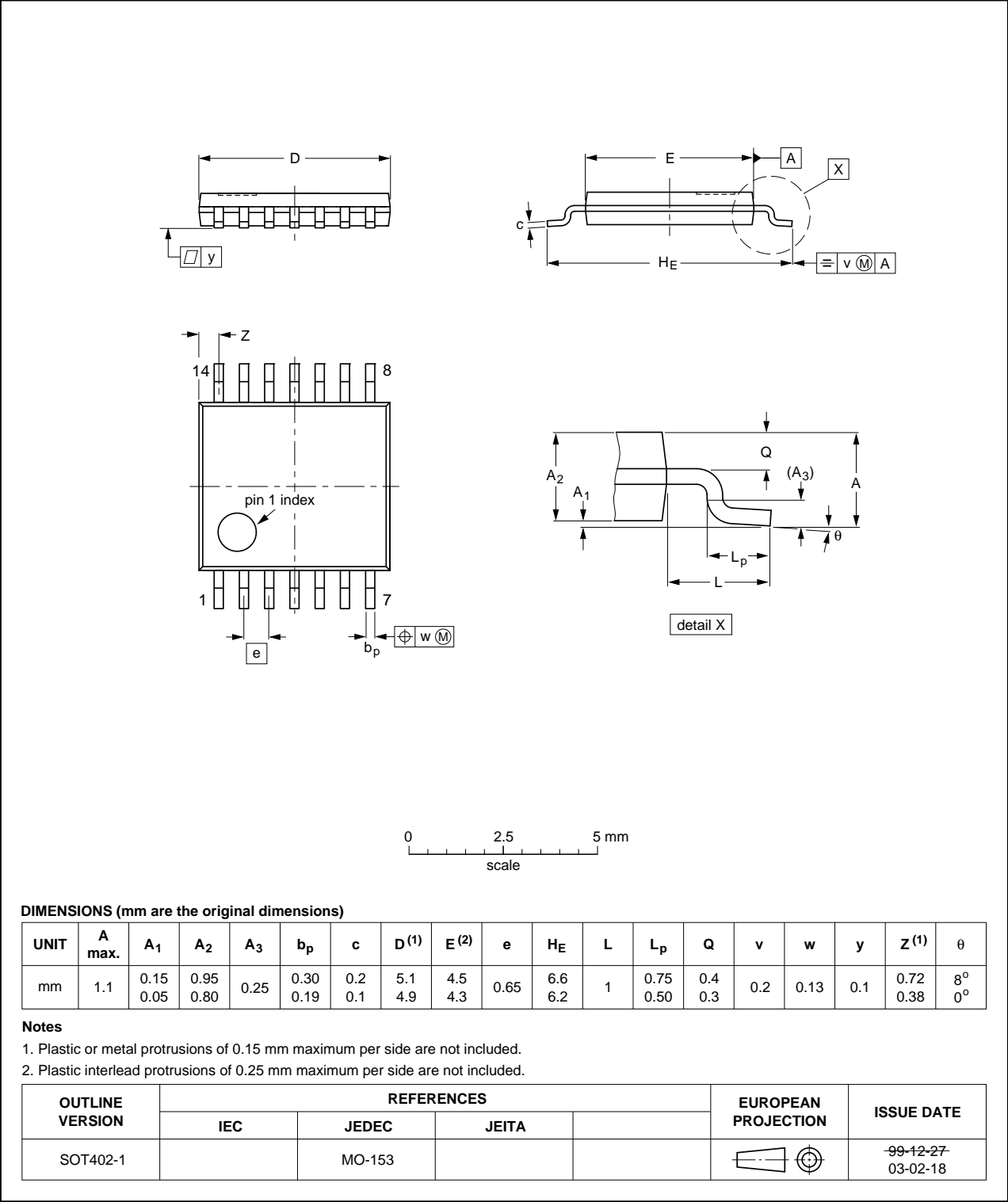
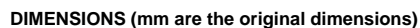



Fig 11. Package outline SOT402-1 (TSSOP14)

SOT762-1



Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

74LVC125A

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
MM	Machine Model
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC125A v.7	20130411	Product data sheet	-	74LVC125A v.6
Modifications:	• Features list corrected (errata)			
74LVC125A v.6	20130305	Product data sheet	-	74LVC125A v.5
74LVC125A v.5	20120208	Product data sheet	-	74LVC125A v.4
74LVC125A v.4	20030507	Product specification	-	74LVC125A v.3
74LVC125A v.3	20020308	Product specification	-	74LVC125A v.2
74LVC125A v.2	19980428	Product specification	-	74LVC125A v.1
74LVC125A v.1	19970801	Product specification	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	3
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
11	AC waveforms	7
12	Package outline	9
13	Abbreviations	13
14	Revision history	13
15	Legal information	14
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	15
16	Contact information	15
17	Contents	16