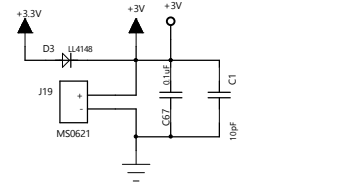
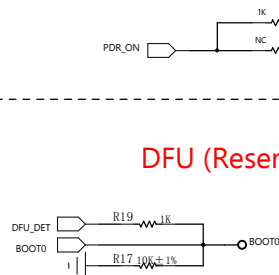
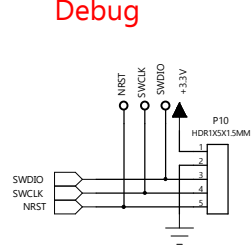
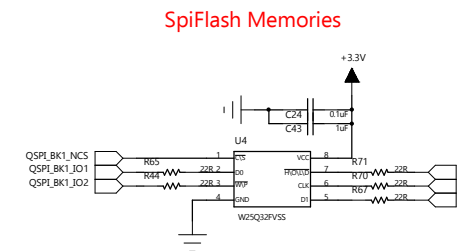
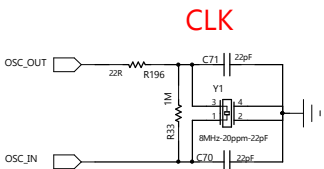
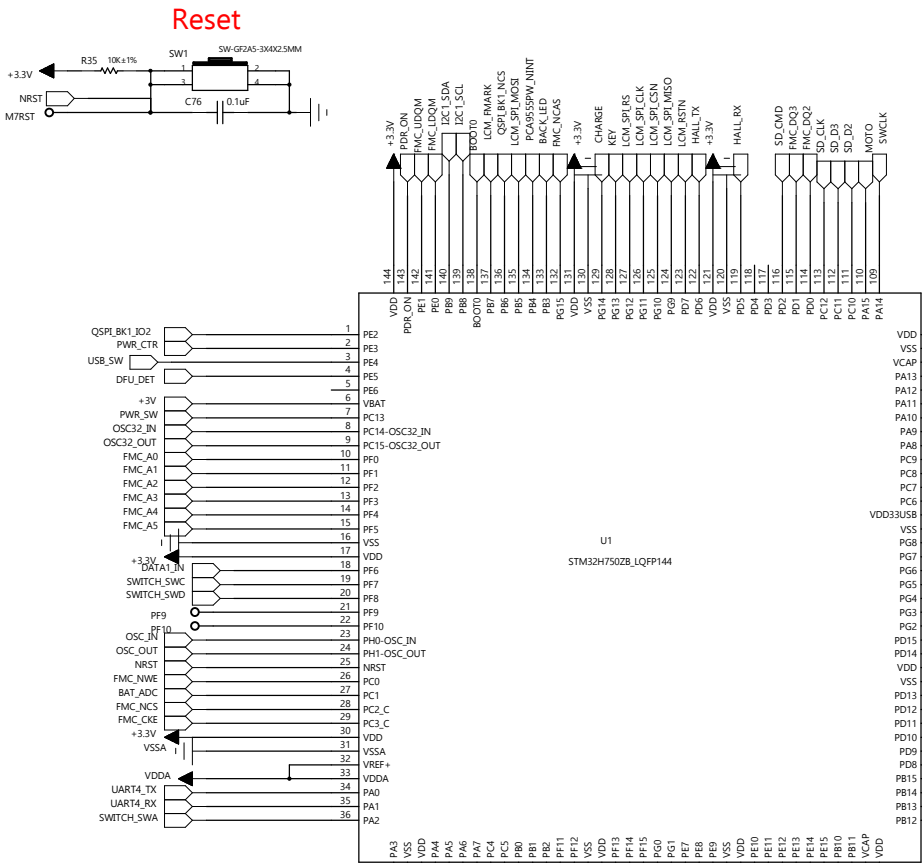


R82 R92放置在MCU I/O口端

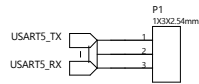
2015.12.14

MAIN-Poart

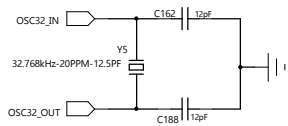
Drawing No:	Version: V1.0
Drawn By: 郑晓	Date: 20240614
Size A3	Sheet: 1 of 3



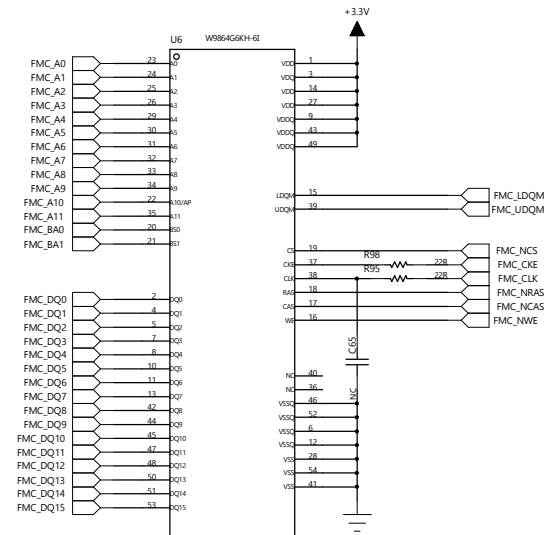
## Debug Uart



## Real-time Clock



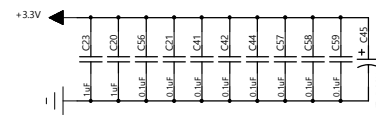
## SDRAM 64M 16bit



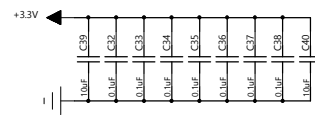
## Rule

CLK	阻抗控制在50Ω，线径10mil，线间距≥20mil，线长≤1000mil
CS CKE RAS CAS WE	线径5mil，线间距≥10mil，与CLK等长，误差≤±100mil
A0-A11 BS0 BS1	线径5mil，线间距≥10mil，与CLK等长，误差≤±100mil
DQ0-DQ7 LDQM	线径5mil，线间距≥8mil，数据组内等长，误差≤±20mil
DQ0-DQ7 UDQM	线径5mil，线间距≥8mil，数据组内等长，误差≤±20mil

## MCUs Power Filtering



## SDRAM Power Filtering



## HW REVER

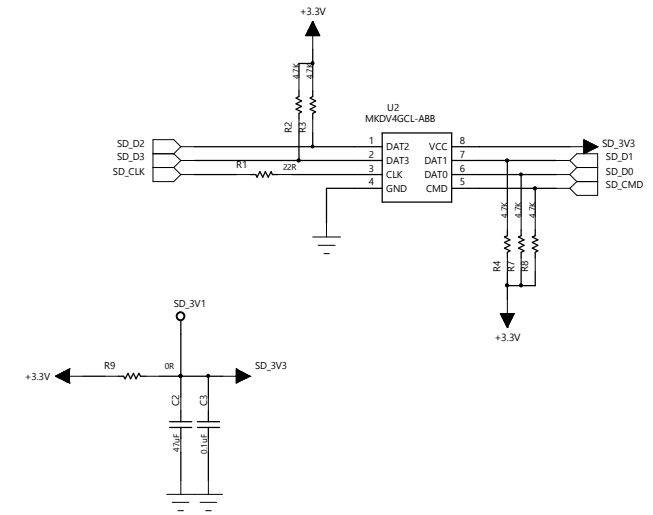
电压	版本	电压	版本
+3.3V	Ver1.0	+1.43V	Ver1.5
+3V	Ver1.1	+1.1V	Ver1.6
+2.64V	Ver1.2	+0.57V	Ver1.7
+2.18V	Ver1.3	+0V	Ver1.8
+1.81V	Ver1.4		

郑晓

Title:	MAIN-MCU/SDRAM
Drawing No:	Version: V1.0
Drawn By: 郑晓	Date: 20241010
Size A3	Sheet: 2 of 3

## SD card

SD card



## BACK Lamp



Title: MAIN-Display	
Drawing No:	Version: V1.0
Drawn By: 郑晓	Date: 20240614
Size A3	Sheet 3 of 3