ECS 326 : Digital Circuits Assessment 3

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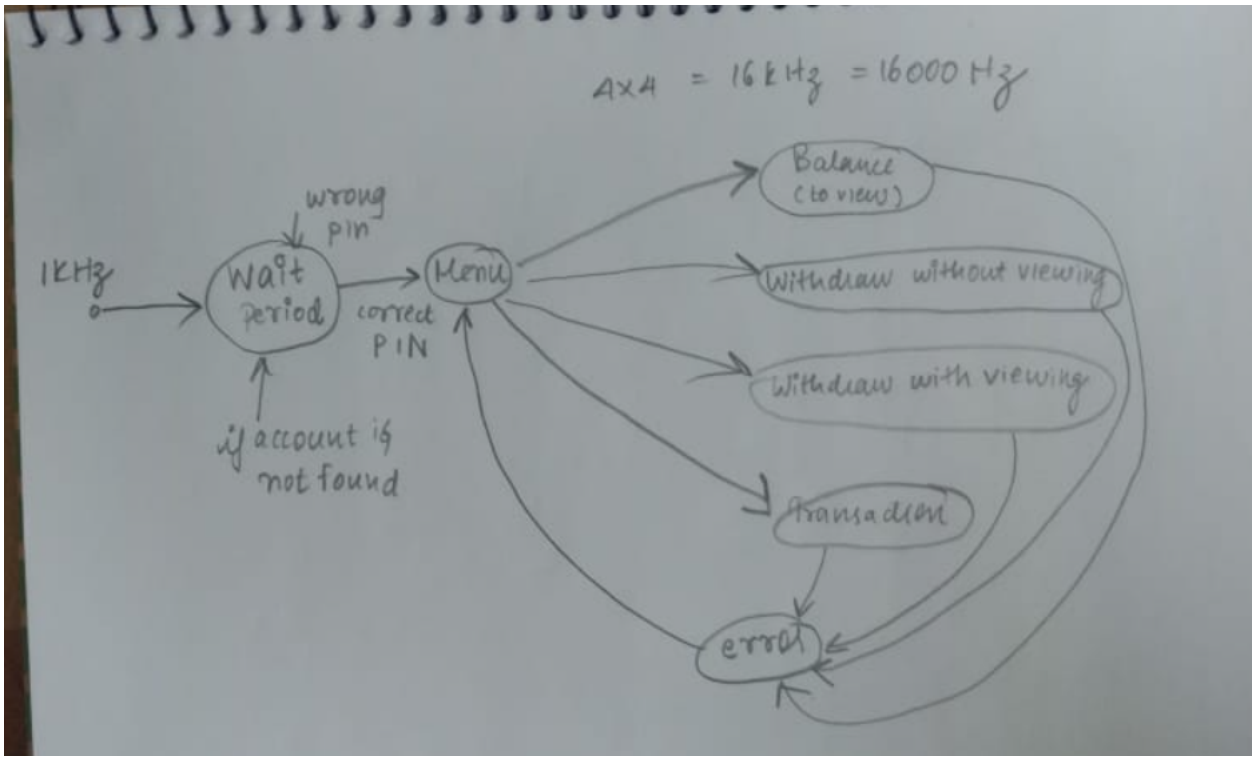
Date : 09.04.2022

The EDA playground for this project can be found on this link : (The codes for both the design, test bench and the simulation can be found in the link)

https://www.edaplayground.com/x/utU_

The idea or intuition behind designing this system :

This system is based on the same question given in Quiz 2 but with a few modifications from my end.
The clock frequency of output in my case would be 4x4kHz or 16000 Hz since the last digit of my roll number is 4.
In this ATM machine, I have added an additional authentication module which has 4 functions namely : view balance, withdraw and view balance and transaction.
A rough diagram for this based on the Finite state machine is shown below (I have drawn a rough sketch on paper to describe the flowchart)



Flowchart for the Finite State Machine customized according to my roll no with a few additional modifications.

Explanation :

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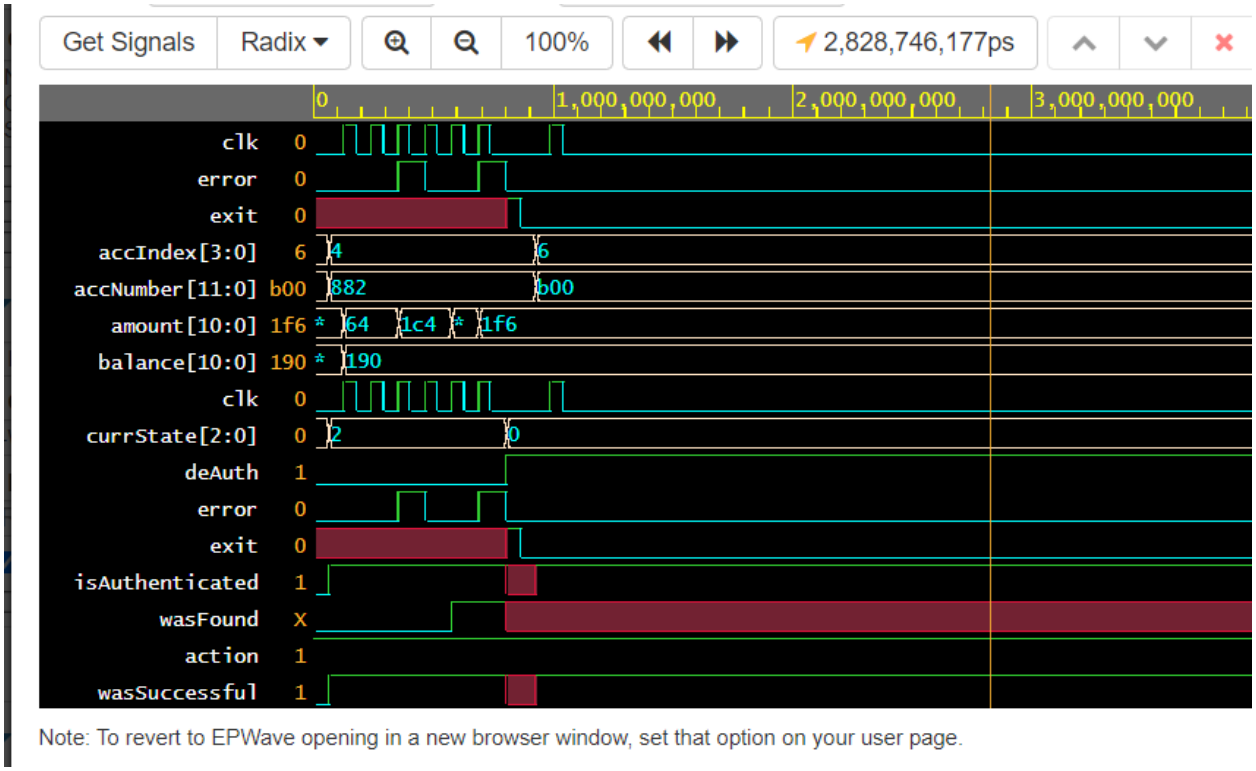
Last digit of my roll number is 4.
Hence the output frequency of the clock should be 4x4kHz or 16kHz which amounts to a time of 1/16s or 0.0000625 seconds.
The time delay function should have 62.5us or 62.5 microseconds for execution. So we use the timescale function where the first value is the time unit, in our case 10 microseconds or 10us And the second value is the precision which is 1ps in our case. So with the time unit, when the simulator displays a value, you just have to multiply the value by this time unit to get the real time. In my case #6.25 represents 6.25 * 10 us which is 62.5us , our required time delay with a precision of 1ps for the simulation corresponding to the output frequency of 16000 Hz given to me.

The simulated graph is as follows :



Link to the private GitHub repository (yet to be made public) :

https://github.com/DRA-chaos/ECS-326-ATM-machine-using-Verilog