EECS Laboratory
Experiment 4

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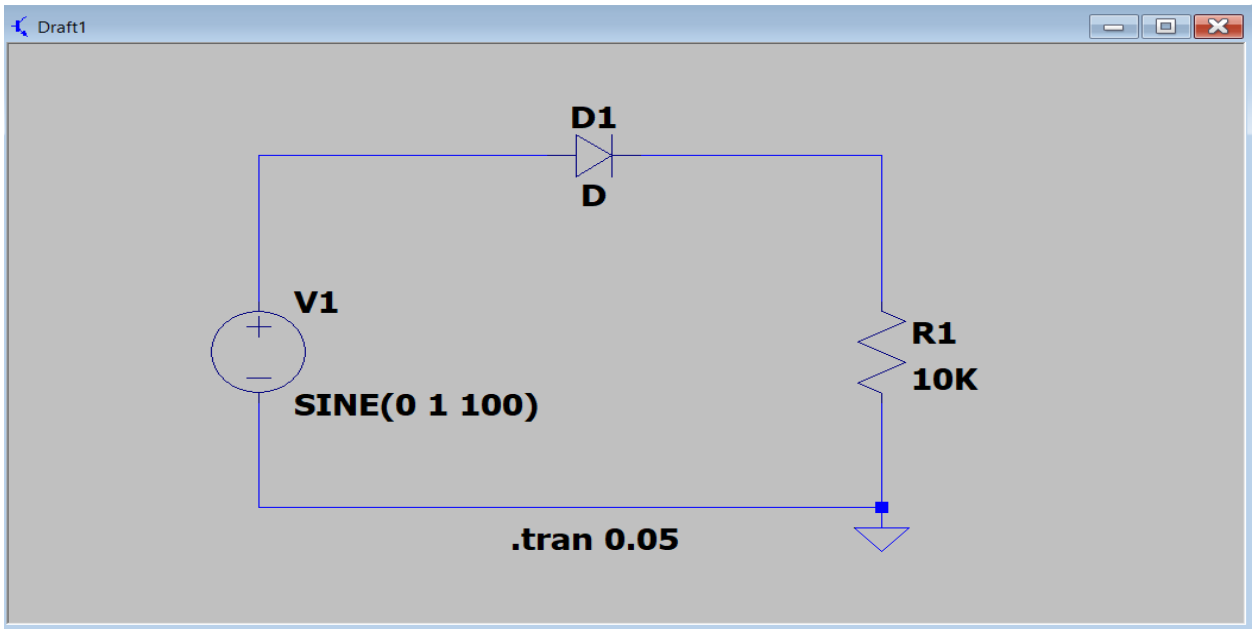
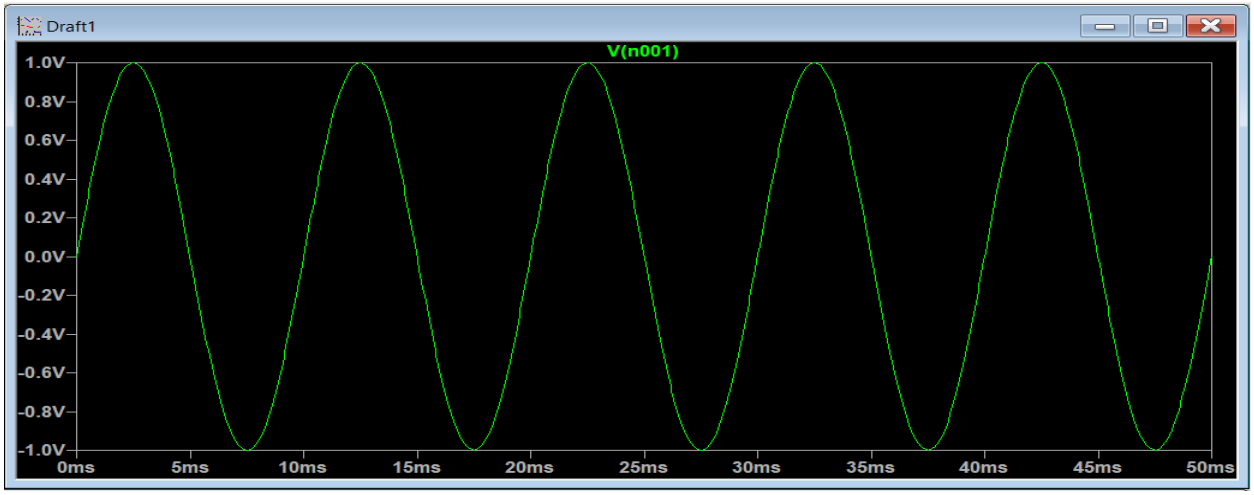
Date : 10.02.2022

4.1. HALF WAVE RECTIFIER

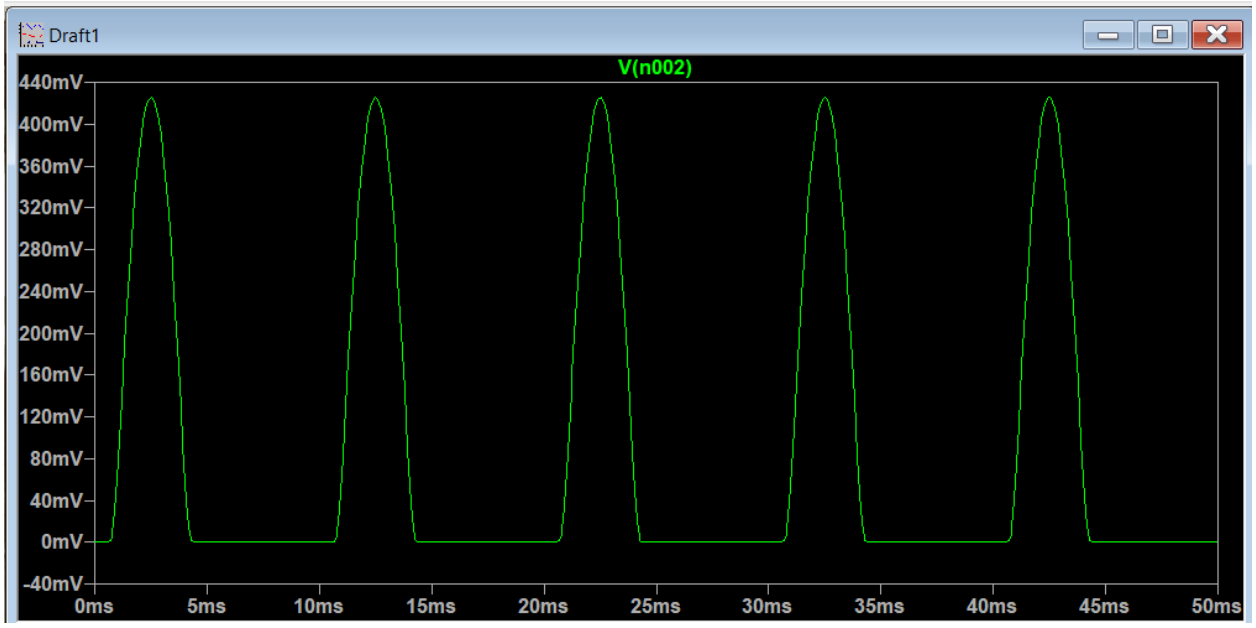
4.1.4.1 Half wave rectifier without a filter (without capacitor)



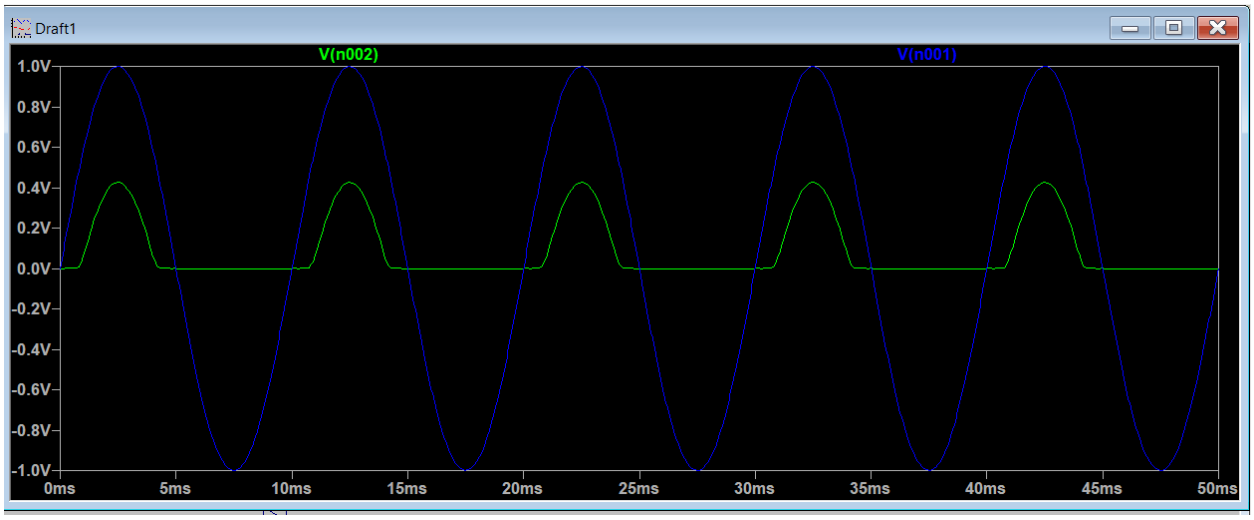
Input waveform

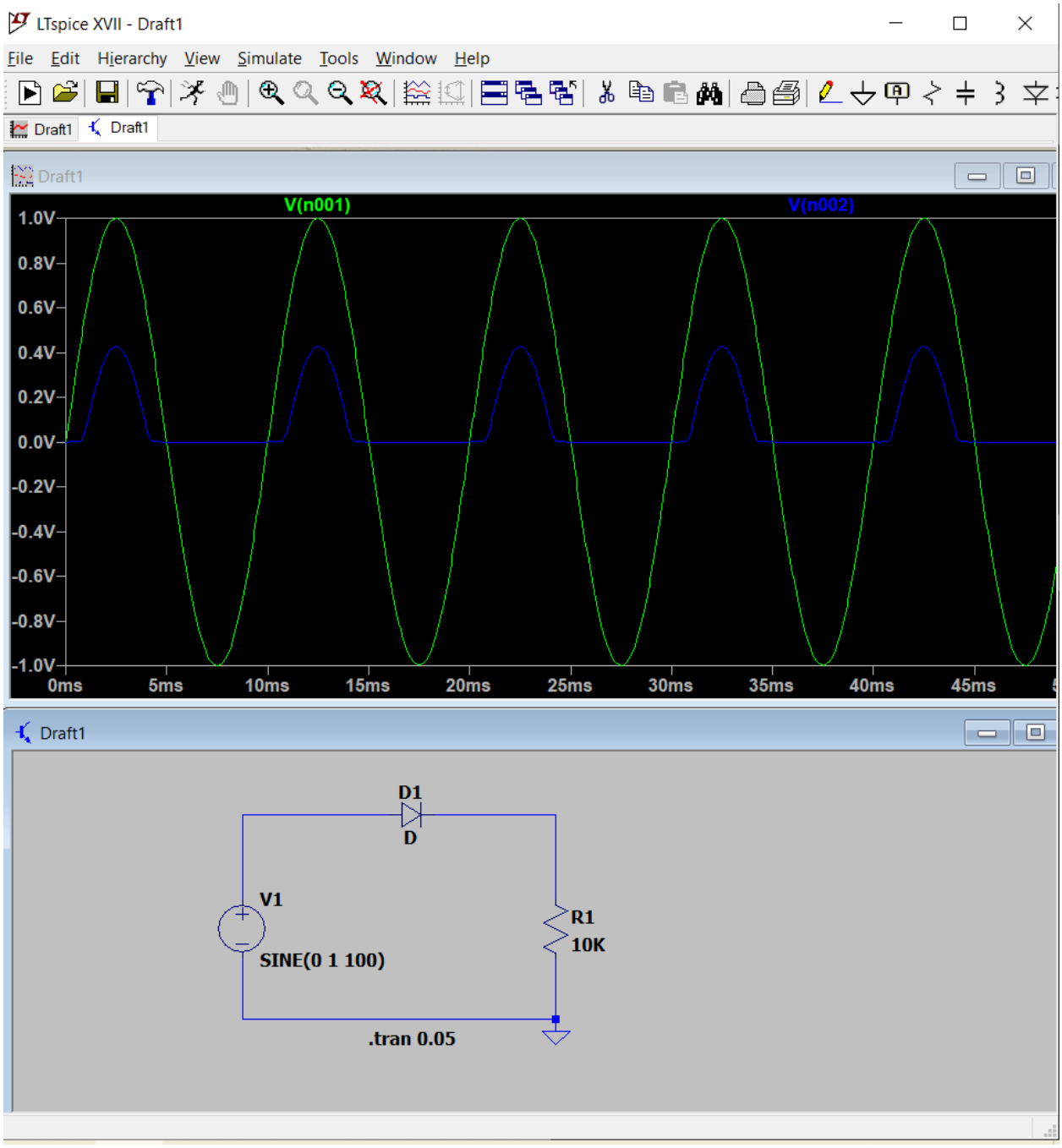


Output waveform



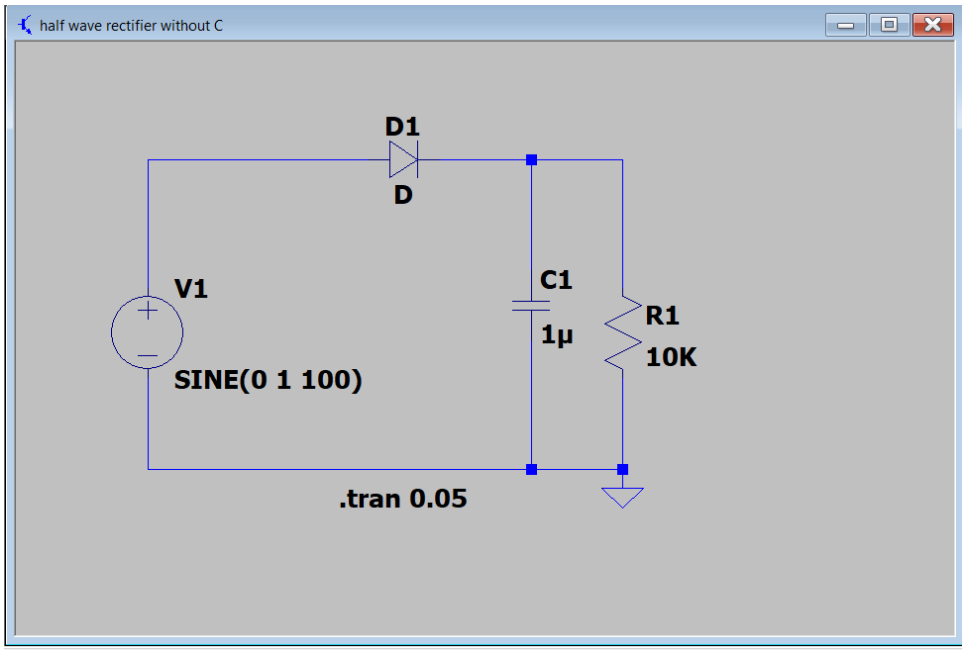
Both input and output waveforms on the same graph

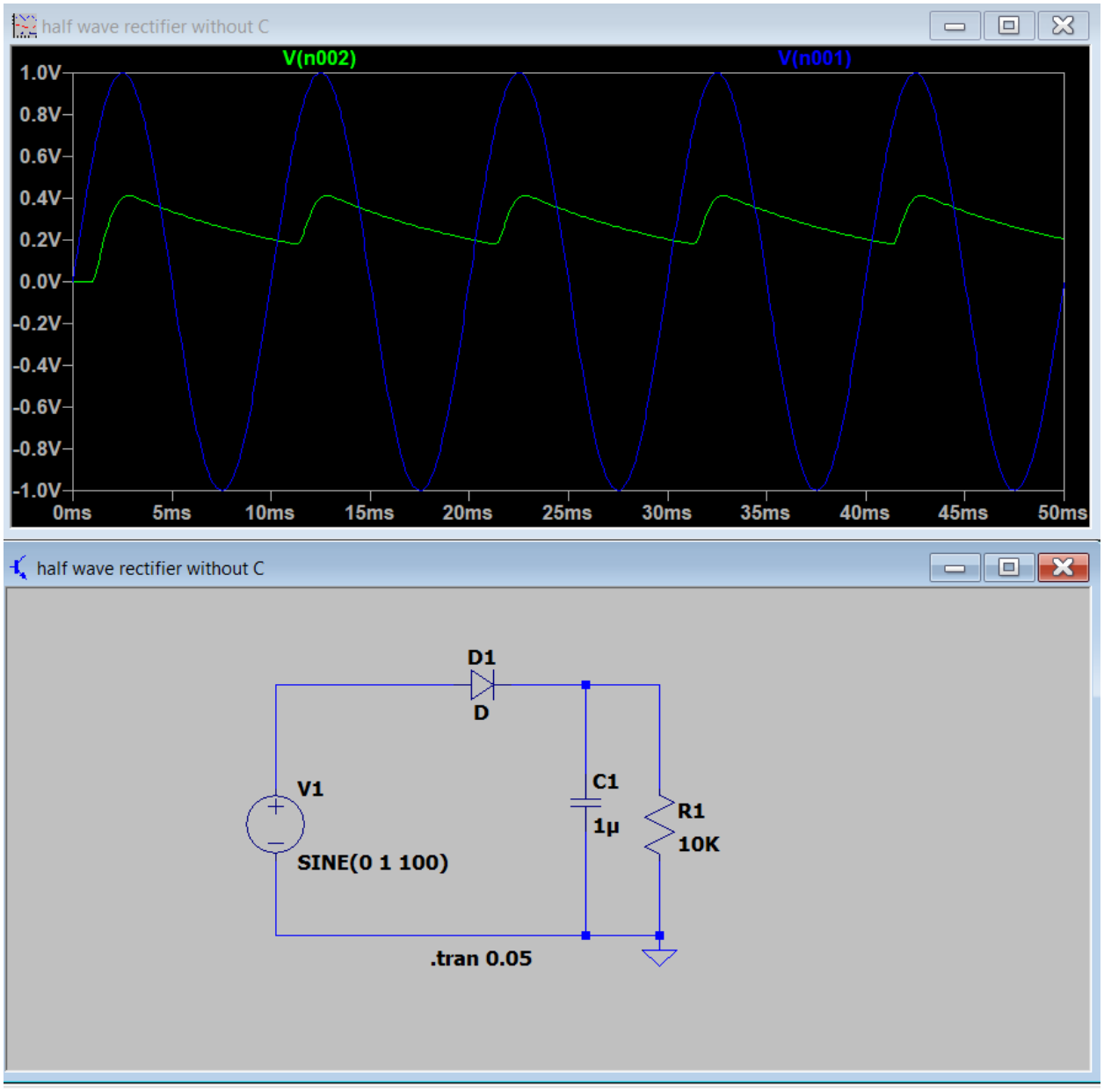



LTspice XVII - Draft1
File Edit Hierarchy View Simulate Tools Window Help
Draft1 Draft1
Draft1
V(n001)
V(n002)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
-0.6V
-0.8V
-1.0V
0ms 5ms 10ms 15ms 20ms 25ms 30ms 35ms 40ms 45ms
Draft1
D1
D
V1
SINE(0 1 100)
R1
10K
.tran 0.05

4.1.4.1 Half wave rectifier with a filter (with smoothing capacitor)

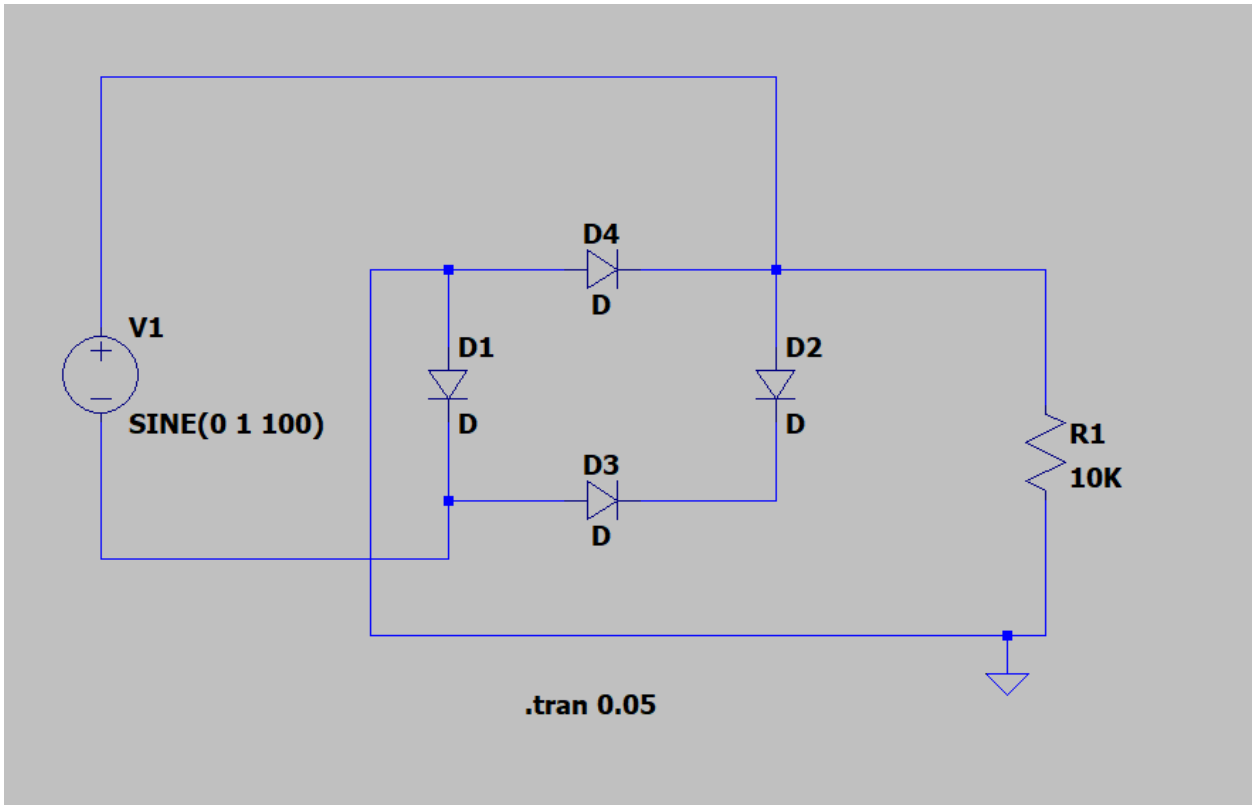
Circuit diagram

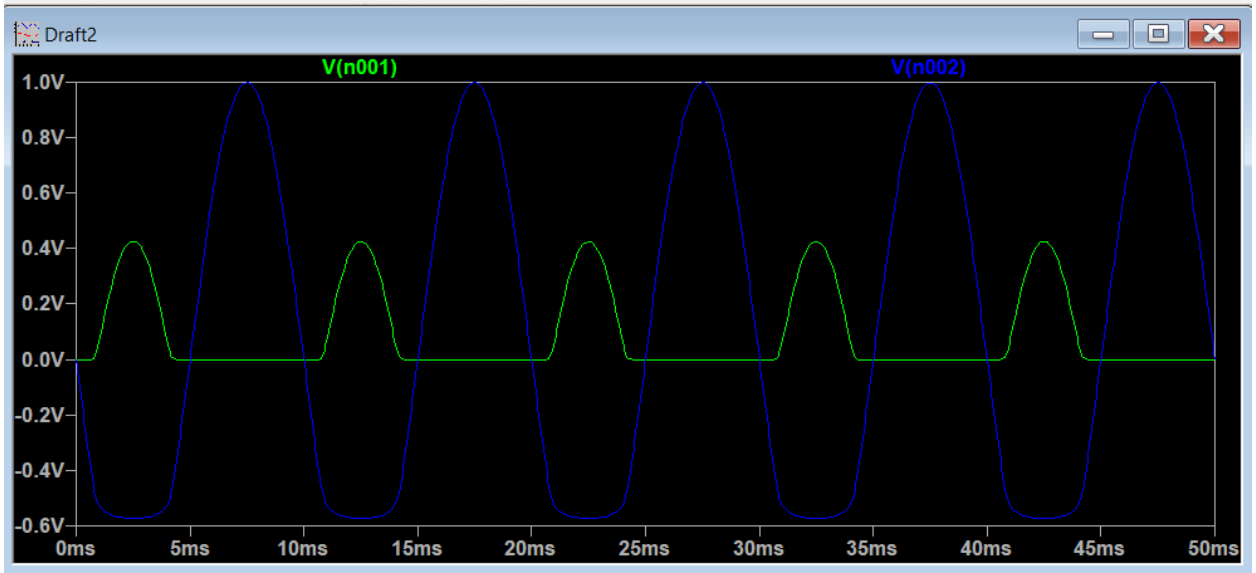


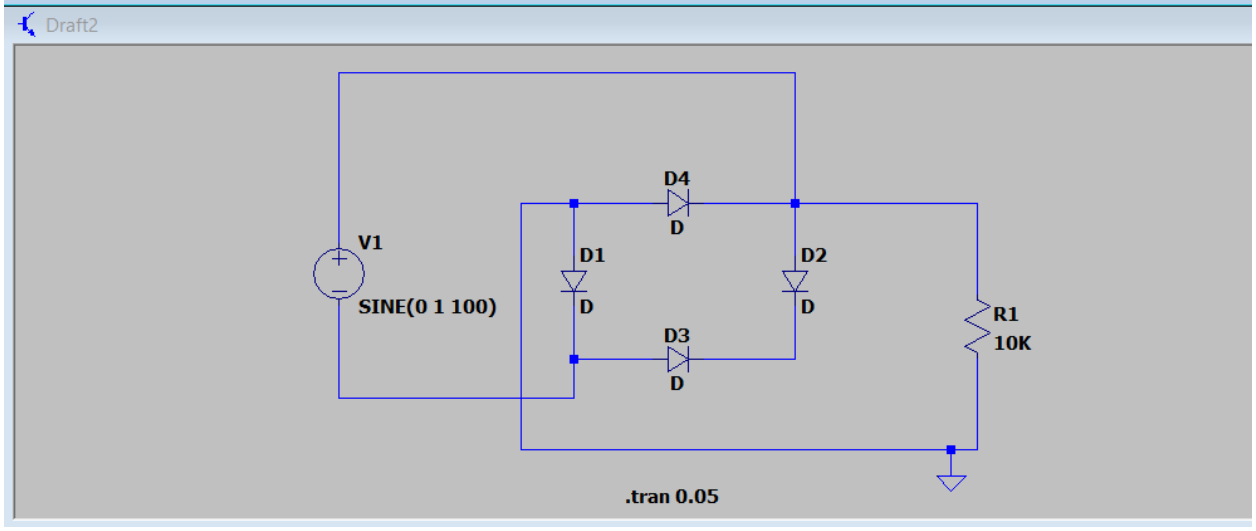

half wave rectifier without C
V(n002)
V(n001)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
-0.6V
-0.8V
-1.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
half wave rectifier without C
D1
D
V1
SINE(0 1 100)
C1
1µ
R1
10K
.tran 0.05

4.2. FULL WAVE RECTIFIER

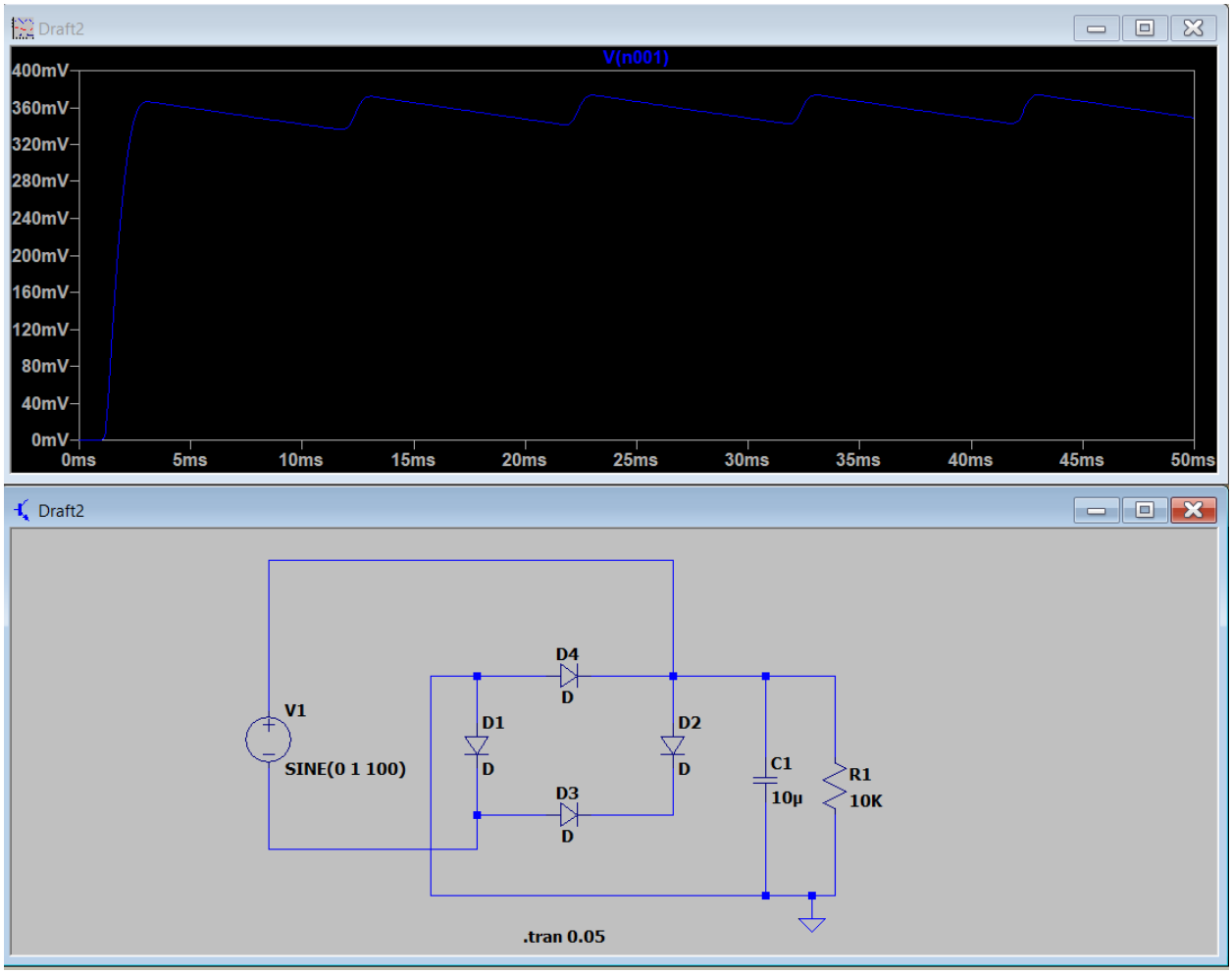
4.2.1 FULL WAVE RECTIFIER WITHOUT CAPACITOR

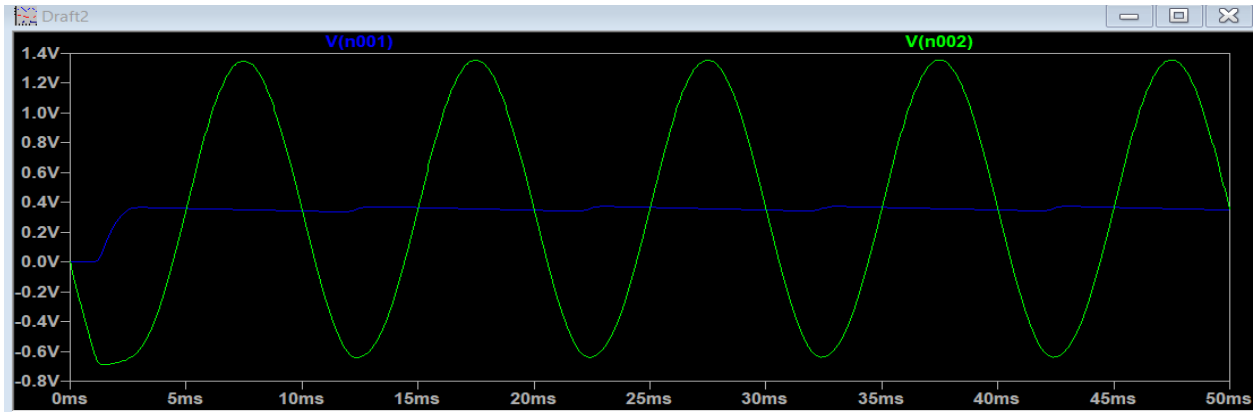



Draft2
V(n001)
V(n002)
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
-0.4V
-0.6V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms


Draft2
D4
D
V1
D1
D
D2
D
SINE(0 1 100)
D3
D
R1
10K
.tran 0.05

4.2.1 FULL WAVE RECTIFIER WITH CAPACITOR





4.2.5 RIPPLE FACTOR CALCULATIONS

Rectifier without filter:

HWR	V_m	$V_{rms} = V_m / 2$	$V_{dc} = V_m/pi$	$r= V_{r,rms}/V_{dc}$
	1V	0.5V	0.318V	1.213
FWR	V_m	$V_{rms} = V_m / \sqrt{2}$	$V_{dc} = 2V_m/pi$	$r=V_{r,rms}/V_{dc}$
	1V	0.707	0.636	0.485

Rectifier with filter :

Type	V_m	V_{rpp}	$V_{r,rms}$	$V_{dc}=V_m- v_{rpp}/2$	$r=V_{r,rms}/V_{dc}$
HWR	0.5V	0.236	0.0681	0.382	0.178
FWR	0.366V	31.05mV	8.96mV	351.045mV	0.025

The values for V_m , V_{rpp} have been taken from the output waveforms shown in the above snippets of LTSpice

CALCULATIONS:

1. HWR without filter:

Ripple factor = √(Vrms/Vdc) 2 -1

2. HWR with filter:

Ripple factor = Vrms/Vdc

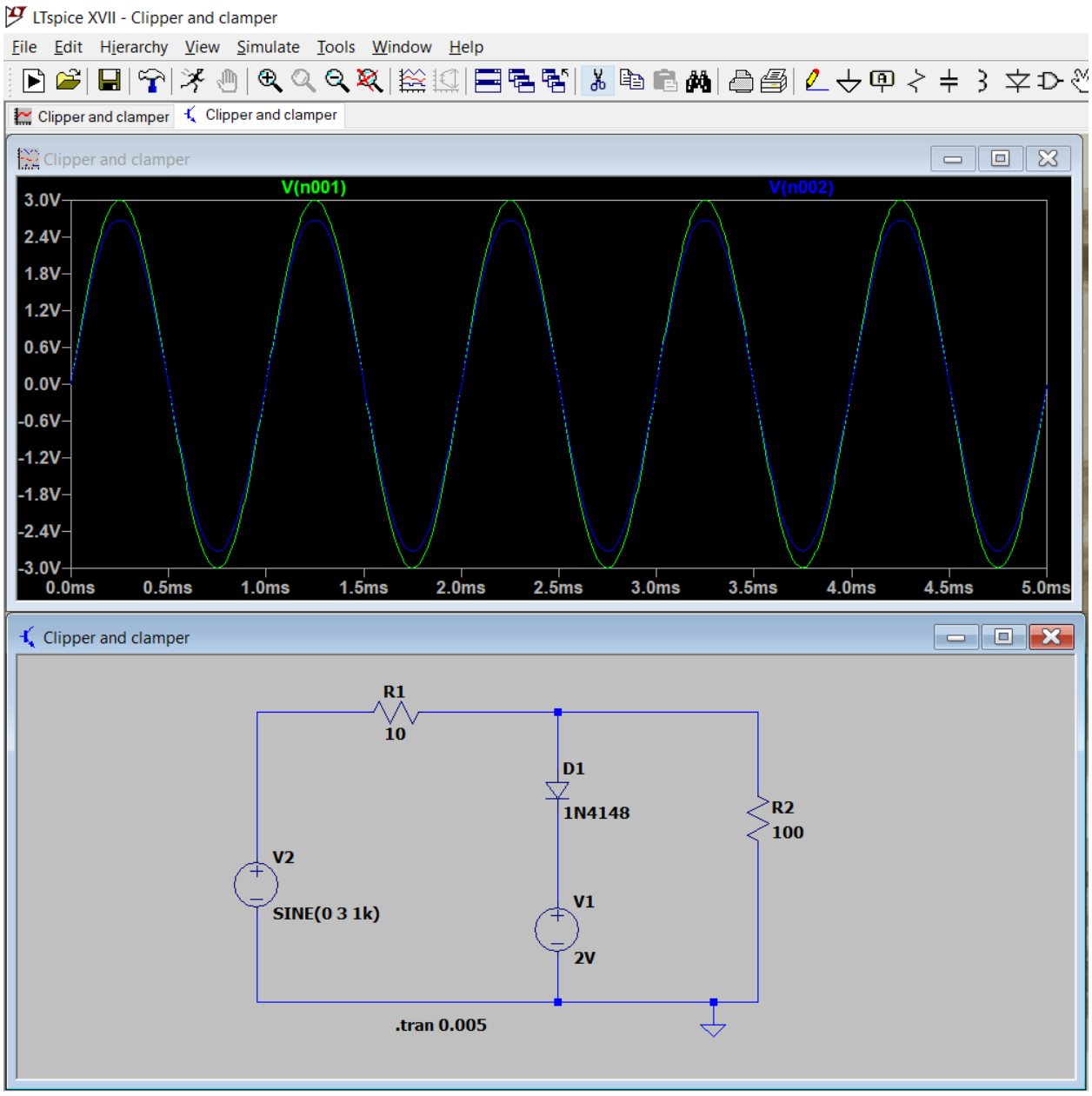
3. FWR without filter:

Ripple factor = √(Vrms/Vdc)2-1

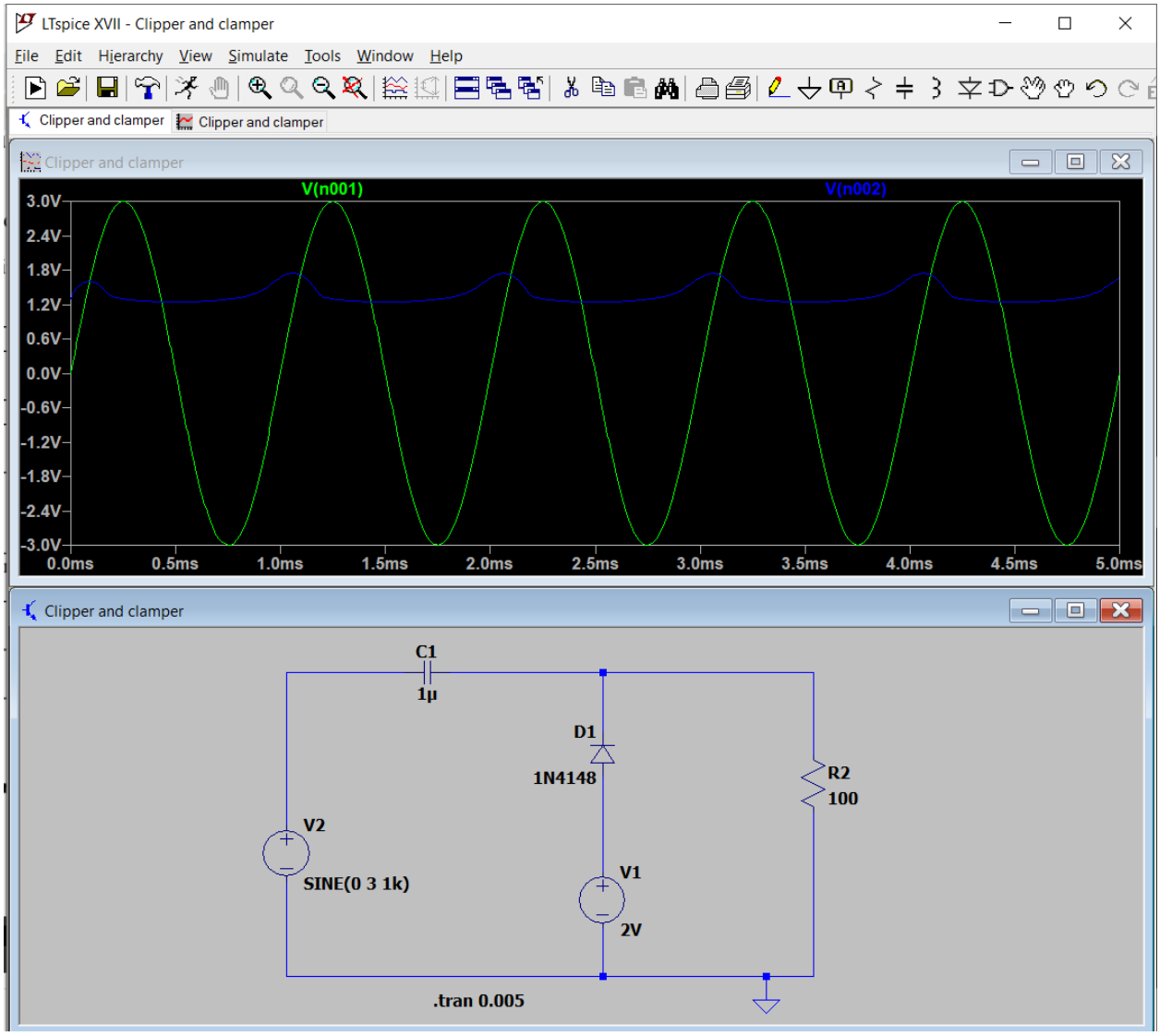
4. FWR with filter:

Ripple factor = Vrms/Vdc

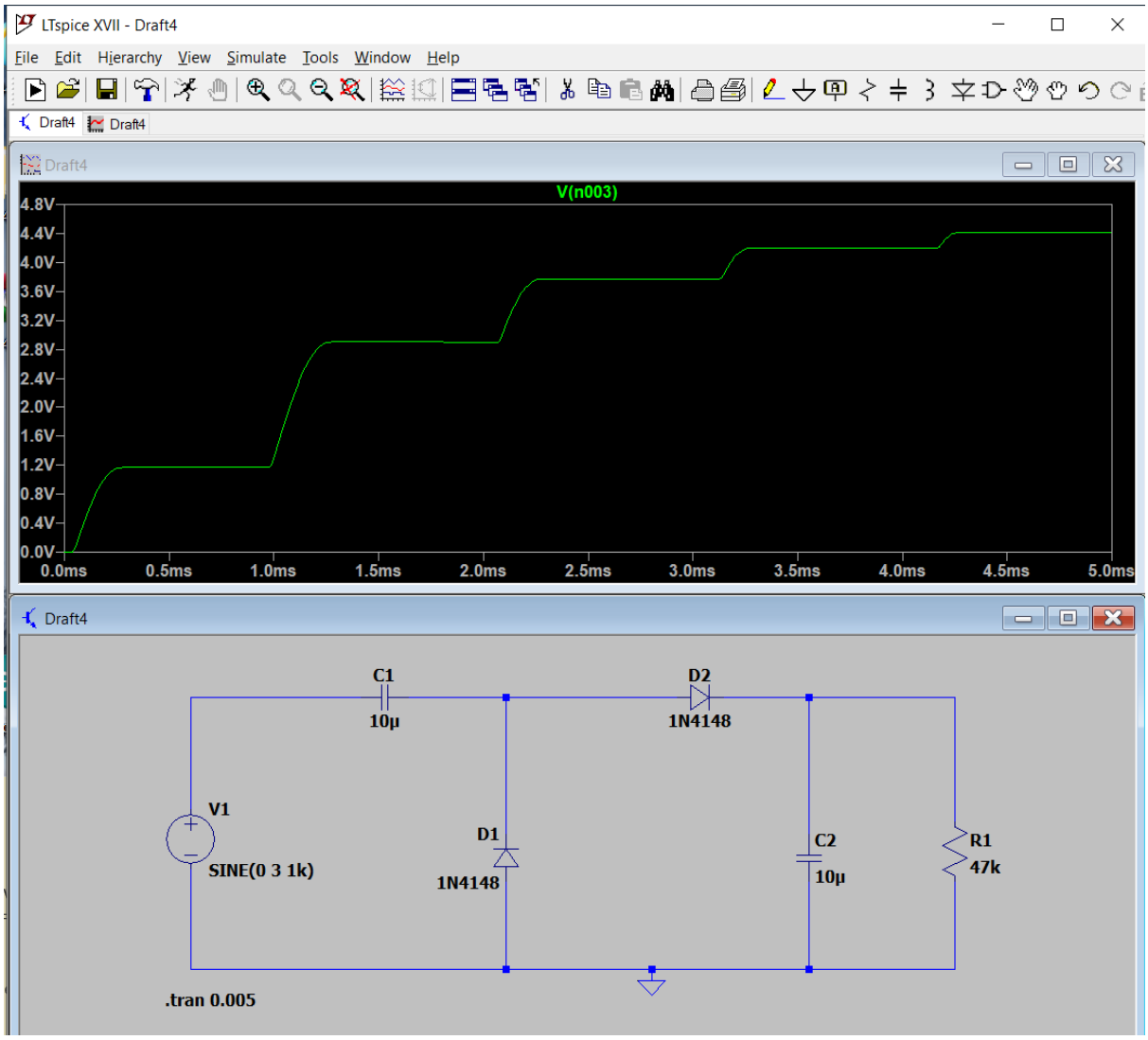
4.3 CLIPPER CIRCUIT



4.4. CLAMPER CIRCUIT

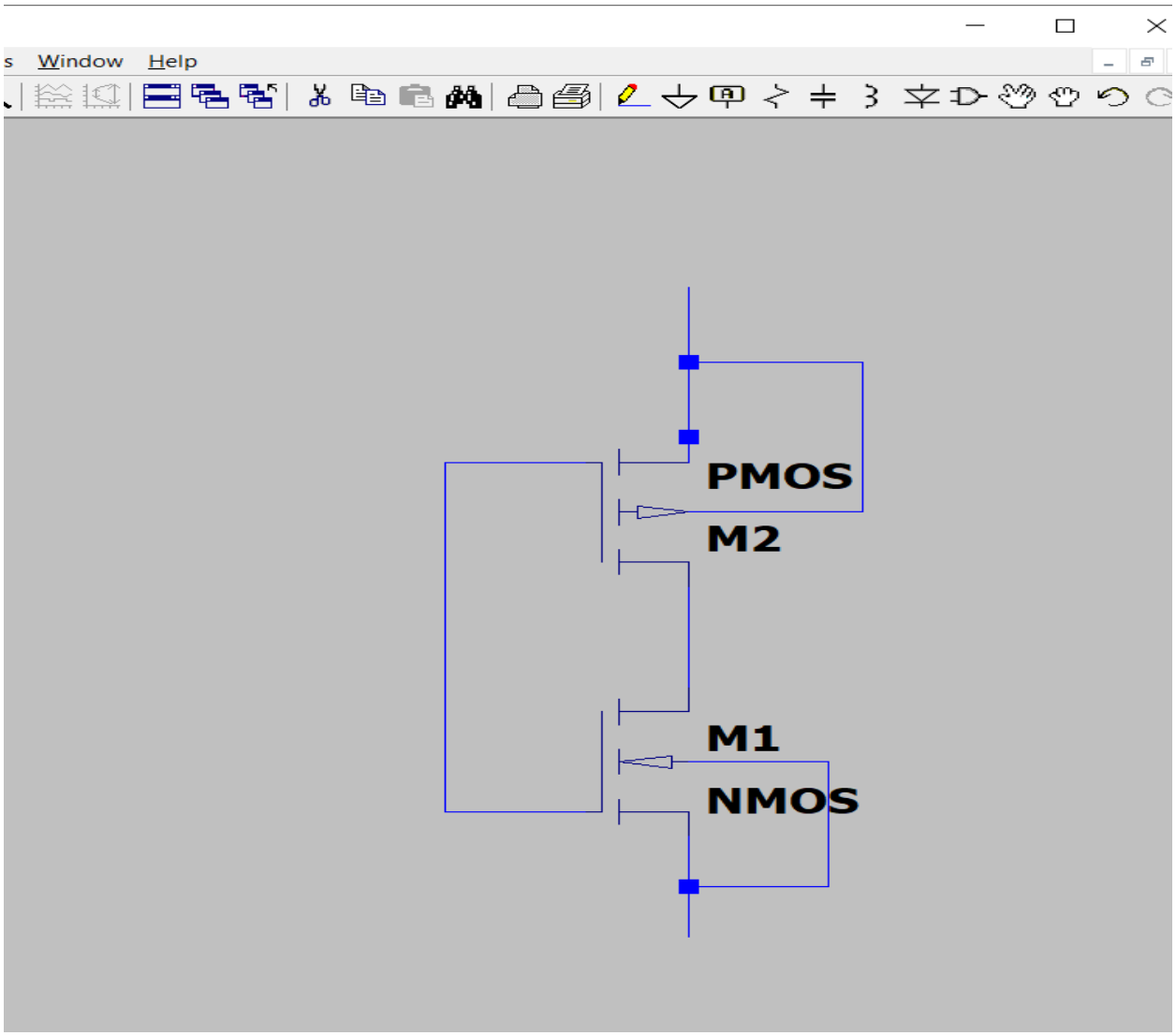


4.5 Voltage Doubler

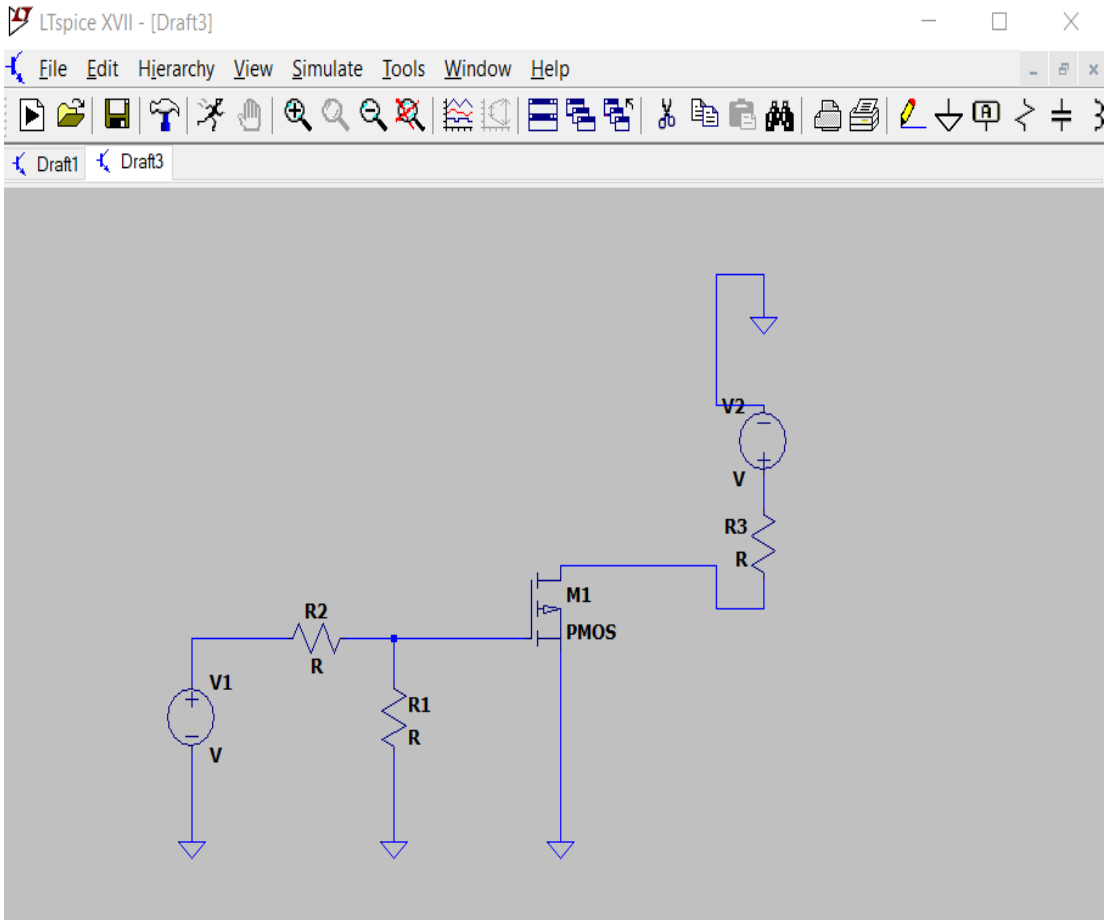


4.6 LOGIC GATES

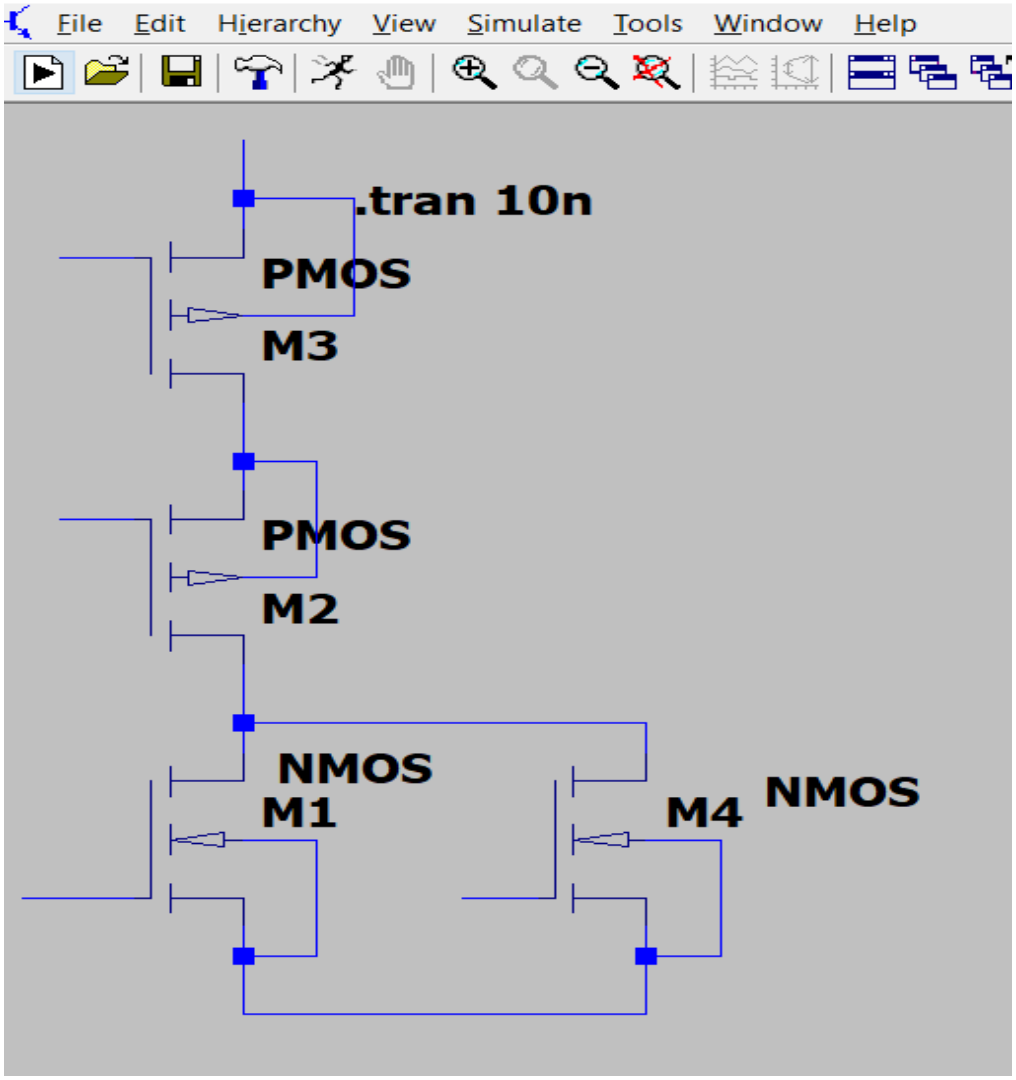
Inverter :



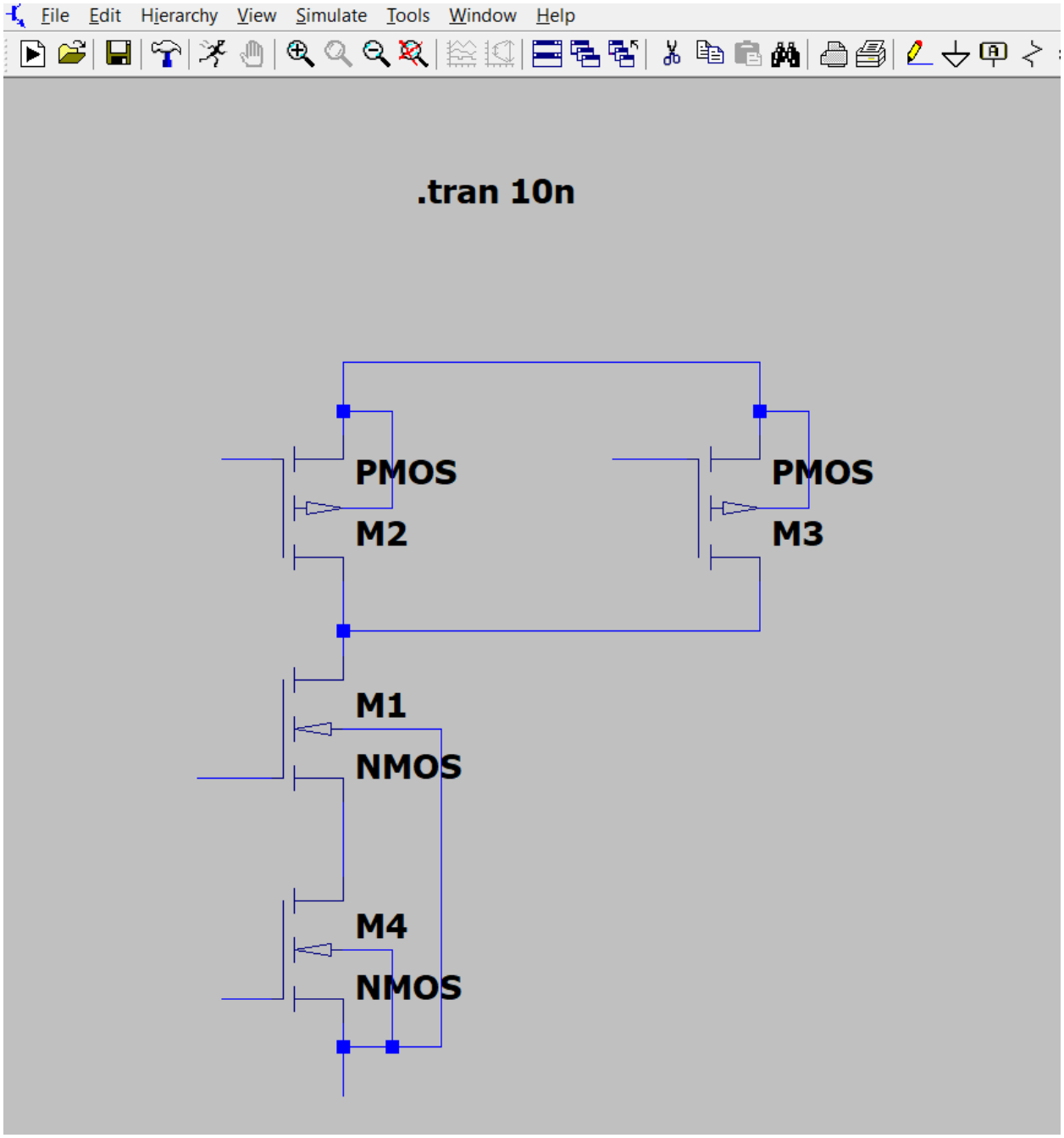
NOT Gate:


LTspice XVII - [Draft3]
File Edit Hierarchy View Simulate Tools Window Help
Draft1 Draft3
V2
V
R3
R
M1
PMOS
R2
R
V1
V
R1
R

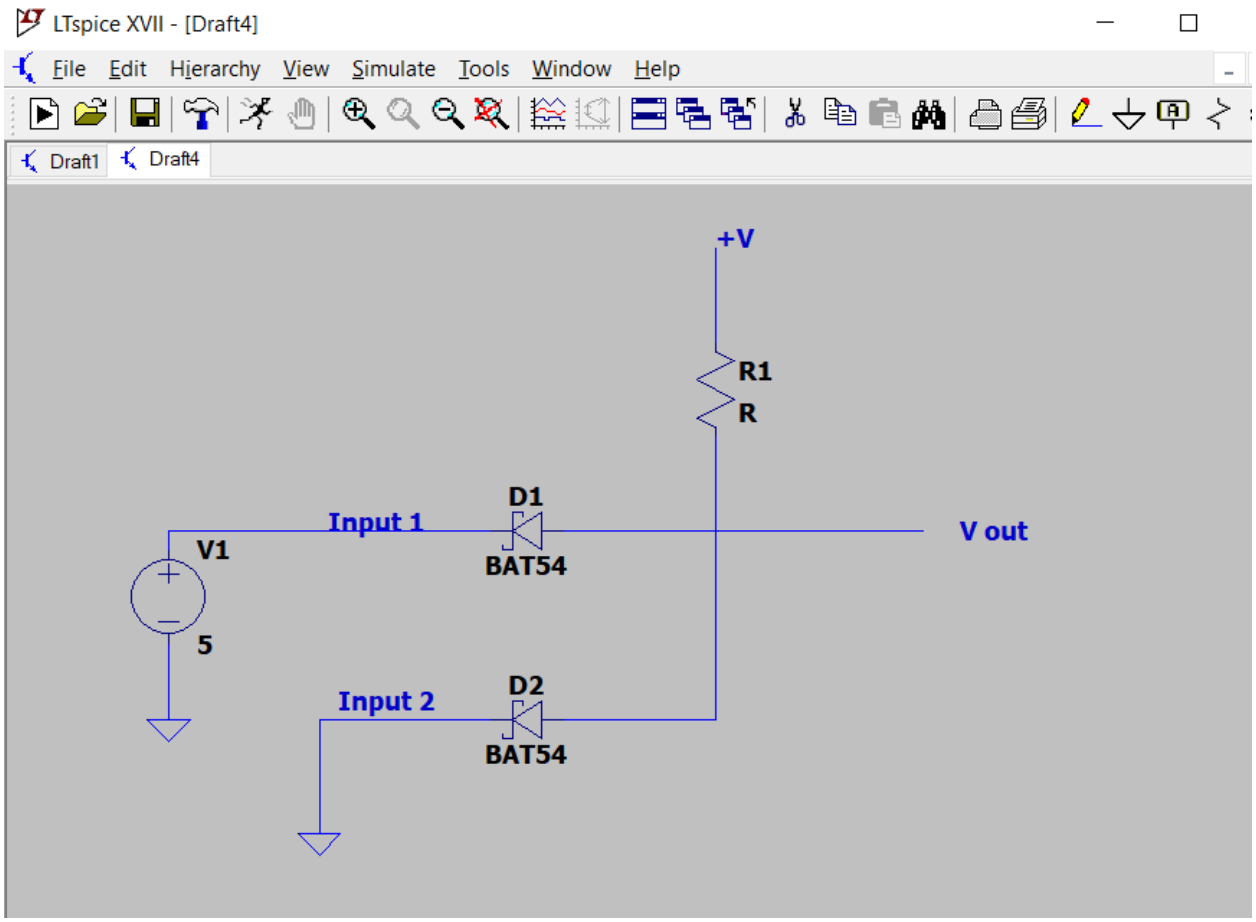
NOR GATE:


File Edit Hierarchy View Simulate Tools Window Help
.tran 10n
PMOS
M3
PMOS
M2
NMOS
M1
M4
NMOS

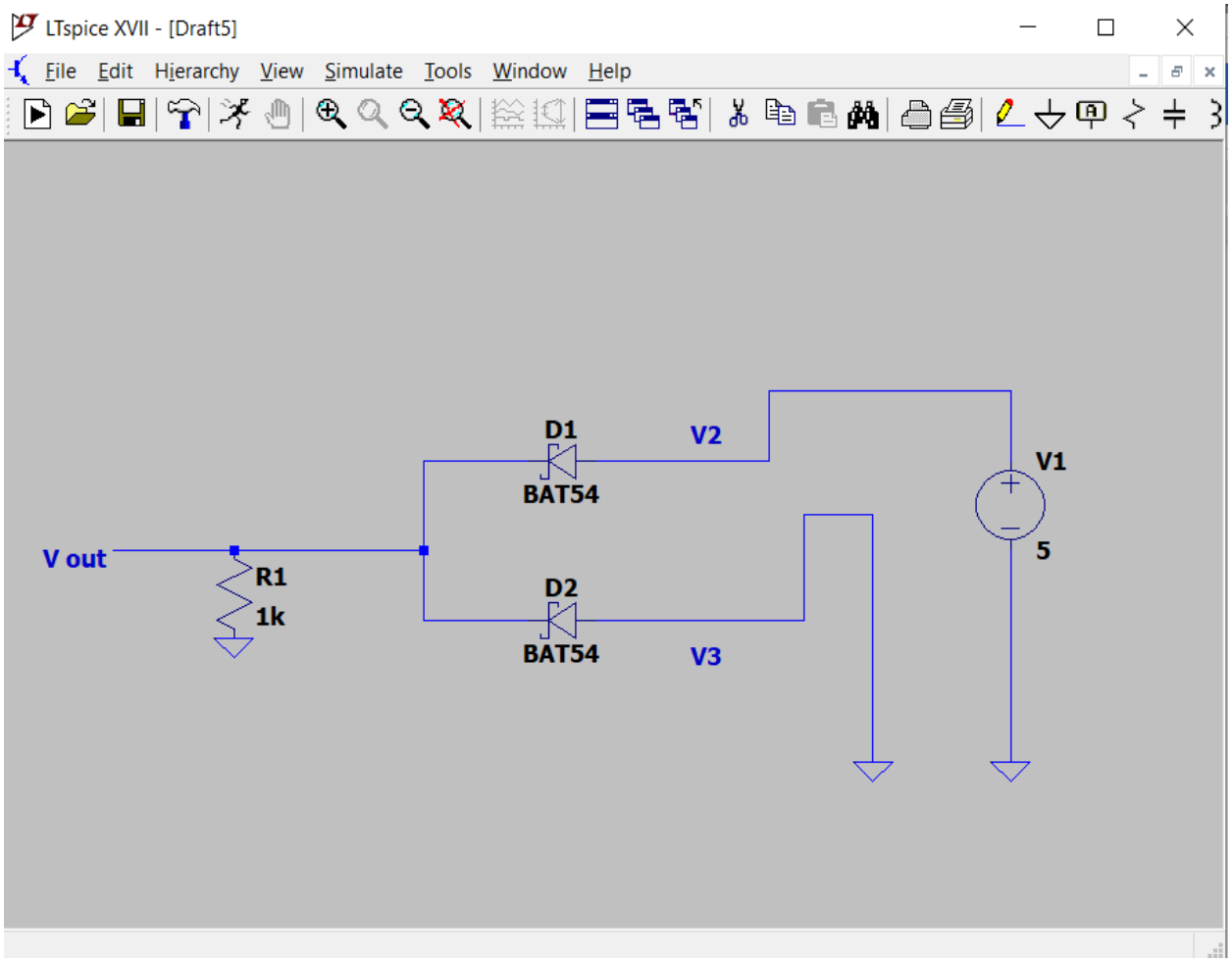
NAND Gate :


File Edit Hierarchy View Simulate Tools Window Help
.tran 10n
PMOS
M2
PMOS
M3
M1
NMOS
M4
NMOS

AND gate:


LTspice XVII - [Draft4]
File Edit Hierarchy View Simulate Tools Window Help
Draft1 Draft4
+V
R1
R
D1
Input 1
V1
BAT54
V out
5
D2
Input 2
BAT54

OR GATE:


LTspice XVII - [Draft5]
File Edit Hierarchy View Simulate Tools Window Help
D1
BAT54
V2
V1
5
V out
R1
1k
D2
BAT54
V3