Lab Report 3.1

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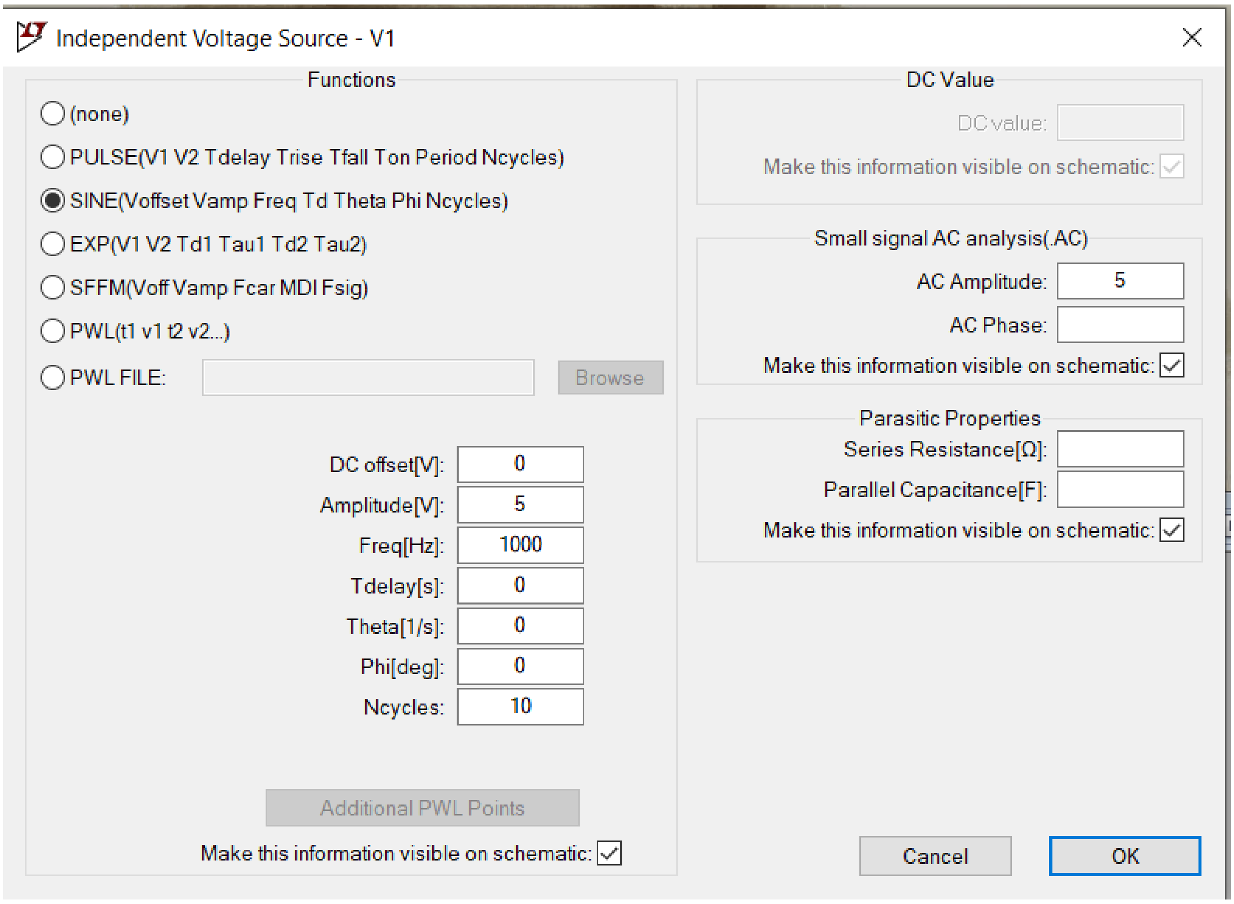
Title of Experiment: Objective 3.1 : For the given RLC circuit, apply input signals of different frequencies and vary the resistance values for a fixed value of L and C and measure output voltage, Vout(t).

Brief Description:

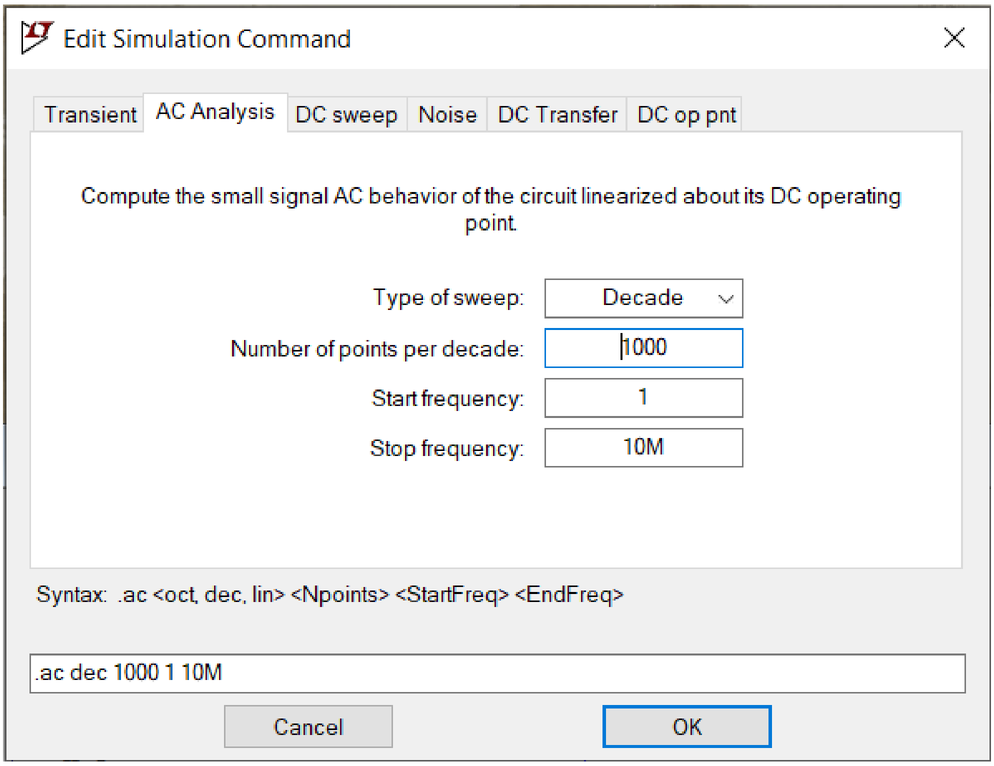
In this experiment, we had to simulate RLC circuits with a sinusoidal input source and AC analysis on LTSpice and then take note of the Voltages across the capacitor with time graphically. The series RLC circuit is composed of an inductor (L) and resistor (R) and capacitor (C) in series along with an input signal with variable frequencies (1Hz-10MHz). Instead of analysing each passive element separately, we can combine all three together into a series RLC circuit. The analysis of a **series RLC circuit** is the same as that for the dual series R_L and R_C circuits we looked at previously, except this time we need to take into account the magnitudes of both X_L and X_C to find the overall circuit reactance. Series RLC circuits are classed as second-order circuits because they contain two energy storage elements, an inductance L and a capacitance C

Schematic diagram:

In our circuit, we consider the following settings for the Independent Voltage Source:



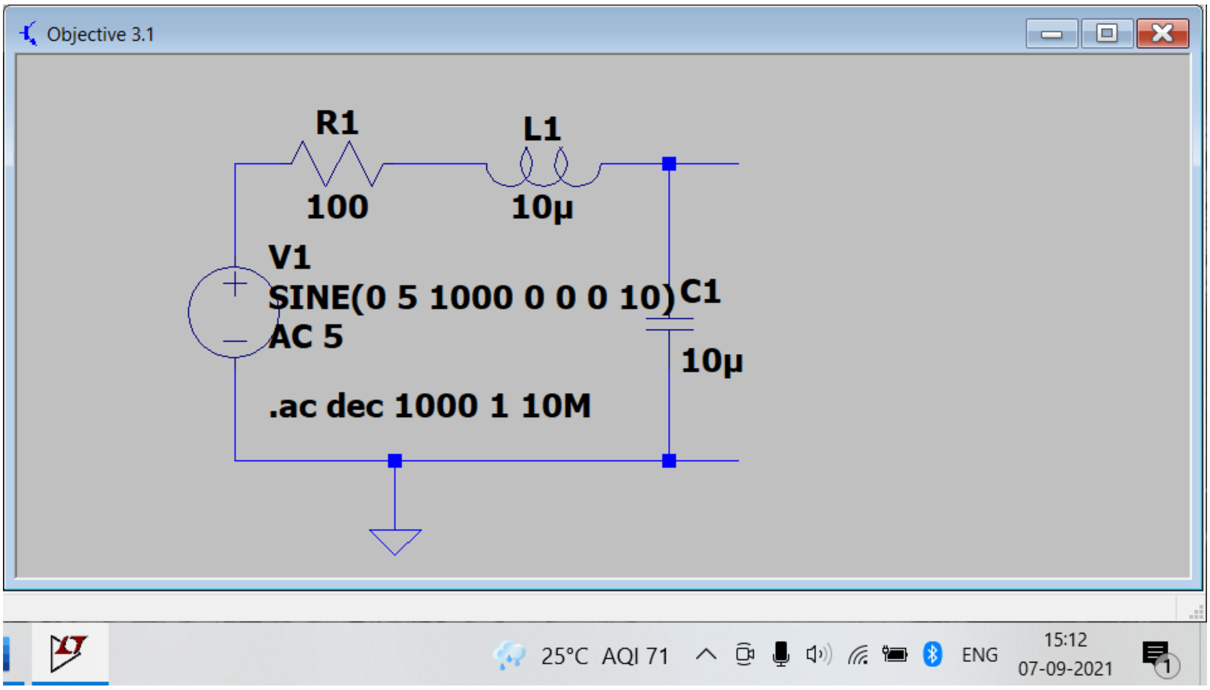
We then use AC analysis of Decade Type with a 1000 points per decade starting from 1Hz- to 10MHz to simulate the circuit.



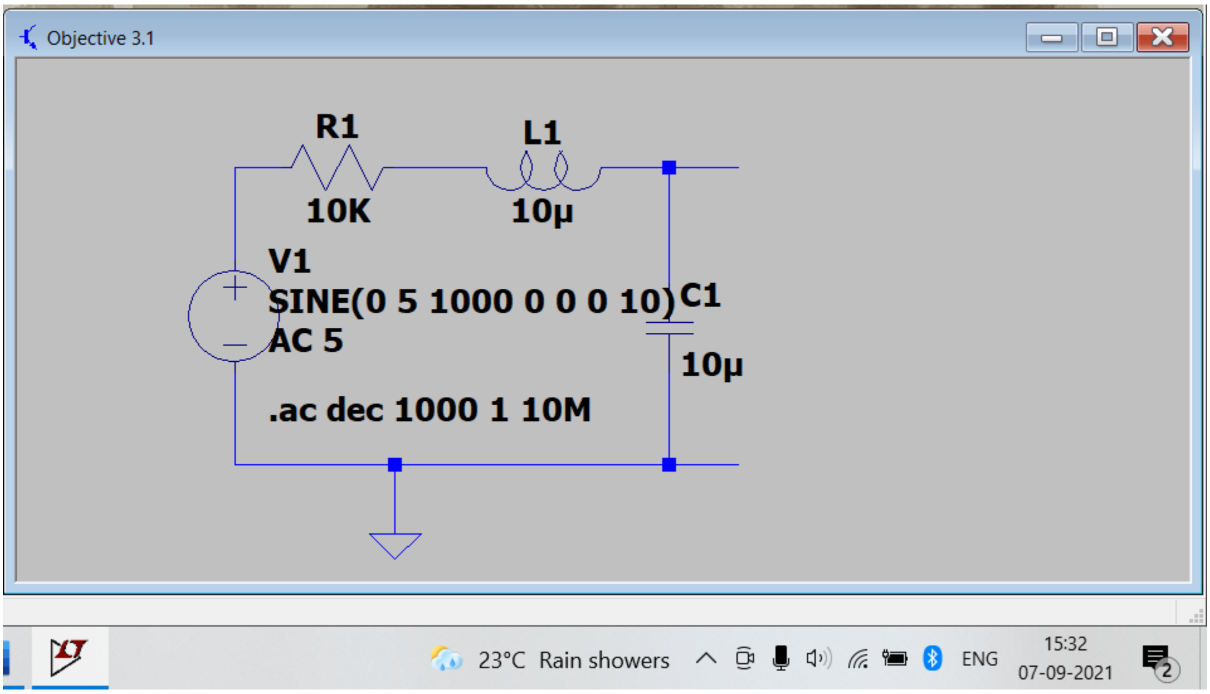
We considered experimenting with the following 3 RLC circuit setups:

Cases

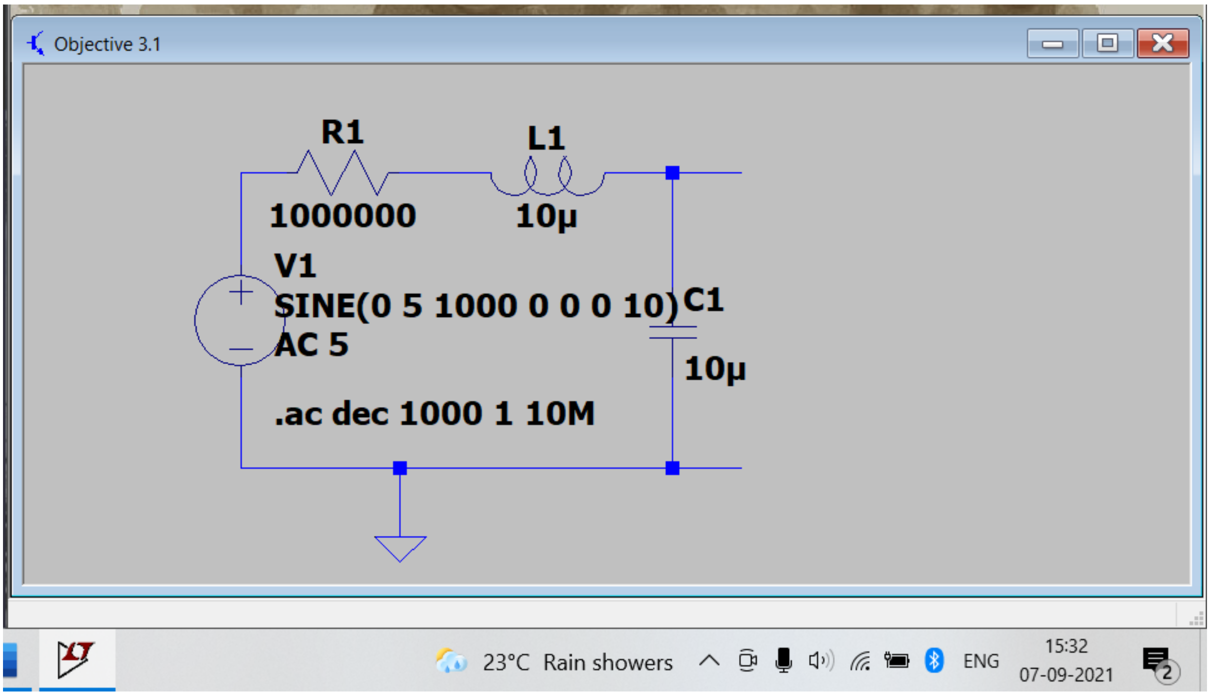
1) R=100Ω ; L=10uH ; C=10uF



2) R=10KΩ ; L=10uH ; C=10uF



3) R=1MΩ ; L=10uH ; C=10uF

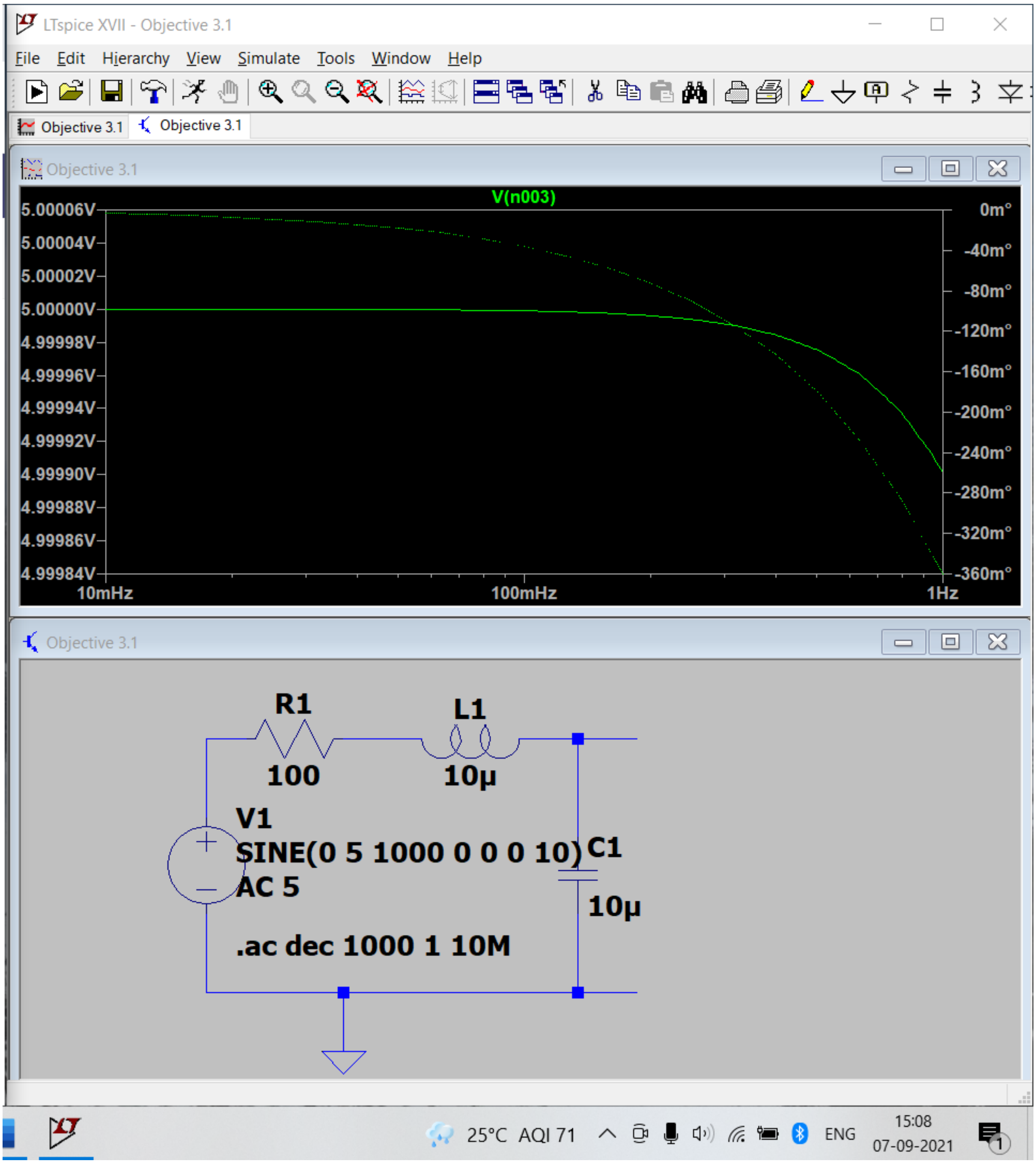


Results:

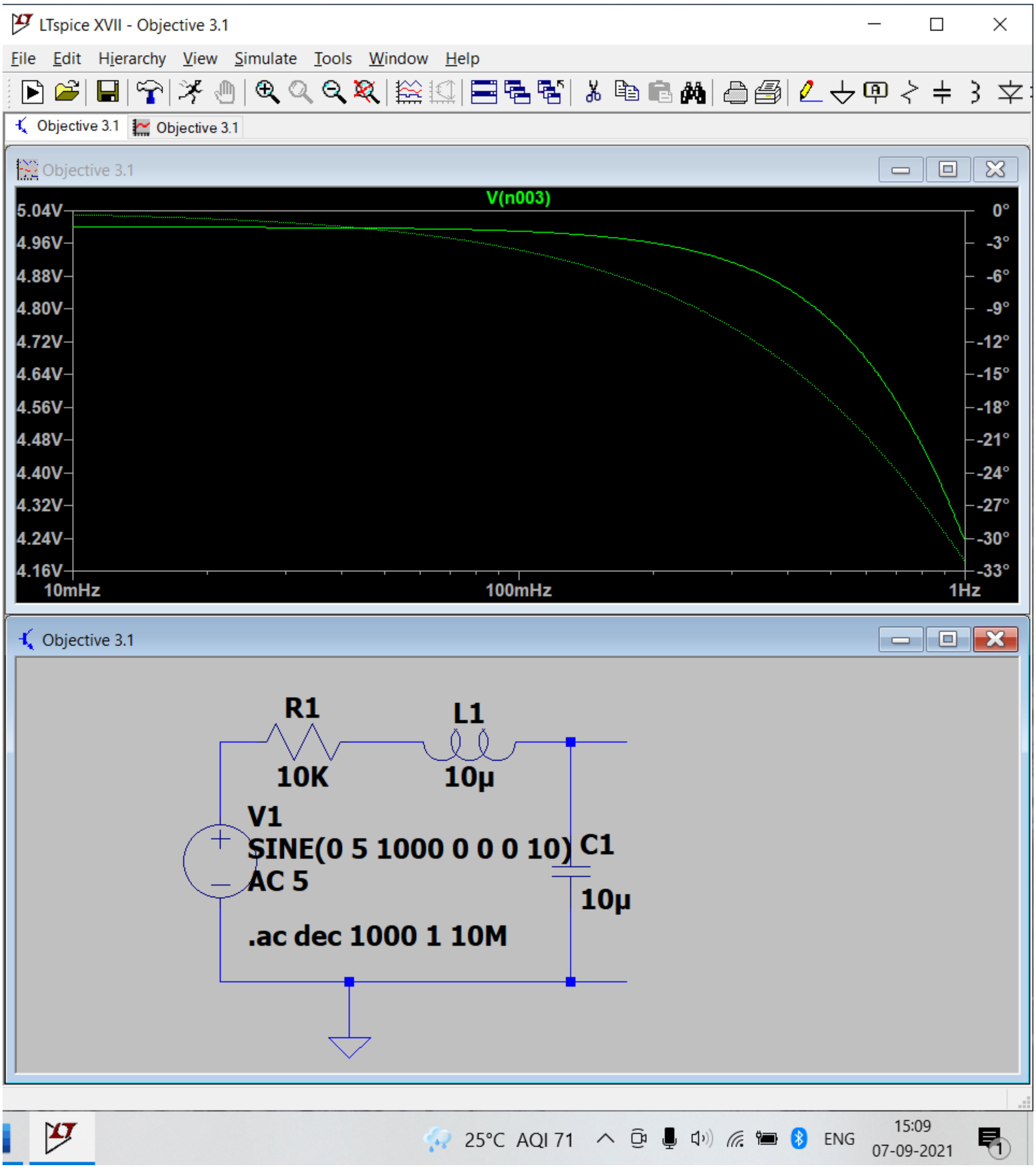
S.No	Resistance (in Ω)	Capacitance(in µF)	Inductance(in µH)
1	100	10	10
2	10000	10	10
3	1000000	10	10

The graphs obtained corresponding to each of the above cases are as follows :

1)

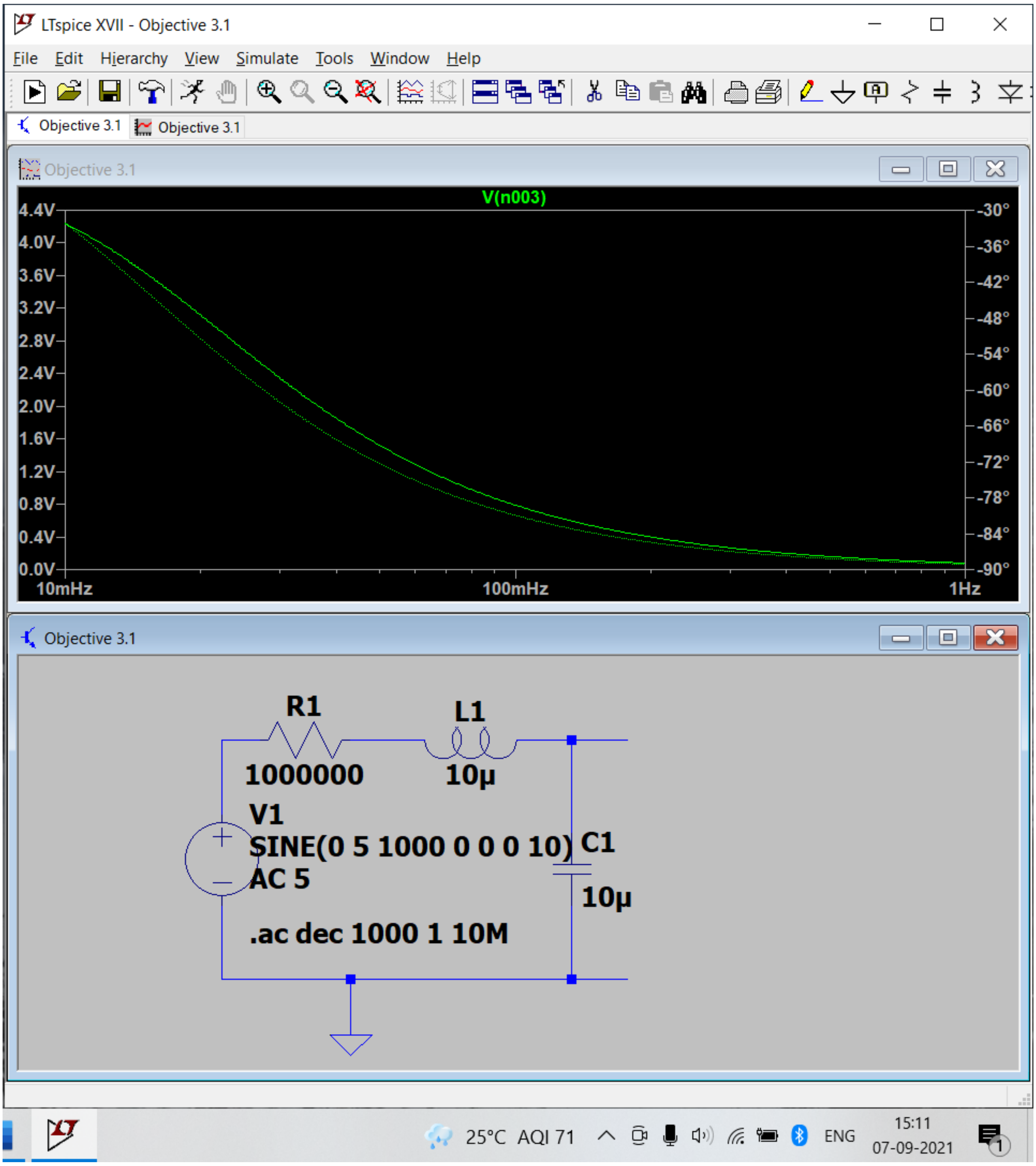


2)



LTspice XVII - Objective 3.1
File Edit Hierarchy View Simulate Tools Window Help
Objective 3.1
Objective 3.1
Objective 3.1
V(n003)
5.04V
4.96V
4.88V
4.80V
4.72V
4.64V
4.56V
4.48V
4.40V
4.32V
4.24V
4.16V
0°
-3°
-6°
-9°
-12°
-15°
-18°
-21°
-24°
-27°
-30°
-33°
10mHz
100mHz
1Hz
Objective 3.1
R1
10K
L1
10µ
V1
SINE(0 5 1000 0 0 0 10)
AC 5
C1
10µ
.ac dec 1000 1 10M
25°C AQI 71
ENG
15:09
07-09-2021

3)


LTspice XVII - Objective 3.1
File Edit Hierarchy View Simulate Tools Window Help
Objective 3.1
Objective 3.1
V(n003)
4.4V
4.0V
3.6V
3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-30°
-36°
-42°
-48°
-54°
-60°
-66°
-72°
-78°
-84°
-90°
10mHz
100mHz
1Hz
Objective 3.1
R1
1000000
L1
10μ
V1
SINE(0 5 1000 0 0 0 10)
AC 5
C1
10μ
.ac dec 1000 1 10M
25°C AQI 71
ENG
15:11
07-09-2021

Discussion:

The following table helps us intuitively understand waveforms and bode plots so obtained.

Element	Resistance	Reactance(X)	Impedance(Z)
Resistor	R	0	Z=R
Inductor	0	ωL	$Z = j\omega L$
Capacitor	0	$1/\omega C$	$Z=1/(j\omega C)$

In case of pure ohmic resistors, the voltage and current waveforms are in phase with each other. In a pure inductor, the voltage waveform leads the current by 90 degrees and in case of a capacitor, the voltage lags current by 90 degrees. This phase difference depends on the reactive value of the components being used as can be seen from the table above.

The RLC circuit helps us analyze each of the circuit elements simultaneously. Contrary to the RC and RL circuits, in this circuit, we considered L and C together while calculating the overall circuit's reactance. This setup being a series circuit, had the same current flowing through each of the elements. We conclude that since reactances of L and C are a function of frequency as can be seen from the table above, hence the sinusoidal response of the circuit happens to vary with input frequency (which can also be inferred from the Bode Plots in terms of output voltage and phase). Additionally, the individual voltage drop of each of the circuit elements will be out of phase with each other.