ZVS Tank Optimization for Class-D Amplifiers in High Frequency WPT Applications

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***Abstract*— Increasing the operation switching frequency of resonant wireless power transfer (WPT) systems could minimize the converter and coil size, for low and medium power applications, as for example in medical implants. Maintaining zero voltage switching (ZVS) is one of the main concerns of designing the inverter at multi-MHz switching frequencies (6.78 MHz and 13.56 MHz industrial scientific medical bands), especially when the coupling is very low. ZVS Class-D amplifiers appear as a good candidate due to their good behavior at high frequency and load-independent characteristic. However, the deadtime in high frequency will cause a big error to design the ZVS tank inductance when the GaN devices are used due to the high body diode forward voltage drop. This paper focuses on the ZVS Class-D amplifier analysis, presenting an accurate modeling of the switching node waveforms, proposing a phase correction method based on first harmonic approximation (FHA) to design the ZVS tank circuit. This model is then used to derive an optimization method for designing the ZVS network. To validate the model, an experimental prototype of a 2W battery charger for medical implant is designed and compared to the analytical solutions and simulations.**

Keywords—wireless power transfer, Class-D amplifier, zero voltage switching (ZVS), 6.78MHz

I. INTRODUCTION

Recently, wireless power transfer (WPT) has been gaining more attention as a means of transferring power without any physical contact. With the merit of safety and convenience, it has been widely used in various application fields [1]-[5] such as biomedical implants, portable mobile devices, mart cordless kitchen appliances and electric vehicle (EV) charging, where the power level of the system ranges from a few milliwatts up to several kilowatts. Among these applications, the magnetic resonance working at multi-megahertz (MHz) is being widely considered as a promising candidate for low power and small size systems [5]. It is because that generally a higher operating frequency (such as 6.78 and 13.56 MHz) is desirable for a more compact and lighter WPT system with a longer transfer distance. Compared to kHz systems, the trade-off is mainly between the higher components and design cost on the one hand and smaller overall size of the entire system on the other hand. Designing a MHz resonant WPT system, the component parasitic elements and component tolerance should be considered.

High-frequency switch-mode inverters can be suitable candidates for the power source in a multi-MHz WPT system. The Class-E and Class-D amplifier topologies that working at MHz frequencies have been proposed in the literature [6]-[11].

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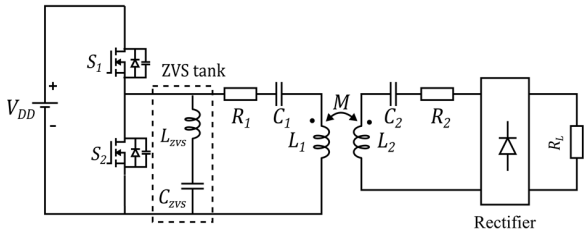

Fig. 1. The schematic of WPT system based on a voltage mode Class-D amplifier.

Generally, Class-E amplifiers provide a very compact and efficient solution for high frequency WPT systems. However, the dependence of the resonant operation point with load and coupling variations complicates the design of this amplifier. The voltage mode Class-D amplifier does not lead to these problems, as no resonance is needed for the operation of this converter. But when working at high frequency, the switching losses can become unacceptable. In a classic voltage mode Class-D amplifier, the switching frequency will be chosen above the resonance to obtain inductive behavior and ZVS condition and reduce the switching losses. Thus, when working above the resonance frequency the input voltage has to be increased to transfer the nominal power, further lower the efficiency. Besides, in high frequency applications, and loosely coupled coils, the power transfer capabilities are very limited, forcing the operation point being at resonant frequency in many cases.

On the other hand, adding a non-resonant ZVS tank to the Class-D amplifier has been proven to be a good alternative to overcome the stated problems [9]-[10]. The ZVS inductor charges and discharges linearly while the top or bottom switches, respectively, are ON, providing enough current to achieve soft switching. In Fig. 1, the schematic of this WPT system based on voltage mode Class-D amplifier is shown. However, in the classical design of Class-D amplifier, the equivalent input voltage is modeled as a square waveform without considering the deadtime which is critical for high frequency application. This non-perfect square waveform caused by the deadtime and forward body diode voltage drop of the switches will introduce a phase shift with respect to its first harmonic, which will cause losses. Thus, designing the ZVS tank circuit to maintain soft switching will be more critical in high frequency applications. Accordingly, this paper proposes a more accurate model and equations to design the ZVS tank. A phase correction method based on First Harmonic Analysis (FHA) is proposed. Experimental results are provided to validate this proposal.

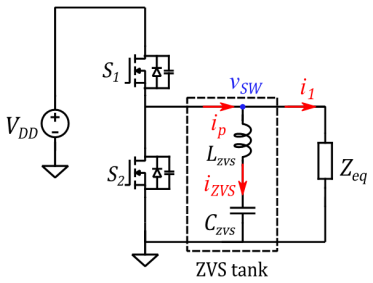

Fig. 2. The equivalent primary schematic working at resonant frequency.

This paper is organized as follows: In Section II, theoretical analysis and design of the Class-D amplifier considering the deadtime is investigated. The equations to design the inductance in the ZVS tank are provided. In Section III, validation by simulation and experimental results are presented. Finally, a summary of the major contribution of this paper is provided in Section IV.

II. ZVS Tank Analysis and Design

The schematic of this system is shown in Fig. 1, consisting of a half-bridge inverter operating in differential mode, along with the series resonant filters, the load, and the ZVS tank. Nonoverlapping switching of S_1-S_2 with 50% duty circle provides a nearly square waveform. The ZVS tank consists of an inductor whose inductance is L_{ZVS}, to provide inductive current to achieve ZVS condition, and a storage capacitor C_{ZVS}, to block DC current in the ZVS tank. L_1 and L_2 are the self-inductances of the transmitting and receiving coils, whose parasitic resistances are R_1 and R_2, respectively. C_1 and C_2 are the compensation capacitors. R_L stands for the load resistance. M is the mutual inductance of L_1 and L_2. The operating frequency f is selected to satisfy:

$$f = \frac{1}{2\pi\sqrt{L_1C_1}} = \frac{1}{2\pi\sqrt{L_2C_2}} \tag{1}$$

The equivalent primary schematic is shown in Fig. 2. When operating at resonance frequency the equivalent load Z_{eq} reflected to the primary will appear resistive, which can be derived as,

$$R_{eq} = R_1 + \frac{\omega^2 M^2}{R_2 + R_0} \tag{2}$$

Where R_0 is the equivalent ac resistance of the load. The switching node voltage v_{sw} is expanded into Fourier's series with components higher than order two neglected, the fundamental component is derived as,

$$v_F = V_F \sin(2\pi f * t + \beta) \tag{3}$$

Where V_F is the first component amplitude of the v_{SW}, β is the phase of the first component. The primary current i_1 can be modeled as a sinusoidal current in phase with the first harmonic of the switching node voltage v_{SW}. The primary current i_1 is derived as,

$$i_1 = \frac{V_F}{R_{eq}} \sin(2\pi f * t + \beta) \tag{4}$$

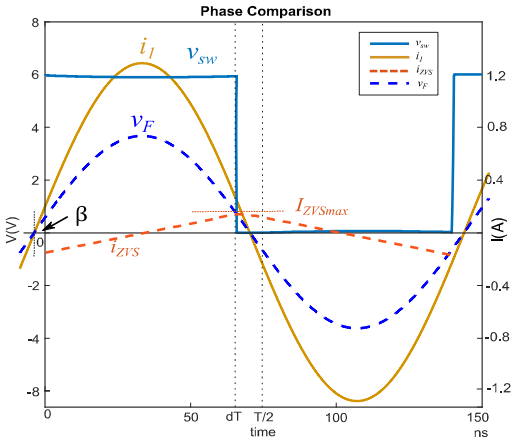

Fig. 3. Main waveforms when v_{SW} is modelled as a square signal with a duty d without considering the transition voltage during the deadtime (L_{ZVS} 300nH).

The primary current before ZVS tank is defined as i_p,

$$i_p = i_{ZVS} + i_1 = I_1 \sin(2\pi f * t + \beta) - \frac{V_{DD}}{2L_{ZVS}}(t - dT) + \\ + I_{ZVS_{max}} \tag{5}$$

V_{DD} represents the input DC voltage. The voltage applied to the L_{ZVS} (V_L) can be approximated as a square voltage alternating between $V_{DD}/2$ and $-V_{DD}/2$. Therefore, the current in the ZVS tank will be triangular, with a peak current of $I_{ZVS_{max}}$. The objective of C_{ZVS} is to provide a constant voltage that assures the symmetry of the voltage applied to L_{ZVS}. The value of the inductance L_{ZVS} must be chosen properly to provide enough current during the dead time to achieve ZVS [9]-[10]. It is important to highlight that the ZVS circuit will not carry the load current. The tank can be optimized to only carry the minimum current to achieve ZVS, minimizing the losses caused by the ESR of C_{ZVS} and L_{ZVS}, which will grow with the increase of the working frequency. The complete ZVS condition can be derived in terms of available inductive charge (Q_L) in comparison with the total charge that must be transitioned in the switches during the dead time (Q_{COSS}) [10]. The total inductive charge Q_L will include the ZVS network charge as while as the load charge by i_1. The output charge can be calculated with the output capacitance of the switches C_{OSS}. When using low power GaN switches, the gate driver well capacitance C_{well} must also be considered in the output charge when calculating ZVS conditions [9], as it cannot be negligible against C_{OSS}. Defining Δt_{DT} as dead time, the charges in the circuit during the dead time can be expressed as,

$$\begin{cases} Q_{C_{oss}} = (2C_{OSS} + C_{well})V_{DD} \\ Q_L = \int_0^{\Delta t_{DT}} (i_{zvs} + i_1)dt \end{cases} \tag{6}$$

When the resonant WPT link works in perfect resonance, the first harmonic of the switching node voltage (V_{SW}), will be in phase with i_1. Conventionally, this voltage will be considered as a square signal with a duty cycle d, a high value of V_{DD}, and a low value of 0. The main waveforms are shown in Fig. 3. With this assumption, i_1 will be zero in the middle of the dead time the phase of i_1 can be derived as,

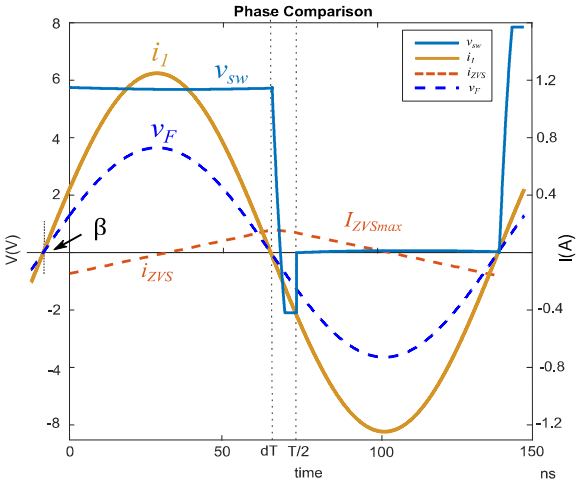

Fig. 4. Main waveforms when transition voltage during the deadtime is considered (L_{ZVS} 300nH).

$$\beta = \frac{\pi}{2} - \pi d \tag{7}$$

Thus, the first component of v_{sw} can be derived,

$$v_F = \frac{2V_{DD}}{\pi}\sin(\pi d)\sin\left(2\pi f * t + \frac{\pi}{2} - \pi d\right) \tag{8}$$

When S_1 is conducting the voltage across ZVS inductor in the network is half of the voltage V_{DD}. The relationship can be expressed as,

$$L_{ZVS} * \frac{I_{ZVSmax} - (-I_{ZVSmax})}{d*T} = \frac{1}{2}V_{DD} \tag{9}$$

As i_1 provides a total net zero charge during the dead time, it will not affect the ZVS condition. i_{ZVS} will provide the whole energy to charge Q_{COSS}. The value of the inductance L_{ZVS} must be chosen in order to provide enough current during the dead time to deplete the output charge of one of the amplifier's switches, and to charge the complementary one. The charge should satisfy:

$$Q_{C_{oss}} \leq Q_L \tag{10}$$

Consequently, from (6), (9) and (10) the critical condition to achieve ZVS for L_{zvs} can be derived,

$$L_{ZVS} \leq \frac{\Delta t_{DT}(2d)}{8f_{sw}(2C_{OSS}+C_{well})} \tag{11}$$

(11) considers the deadtime in the ZVS network design, which is nonnegligible in high frequency application when designing the ZVS tank.

But the voltage v_{sw} during the deadtime is not zero as we assume as shown in Fig. 4, the first component of real v_{sw} will lead the square waveform v_{sw} by more than (π/2-πd) degree, which will cause that i_1 crosses zero before the middle of the deadtime. It will also result in an error when designing L_{zvs},

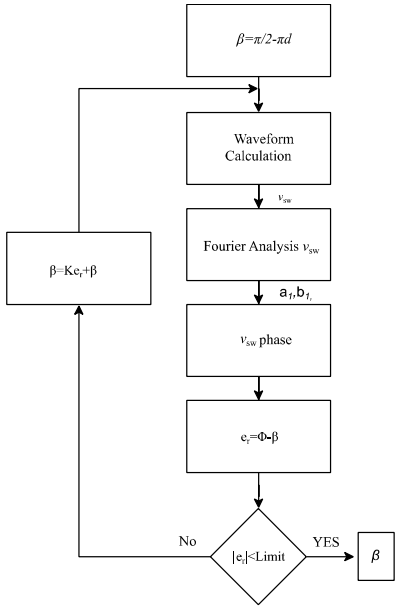

Fig. 5. Algorithm Flowchart to calculate the phase.

which cannot be sufficient to achieve ZVS, leading to additional switching losses. Therefore, the discharge by i_1 during the deadtime should be considered when design the inductance of L_{zvs}. In order to correctly model the system and obtain a more accurate inductance value, i_1 and v_{sw} during the deadtime must also be considered, which supposes correctly estimation of β. For low power, high frequency applications the distortion of v_{sw} waveforms during deadtime will influence the first component's phase, and the error for using a typical FHA approximation might not be acceptable for the design equations. Deriving the equation for β is not realistic, as in perfect resonance i_1 should be in phase with the first harmonic of v_{sw}, but the v_{sw} waveform during the deadtime also depends on i_1. This cross-relationship complicates the calculation of β that fulfills the stated condition. In this paper, an iterative and numerical process to calculate the first component's phase is proposed. A flow chart for this process is shown in Fig. 5. The calculation process is carried out as follows:

First, the algorithm starts with assuming an arbitrary phase β for i_1, for example, assume that i_1 crosses 0 in the middle of the deadtime, the ideal phase of i_1 will be π/2-πd, and the amplitude does not change. Following, based on (5), the waveform of v_{sw} during the deadtime is solved. Then, Fourier analysis is used to calculate v_F (the first component of v_{sw}). The resultant calculated phase of v_F is then compared with the initial phase β assumed in the first step. If the difference between them is not within tolerance, β is then modified proportionally with the error. This process is repeated until the error within the specified tolerance. After some iterations, i_1 and v_F are in phase, the current phase β is found.

The voltage during the deadtime interval ($dT < t < dT+\Delta t_{DT}$) can be expressed as:

$$v_{sw}(t) = V_{DD} - \Delta V_C = V_{DD} - \frac{\int_{dT}^{t}(i_{zvs}+i_1)dt}{(2C_{OSS}+C_{well})} \tag{12}$$

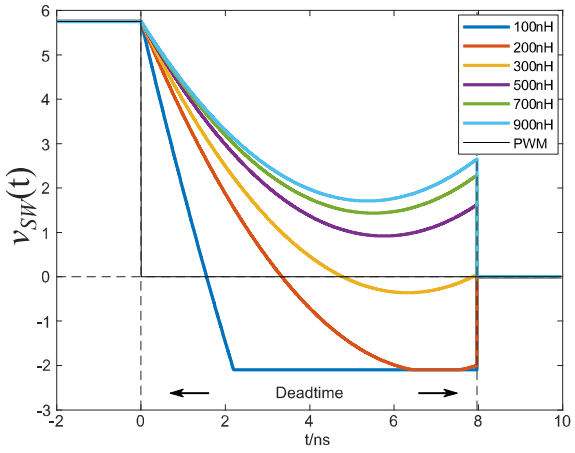

Fig. 6 Transition voltage during the deadtime with different inductance values.

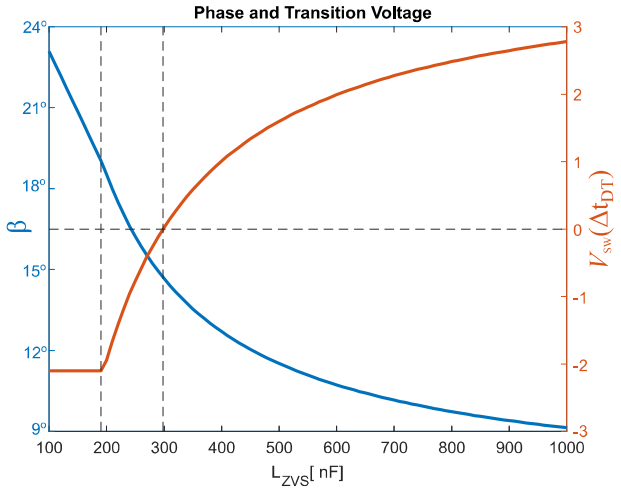

Fig. 7. Phase β and Transition voltage V_{SW} (Δt_{DT}) at the end of the dead time as a function of L_{ZVS}.

If this process is repeated for different L_{ZVS} values, the relation between L_{ZVS} and the current phase β can be found. When the real phase β is known, the instantaneous transition voltages v_{sw}(t) during the deadtime for different L_{zvs} values can be derived, the waveforms of v_{sw}(t) during the deadtime for each L_{zvs} are shown in Fig. 6. The calculated inductance value without considering the deadtime is 500nH. The purple line in Fig. 6 depicts the real transition voltage during the deadtime, while it can be seen with 500nH inductance the ZVS cannot be fully achieved. The maximum inductance value to achieve ZVS is 300nH.

Once the phase is calculated, the ZVS condition and the transition voltage V_{sw} (Δt_{DT}) at the end of the dead time can be derived for each L_{ZVS} value, which is expressed by (13) as shown

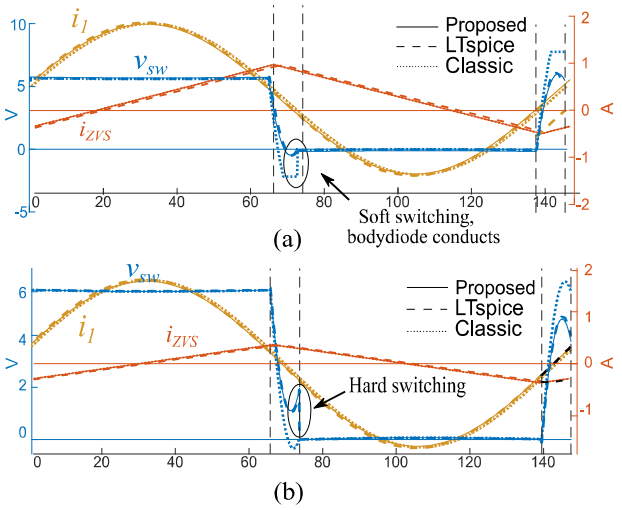

Fig. 8 Main waveforms comparison with different Lzvs, (a) L_{ZVS}=300nH (b) L_{ZVS}=500nH.

at the bottom of this page. The relation of β and V_{sw} (Δt_{DT}) depend on the inductance L_{zvs} is shown in Fig. 7. Four conditions can be divided to analyze it, as following:

- $V_{SW}(\Delta t_{DT}) > 0$: In this case the ouput current i_1+i_{ZVS} is not enough to transfer the whole output electric charge of the switches. The other switch will turn-on with non-zero voltage. The transition voltage will not be zero and switching losses will appear.
- $V_{SW}(\Delta t_{DT}) = 0$: Perfect ZVS condition is fullfilled, no switching losses are present. The L_{ZVS} that achieves this condition, is considered as the optimum inductance.
- $-V_{bodydiode} < V_{SW}(\Delta t_{DT}) < 0$: In this case i_1+i_{ZVS} is higher than necessary, too much inductive charge is present during the dead time. Negative current will circulate through the switches. At this moment, the body diode of the switches is not conducting. $V_{bodydiode}$ denotes the forward voltage drop of the body diode of GaN device.
- $V_{SW}(\Delta t_{DT}) < -V_{bodydiode}$: When the output current keeps increasing and the transition voltage drops to the forward voltage of the body diode of the switches, current starts to flow through the body diode, and voltage is clamped to -$V_{bodydiode}$. In this scenario a part of switching losses, inverse conduction losses appear due to voltage drop. When v_{sw} at the end of the dead time (Fig. 6) is negative or the body diode of GaN conducts, it means ZVS is achieved. When V_{SW}(Δt_{DT}) = 0, L_{zvs} =300nH, the perfect ZVS condition is fulfilled. While, the inductance value calculated from the traditional equation is 500nH, which cannot be achieved ZVS.

$$V_{SW}(\Delta t_{DT}) = V_{DD} + \frac{TI_1}{\pi(2C_{OSS}+C_{well})}\cos\left(\frac{2\pi\Delta t_{DT}}{T}+2\pi d+\beta\right) - \frac{TI_1}{\pi(2C_{OSS}+C_{well})}\cos(2\pi d+\beta)$$
$$+\frac{V_{DD}}{4L_{ZVS}(2C_{OSS}+C_{well})}\left(\Delta t_{DT}{}^2\right) - \frac{I_{ZVSmax}}{(2C_{OSS}+C_{well})}\Delta t_{DT} \quad (13)$$

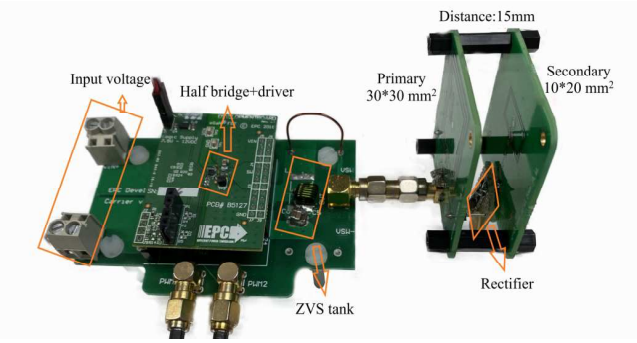

Fig. 9 Experimental Prototype.

TABLE I. MAIN PARAMETERS OF THE SYSTEM

Symbol	Quantity	Value
Vs	Input voltage	6V
f	Operating frequency	6.78MHz
d	Duty cycle	0.46
M	Mutual inductance	620nH
k	Coupling factor	0.06
R_1	Primary coil ac resistance	0.73Ω
R_2	Secondary coil ac resistance	1.23Ω
L_1	Primary inductance	1.55uH
L_2	Secondary inductance	1.55uH
C_1	Primary capacitance	356pF
C_2	Primary capacitance	356pF
R_L	Load resistance	7Ω
$V_{bodydiode}$	Body diode reverse conduct voltage	2.1V

Although the last three conditions are typically considered as ZVS, for low power and high frequency applications, the switches body diode voltage drop can be comparable to V_{DD}, especially if using GaN devices. In this case the optimum L_{ZVS} should be chosen to minimize the switching losses.

A comparison between the analytical model of the proposed and the classic, and the simulation result is shown in Fig. 8. The simulation tool used is LTspice, all the components in the LTspice models are provided by the manufacturers, including the parasitic effects and non-ideal behavior of the switches. It can be seen there is an error between the classic model and the simulation results. However, the proposed model matches well with it. When L_{zvs} is 500nH, ZVS is fully achieved in the classic model, while it is not achieved in the simulation.

III. VALIDATION

A WPT prototype based on battery charger for medical implant devices is built and tested to validate the proposal. The experimental setup is shown in Fig. 9. Switches S_1 and S_2 chosen for the half-bridge are GaN devices (EPC2035). The coils developed are printed-circuit-board coils with a separation distance of 1.5cm transmitter (3×3 cm^2) and receiver (1×2 cm^2). The drivers employed for the high frequency GaN devices are LT5113 from TI. The system works at 6.78MHz (the resonant

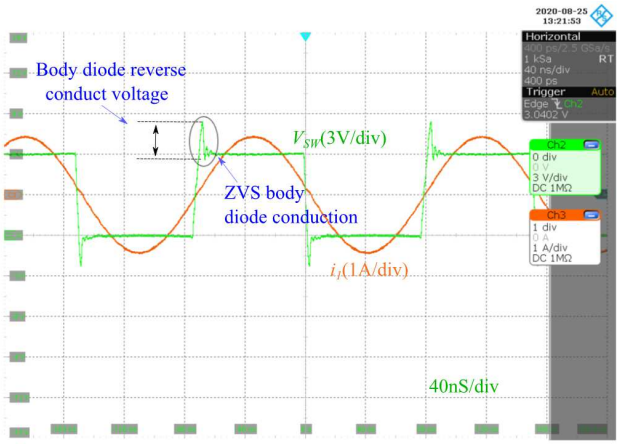

Fig. 10. Input ac voltage and current waveforms based on experiment (L_{ZVS} =300nH).

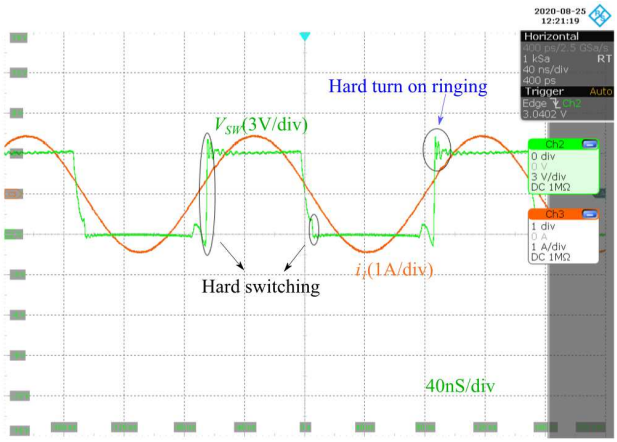

Fig. 11. Input ac voltage and current waveforms based on experiment (L_{ZVS} =500nH).

frequency of primary and secondary). The diodes using for the rectifier are BAT60A from Infineon.

In order to validate the concept presented in this paper, two different values of L_{ZVS} are compared, the predicted optimum inductances with the proposed procedure (Fig. 5.) (300nH) and with the traditional approach (500nH). Fig. 10 and Fig. 11 are experimental results with the two-inductance value, which are in good agreement with the simulation results shown in Fig. 8. The bule waveforms depict the switching node voltage v_{sw}. The orange waveforms denote the primary current through the coil i_1. Fig. 10 shows that the switches in the inverter stage achieve perfect ZVS during the deadtime with an inductance value of 300nH in the ZVS tank. The body diode reverse conduct voltage can be clearly seen in Fig. 10, which indicate that ZVS is achieved on GaN devices. What I should high light here is that the black circles in Fig. 10 and Fig. 11 are different, the one in Fig. 11 shows hard turning on ringing, while the one in Fig. 9 means ZVS is achieved and body diode of GaN is conducting.

The measured system efficiencies are shown in Fig. 12. The triangle line depicts the efficiency measured with L_{ZVS} =300nH, which is slightly higher than 500nH. The new proposed phase

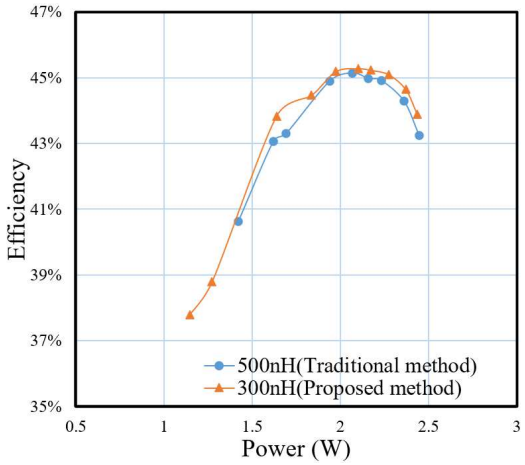

Fig. 12 Efficiency comparison.

calculation method predicts in a very precise manner the i_1 phase, and in consequence the v_{SW} waveform, whereas the classic FHA method fails to predict the ZVS condition. It can also be observed that minimum differences between the phases can lead to high discrepancies in the behavior of the voltage in the switching node.

IV. CONCLUSIONS

This paper presents a more accurate modeling to design the ZVS tank for class-D amplifier in high frequency low coupling WPT applications, taken in to account the deadtime and voltage drop on the body diode conduction. An experimental prototype for medical implant [12] has been built to validate this proposal. With the proposed method, the optimum L_{ZVS} (in ZVS tank) calculated in this paper effectively achieves perfect ZVS condition with a transition voltage of zero volts. System efficiency can be improved compared to the traditional method. All the assumptions made for the analysis are in good agreement with the experimental results. Therefore, it is considered that the proposed method allows for a better analysis for high frequency class-D ZVS amplifiers that results in more accurate design equations to optimize the amplifier. It is worth noting that the usefulness of the proposed algorithm is not relegated exclusively to perfect resonance, since if non-resistive loads were present, the error could be redefined as the difference between the obtained phase and the expected phase because of this new load, iterating until the difference is within a specified range. With this method the optimum inductance value of the inductor in the ZVS tank can be found under different coupling and coupling conditions.

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