Kan Zhu

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OBJECTIVE

A highly motivated engineer seeking a position in low-level programming and hardware-software codesign research.

HONORS & AWARDS

HONORS

Academic Excellence Scholarship for Undergraduates

SKILLS & INTERESTS

COMPUTER

C, C++, Assembly, Java, MATLAB, Verilog, Embedded system, Git, Latex, Microsoft Office, VHDL

LANGUAGES

English – Full Professional Proficiency
Mandarin – Native fluency

INTERESTS

Operating systems, Compilers, Hardware design, Verilog, Badminton, Music

RELEVANT COURSES

Computer Architecture, Intro to Operating Systems, Formal Verification, Embedded System Design, Compiler Construction, Analog Circuits, Instruction to Signal and Systems, Quantum Mechanics

EDUCATION

University of Michigan – GPA 4.00/4.00 — **Ann Arbor, MI**
Major: BS Computer Engineering — September 2021 – Sept 2023

Shanghai Jiao Tong University – GPA 3.82 / 4.00 — **Shanghai, China**
Major: BS Electrical and Computer Engineering — September 2019 – September 2021
Ranking: 10 / 300

RESEARCH EXPERIENCE

EFESLAB, University of Michigan — **Ann Arbor, MI**
Google Data Center Applications Analysis — May 2022 – Present

- Investigated the thread switch behavior and its performance implication
- Identified the performance bottleneck and optimization directions
- Evaluated state-of-the-art prefetchers and replacement policies
- Classified workload and create representative workload subset

PROFESIONAL EXPERIENCE

Shanghai Jiao Tong University — **Shanghai, China**
VG101 Introduction to Programming teaching assistant — May 2021 – July 2021

- Composed lab materials and designed class exercises
- Lead coding lab sections to help students practice programming skills
- Held recitation classes to summarize the key class points for 30 students every week

Student Science and Technology Innovation Association — **Shanghai, China**
Consultant — May 2020 – July 2021

- Hosted cryptography workshop to discuss modern advancements in the technology
- Organized Machinery Competition for the design of a robot to complete several tasks and served as head referee for the competition

RELAVENT COURSE PROJECTS

EECS 470 – COMPUTER ARCHITECTURE — **Ann Arbor, MI**
R10K Based Out of Order Processor — January 2022

- Implemented a ROB, RS, Map Table, Arch. Map Table and Free List, LSQ, D-Cache, I-Cache, together with the necessary Functional Units to deal with high memory latency
- Designed a unit test for each module including several corner cases and an integrated test to comprehensively validate the entire system under pressure
- Included features such as a 2-way superscalar to support multiple instructions, early branch resolution using b-mask to avoid flush/ squash delays, non-blocking I-cache and D-cache, pipeline memory access, and a GUI debugger to improve efficiency

In-Order Processor

- Included data forwarding into an In-Order processor design
- Featured branch speculation and squash

EECS 482 – Introduction to Operating Systems — **Ann Arbor, MI**
Operating System Components — January 2022

- Practiced multithreading programming
- Developed a thread library to provide mutex and conditional variable interfaces
- Implemented a pager to manage memory space for multiple processes
- Created a network file server handling concurrent user requests

EECS 483 – Compiler Construction — **Ann Arbor, MI**
Decaf Compiler — January 2022

- Created a Lexical analyzer using Flex and Syntax analyzer using Bison
- Implemented a Semantic analyzer, TAC code generator, and Code optimizer
- Included features such as class inheritance and polymorphism

SYNERGISTIC ACTIVITIES

Android client development for Quicker — **Ann Arbor, MI**
Contributor — Dec 2021 – Present

- Fixed a bug that occurred when rotating the phone in Android clients of Quicker, a commercial software providing shortcuts for Windows
- Added remote keyboard and touchpad feature