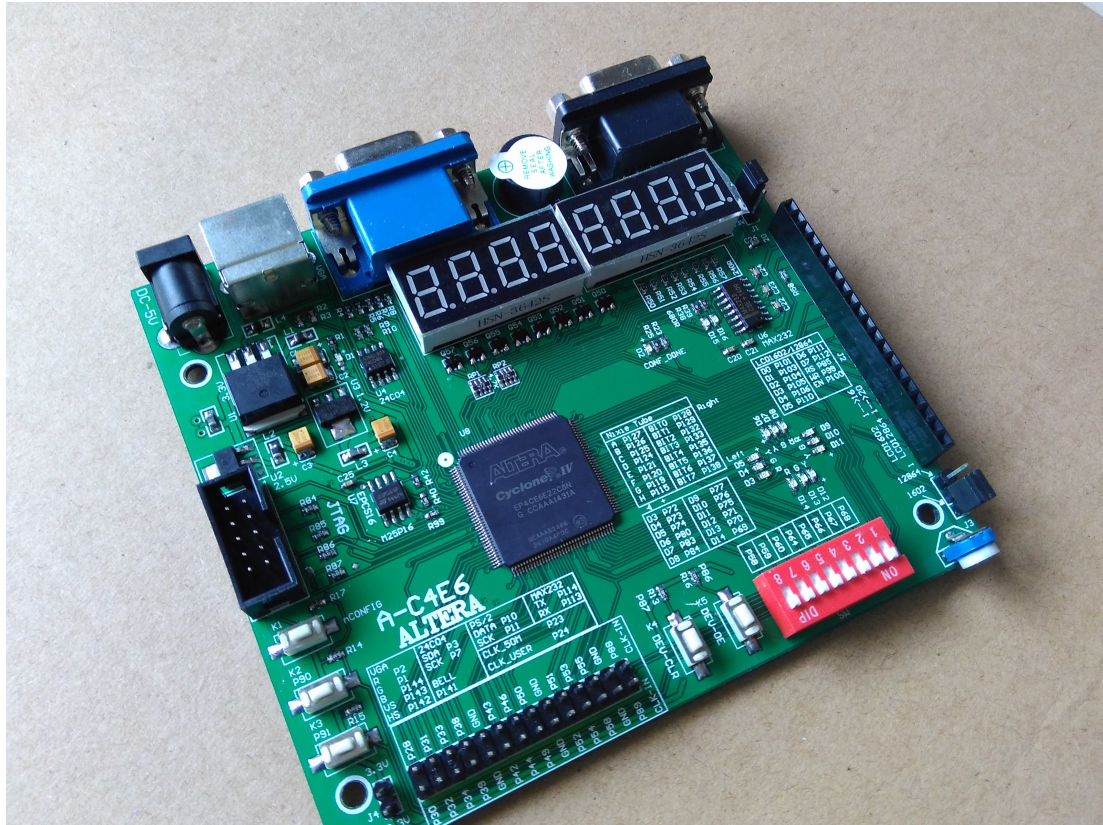


Email:906606596@qq.com

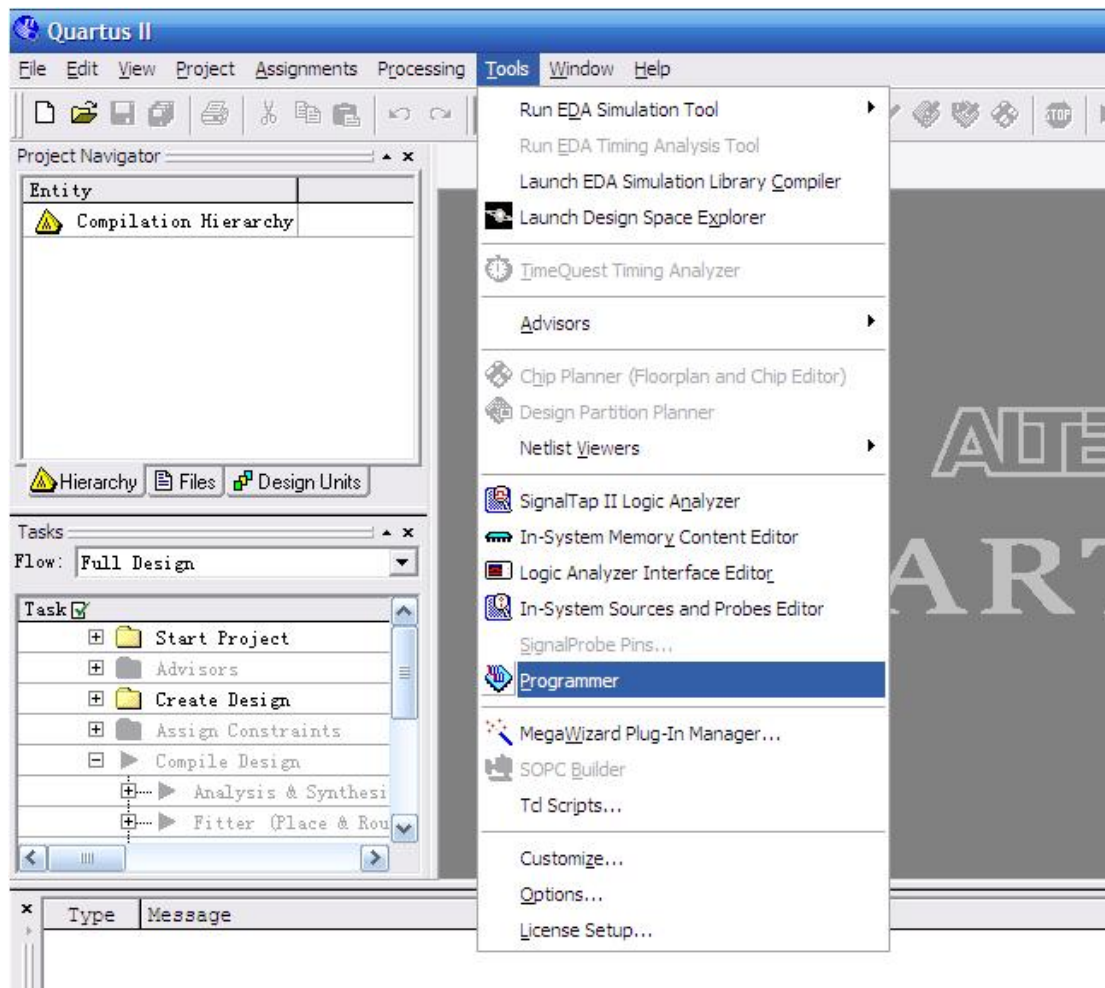
Firstly, we introduce the JTAG interface. We know that FPGA is itself a SRAM structure. Use JTAG to download program, power, will be lost. JTAG interface the FPGA is mainly used to debug a program. For example, we use FPGA, you can use the SignalTap logic analyzer to bring their own internal FPGA, the data transfer to QuartusII above analysis. In NIOS II/SOPC, JTAG_UART can be used to print data. FPGA through JTAG download.SOF file

FPGA in the JTAG mode, board LED D2 will light when you Download, if FPGA . success of configuration. LED D2 will not light .

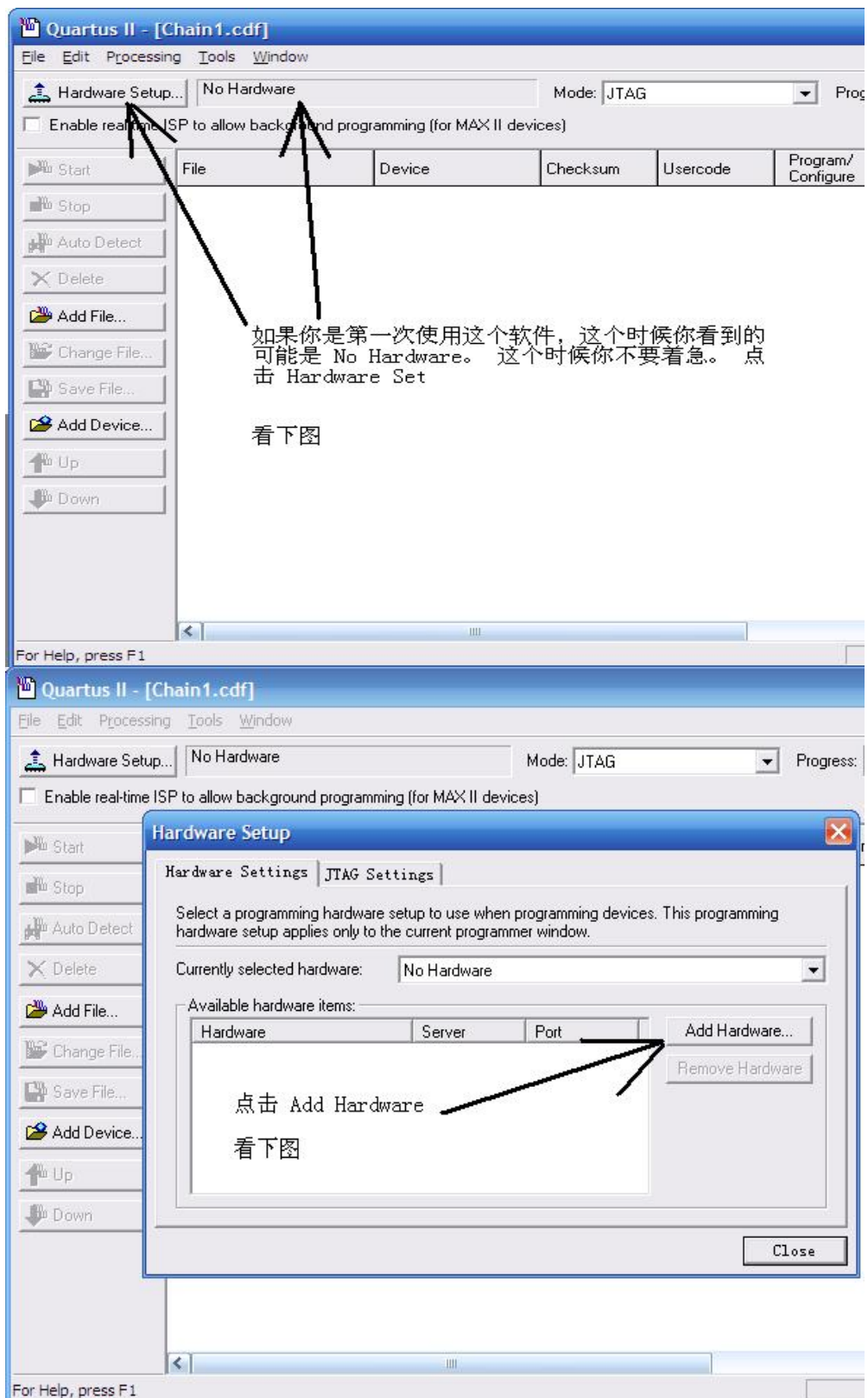


**For example you can do it
Open Quartusii**

Email:906606596@qq.com

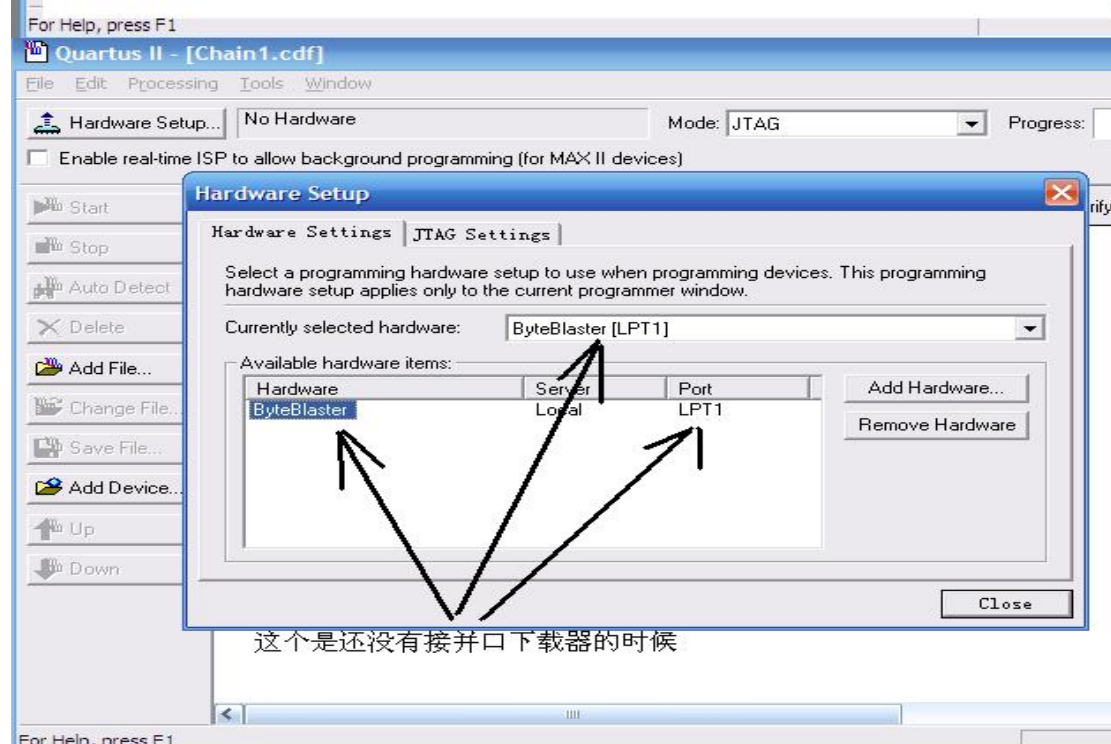


Now our add ByteBlasterII download cable

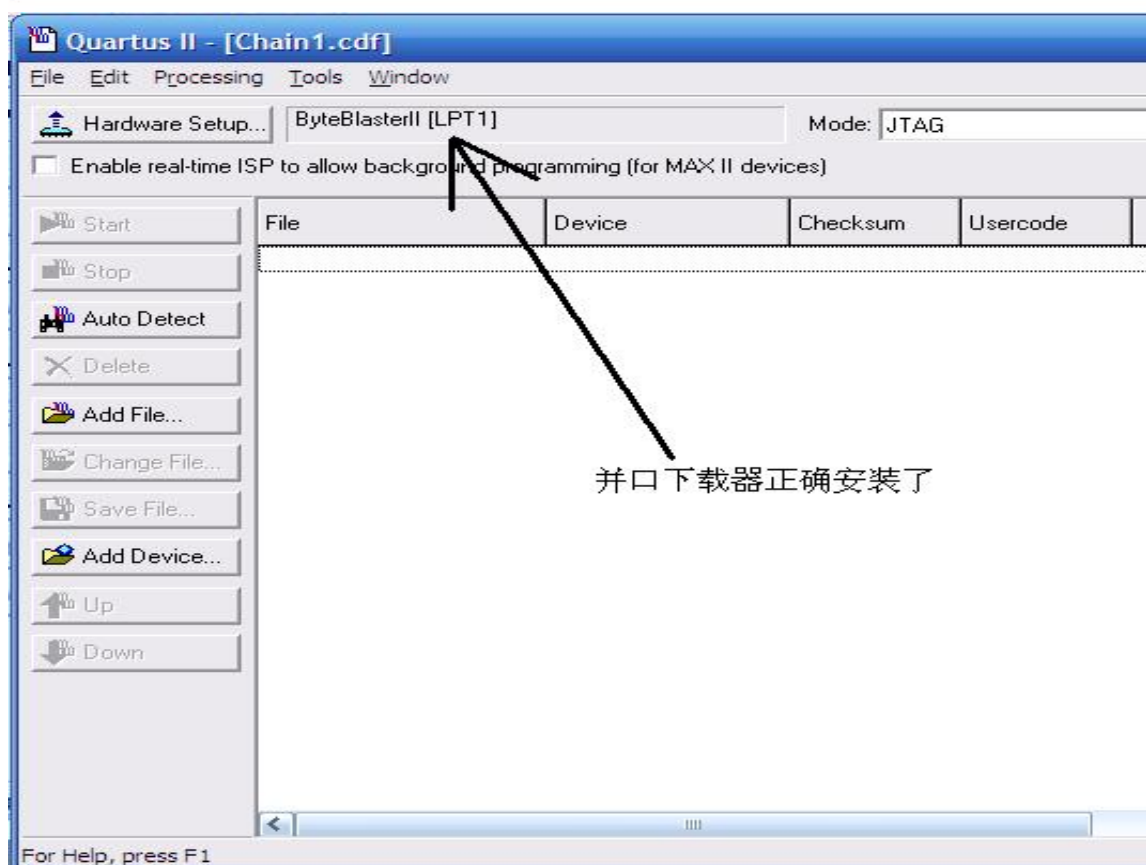
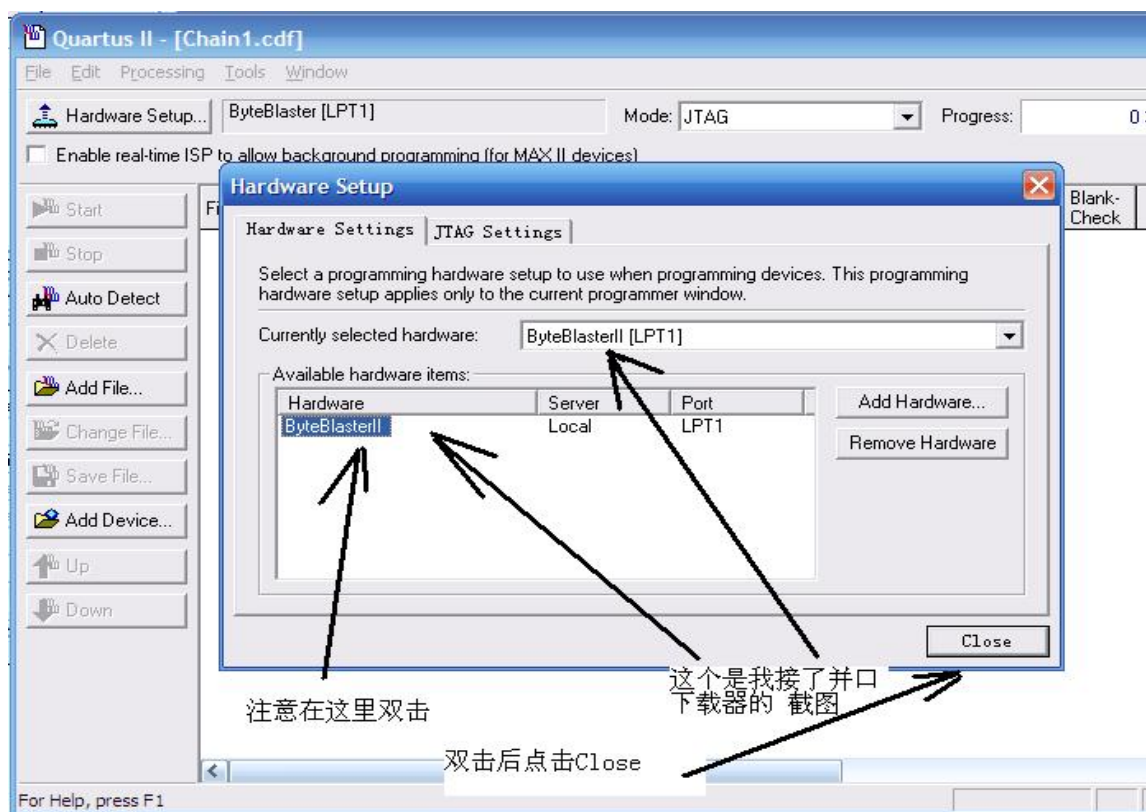


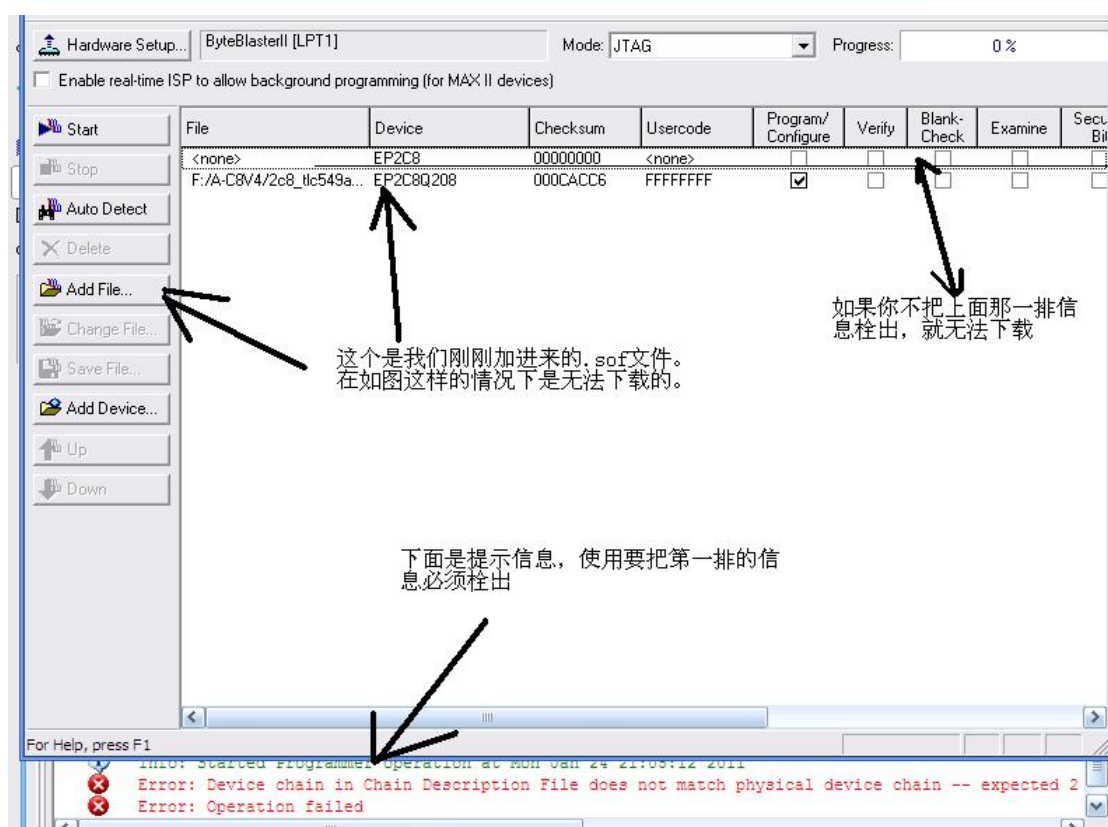
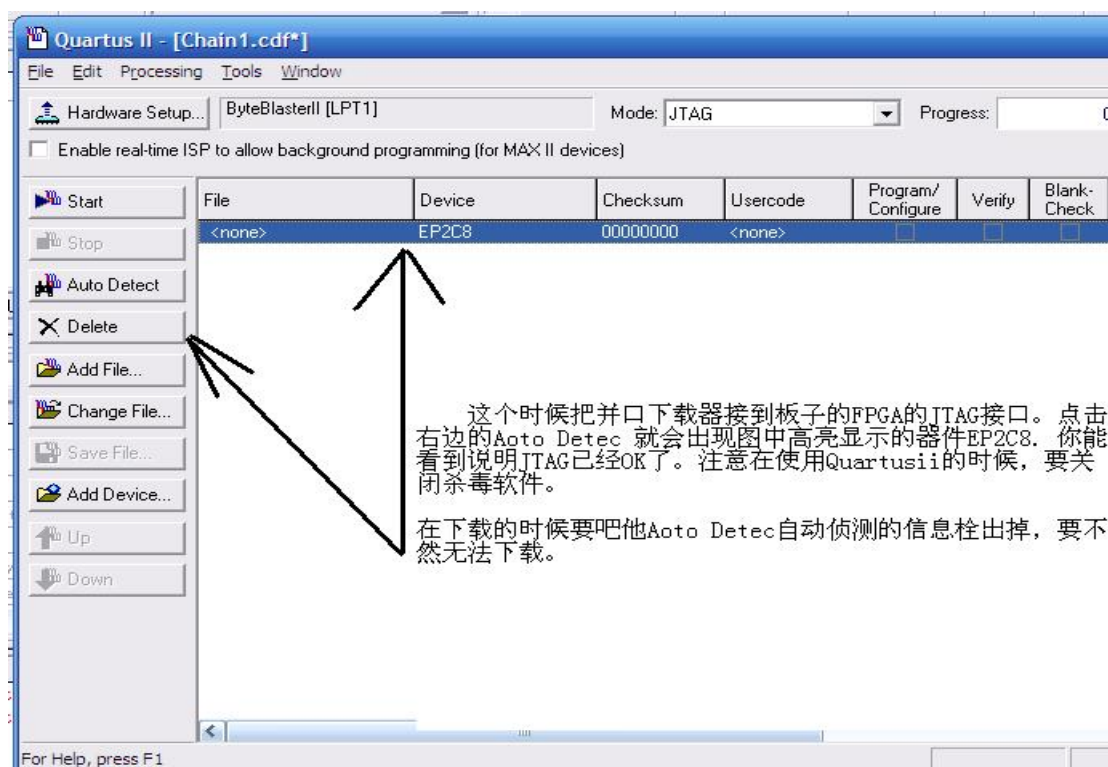


看到这里，差不多就要成功了，如果你还没有看到这个。可能是你的软件还没有弄好。当然你的电脑必须要有25孔的并口。注意要看到ByteBlasterMV or ByteBlasterII 这个和有没有板子没有关系的。我现在截图的就是没有接任何东西的。在点一下 OK

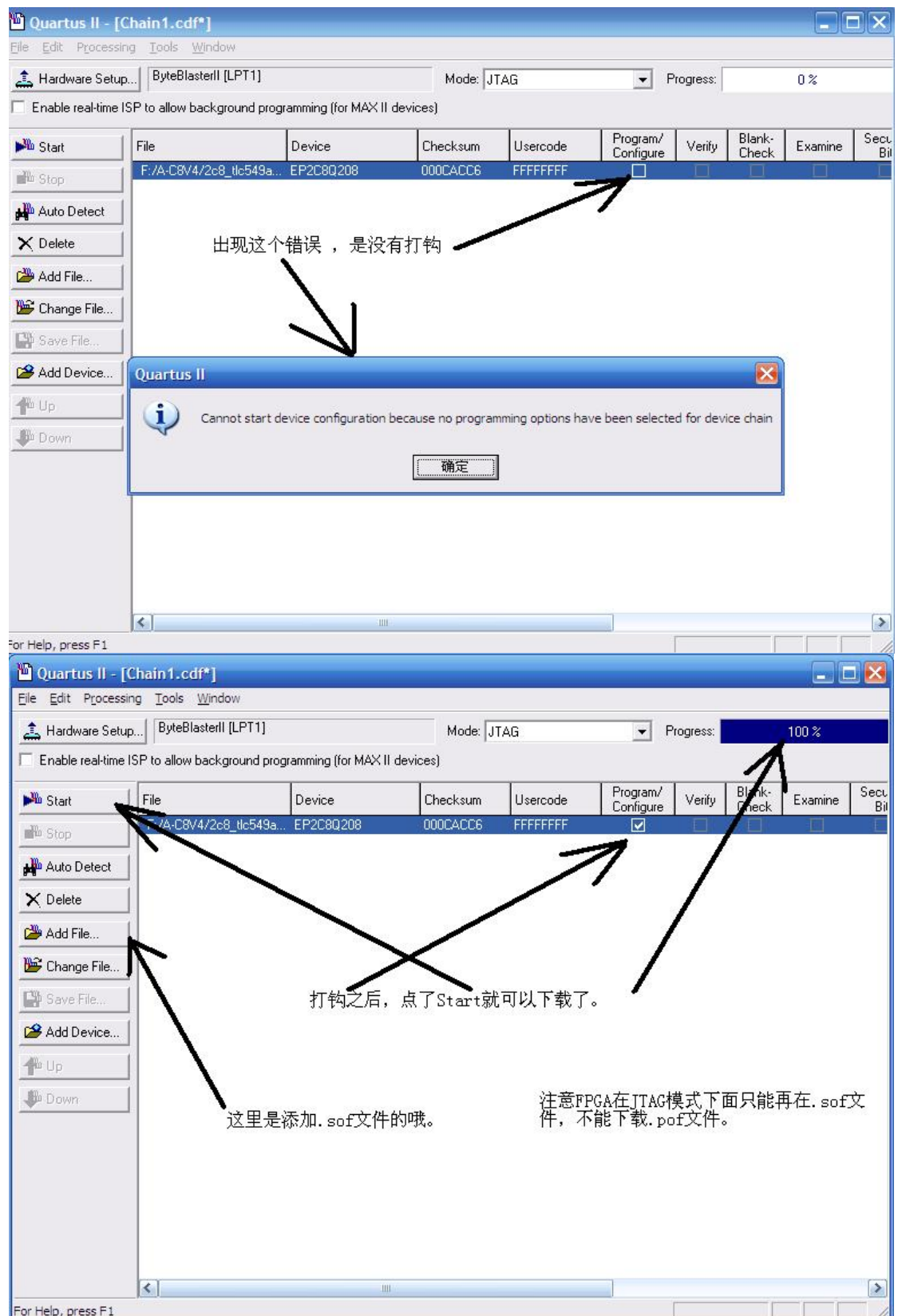


这个是还没有接并口下载器的时候





Email:906606596@qq.com

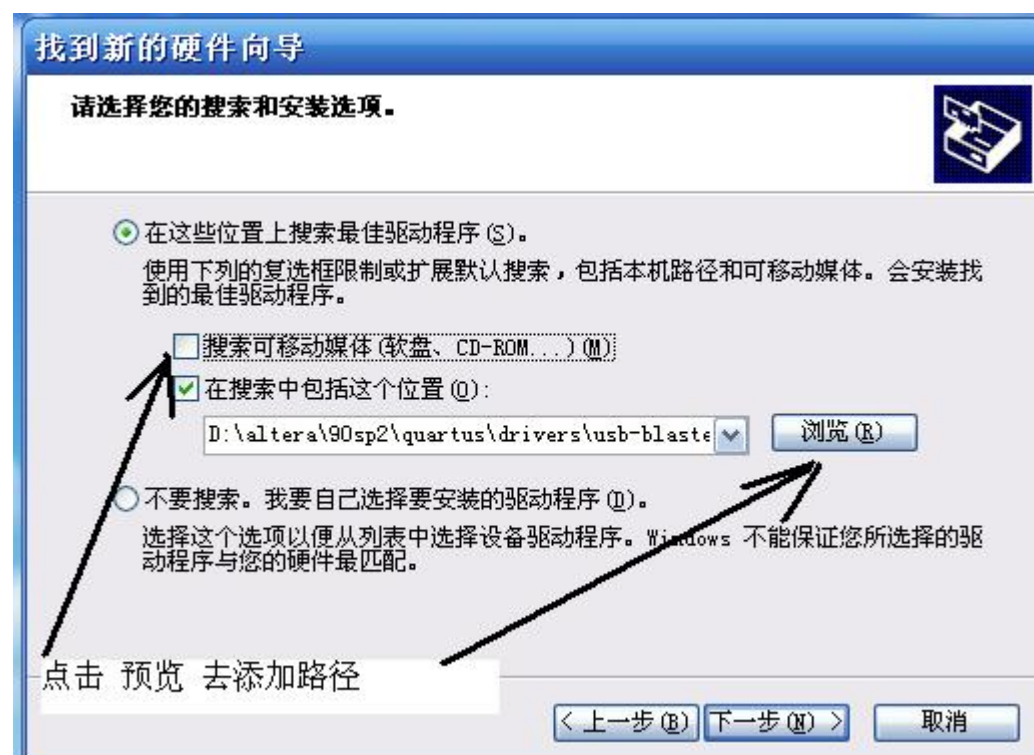


Now our use USB Blaster download cable

Email:906606596@qq.com

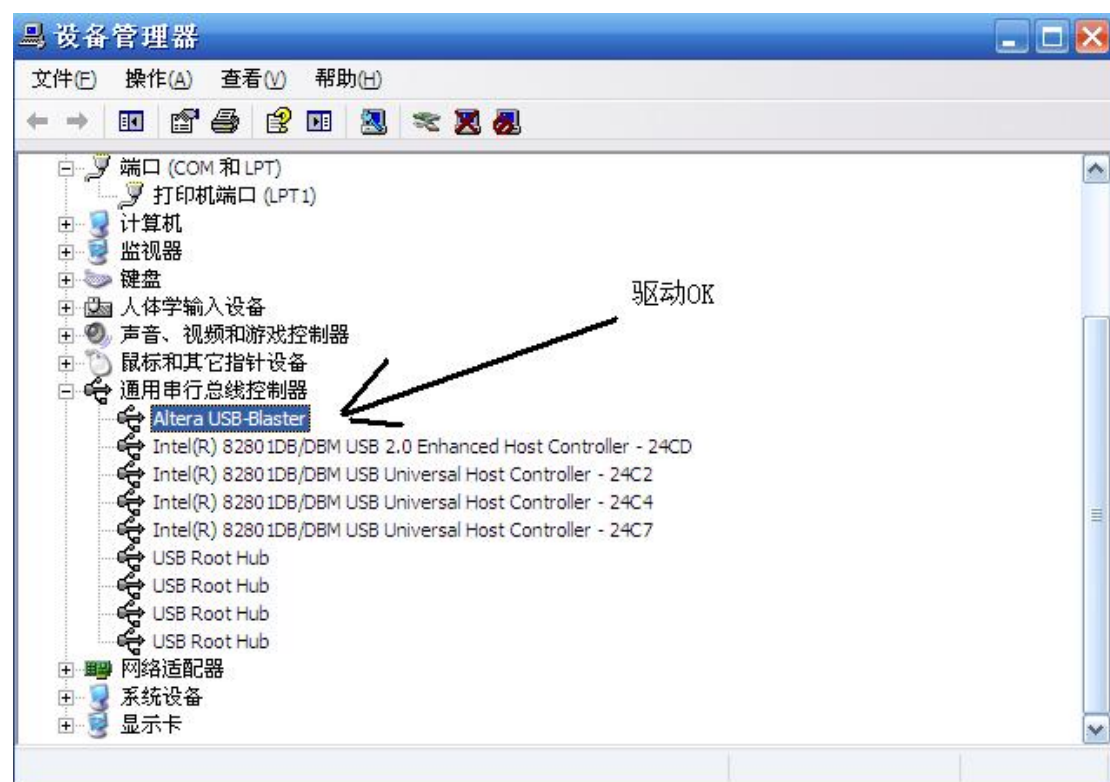






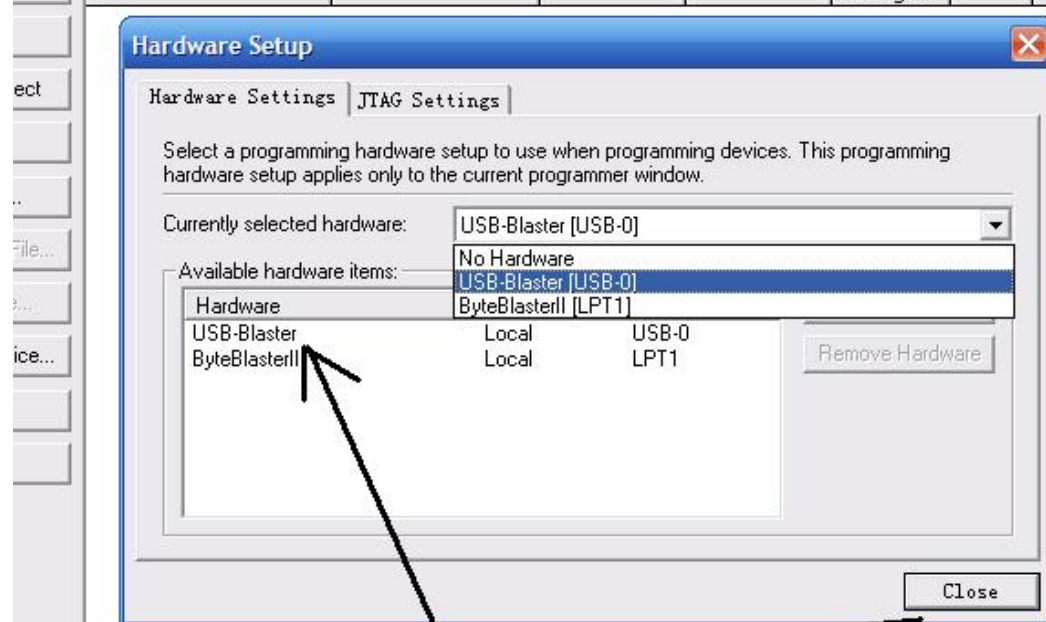






al-time ISP to allow background programming (for MAX II devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check
------	--------	----------	----------	-----------------------	--------	-----------------



使用USB下载器的时候不要忘记
双击USB-Blaster

在点击 Close

