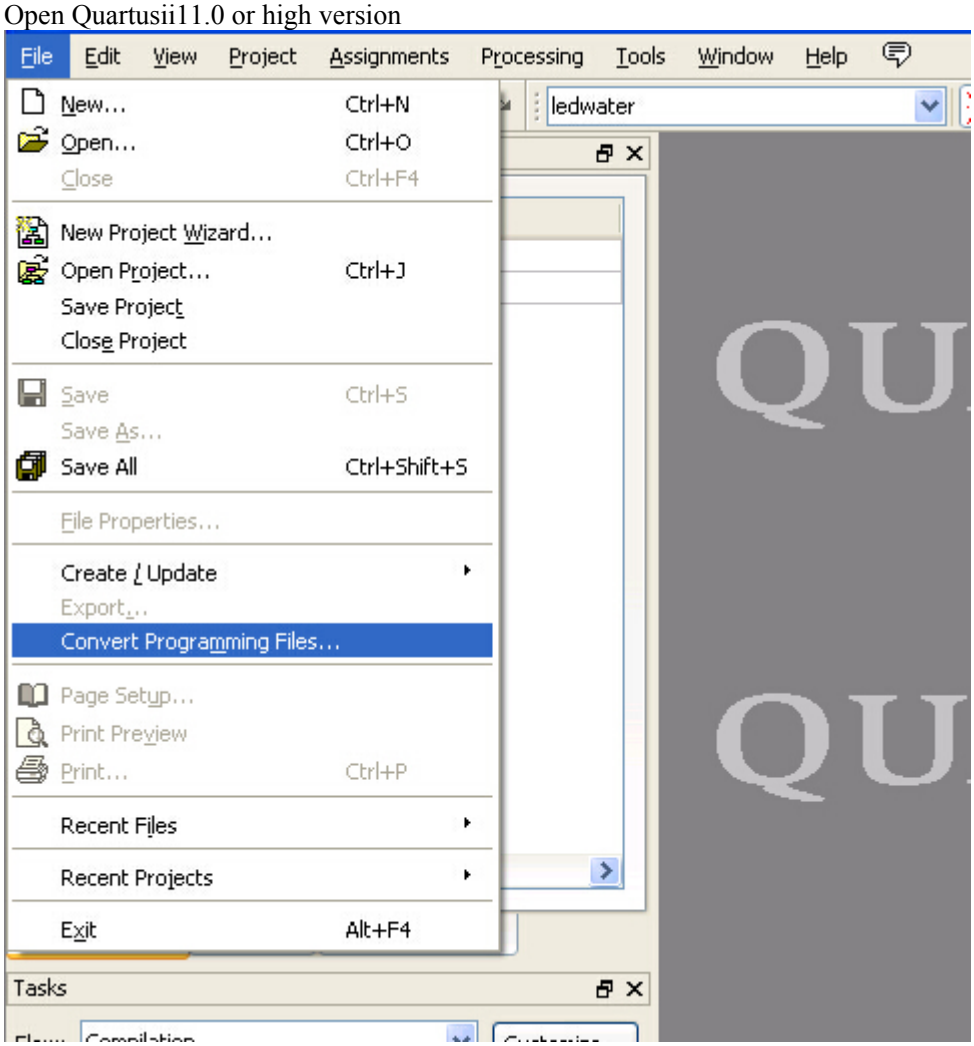
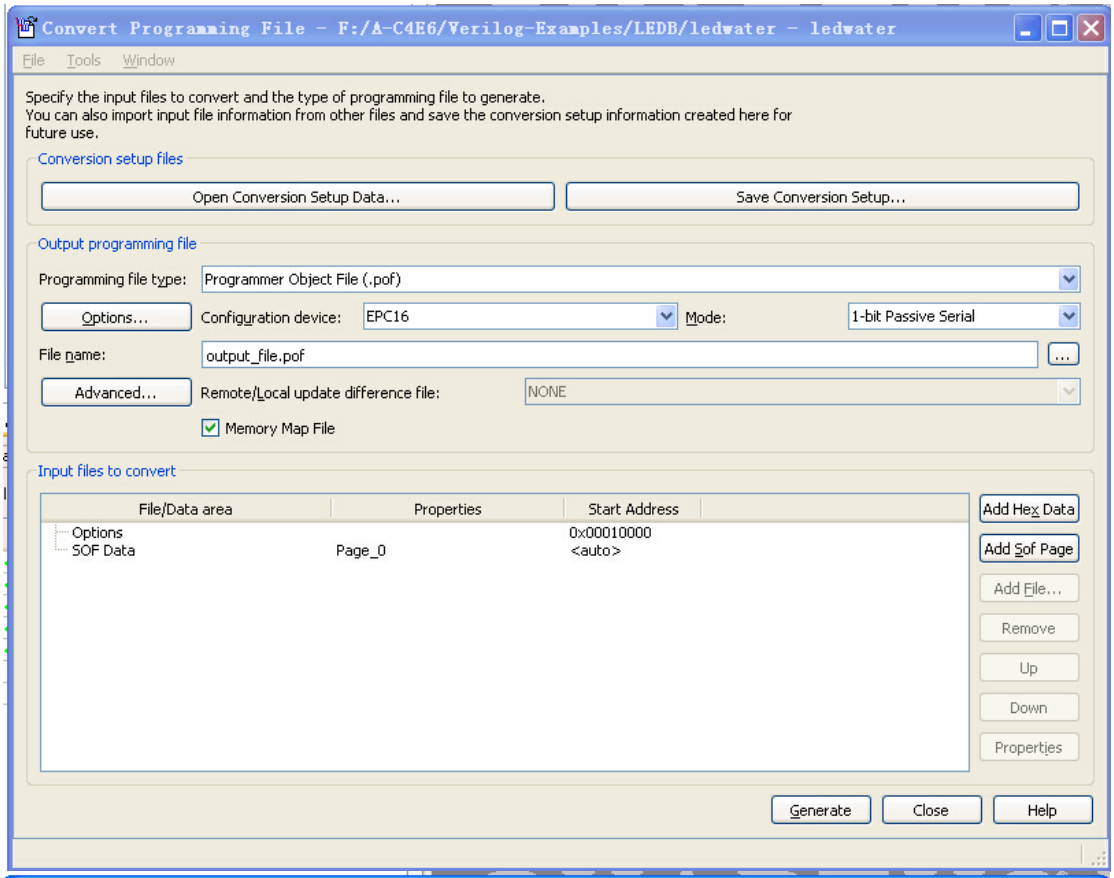
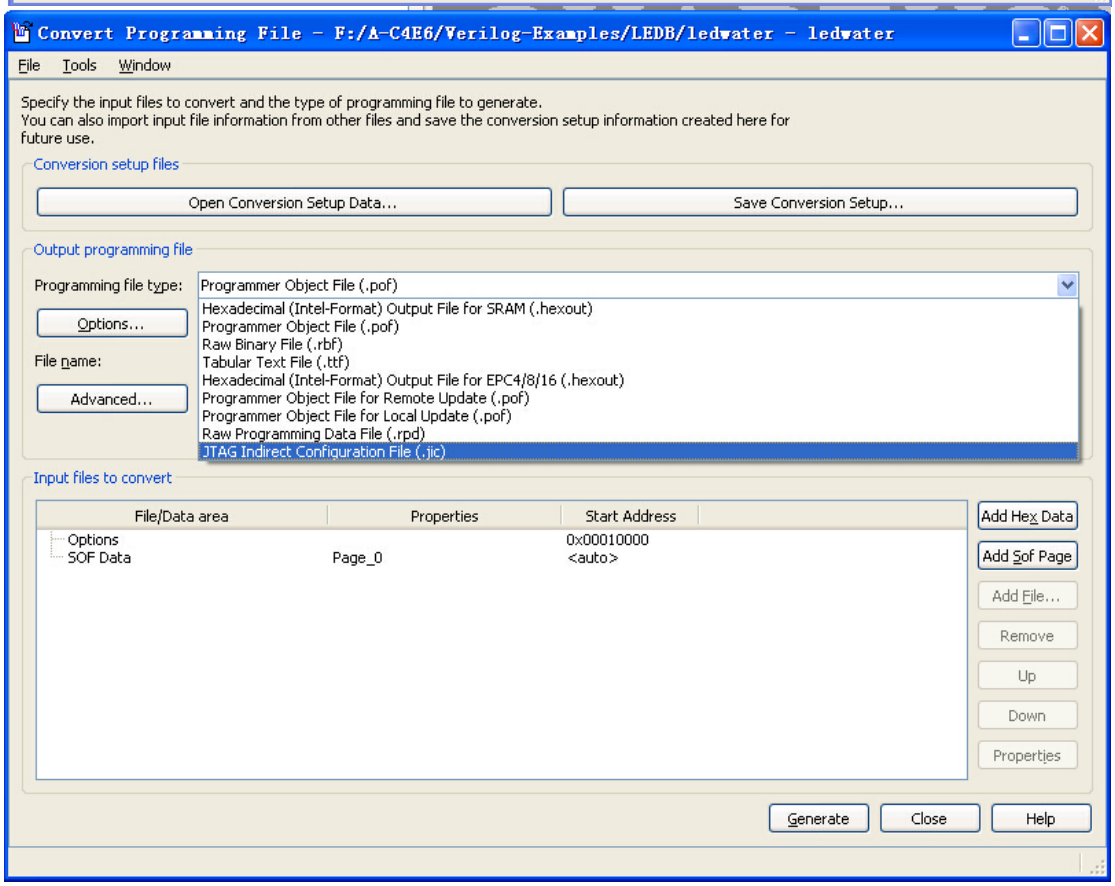
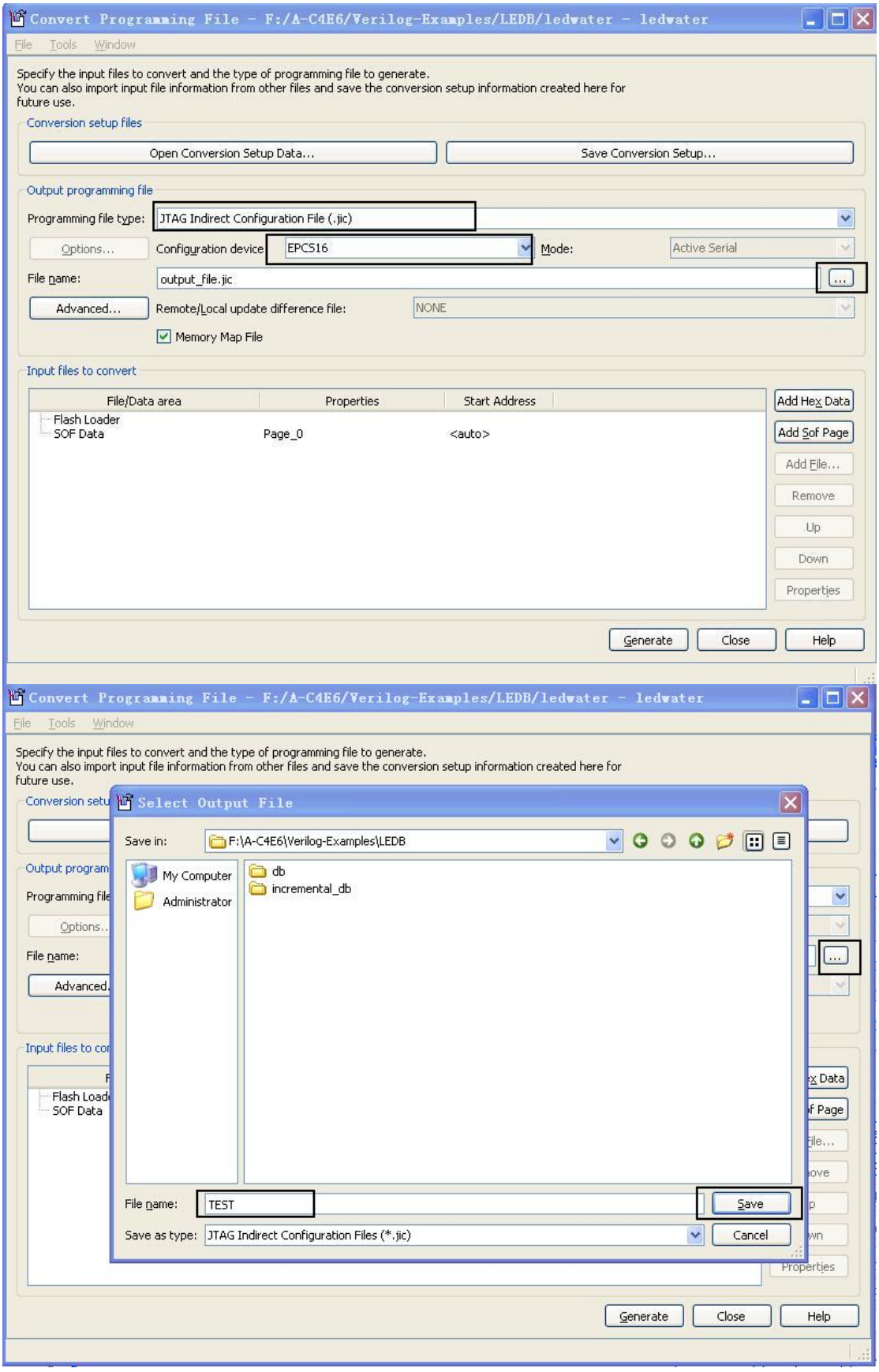
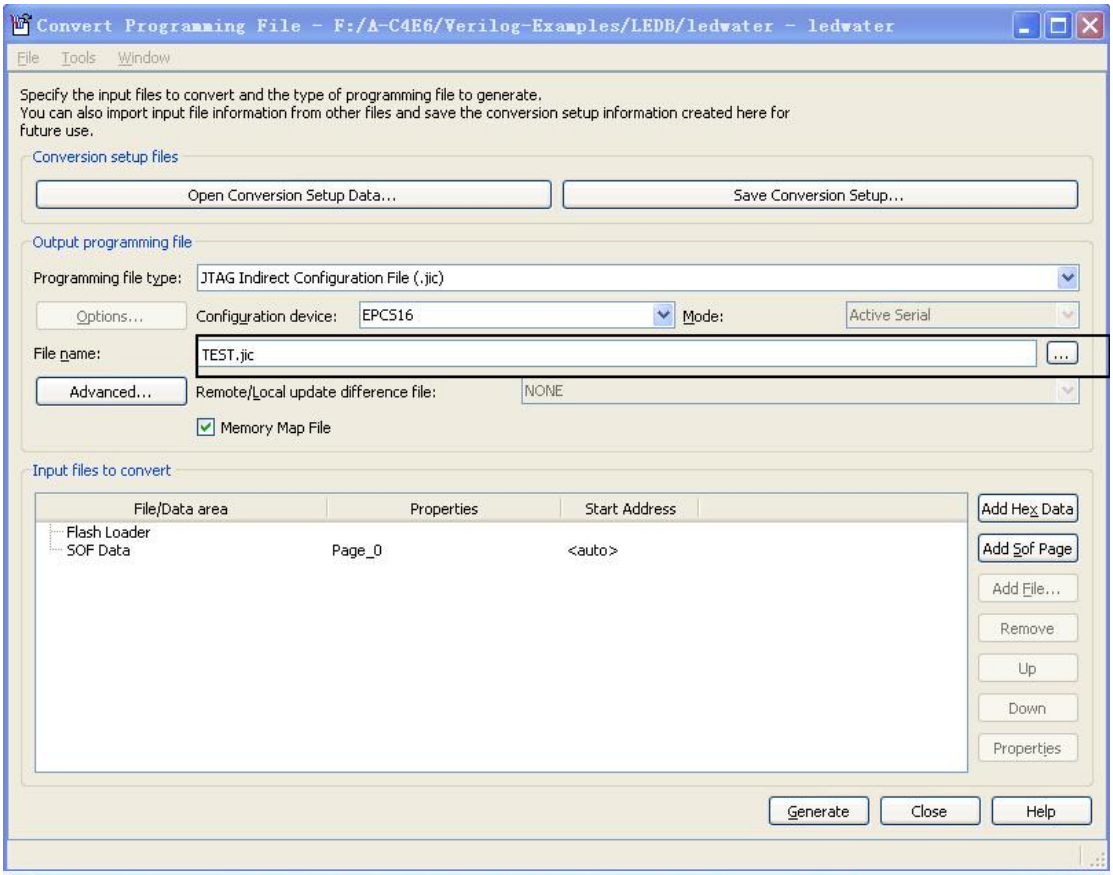
You can do it ,do it like me . JTAG download .JIC to EPCS16
Open Quartusii11.0 or high version

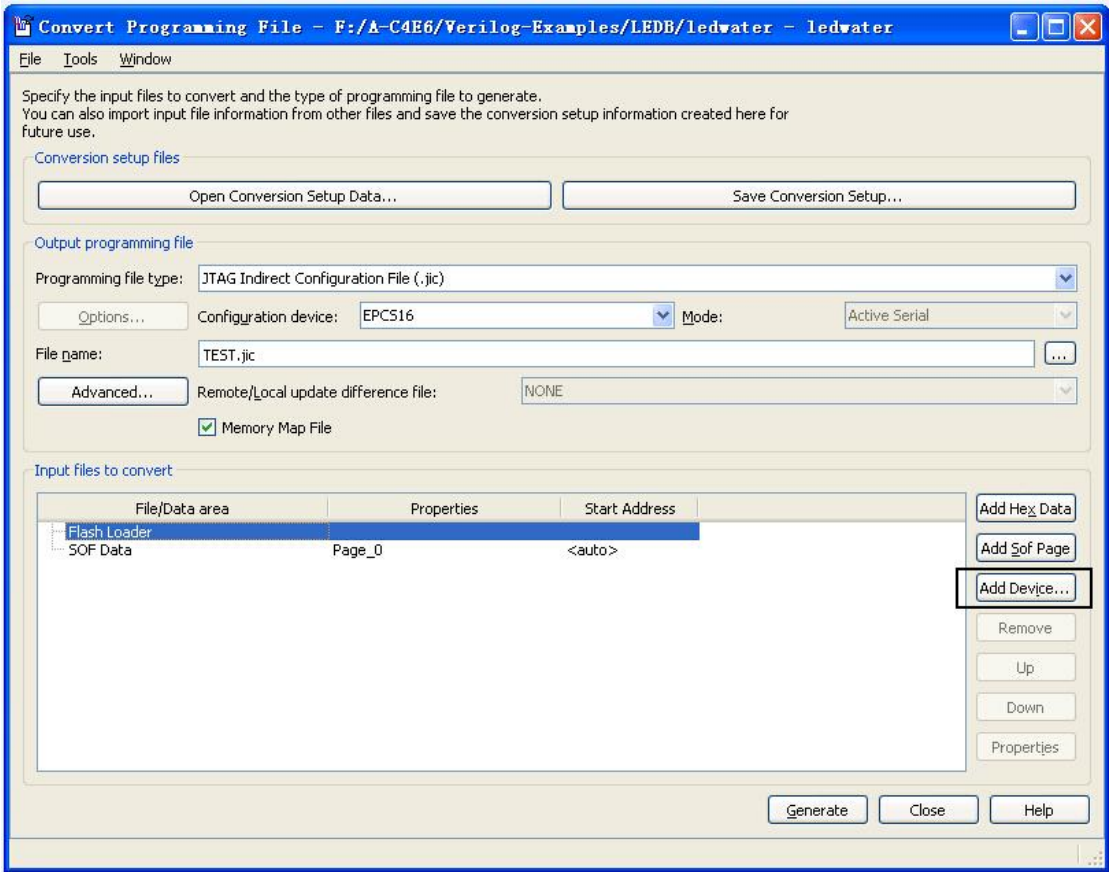


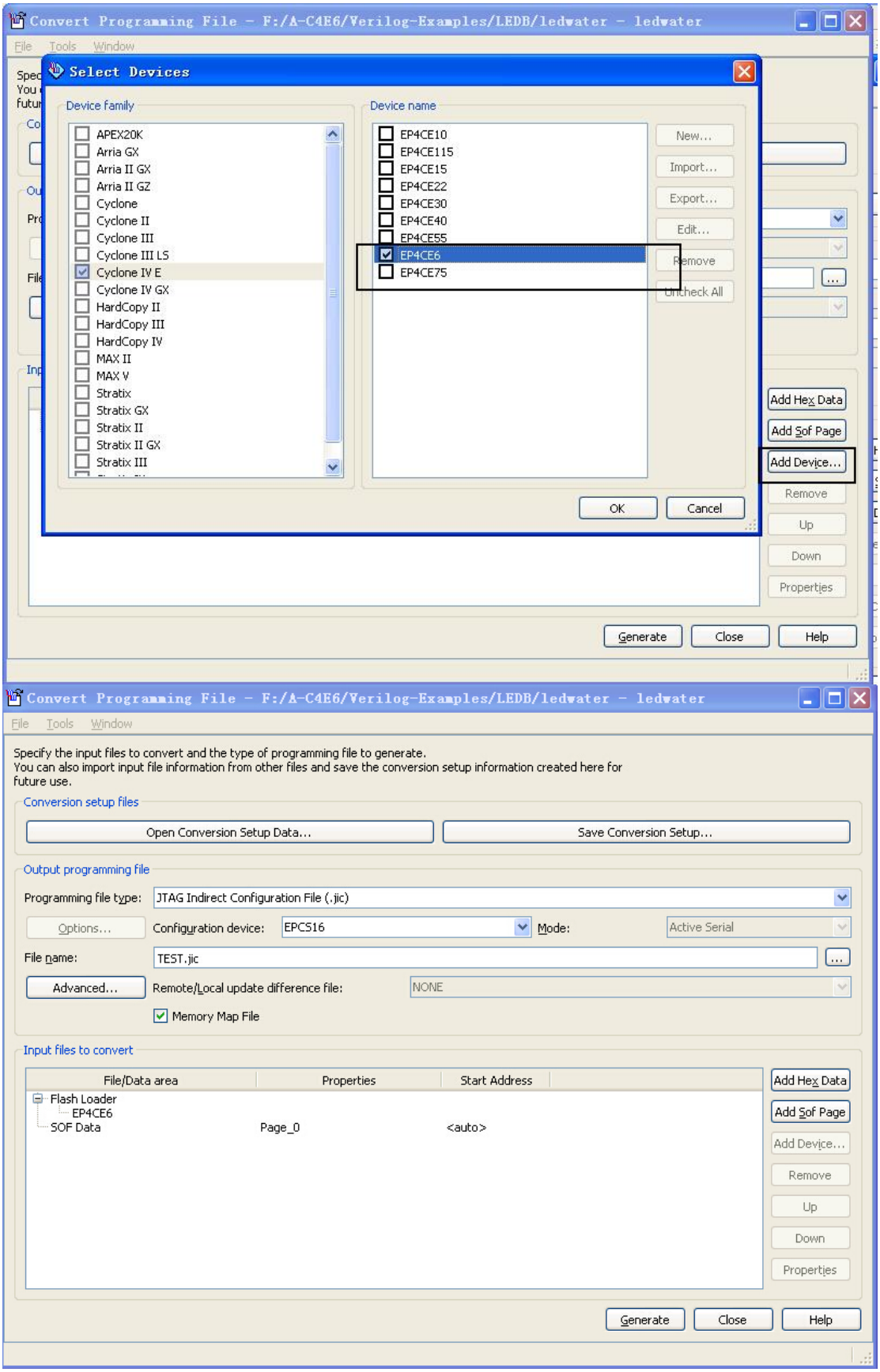

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: Programmer Object File (.pof)
Options...
Configuration device: EPC16
Mode: 1-bit Passive Serial
File name: output_file.pof
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Options 0x00010000
SOF Data Page_0 <auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

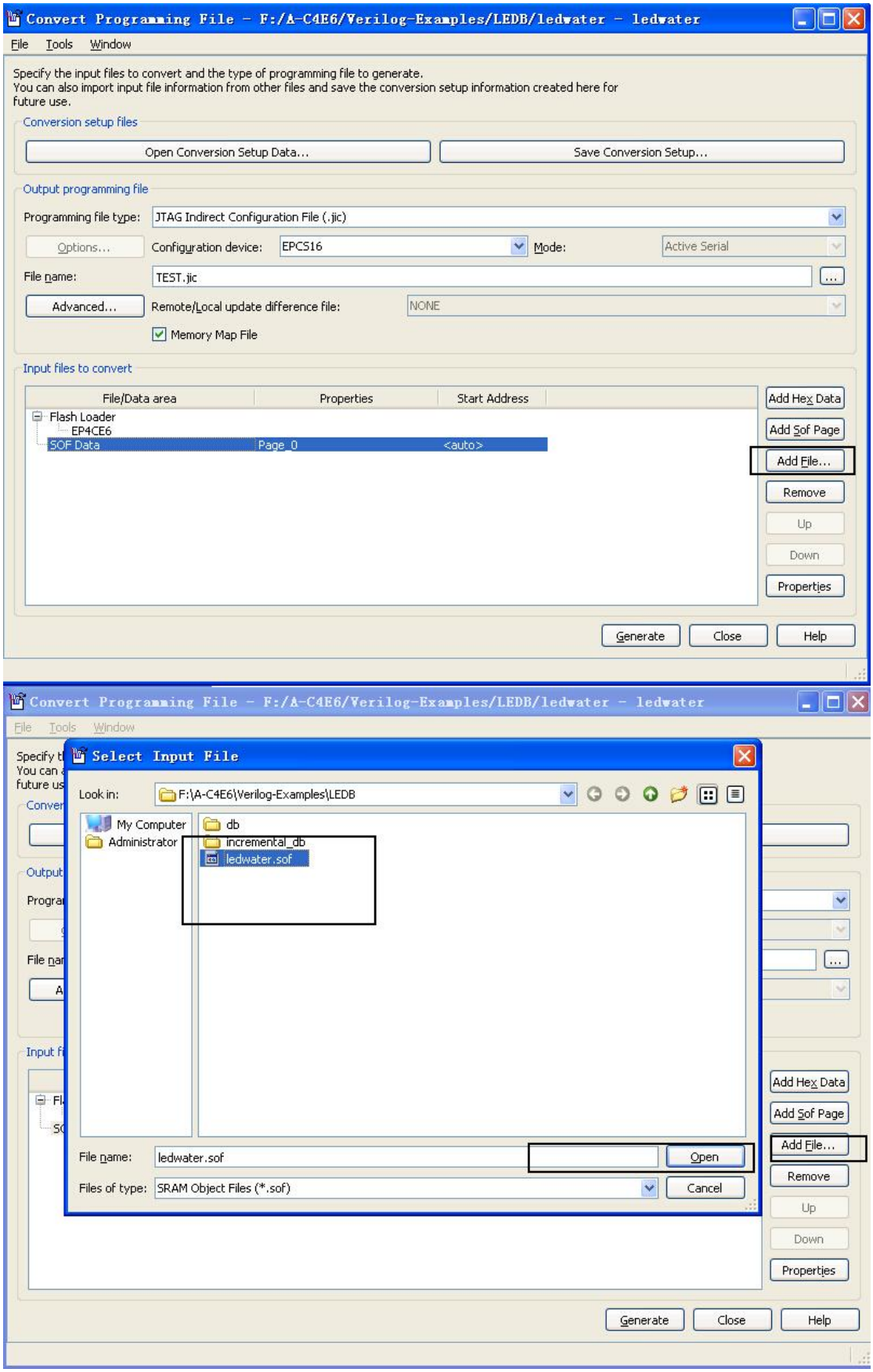

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: Programmer Object File (.pof)
Hexadecimal (Intel-Format) Output File for SRAM (.hexout)
Programmer Object File (.pof)
Raw Binary File (.rbf)
Tabular Text File (.ttf)
Hexadecimal (Intel-Format) Output File for EPC4/8/16 (.hexout)
Programmer Object File for Remote Update (.pof)
Programmer Object File for Local Update (.pof)
Raw Programming Data File (.rpd)
JTAG Indirect Configuration File (.jic)
Options...
File name:
Advanced...
Input files to convert
File/Data area
Properties
Start Address
Options 0x00010000
SOF Data Page_0 <auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

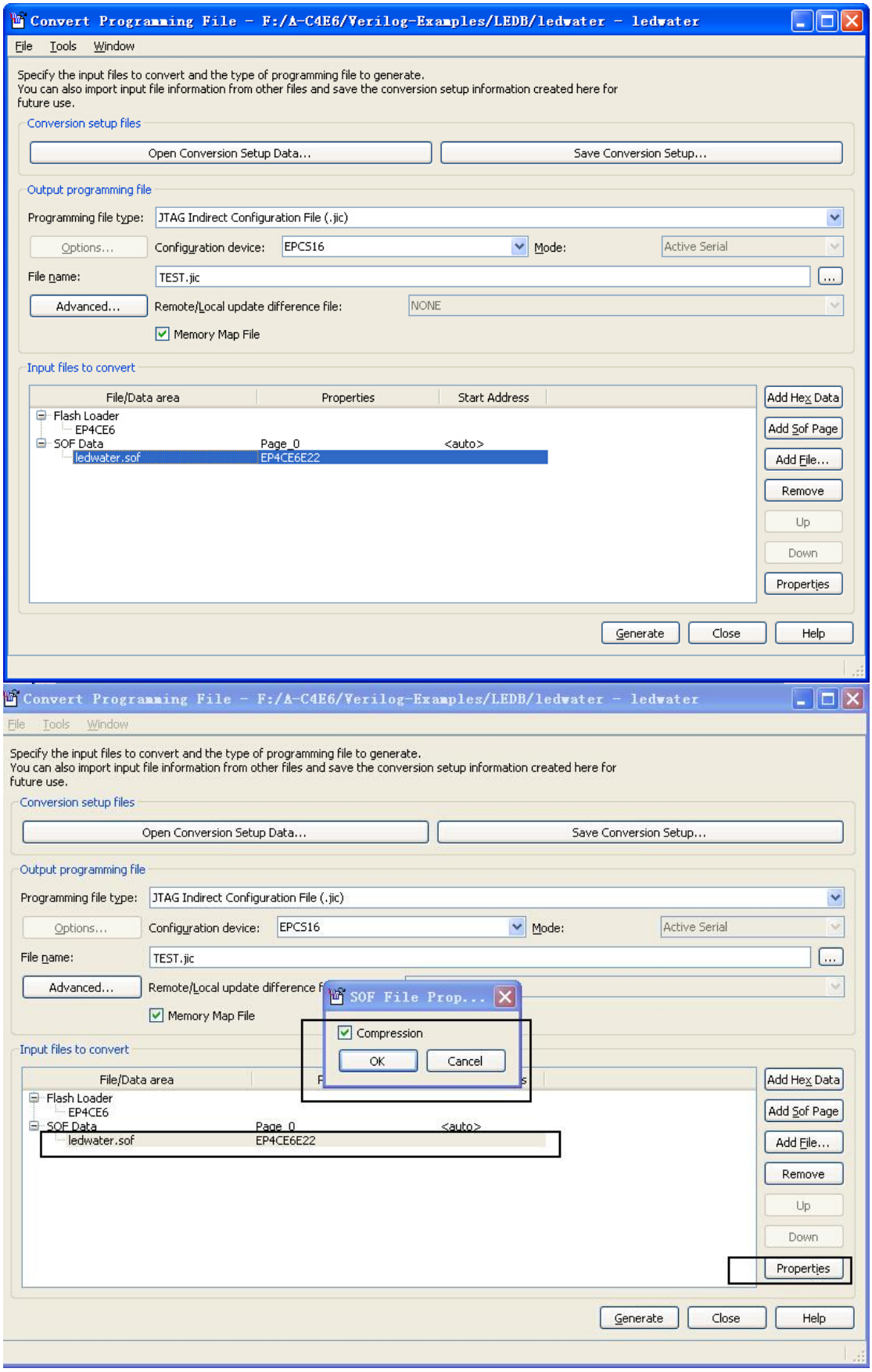

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: output_file.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help
Select Output File
Save in: F:\A-C4E6\Verilog-Examples\LEDB
My Computer
Administrator
db
incremental_db
File name: TEST
Save as type: JTAG Indirect Configuration Files (*.jic)
Save
Cancel

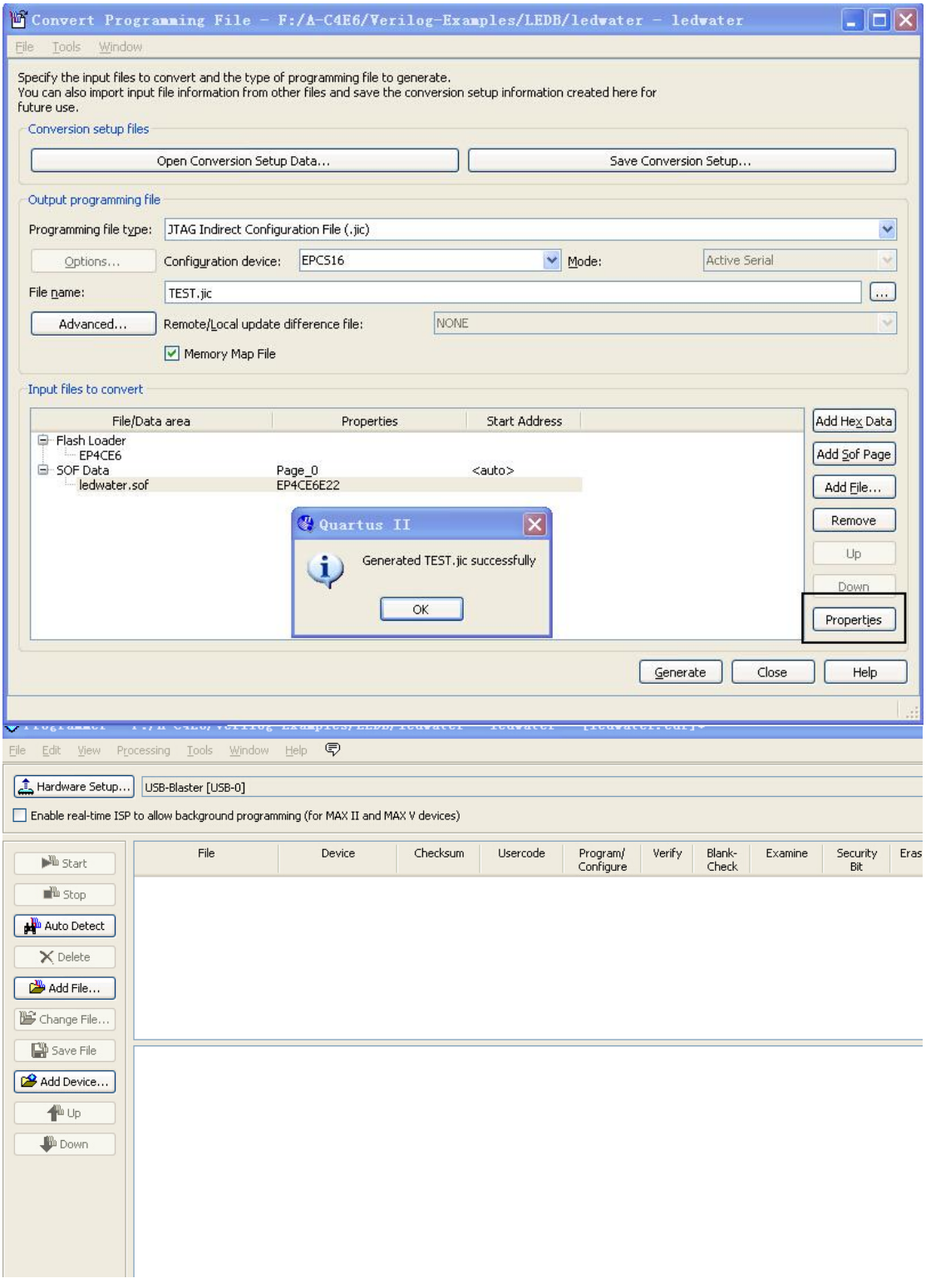

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

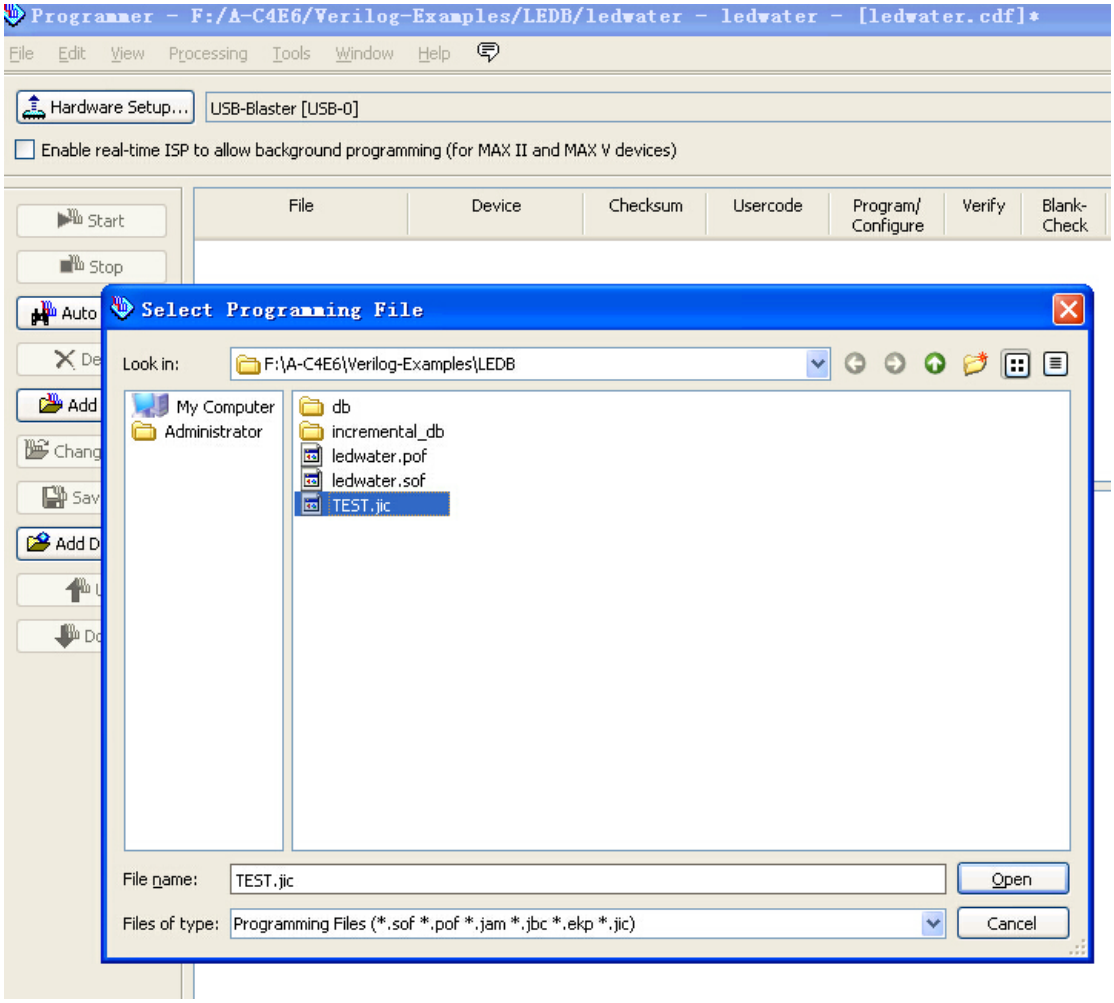

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add Device...
Remove
Up
Down
Properties
Generate
Close
Help

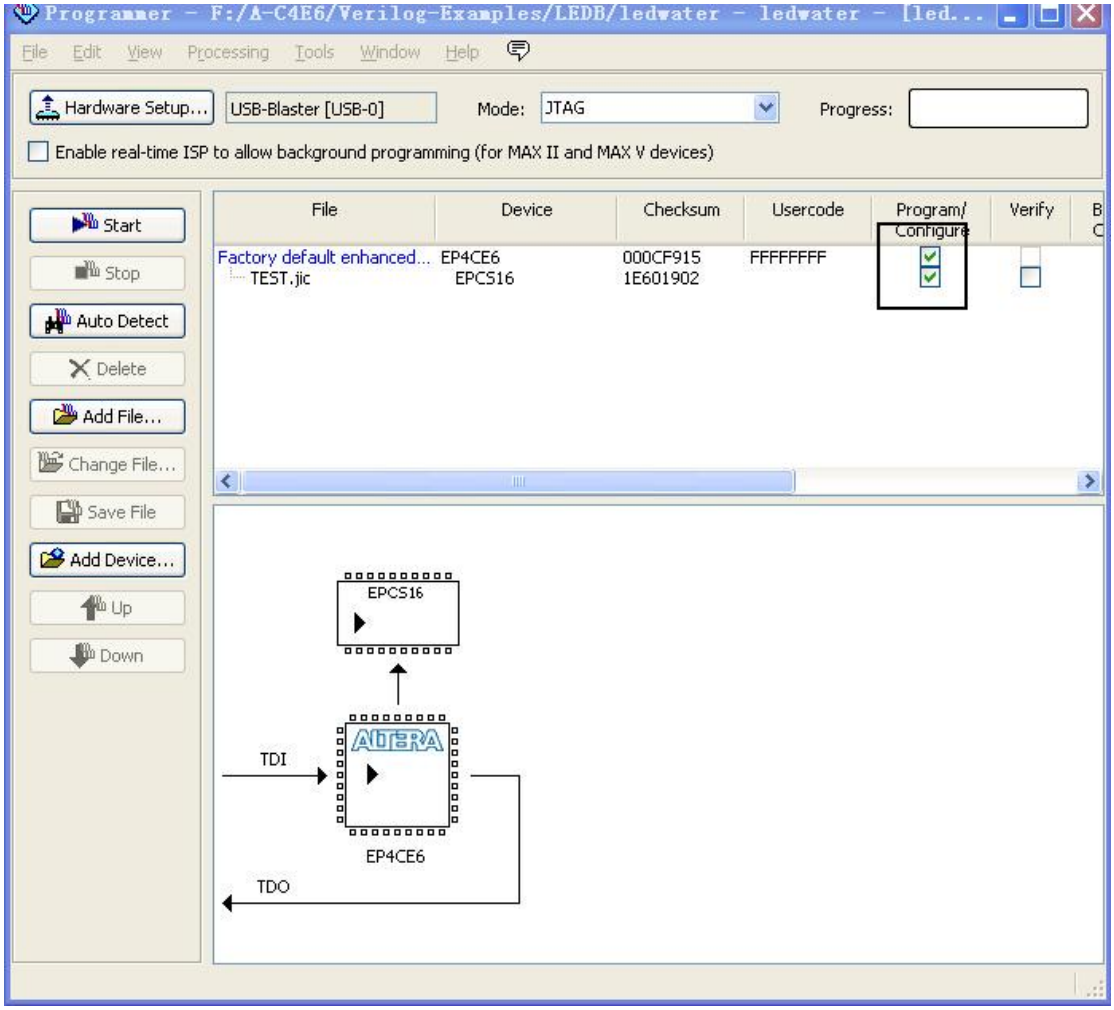

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Select Devices
Device family
APEX20K
Arria GX
Arria II GX
Arria II GZ
Cyclone
Cyclone II
Cyclone III
Cyclone III LS
Cyclone IV E
Cyclone IV GX
HardCopy II
HardCopy III
HardCopy IV
MAX II
MAX V
Stratix
Stratix GX
Stratix II
Stratix II GX
Stratix III
Device name
EP4CE10
EP4CE115
EP4CE15
EP4CE22
EP4CE30
EP4CE40
EP4CE55
EP4CE6
EP4CE75
New...
Import...
Export...
Edit...
Remove
Uncheck All
OK
Cancel
Add Hex Data
Add Sof Page
Add Device...
Remove
Up
Down
Properties
Generate
Close
Help
Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
EP4CE6
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add Device...
Remove
Up
Down
Properties
Generate
Close
Help

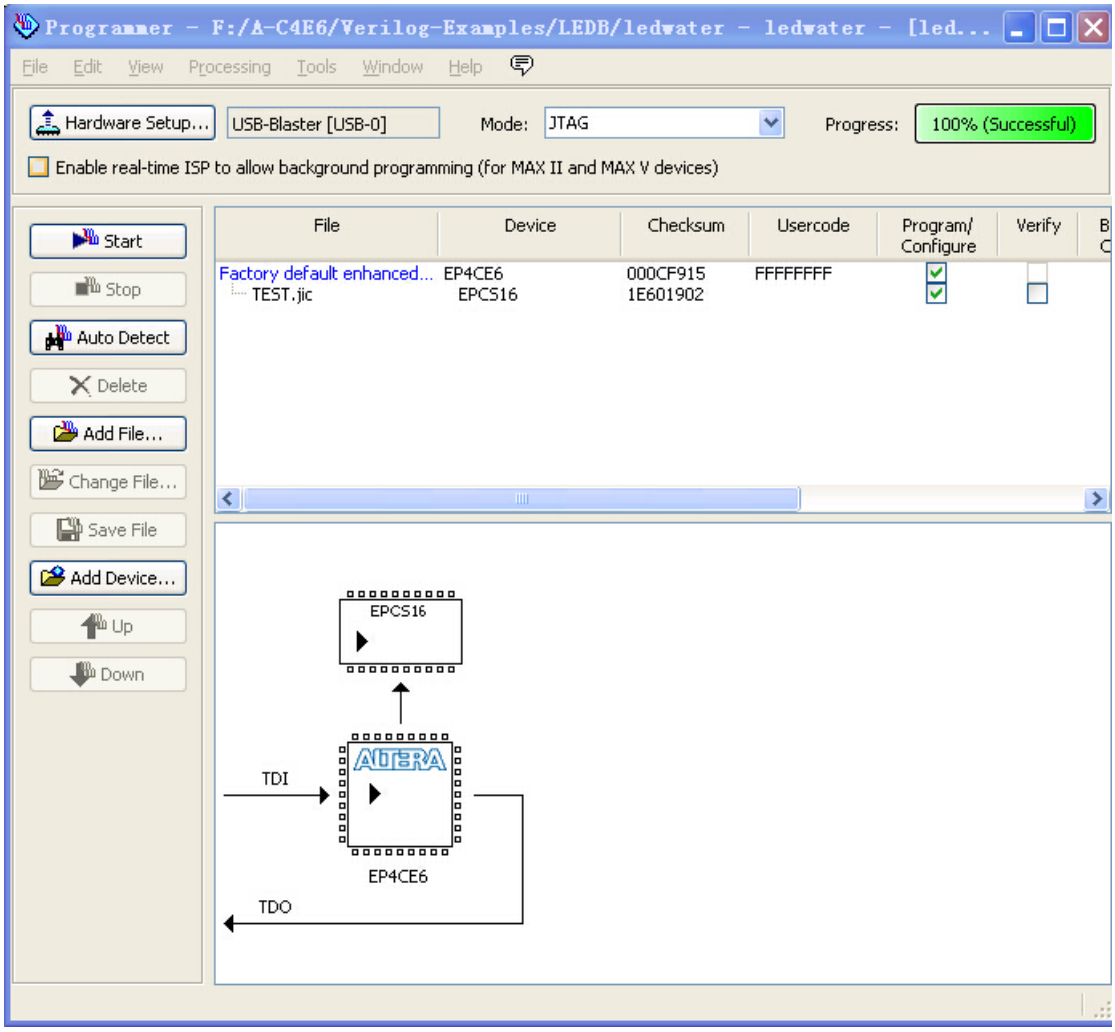

Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
EP4CE6
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help
Select Input File
Look in: F:\A-C4E6\Verilog-Examples\LEDB
My Computer
Administrator
db
incremental_db
ledwater.sof
File name: ledwater.sof
Open
Files of type: SRAM Object Files (*.sof)
Cancel


Convert Programming File - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
EP4CE6
SOF Data
Page_0
<auto>
ledwater.sof
EP4CE6E22
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help
SOF File Prop...
Compression
OK
Cancel


Convert Programming File - F:/A-C4E6/Verilog-Examples/LED8/ledwater - ledwater
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS16
Mode: Active Serial
File name: TEST.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
EP4CE6
SOF Data
Page_0
<auto>
ledwater.sof
EP4CE6E22
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Quartus II
Generated TEST.jic successfully
OK
Generate
Close
Help
File Edit View Processing Tools Window Help
Hardware Setup...
USB-Blaster [USB-0]
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit


Programmer - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater - [ledwater.cdf]*
File Edit View Processing Tools Window Help
Hardware Setup...
USB-Blaster [USB-0]
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto
Add
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Select Programming File
Look in:
F:\A-C4E6\Verilog-Examples\LEDB
My Computer
Administrator
db
incremental_db
ledwater.pof
ledwater.sof
TEST.jic
File name:
TEST.jic
Open
Files of type:
Programming Files (*.sof *.pof *.jam *.jbc *.ekp *.jic)
Cancel


Programmer - F:/A-C4E6/Verilog-Examples/LEDB/ledwater - ledwater - [led...
File Edit View Processing Tools Window Help
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Factory default enhanced...
EP4CE6
000CF915
FFFFFFFF
TEST.jic
EPCS16
1E601902
EPCS16
TDI
EP4CE6
TDO



You can power off and power on . Or press K1 REconfiger FPGA. . Will be ok .