Key detection experiment in Vivado

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1 Document Introduction

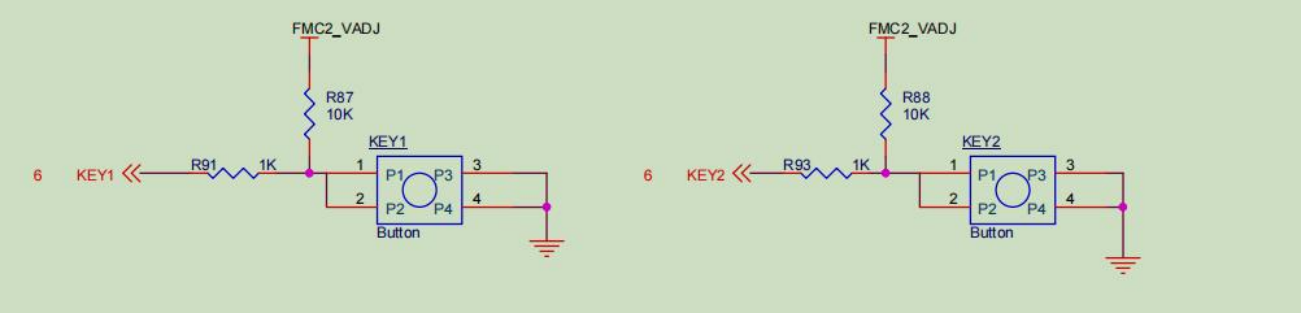
Through the button detection experiment, check whether the key function of the development board is normal, understand the specific relationship between the hardware description language and the FPGA, and learn the use of Vivado RTL ANALYSIS.

2 Experiment Environment

- Windows 7 SPI 64 bit
- Vivado (vivado2017.4)
- ALINX Brand FPGA Development Board (AXKU040 FPGA Development Board)

3 Experiment Principle

3.1 Key HardwareCircuit

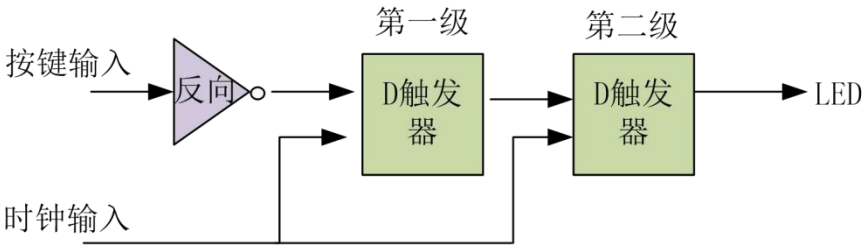


Keys Hardware Circuit on AXKU040 FPGA Development Board

As can be seen from the circuit, the key of the circuit is high when it is released, and low when it is pressed.

3.2 Programming

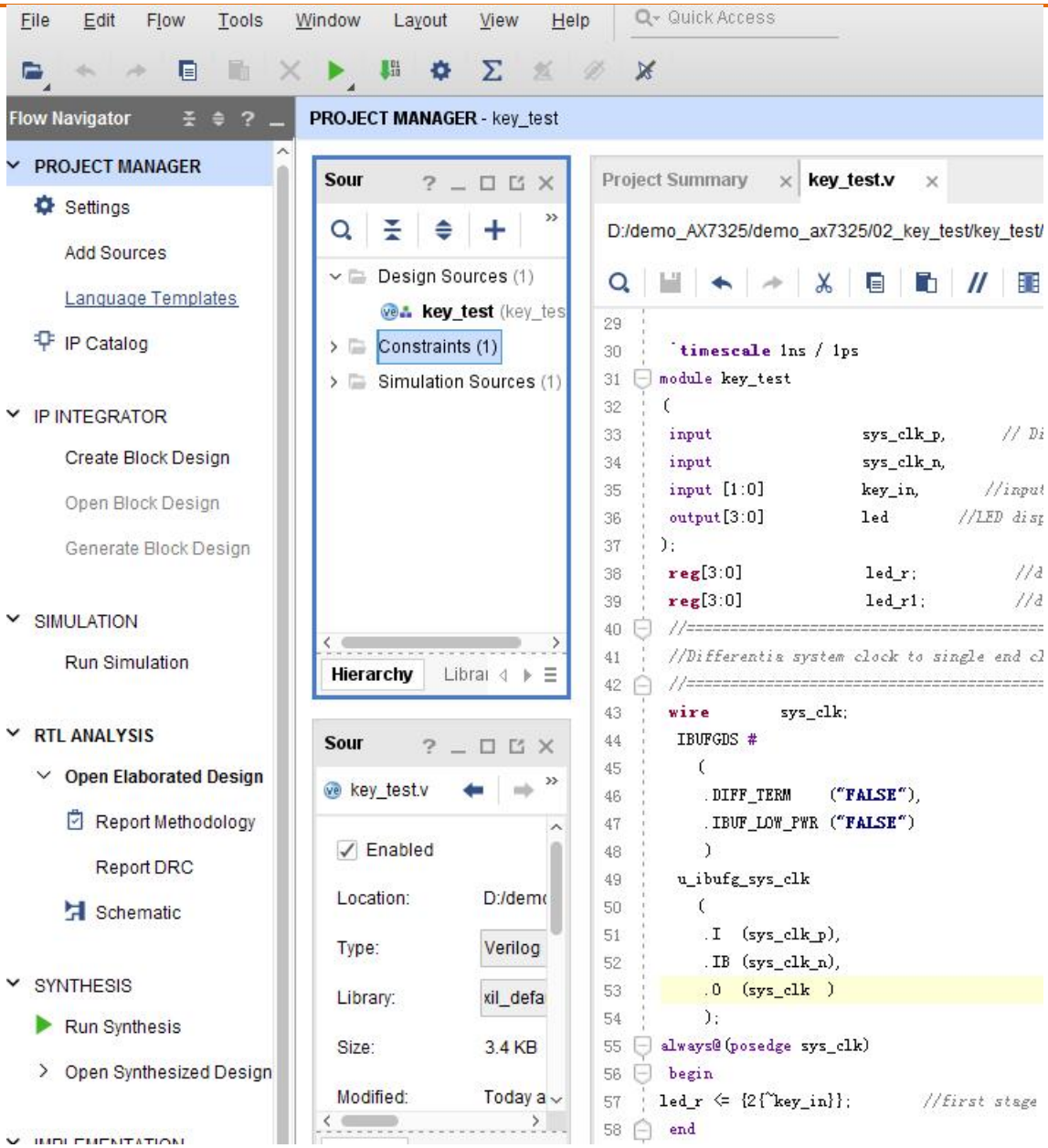
The program looks at the connection between the hardware description language and the FPGA hardware through a simple hardware description language. First, we pass the key input through a non-gate and then pass through two sets of D flip-flops. The signal that passes through the D flip-flop is latched on the rising edge of the D flip-flop clock input and then sent to the output.



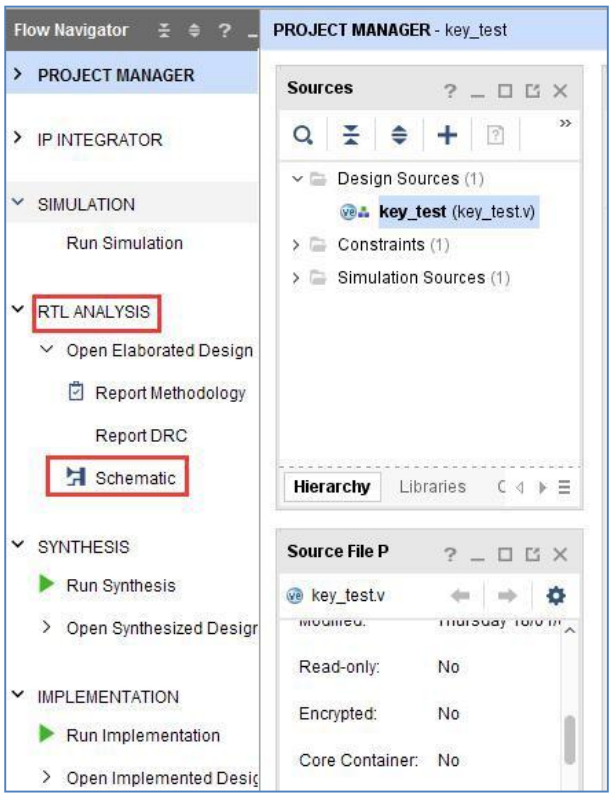
Before the hardware description language coding, we have completed the hardware construction, which is a normal development process. With hardware design ideas, whether through drawing or Verilog HDL, VHDL can complete the design, according to the design of complex programs and familiar procedures for a language to select tools.

4 Project Analysis

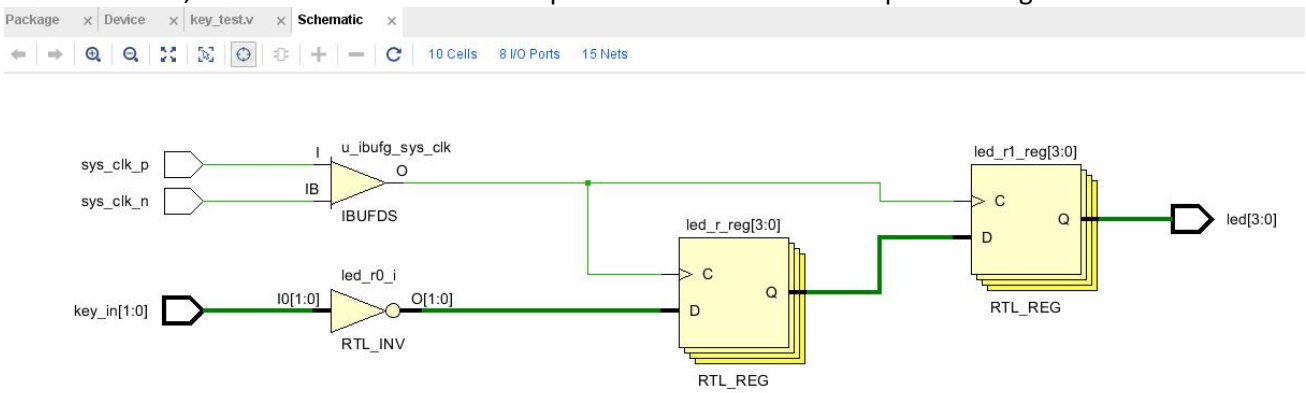
(1) First, Create the test project of the key, add the verilog testing code, and complete the process of compiling and assigning pins



(2) We can view the design using the “RTL ANALYSIS” tool



(3) By analyzing the RTL graph, it can be seen that the first-stage D flip-flop is input after being inverted, and the second-level direct input is consistent with the expected design.



5 Experimental result

After the Bit program is downloaded to the development board, the AXKU040 FPGA development board,"LED1", "LED2", "LED3", "LED4" are all OFF.

Press “KEY1”, Then “LED1” and “LED3” are all on, “LED2” and “LED4” are all off.

Press “KEY2”, Then “LED2” and “LED4” are all on, “LED1” and “LED3” are all off.

6 Appendix

key_test.v(verilog Code)

```
`timescale 1ns / 1ps
module key_test
(
 input                   sys_clk_p,        // Differentia system clock 200Mhz input on board
 input                   sys_clk_n,
 input [1:0]             key_in,          //input four key signal,when the keydown,the value is 0
 output[3:0]             led              //LED display ,when the siganl high,LED lighten
);
 reg[3:0]                led_r;             //define the first stage register , generate four
D Flip-flop
 reg[3:0]                led_r1;            //define the second stage register ,generate four
D Flip-flop
 //=============================================================================
 //Differentia system clock to single end clock
 //=============================================================================
 wire         sys_clk;
  IBUFGDS #
    (
     .DIFF_TERM    ("FALSE"),
     .IBUF_LOW_PWR ("FALSE")
     )
  u_ibufg_sys_clk
    (
     .I  (sys_clk_p),
     .IB (sys_clk_n),
     .O  (sys_clk  )
     );
always@(posedge sys_clk)
 begin
led_r <= {2{~key_in}};          //first stage latched data
 end

always@(posedge sys_clk)
begin
led_r1 <= led_r;        //second stage latched data
end

 assign led = led_r1;
endmodule
```