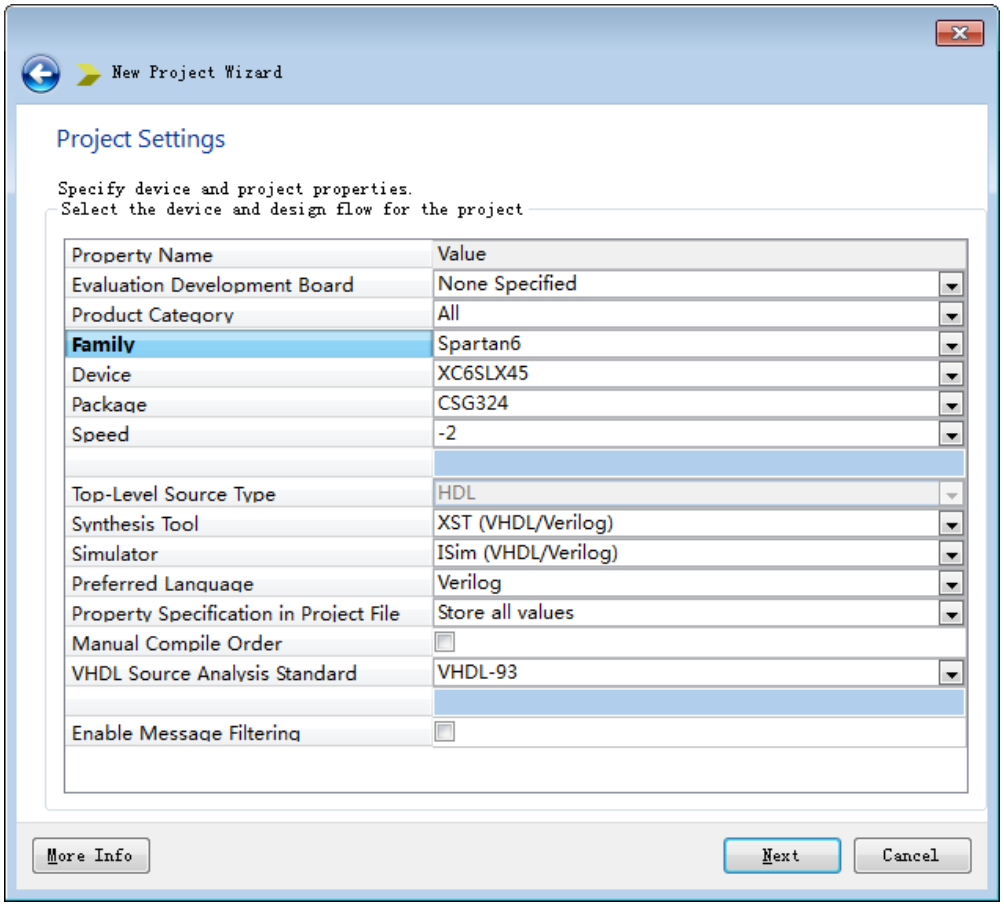
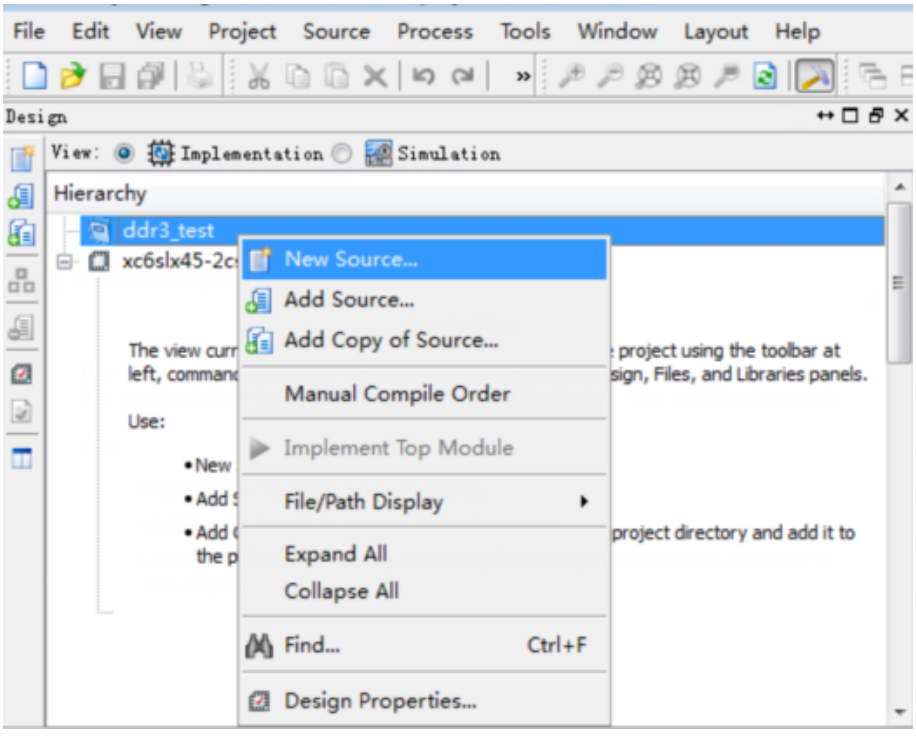
Debug DDR3
in Xilinx Environment

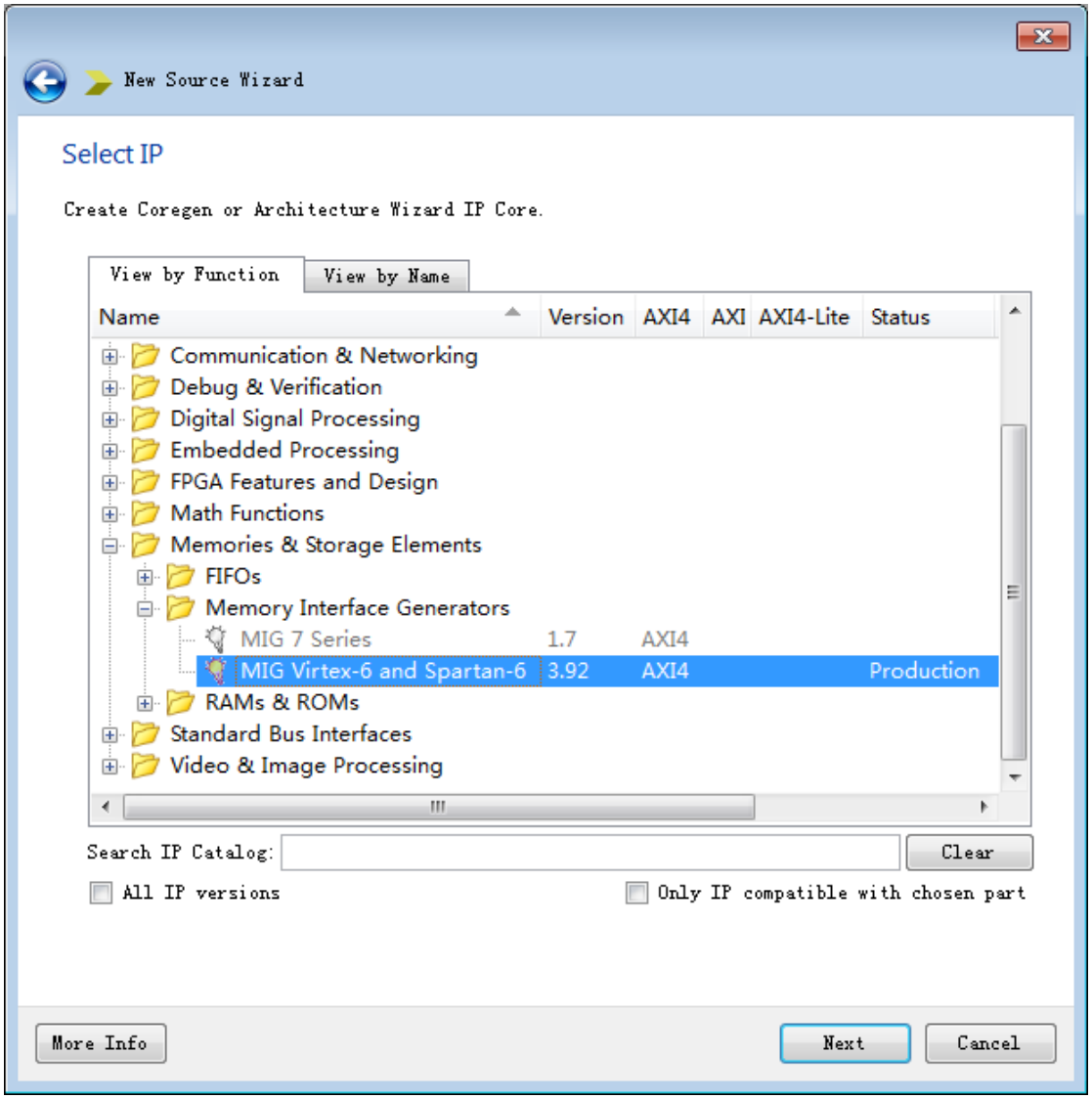
ALINX

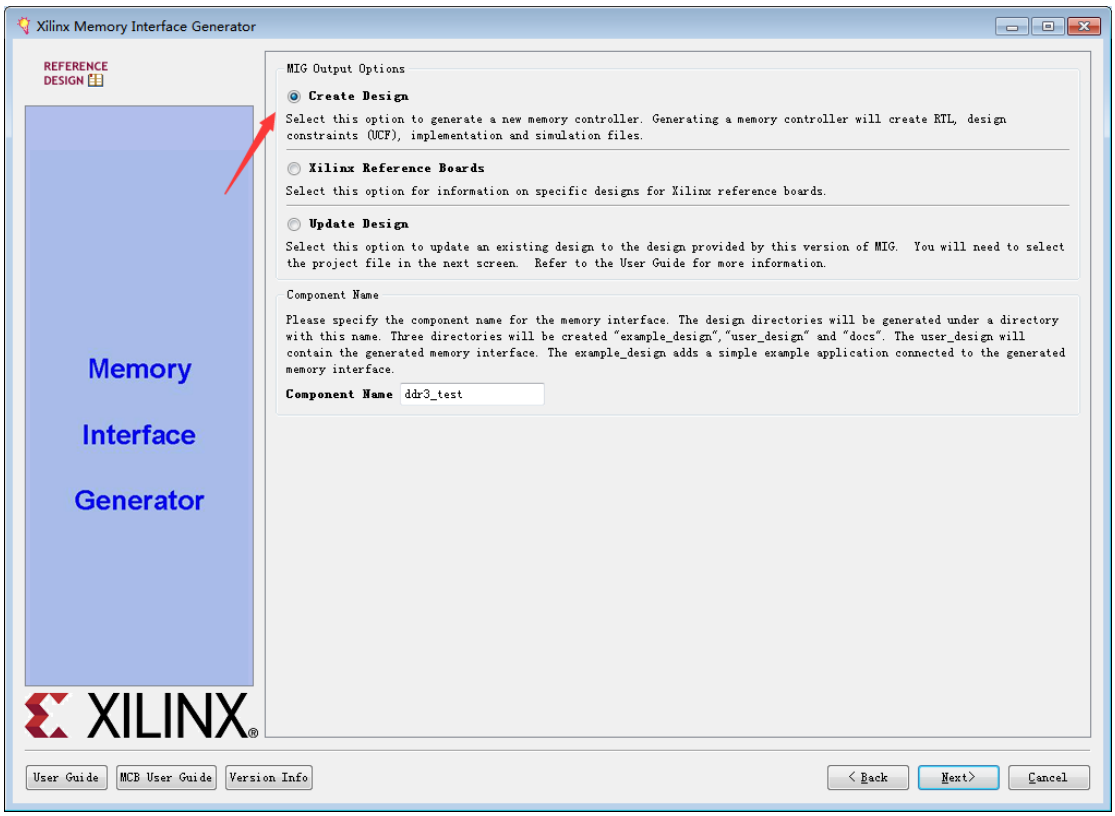
new_project


New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Spartan6
Device
XC6SLX45
Package
CSG324
Speed
-2
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
Next
Cancel


File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
ddr3_test
xc6slx45-2c
New Source...
Add Source...
Add Copy of Source...
Manual Compile Order
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
project using the toolbar at
sign, Files, and Libraries panels.
project directory and add it to

Add IPcore


New Source Wizard
Select IP
Create Coregen or Architecture Wizard IP Core.
View by Function
View by Name
Name
Version
AXI4
AXI
AXI4-Lite
Status
Communication & Networking
Debug & Verification
Digital Signal Processing
Embedded Processing
FPGA Features and Design
Math Functions
Memories & Storage Elements
FIFOs
Memory Interface Generators
MIG 7 Series
1.7
AXI4
MIG Virtex-6 and Spartan-6
3.92
AXI4
Production
RAMs & ROMs
Standard Bus Interfaces
Video & Image Processing
Search IP Catalog:
Clear
All IP versions
Only IP compatible with chosen part
More Info
Next
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory
Interface
Generator
XILINX
MIG Output Options
Create Design
Select this option to generate a new memory controller. Generating a memory controller will create RTL, design constraints (UCF), implementation and simulation files.
Xilinx Reference Boards
Select this option for information on specific designs for Xilinx reference boards.
Update Design
Select this option to update an existing design to the design provided by this version of MIG. You will need to select the project file in the next screen. Refer to the User Guide for more information.
Component Name
Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.
Component Name ddr3_test
User Guide
MCB User Guide
Version Info
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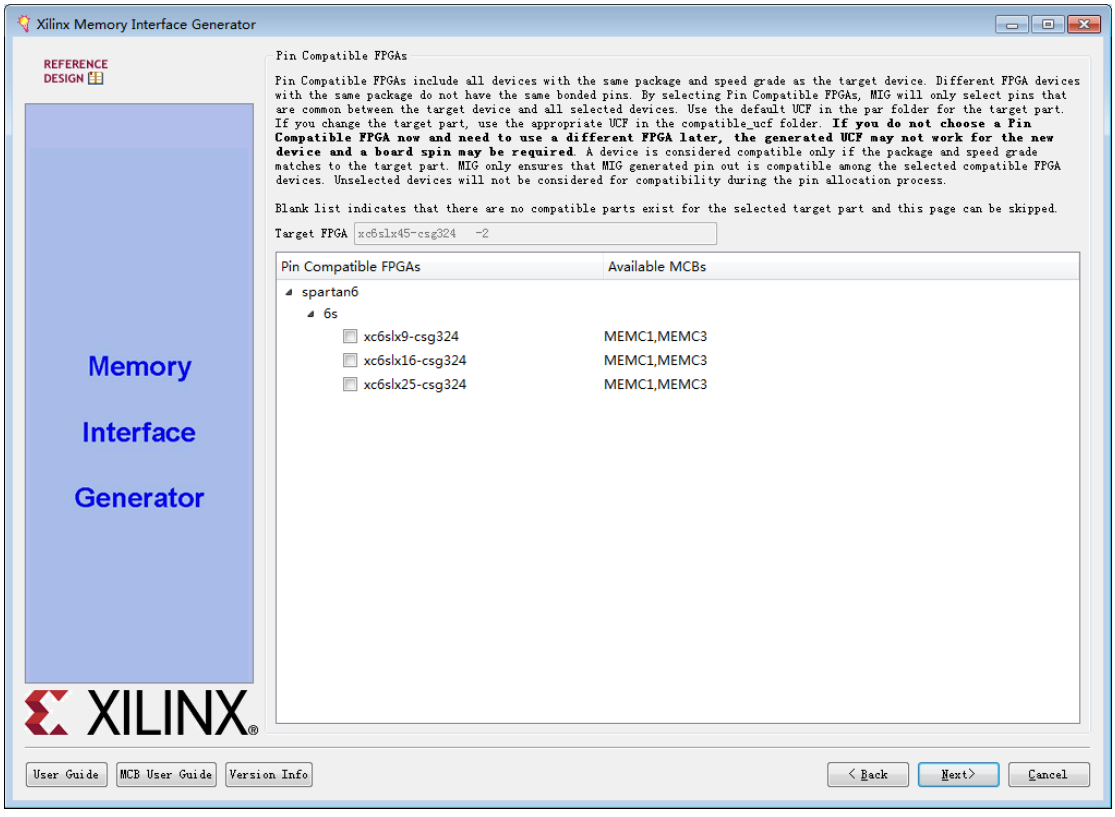
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory
Interface
Generator
XILINX
Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If you change the target part, use the appropriate UCF in the compatible_ucf folder. If you do not choose a Pin Compatible FPGA now and need to use a different FPGA later, the generated UCF may not work for the new device and a board spin may be required. A device is considered compatible only if the package and speed grade matches to the target part. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
Blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Target FPGA xc6slx45-csg324 -2
Pin Compatible FPGAs
Available MCBs
spartan6
6s
xc6slx9-csg324
MEMC1,MEMC3
xc6slx16-csg324
MEMC1,MEMC3
xc6slx25-csg324
MEMC1,MEMC3
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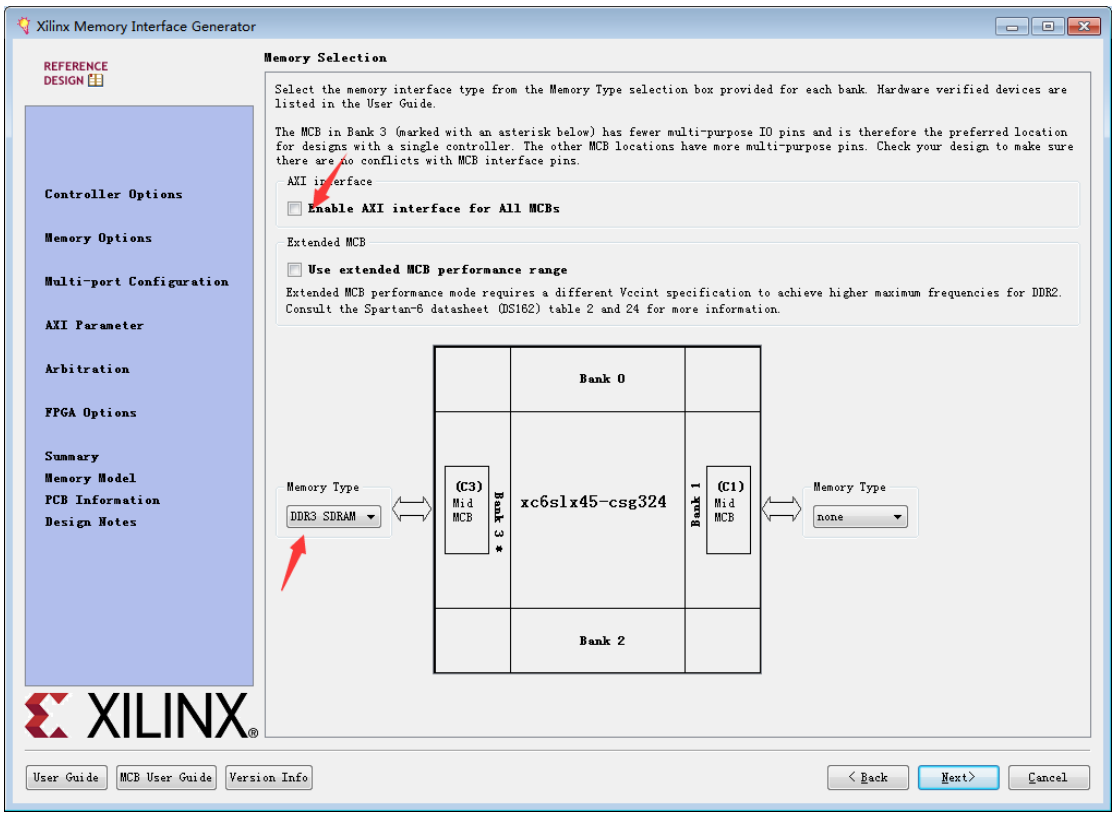
Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory Selection
Select the memory interface type from the Memory Type selection box provided for each bank. Hardware verified devices are listed in the User Guide.
The MCB in Bank 3 (marked with an asterisk below) has fewer multi-purpose IO pins and is therefore the preferred location for designs with a single controller. The other MCB locations have more multi-purpose pins. Check your design to make sure there are no conflicts with MCB interface pins.
AXI interface
Enable AXI interface for All MCBs
Extended MCB
Use extended MCB performance range
Extended MCB performance mode requires a different Vccint specification to achieve higher maximum frequencies for DDR2. Consult the Spartan-6 datasheet (DS162) table 2 and 24 for more information.
Controller Options
Memory Options
Multi-port Configuration
AXI Parameter
Arbitration
FPGA Options
Summary
Memory Model
PCB Information
Design Notes
Bank 0
Bank 1
Bank 2
Bank 3 *
(C3) Mid MCB
(C1) Mid MCB
xc6slx45-csg324
Memory Type
DDR3 SDRAM
Memory Type
none
XILINX
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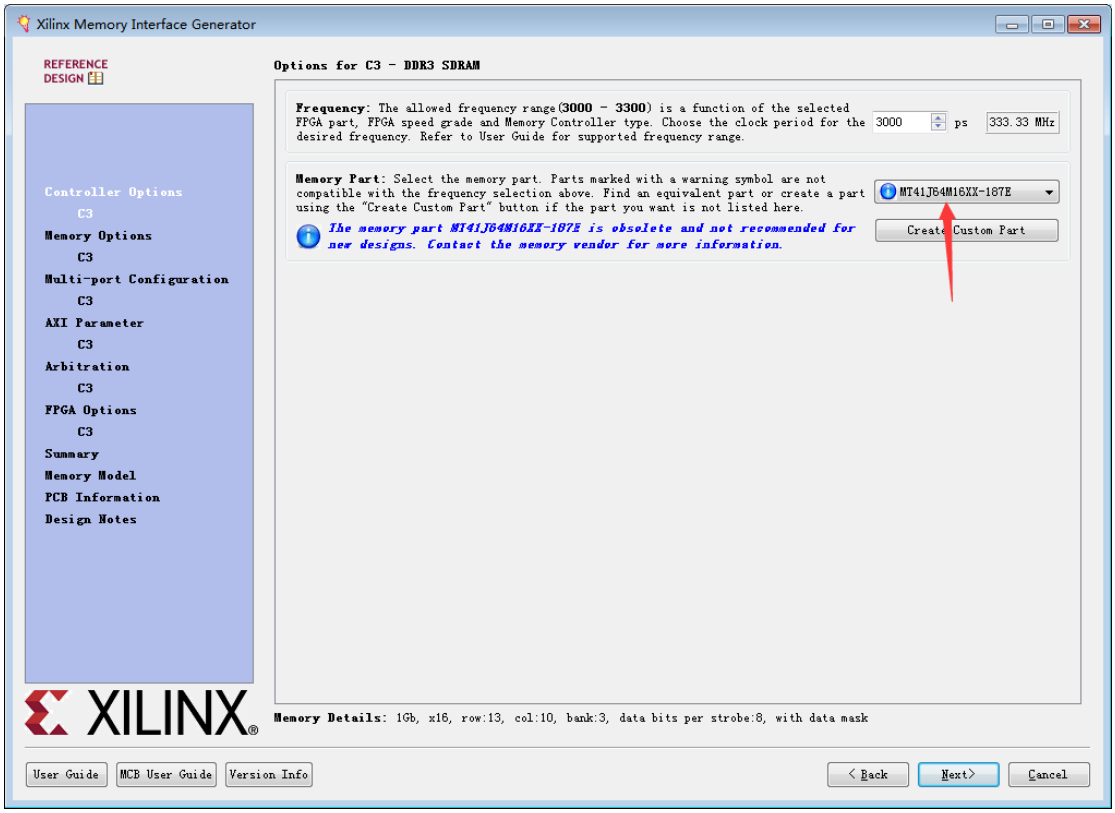
Xilinx Memory Interface Generator
REFERENCE DESIGN
Options for C3 - DDR3 SDRAM
Frequency: The allowed frequency range (3000 - 3300) is a function of the selected FPGA part, FPGA speed grade and Memory Controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.
3000
ps
333.33 MHz
Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part you want is not listed here.
MT41J64M16XX-187E
The memory part MT41J64M16XX-187E is obsolete and not recommended for new designs. Contact the memory vendor for more information.
Create Custom Part
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
Memory Details: 1Gb, x16, row:13, col:10, bank:3, data bits per strobe:8, with data mask
XILINX
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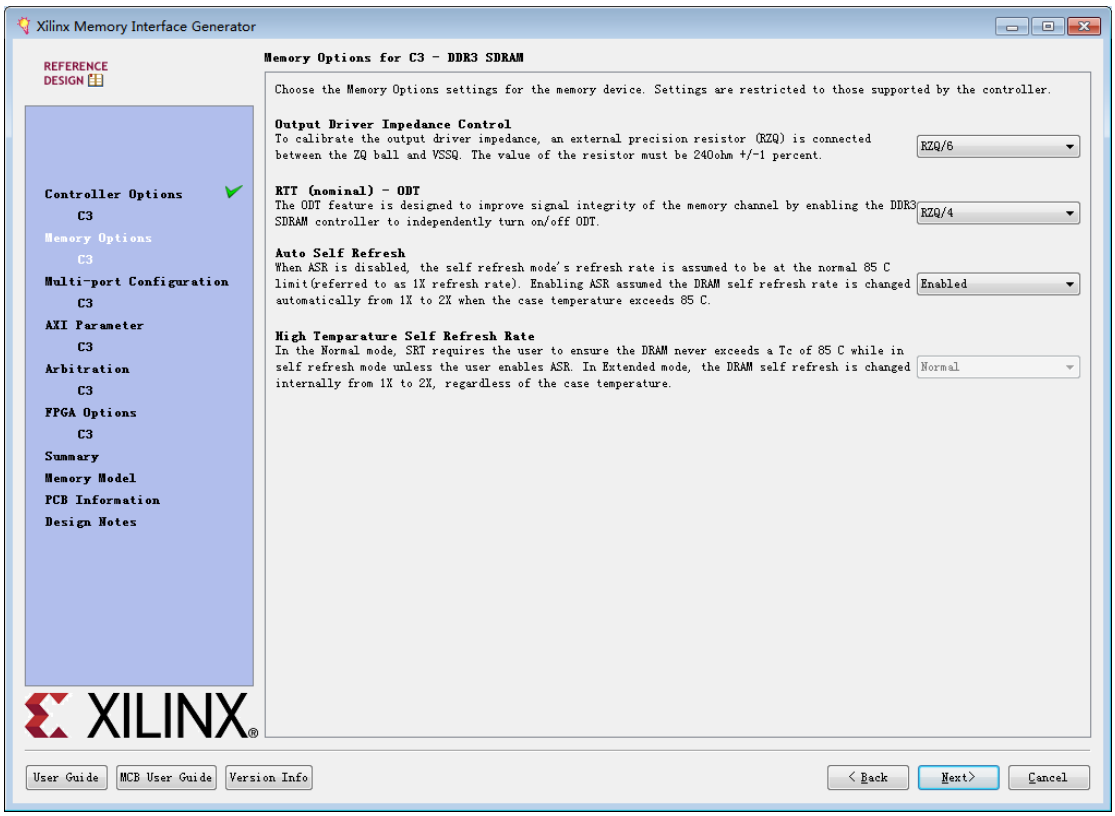
Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory Options for C3 - DDR3 SDRAM
Choose the Memory Options settings for the memory device. Settings are restricted to those supported by the controller.
Output Driver Impedance Control
To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and VSSQ. The value of the resistor must be 240ohm +/-1 percent.
RZQ/6
RTT (nominal) - ODT
The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT.
RZQ/4
Auto Self Refresh
When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85 C limit(referred to as 1X refresh rate). Enabling ASR assumed the DRAM self refresh rate is changed automatically from 1X to 2X when the case temperature exceeds 85 C.
Enabled
High Temparature Self Refresh Rate
In the Normal mode, SRT requires the user to ensure the DRAM never exceeds a Tc of 85 C while in self refresh mode unless the user enables ASR. In Extended mode, the DRAM self refresh is changed internally from 1X to 2X, regardless of the case temperature.
Normal
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
XILINX
User Guide
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Version Info
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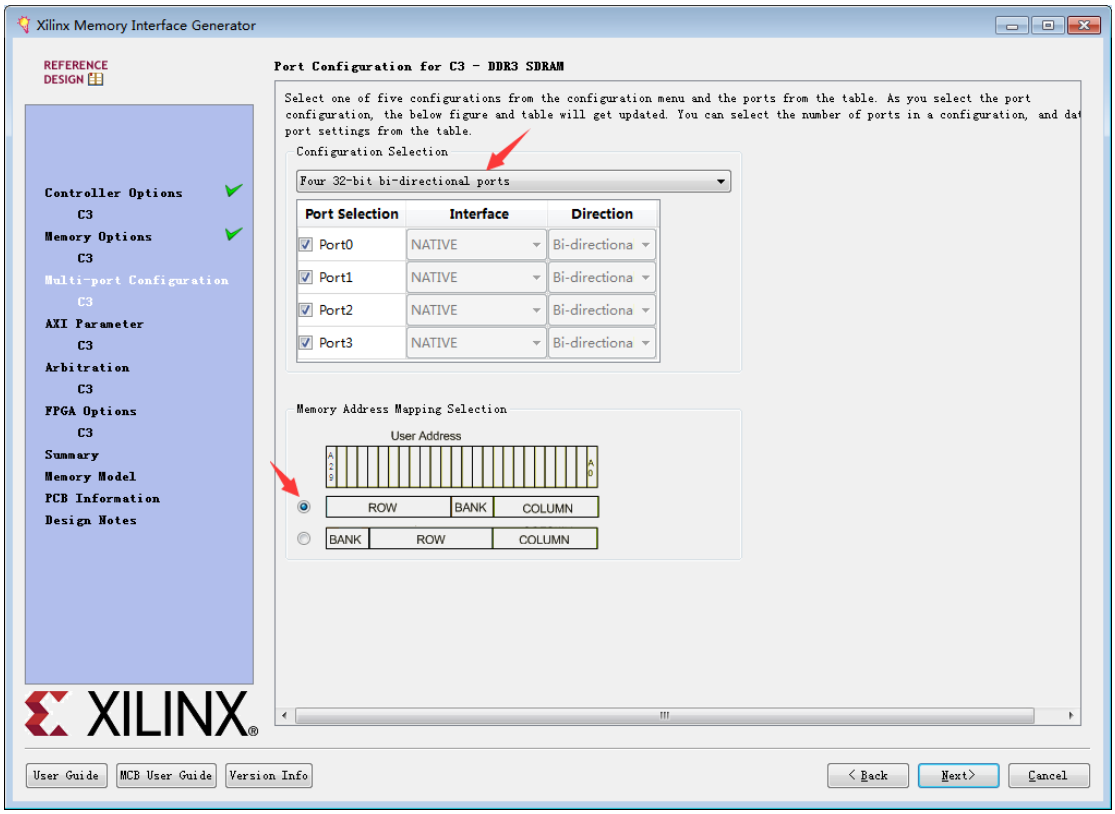
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Port Configuration for C3 - DDR3 SDRAM
Select one of five configurations from the configuration menu and the ports from the table. As you select the port configuration, the below figure and table will get updated. You can select the number of ports in a configuration, and da port settings from the table.
Configuration Selection
Four 32-bit bi-directional ports
Port Selection
Interface
Direction
Port0
Port1
Port2
Port3
NATIVE
Bi-directiona
Memory Address Mapping Selection
User Address
ROW
BANK
COLUMN
BANK
ROW
COLUMN
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
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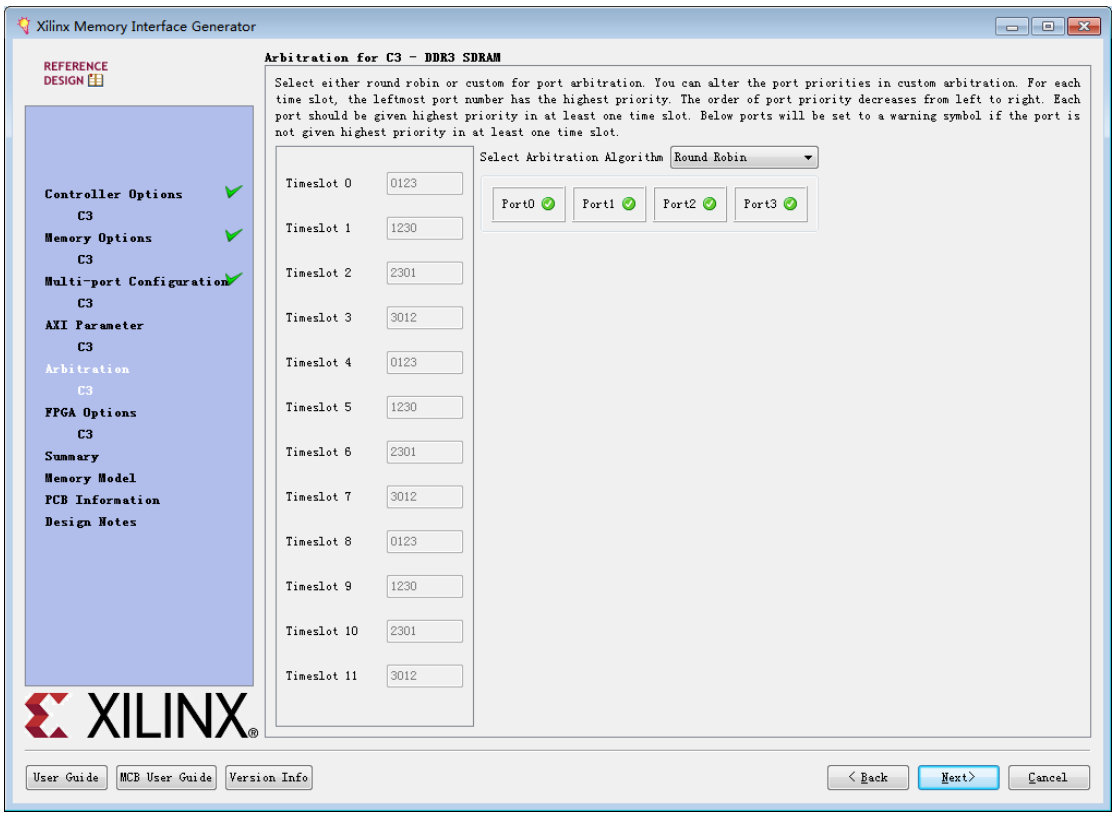
Xilinx Memory Interface Generator
REFERENCE DESIGN
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
Arbitration for C3 - DDR3 SDRAM
Select either round robin or custom for port arbitration. You can alter the port priorities in custom arbitration. For each time slot, the leftmost port number has the highest priority. The order of port priority decreases from left to right. Each port should be given highest priority in at least one time slot. Below ports will be set to a warning symbol if the port is not given highest priority in at least one time slot.
Select Arbitration Algorithm
Round Robin
Timeslot 0 0123
Timeslot 1 1230
Timeslot 2 2301
Timeslot 3 3012
Timeslot 4 0123
Timeslot 5 1230
Timeslot 6 2301
Timeslot 7 3012
Timeslot 8 0123
Timeslot 9 1230
Timeslot 10 2301
Timeslot 11 3012
Port0
Port1
Port2
Port3
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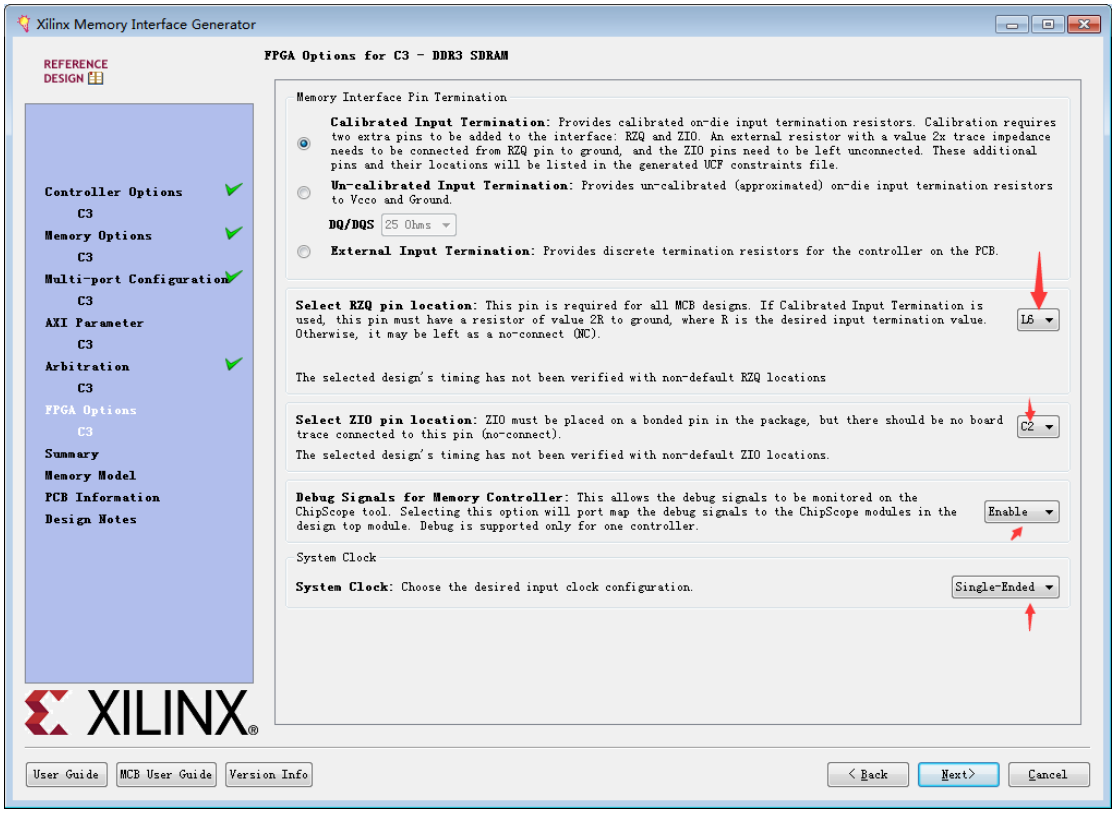
Cancel


Xilinx Memory Interface Generator
REFERENCE DESIGN
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
FPGA Options for C3 - DDR3 SDRAM
Memory Interface Pin Termination
Calibrated Input Termination: Provides calibrated on-die input termination resistors. Calibration requires two extra pins to be added to the interface: RZQ and ZIO. An external resistor with a value 2x trace impedance needs to be connected from RZQ pin to ground, and the ZIO pins need to be left unconnected. These additional pins and their locations will be listed in the generated UCF constraints file.
Un-calibrated Input Termination: Provides un-calibrated (approximated) on-die input termination resistors to Vcco and Ground.
DQ/DQS 25 Ohms
External Input Termination: Provides discrete termination resistors for the controller on the PCB.
Select RZQ pin location: This pin is required for all MCB designs. If Calibrated Input Termination is used, this pin must have a resistor of value 2R to ground, where R is the desired input termination value. Otherwise, it may be left as a no-connect (NC).
L6
The selected design's timing has not been verified with non-default RZQ locations
Select ZIO pin location: ZIO must be placed on a bonded pin in the package, but there should be no board trace connected to this pin (no-connect).
C2
The selected design's timing has not been verified with non-default ZIO locations.
Debug Signals for Memory Controller: This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. Debug is supported only for one controller.
Enable
System Clock
System Clock: Choose the desired input clock configuration.
Single-Ended
XILINX
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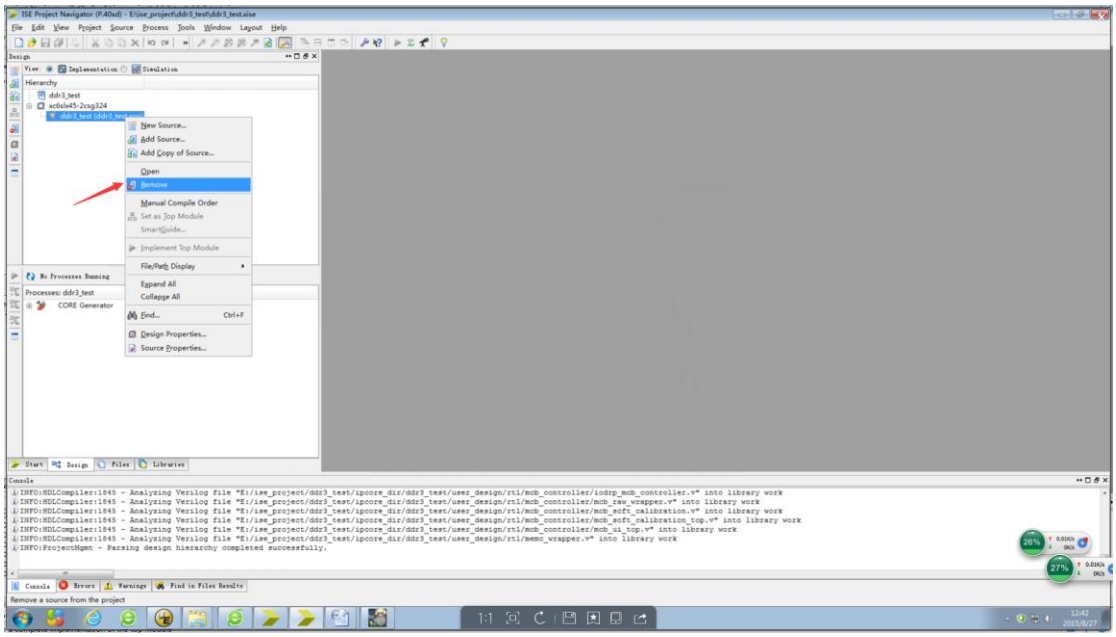
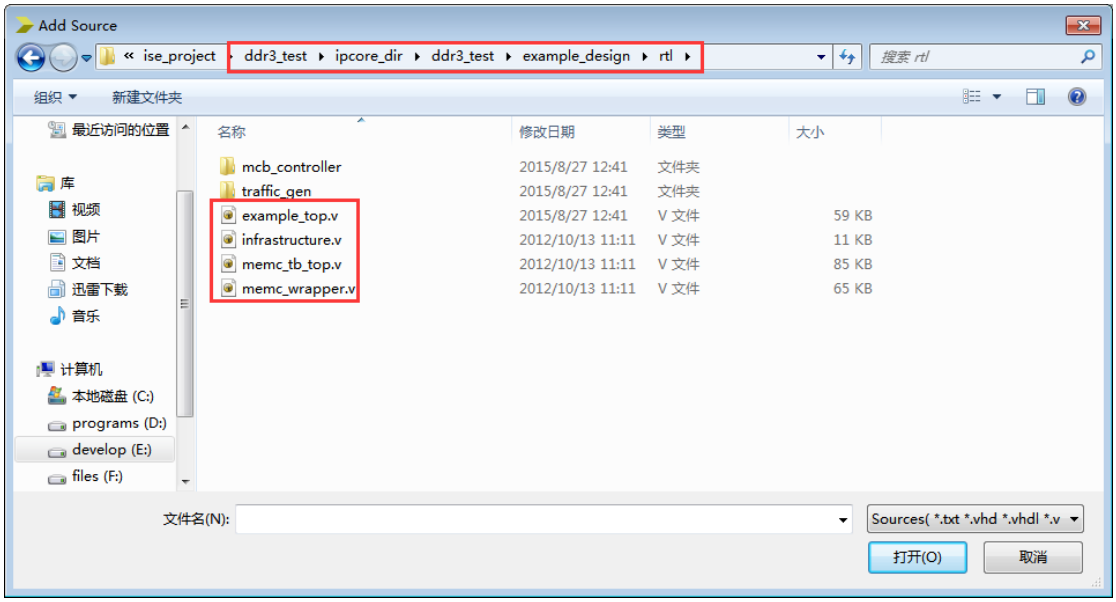
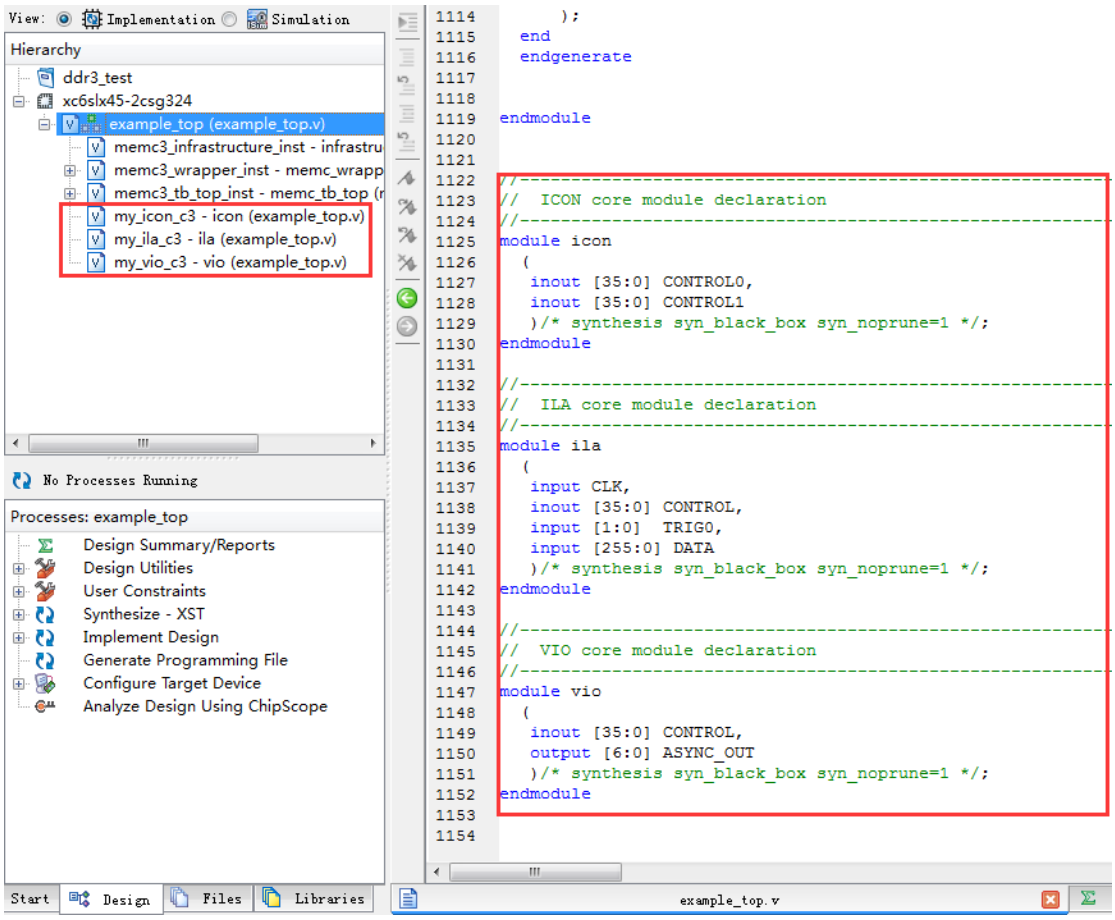
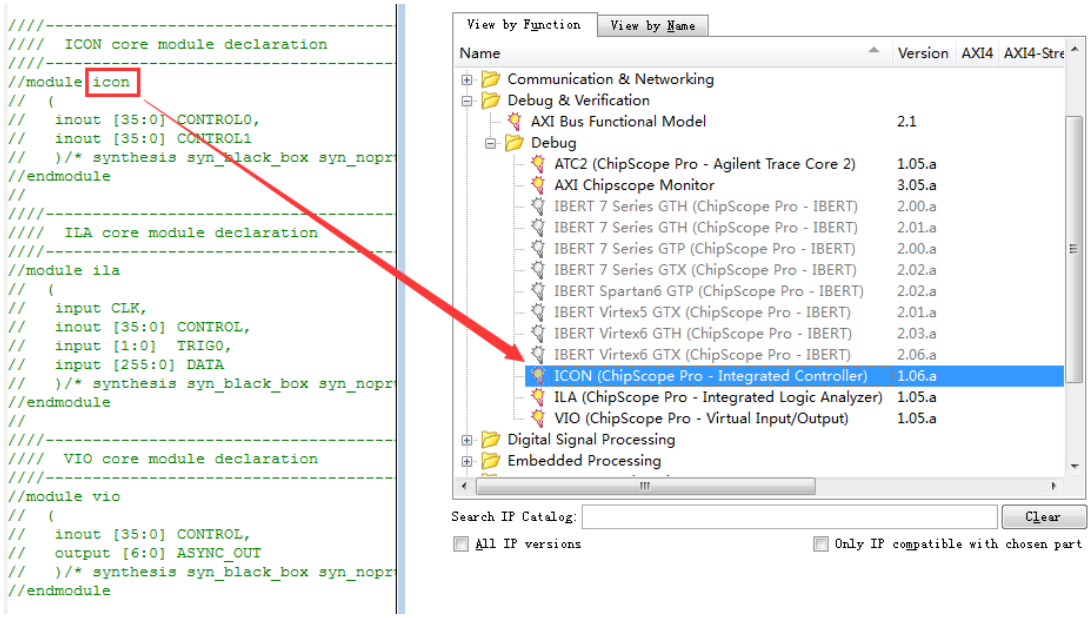
Cancel

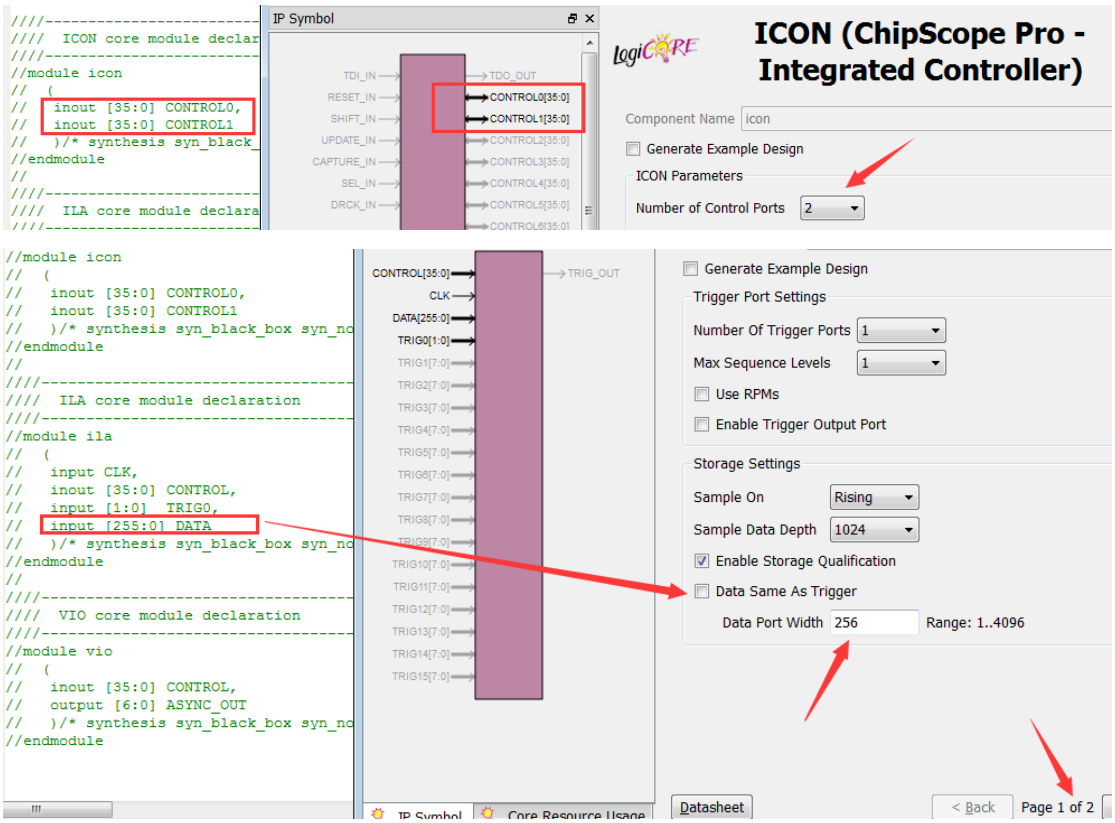

New Source...
Add Source...
Add Copy of Source...
Open
Remove
Manual Compile Order
Set as Top Module
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
Source Properties...

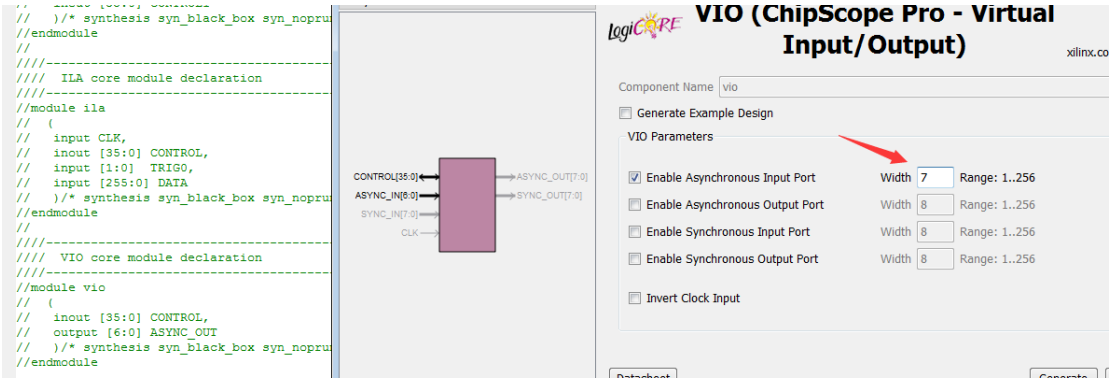

Add Source
ise_project ▸ ddr3_test ▸ ipcore_dir ▸ ddr3_test ▸ example_design ▸ rtl ▸
搜索 rtl
组织
新建文件夹
最近访问的位置
库
视频
图片
文档
迅雷下载
音乐
计算机
本地磁盘 (C:)
programs (D:)
develop (E:)
files (F:)
名称
修改日期
类型
大小
mcb_controller 2015/8/27 12:41 文件夹
traffic_gen 2015/8/27 12:41 文件夹
example_top.v 2015/8/27 12:41 V 文件 59 KB
infrastructure.v 2012/10/13 11:11 V 文件 11 KB
memc_tb_top.v 2012/10/13 11:11 V 文件 85 KB
memc_wrapper.v 2012/10/13 11:11 V 文件 65 KB
文件名(N):
Sources(*.txt *.vhd *.vhdl *.v
打开(O)
取消

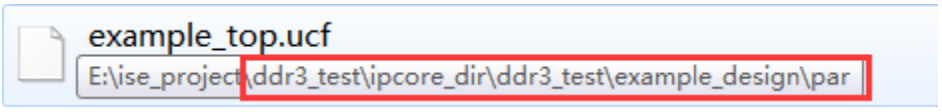


The original three modules (example_top.v pull to the end) need to remove the comment, add IPcore instead









Modify

```
##############################################################################
# Status Signals
##############################################################################

NET  "error"                            IOSTANDARD = LVCMOS33 ;
NET  "calib_done"                       IOSTANDARD = LVCMOS33 ;
NET  "calib_done"                       LOC = "R3" ;
NET  "error"                            LOC = "T3" ;   板子上的LED灯

##############################################################################
```