Genesys Logic, Inc.

GL3523-30

USB 3.1 Gen 1 Hub Controller

Datasheet

Revision 1.10
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Revision History

Revision	Date	Description
1.00	07/02/2018	Formal release
1.10	09/03/2018	Update GL3523-S Pin-out Diagram p.18

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CHAPTER 1 GENERAL DESCRIPTION

Genesys GL3523 is a 4-port, low-power, and configurable hub controller. It is compliant with the USB 3.1 specification. GL3523 integrates Genesys Logic self-developed USB 3.1 Gen 1 Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY. It supports Super Speed, Hi-Speed, and Full-Speed USB connections and is fully backward compatible to all USB 2.0 and USB 1.1 hosts. GL3523 also implements multiple TT* (Note1) architecture providing dedicated TT* to each downstream (DS) port, which guarantees Full-Speed(FS) data passing bandwidth when multiple FS devices perform heavy loading operations. Furthermore, GL3523 has built-in 5V to 3.3V and 5V to 1.2V regulators, which saves customers' BOM cost, and eases for PCB design.

GL3523 features the native fast-charging and complies with USB-IF battery charging specification rev1.2, it could fast-charge Apple, Samsung Galaxy devices, and any device complaint with BC1.2/1.1. It also allows portable devices to draw up to 1.5A from GL3523 charging downstream ports (CDP[1]) or dedicated charging port (DCP[2]). It can enable systems to fast charge handheld devices even during "Sleep" and "Power-off" modes.

With different part numbers, GL3523 also has USB Type-C function integrated (GL3523-S).

All available packages for GL3523 are listed as the following tables.

Product Series	Package Type	Number of DFPs	Power Mgmt.	LED Support
GL3523-30	QFN 76	4	Individual/ Gang	Green/Amber
	QFN 64	4	Individual/ Gang	N/A
	QFN 48	2	Individual/ Gang	N/A
GL3523-S3 (USB-C Integrated)	VFBGA144 (5C)	4	Individual/ Gang	Green/Amber
	QFN88 (2C3A)	4	Individual/ Gang	Amber
	QFN88 (1C4A)	4	Individual/ Gang	Green/Amber
	QFN76 (3C)	2	Individual/ Gang	N/A
	QFN64 (1C2A)	2	Individual/ Gang	Green/Amber

GL3523 Total Packages

*Note: TT (transaction translator) implements the control logic defined in Section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub.

[1] CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.

[2] DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

CHAPTER 2 FEATURES

- Compliant with USB 3.1 Gen 1 Specification
  - Upstream port supports SuperSpeed (SS), HighSpeed (HS) and FullSpeed (FS) traffic
  - Downstream ports support SS, HS, FS, and LowSpeed (LS) traffic
  - 1 control pipe and 1 interrupt pipe
  - Backward compatible to USB specification Revision 2.0/1.1
- Native USB Type-C support in GL3523-S series
  - Compliant with USB Type-C Cable and Connection Specification Revision 1.0
  - Featuring USB Type-C functions
  - Detecting flip-able/reversible plugging
  - Discovering/configuring VBUS
  - Supporting USB Type-C Current modes , including USB Default, 1.5A@5V, 3A@5V
  - Configuring/Supporting VCONN Power and having VCONN over-current protection
- Featuring fast-charging on all downstream ports and upstream port
  - Compliant with USB Battery Charging Revision v1.2, supporting CDP, DCP, and ACA-Dock
  - Downstream ports can be turned from a Standard Downstream Port (SDP) into Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
  - Downstream devices can be charged while upstream VBUS is not present, which can be applied on wall charger applications
  - Upstream port is capable of charging and data communicating simultaneously for portable devices supporting ACA-Dock or proprietary charging protocols
  - Supporting Apple 1A/2.1A/2.4A and Samsung Galaxy devices fast-charging
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - 1 cycle instruction execution (maximum)
  - Performance: 12 MIPS @ 12.5MHz (maximum)
  - With 256-byte RAM, 20K-byte internal ROM, and 24K-byte SRAM
- Multiple Transaction Translator (TT) architecture
  - Providing dedicated TT control logics for each downstream port
  - Superior performance when multiple FS devices operate concurrently
- Integrated USB transceiver
  - Improving output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- Advanced power management and low power consumption
  - Supporting USB 3.1 U0/U1/U2/U3 power management states
  - Supporting USB Link Power Management (LPM) L0/L1/L2
  - Supporting individual/gang mode over-current detection for all downstream ports
  - Supporting both low/high-enabled power switches
  - Patented Smart Power Management
- Configurable settings by firmware in SPI flash
  - Configurable charging port
  - Configurable 4/3/2 downstream ports, downstream port can be disabled/enabled by each specific port for USB3.1/USB2.0
  - Configurable Upstream and Downstream Ports in GL3523-S
  - Supporting multiple upstream ports in GL3253-S OV3S1 and OV5S1 packages
  - Supporting full in-system programming firmware upgrade by SPI-flash and configuration by EEPROM
  - Supporting compound-device (non-removable setting on downstream ports)
  - Supporting customization VID/PID

- Flexible design
  - Supporting Poly-fuse/Power-switch
  - Automatic switching between self-powered and bus-powered modes
  - Supporting electrical tuning for each specific port
  - Supporting programmable breathing LED
  - Supporting register setting by firmware
  - Supporting vendor command and SMBUS
  - Allow downstream ports to connect up to 8 devices, 4 x USB3.1 non-removable devices with 4 x USB2.0 non-removable devices or exposed ports
- Low BOM cost
  - Single external 25 MHz crystal / Oscillator clock input
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Built-in 5 to 3.3V and 5 to 1.2V regulator
- Different package types available for various applications
- Applications
  - Standalone USB hub/Docking station
  - Tablet/Ultrabook/NB
  - Motherboard
  - Monitor built-in hub, GPIOs can be programmed as I2C interface to easily update scalar firmware through USB interface
  - TV built-in hub
  - Compound device, such as hub-reader application
  - USB wall charger
  - Other consumer electronics
  - Customized applications
    - Dynamically disable/enable ports
    - GPIO signaling of ambient light sensor or rotation/position sensor

CHAPTER 3 PIN ASSIGNMENT

3.1 GL3523 Pin-out Diagram

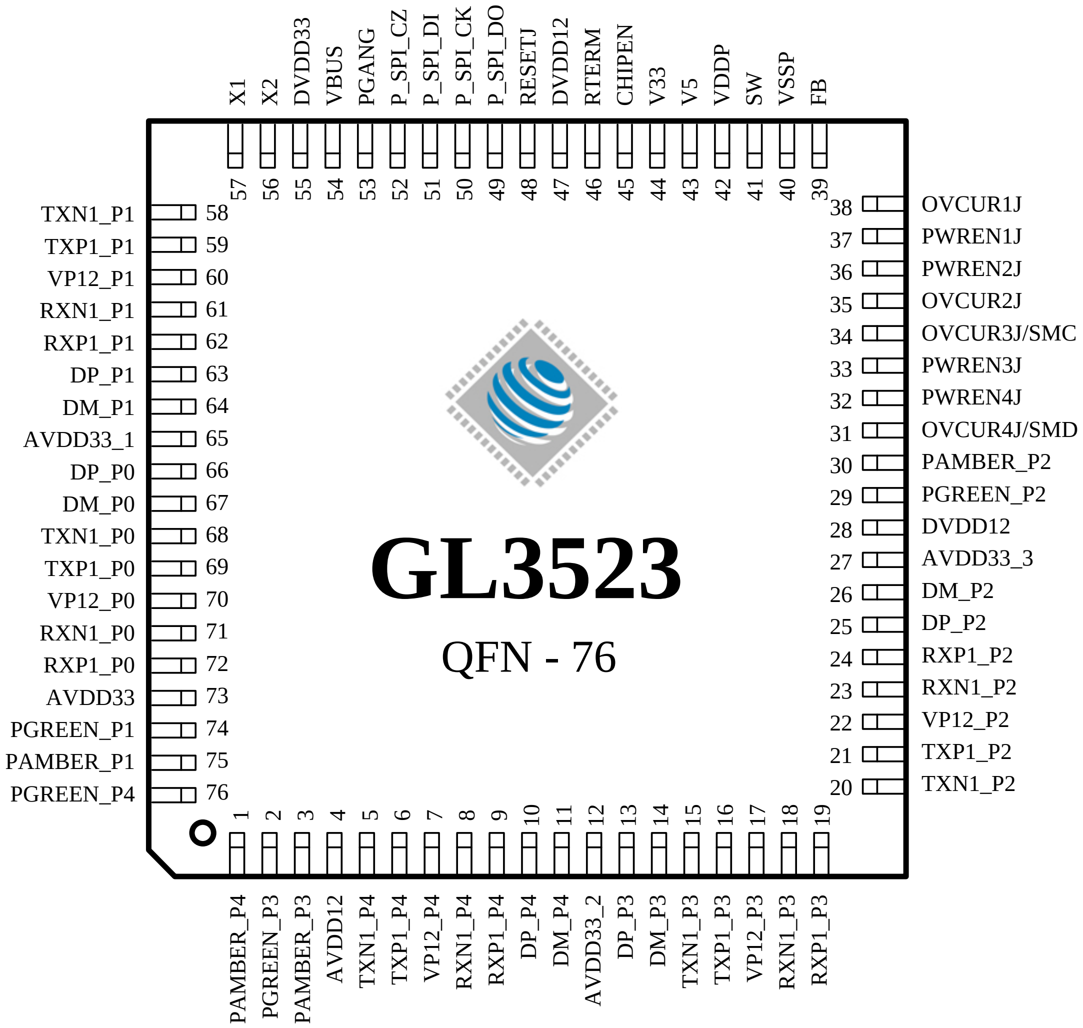


Figure 3.1 - GL3523 QFN 76 Pin-out Diagram

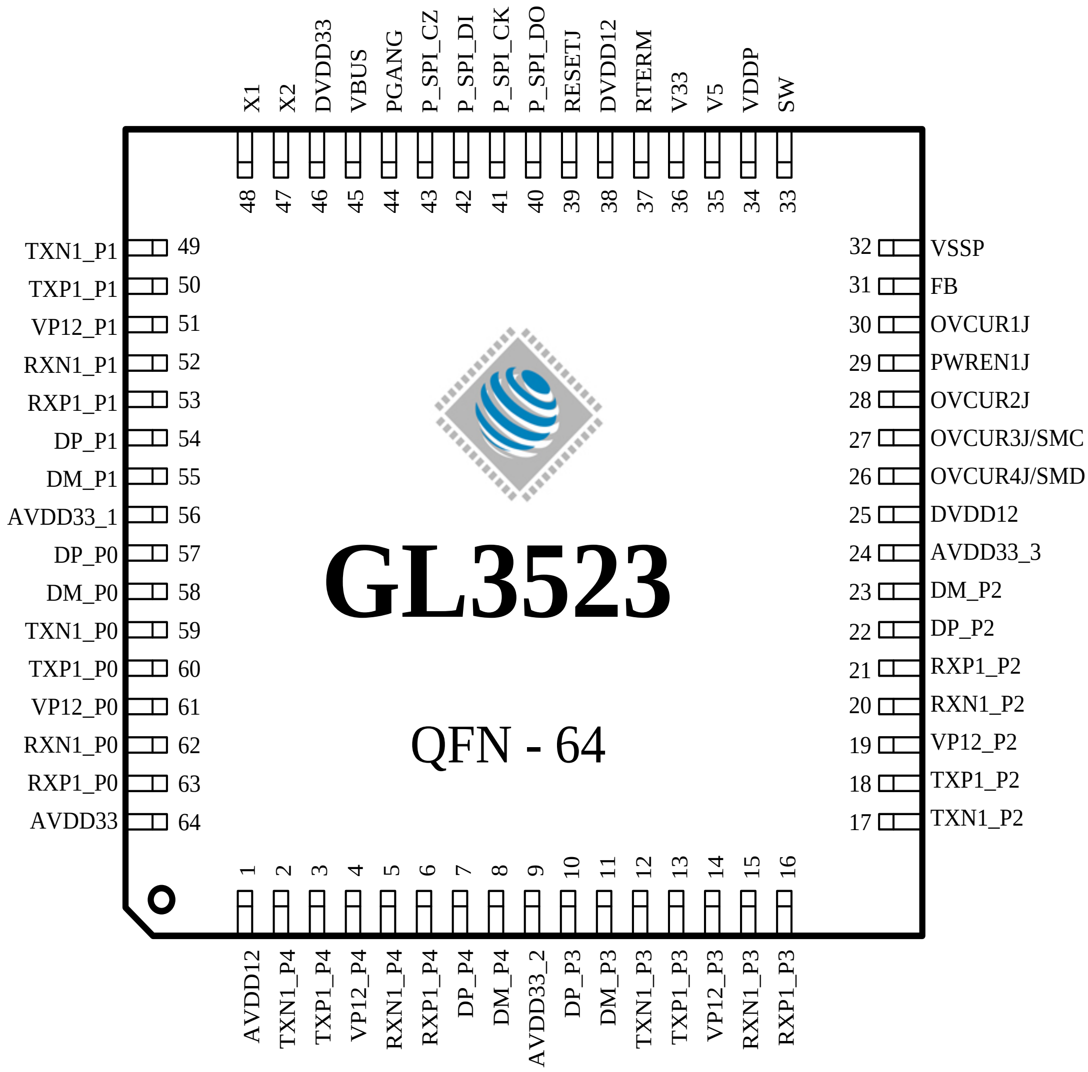


Figure 3.2 - GL3523 QFN 64 Pin-out Diagram

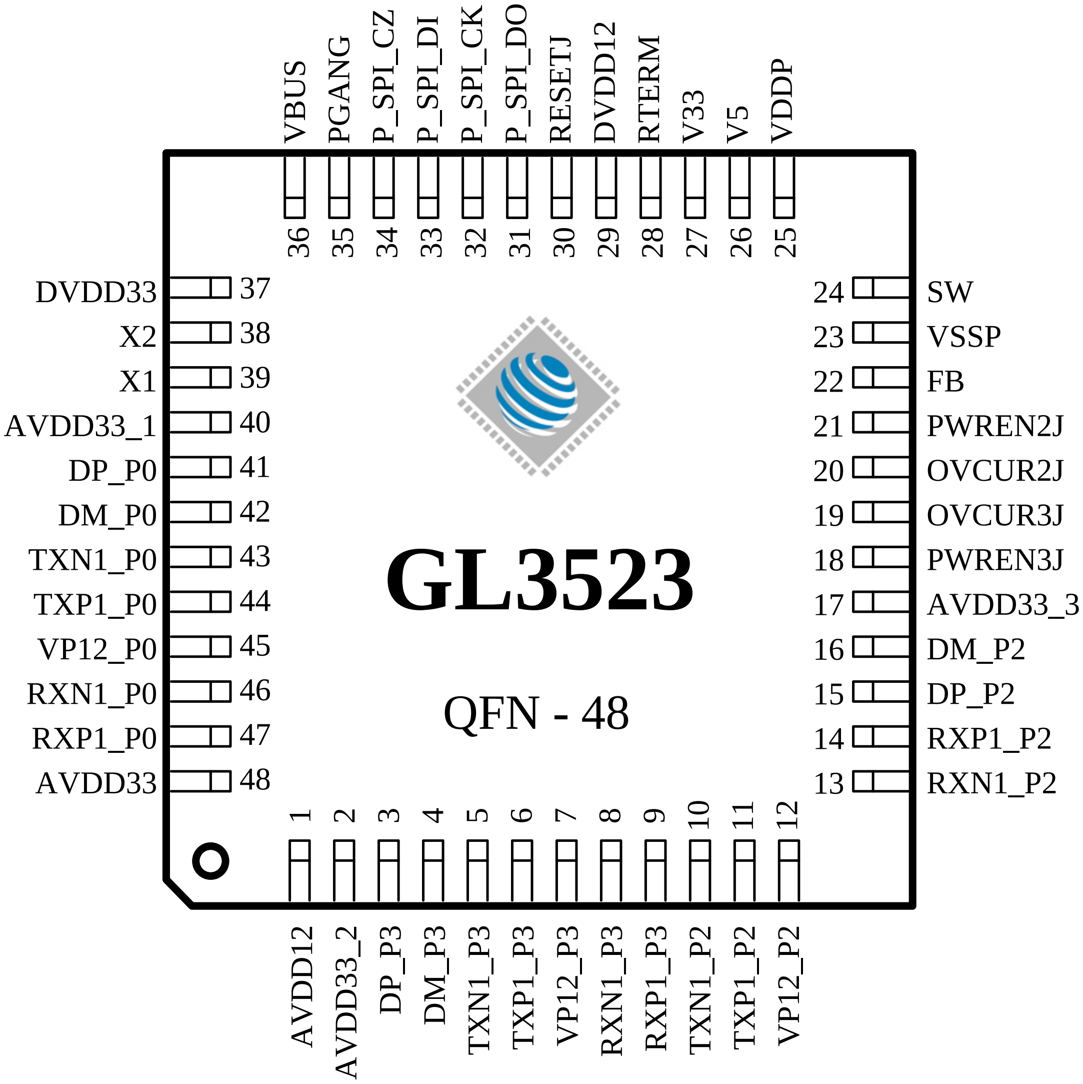


Figure 3.3 - GL3523 QFN 48 Pin-out Diagram

3.2 GL3523 Pin Descriptions

USB Interface					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
TXN1_P0 TXP1_P0	68 69	59 60	43 44	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of USPORT
RXN1_P0 RXP1_P0	71 72	62 63	46 47	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of USPORT
TXN1_P1 TXP1_P1	58 59	49 50	-	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT1
RXN1_P1 RXP1_P1	61 62	52 53	-	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT1
TXN1_P2 TXP1_P2	20 21	17 18	10 11	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT2
RXN1_P2 RXP1_P2	23 24	20 21	13 14	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT2
TXN1_P3 TXP1_P3	15 16	12 13	5 6	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT3
RXN1_P3 RXP1_P3	18 19	15 16	8 9	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT3
TXN1_P4 TXP1_P4	5 6	2 3	-	O	USB3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT4
RXN1_P4 RXP1_P4	8 9	5 6	-	I	USB3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT4
DM_P0 DP_P0	67 66	58 57	42 41	B	USB 2.0 DM/DP for USPORT
DM_P1 DP_P1	64 63	55 54	-	B	USB 2.0 DM/DP for DSPORT1
DM_P2 DP_P2	26 25	23 22	16 15	B	USB 2.0 DM/DP for DSPORT2
DM_P3 DP_P3	14 13	11 10	4 3	B	USB 2.0 DM/DP for DSPORT3
DM_P4 DP_P4	11 10	8 7	-	B	USB 2.0 DM/DP for DSPORT4

Hub Interface					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
PGREEN1~4	74,29, 2,76	-	-	B	Green LED indicator for DSPORT1~4
PAMBER1~4	75,30, 3,1	-	-	B	Amber LED indicator for DSPORT1~4
PWREN1~4J	37,36, 33,32	29	21 18	B	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.
OVCUR1~4J	38,35, 34,31	30,28, 27,26	20 19	I (pd)	Active low. Over current indicator for DSPORT1~4 The OVCUR pin of DFP1 will be the only over-current flag

					for GANG mode. *In reset state : OVCUR3J will be SMC, OVCUR4J will be SMD * SMBUS function is only available in QFN76 and QFN64
PGANG	53	44	35	I	Default put in input mode after power-on reset. Individual/gang mode is strapped during this period.

Clock and Reset Interface					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
X1	57	48	39	I	Crystal / OSC clock input
X2	56	47	38	O	Crystal clock output.
RESETJ	48	39	30	I (pd)	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.
CHIPEN	45	-	-	I (pu)	0: Disable whole chip and keep hub in lowest power state (standby mode) 1: Normal state

SPI Interface					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
P_SPI_CK	50	41	32	B	For SPI data clock
P_SPI_CZ	52	43	34	B	For SPI data chip enable
P_SPI_DO	49	40	31	B	For SPI data Input
P_SPI_DI	51	42	33	B	For SPI data Output

Power/Ground Interface					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
VP12_P0~P4	70,60,22,17,7	61,51,19,14,4	45,12,7	P	Analog 1.2V power input for Analog circuit
AVDD12	4	1	1	P	Analog 1.2V power input for Analog PLL circuit
DVDD12	28,47	25,38	29	P	1.2V digital power input for digital circuits
DVDD33	55	46	37	P	3.3V digital power input for digital circuits
AVDD33 AVDD33_1 AVDD33_2 AVDD33_3	73 65 12 27	64 56 9 24	48 40 2 17	P	Analog 3.3V power input
VBUS	54	45	36	I	VBUS detection pin for valid VBUS
V33	44	36	27	P	5V-to-3.3V regulator Vout & 3.3 input
V5	43	35	26	P	5V Power input. It should be connected to V33 if using external 3.3V regulator

Switching Regulator (5V to 1.2V)					
Pin Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
FB	39	31	22	A	Switcher Feedback Voltage. This pin is the inverting input of the error amplifier. VOUT senses the switcher output through an external resistor divider network. For the fixed voltage version, connect this pin to the output voltage.
SW	41	33	24	A	Internal Switches Output. Connect this pin to the output inductor.
VDDP	42	34	25	P	Dedicated 5V power input for embedded switching regulator
VSSP	40	32	23	P	Dedicated Ground for embedded switching regulator

Miscellaneous Interface					
Name	**QFN 76**	**QFN 64**	**QFN 48**	**Type**	**Description**
RTERM	46	37	28	A	A 20Kohm resister must be connected between RTERM and Ground

Note: Analog circuits are quite sensitive to power and ground noise, so please take care the power routing and the ground plane for PCB design. For detailed information, please refer to **USB3.1 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

3.3 GL3523-S Series Pin-out Diagram

1	2	3	4	5	6	7	8	9	10	11	12	
TXP2_P3	TXN2_P3	TXN1_P2	RXN1_P2	DM_P2	RXP2_P2	TXP2_P2	PAMBER_P2	OVCUR2J	OVCUR1J	VSSP	SW	M
RXP2_P3	RXN2_P3	TXP1_P2	RXP1_P2	DP_P2	RXN2_P2	TXN2_P2	PGREEN_P2	PWREN2J	PWREN1J	VSSP	SW	L
DM_P3	DP_P3	VP12_P3	VP12_P2	VP12_P2	PWREN4J	PWREN3J	OVCUR3J/SMC	DVDD12	FB	VDDP	VDDP	K
RXN1_P3	RXP1_P3	VP12_P3	AVDD33_2	AVDD33_3	OVCUR4J/SMD	AVDD33_3	GND	PSELF	RTERM	V33	V5_CC	J
TXN1_P3	TXP1_P3	GND	AVDD33_2	GND	GND	GND	GND	GND	CC1_P4	P_SPI_DO	CHIPEN	H
TXP2_P4	TXN2_P4	PAMBER_P3	PGREEN_P3	GND	GND	GND	GND	CC1_P3	CC2_P4	P_SPI_DI	P_SPI_CK	G
RXP2_P4	RXN2_P4	PGREEN_P4	PAMBER_P4	GND	GND	GND	GND	CC2_P3	CC1_P2	CC1_P1	P_SPI_CZ	F
DM_P4	DP_P4	PGREEN_P1	GND	GND	GND	GND	GND	GND	CC2_P2	CC1_P0	CC2_P1	E
RXN1_P4	RXP1_P4	PAMBER_P1	VP12_P0	GND	AVDD33	GND	AVDD33_1	DVDD33	DVDD12	PGANG	CC2_P0	D
TXN1_P4	TXP1_P4	AVDD12	VP12_P0	VP12	GND	GND	AVDD33_1	VP12_P1	VP12_P1	RESETJ	VBUS	C
VP12_P4	TXN2_P0	RXN2_P0	DP_P0	RXP1_P0	TXP1_P0	TXN2_P1	RXN2_P1	DP_P1	RXP1_P1	TXP1_P1	X2	B
VP12_P4	TXP2_P0	RXP2_P0	DM_P0	RXN1_P0	TXN1_P0	TXP2_P1	RXP2_P1	DM_P1	RXN1_P1	TXN1_P1	X1	A

Figure 3.4 - GL3523-S VFBGA144 Ball Diagram (Bottom View)

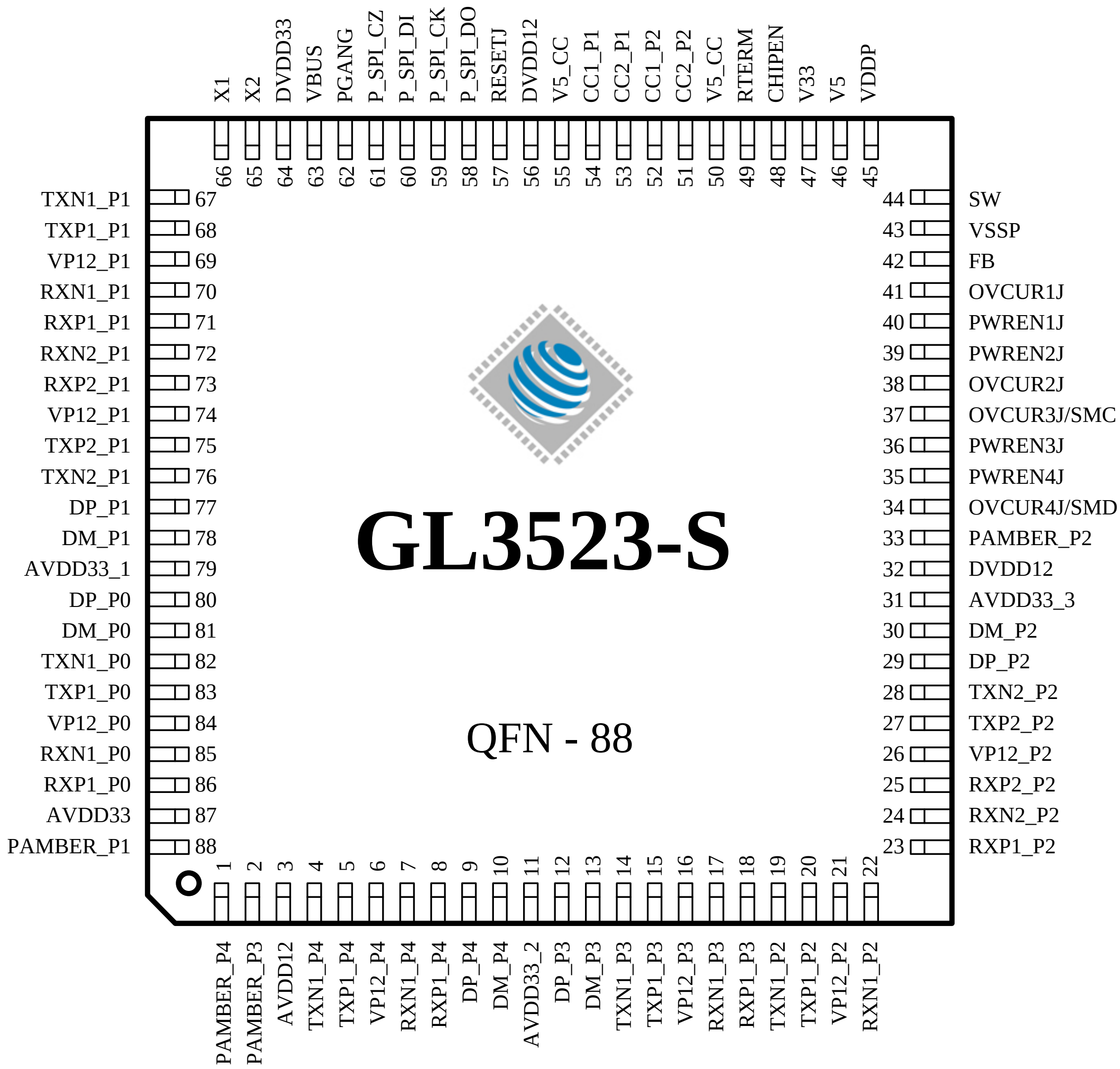


Figure 3.5 - GL3523-S QFN88 (2C3A) Pin-out Diagram

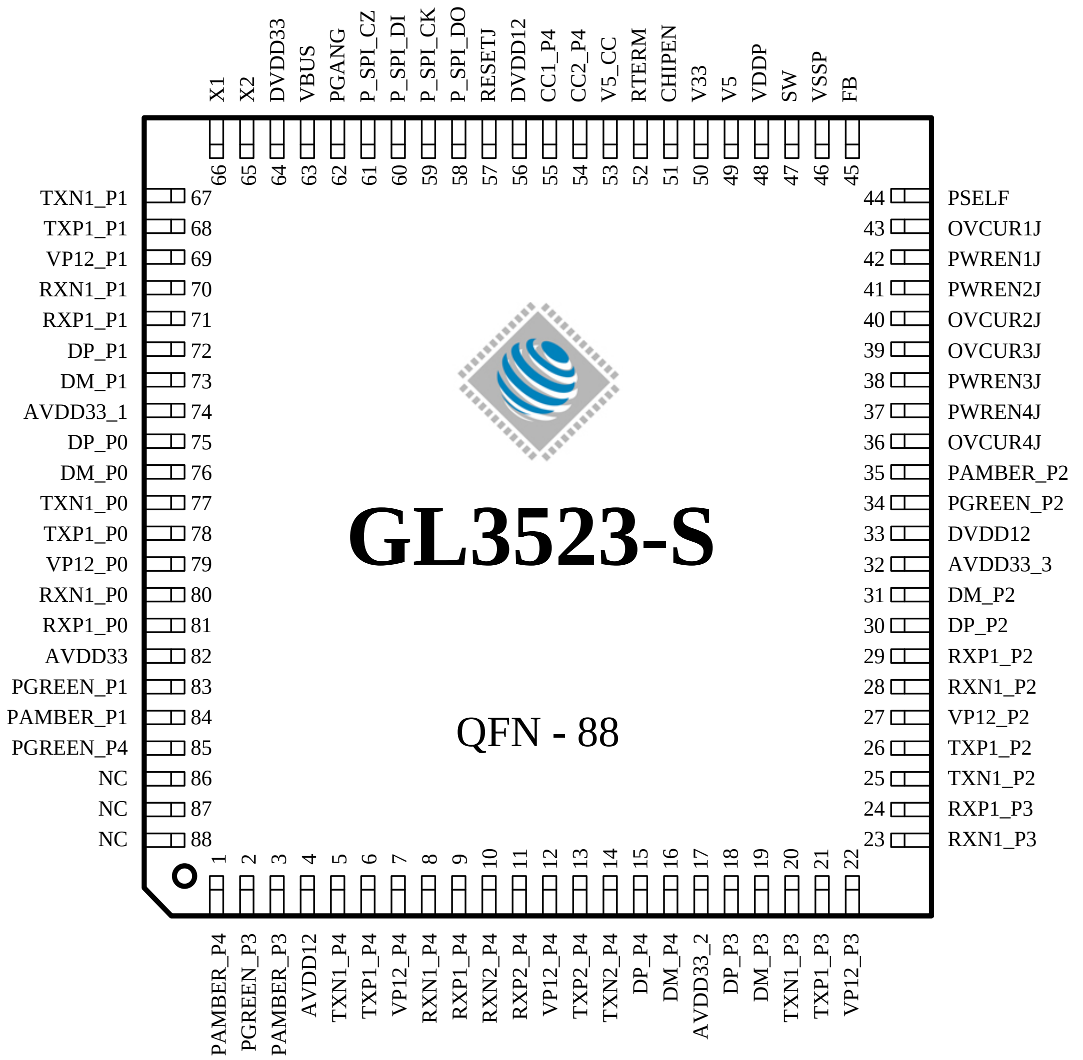


Figure 3.6 - GL3523-S QFN88 (1C4A) Pin-out Diagram

Figure 3.7 - GL3523-S QFN76 Pin-out Diagram

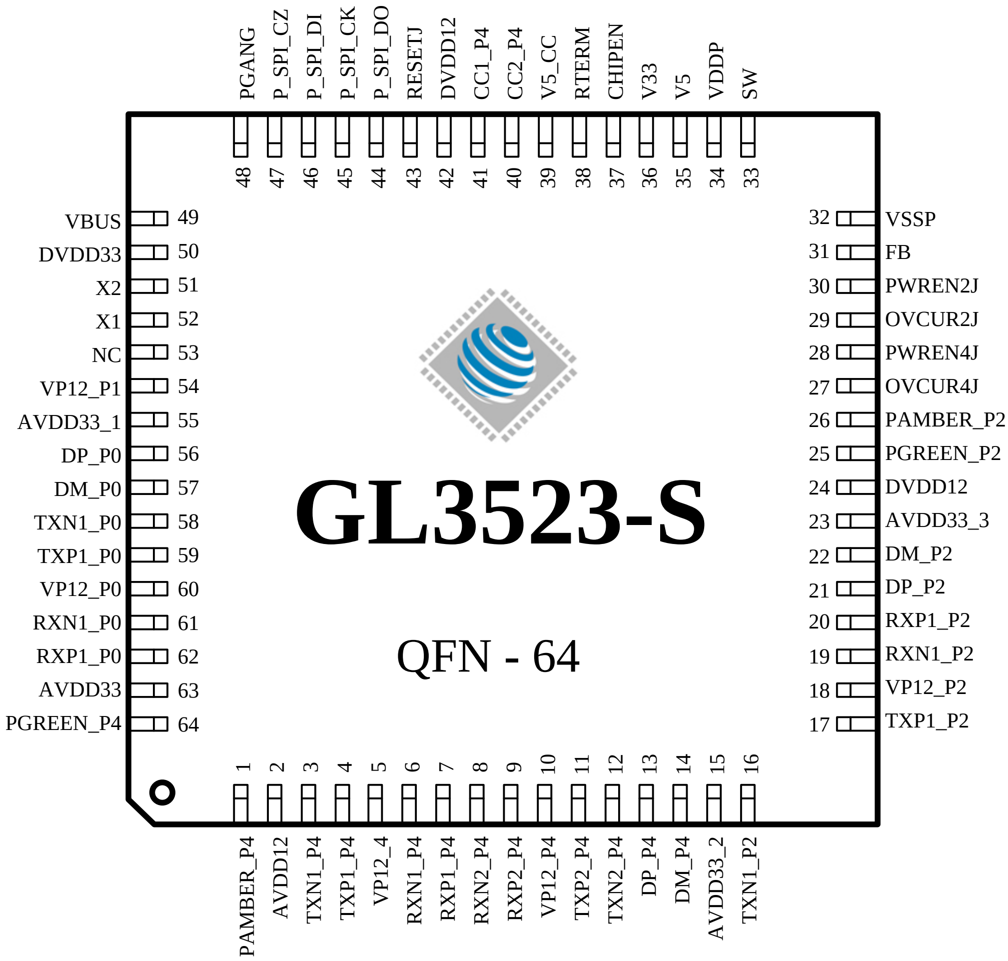


Figure 3.8 - GL3523-S QFN64 (1C2A) Pin-out Diagram

3.4 GL3523-S Pin Descriptions

USB Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
TXN1_P0 TXP1_P0	A6 B6	82 83	77 78	66 67	58 59	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of USPORT
TXN2_P0 TXP2_P0	B2 A2	-	-	75 74	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of USPORT for Type-C
RXN1_P0 RXP1_P0	A5 B5	85 86	80 81	69 70	61 62	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of USPORT
RXN2_P0 RXP2_P0	B3 A3	-	-	71 72	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of USPORT for Type-C
TXN1_P1 TXP1_P1	A11 B11	67 68	67 68	-	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT1
TXN2_P1 TXP2_P1	B7 A7	76 75	-	-	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT1 for Type-C
RXN1_P1 RXP1_P1	A10 B10	70 71	70 71	-	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT1
RXN2_P1 RXP2_P1	B8 A8	72 73	-	-	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT1 for Type-C
TXN1_P2 TXP1_P2	M3 L3	19 20	25 26	17 18	16 17	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT2
TXN2_P2 TXP2_P2	L7 M7	28 27	-	26 25	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT2 for Type-C
RXN1_P2 RXP1_P2	M4 L4	22 23	28 29	20 21	19 20	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT2
RXN2_P2 RXP2_P2	L6 M6	24 25	-	22 23	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT2 for Type-C
TXN1_P3 TXP1_P3	H1 H2	14 15	20 21	5 6	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT3
TXN2_P3 TXP2_P3	M2 M1	-	-	14 13	-	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT3 for Type-C
RXN1_P3 RXP1_P3	J1 J2	17 18	23 24	8 9	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT3
RXN2_P3 RXP2_P3	L2 L1	-	-	10 11	-	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT3 for Type-C
TXN1_P4 TXP1_P4	C1 C2	4 5	5 6	-	3 4	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT4
TXN2_P4 TXP2_P4	G2 G1	-	14 13	-	12 11	O	USB 3.1 Gen 1 Differential Data Transmitter TX-/TX+ of DSPORT4 for Type-C
RXN1_P4 RXP1_P4	D1 D2	7 8	8 9	-	6 7	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT4
RXN2_P4 RXP2_P4	F2 F1	-	10 11	-	8 9	I	USB 3.1 Gen 1 Differential Data Receiver RX-/RX+ of DSPORT4 for Type-C
DM_P0 DP_P0	A4 B4	81 80	76 75	65 64	57 56	B	USB 2.0 DM/DP for USPORT
DM_P1 DP_P1	A9 B9	78 77	73 72	-	-	B	USB 2.0 DM/DP for DSPORT1

DM_P2 DP_P2	M5 L5	30 29	31 30	28 27	22 21	B	USB 2.0 DM/DP for DSPORT2
DM_P3 DP_P3	K1 K2	13 12	19 18	4 3	-	B	USB 2.0 DM/DP for DSPORT3
DM_P4 DP_P4	E1 E2	10 9	16 15	-	14 13	B	USB 2.0 DM/DP for DSPORT4

Type-C Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
CC1_P0 CC2_P0	E11 D12	-	-	50 49	-	I/O	Configuration Channel for USPORT
CC1_P1 CC2_P1	F11 E12	54 53	-	-	-	I/O	Configuration Channel for DSPORT1
CC1_P2 CC2_P2	F10 E10	52 51	-	47 46	-	I/O	Configuration Channel for DSPORT2
CC1_P3 CC2_P3	G9 F9	-	-	45 44	-	I/O	Configuration Channel for DSPORT3
CC1_P4 CC2_P4	H10 G10	-	55 54	-	41 40	I/O	Configuration Channel for DSPORT4

Hub Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
PGREEN _P1~4	E3,L8, G4,F3	-	83,34,2,8 5	-	25, 64	B	Green LED indicator for DSPORT1~4
PAMBER _P1~4	D3,M8,G 3,F4	88,33, 2,1	84,35,3,1	-	26, 1	B	Amber LED indicator for DSPORT1~4
PWREN1 ~4J	L10,L9, K7,K6	40,39, 36,35	42,41,38, 37	34,31	30 28	B	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.
OVCUR1 ~4J	M10,M9, K8,J6	41,38, 37,34	43,40,39, 36	33,32	29 27	I (pd)	Active low. Over current indicator for DSPORT1~4 The OVCUR pin of DFP1 will be the only over-current flag for GANG mode. ▪ In reset state : OVCUR3J will be SMC, OVCUR4J will be SMD ▪ SMBUS function is only available in VFBGA144 and QFN88
PGANG	D11	62	62	57	48	I	Default put in input mode after power-on reset. Individual/gang mode is strapped during this period.
PSELF	J9	-	44	-	-	I	0: Hub is bus-powered. 1: Hub is self-powered.

Clock and Reset Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
X1	A12	66	66	61	52	I	Crystal / OSC clock input
X2	B12	65	65	60	51	O	Crystal clock output.
RESETJ	C11	57	57	52	43	I	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.
CHIPEN	H12	48	51	42	37	I (pu)	0: Disable whole chip and keep hub in lowest power state (standby mode) 1: Normal state

SPI Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
P_SPI_CK	G12	59	59	54	45	B	For SPI data clock
P_SPI_CZ	F12	61	61	56	47	B	For SPI data chip enable
P_SPI_DO	H11	58	58	53	44	B	For SPI data Input
P_SPI_DI	G11	60	60	55	46	B	For SPI data Output

Power/Ground Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
VP12_P0~4	C5,C4,D4,C9,C10K4,K5, J3,K3 A1,B1	84,74,69, 26,21, 16,6	79,69,7,27,22,12	62,73,68,24,19,7,12	60, 54,18 10,5	P	Analog 1.2V power input for Analog circuit
AVDD12	C3	3	4	1	2	P	Analog 1.2V power input for Analog PLL circuit
DVDD12	K9,D10	32,56	33,56	30,51	24,42	P	1.2V digital power input for digital circuits
DVDD33	D9	64	64	59	50	P	3.3V digital power input for digital circuits
AVDD33 AVDD33_1 AVDD33_2 AVDD33_3	D6, C8,D8, H4,J4, J5,J7	87 79 11 31	82 32	76,63,2, 29	63 55 15 23	P	Analog 3.3V power input
GND	C6,C7,D5,D7,E4~9, F5~8, G5~8, H3, H5~9, J8	-	-	-	-	P	Digital/Analog ground
VBUS	C12	63	63	58	49	I	VBUS detection pin for valid input
V33	J11	47	50	41	36	P	5V-to-3.3V regulator Vout & 3.3 input
V5	-	46	49	40	35	P	5V Power input. It should be connected to V33 if using external 3.3V regulator

V5_CC	J12	50,55	53	48	39	P	5V Power input of CC. It has to be supplied with 5V to make CC functioning.

Switching Regulator (5V to 1.2V)							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN 76**	**QFN64**	**Type**	**Description**
FB	K10	42	45	35	31	A	Feedback sense, output 1.2V
SW	L12, M12	44	47	38	33	A	Internal switches output. Connect this pin to the output inductor
VDDP	K11,K12	45	48	39	34	P	Dedicated 5V power input for embedded switching regulator
VSSP	L11, M11	43	46	37	32	P	Dedicated Ground for embedded switching regulator

Miscellaneous Interface							
Name	**VFBGA 144**	**QFN88 (2C3A)**	**QFN88 (1C4A)**	**QFN76**	**QFN64**	**Type**	**Description**
RTERM	J10	49	52	43	38	A	A 20Kohm resister must be connected between RTERM and Ground
NC	-	-	86,87,88	15,16, 36	53	--	Not Connect

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **USB 3.1 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

CHAPTER 4 FUNCTION DESCRIPTION

4.1 GL3523 Functional Block

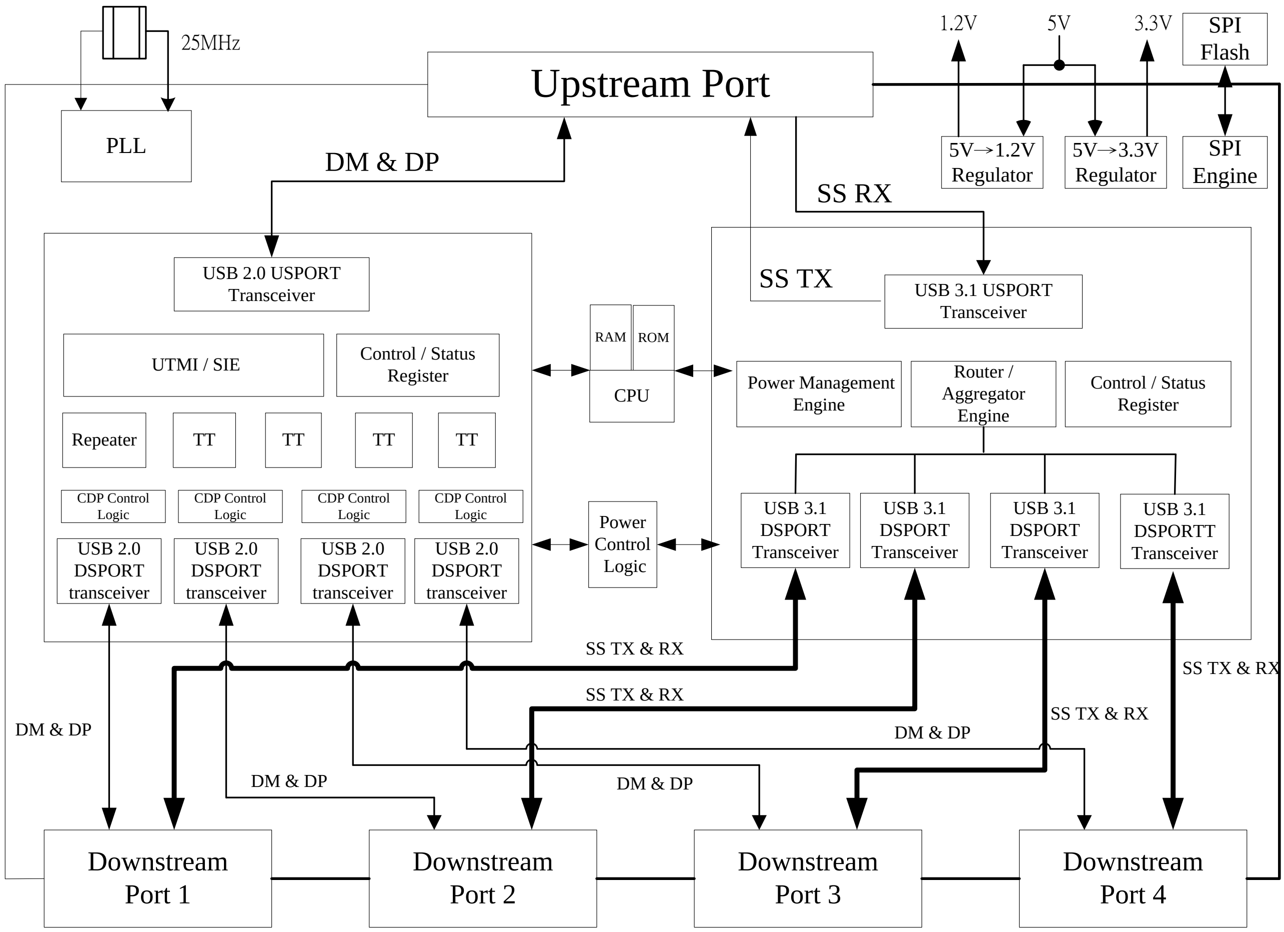


Figure 4.1 – GL3523 Architecture Diagram

4.2 GL3523-S Functional Block

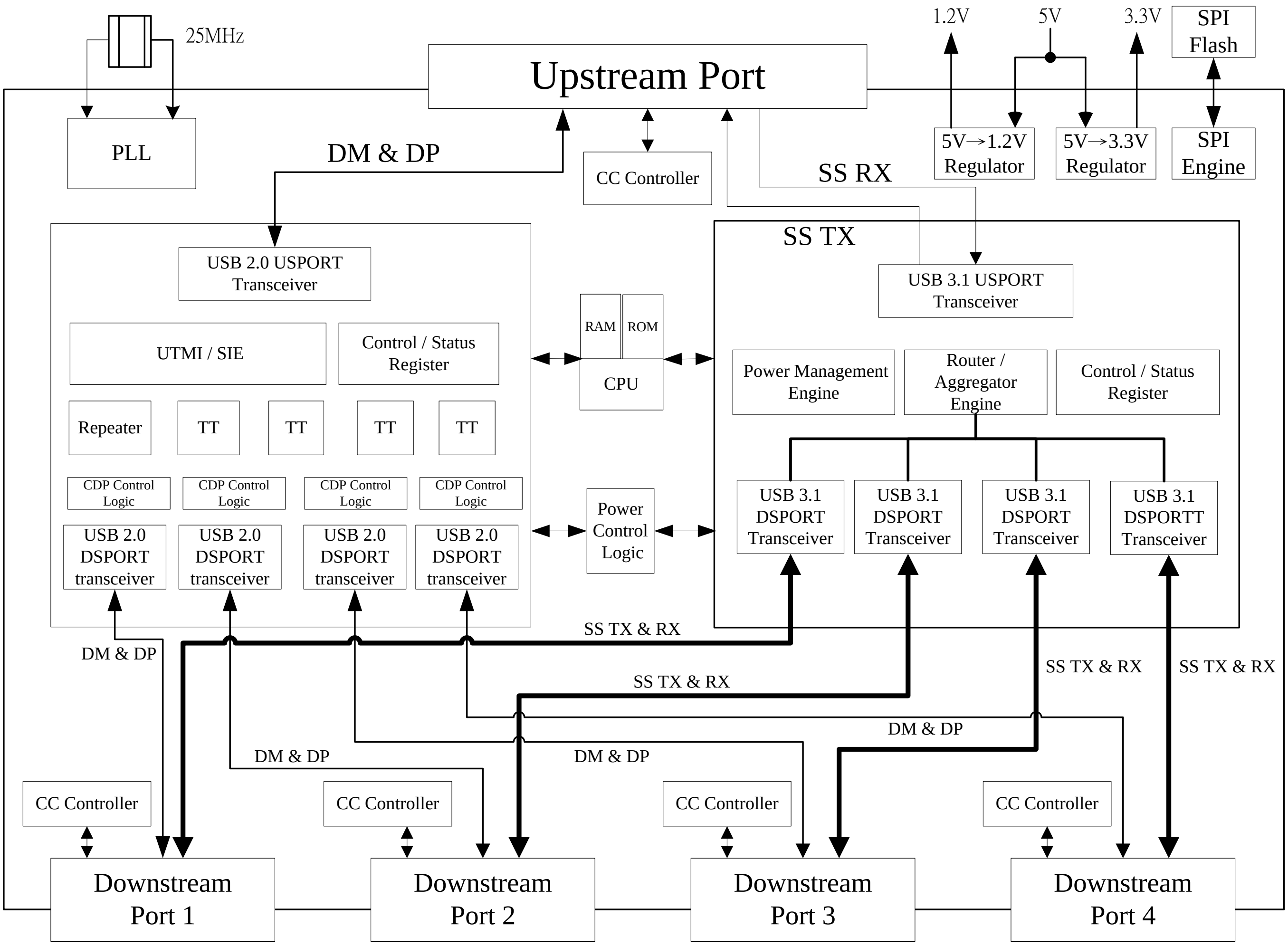


Figure 4.2 – GL3523-S Architecture Diagram

4.3 General Description

4.3.1 USB 2.0 USPORT Transceiver

USB 2.0 USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in Chapter 7 of USB specification revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL3523 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL3523 is plugged into a 2.0 host/hub.

4.3.2 USB 3.1 Gen 1 USPORT Transceiver

USB3.1 Gen 1 USPORT (upstream port) transceiver is the analog circuit that has elastic buffer and supports receiver detection, data serialization and de-serialization. Besides, it has PIPE interface with SuperSpeed Link Layer

4.3.3 PLL (Phase Lock Loop)

PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

4.3.4 Regulator

GL3523 build in internal regulators convert 5V input to 3.3V/1.2V output.

4.3.5 SPI Engine

SPI engine is to move code from external flash to the internal RAM.

4.3.6 RAM/ROM/CPU

The micro-processor unit of GL3523 is an 8-bit RISC processor with 20K-byte ROM and 256-bytes RAM. It operates at 12MIPS of 12 MHz clock(maximum) to decode the USB command issued from host and then prepares the data to respond to the host.

4.3.7 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

4.3.8 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in Chapter 8 of USB specification revision 2.0. It co-works with μC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

4.3.9 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL3523 possesses higher flexibility to control the USB protocol easily and correctly.

4.3.10 Power Management Engine

The power management of GL3523 is compliant with USB3.1 Gen 1 specification. When operating in SuperSpeed mode, GL3523 supports U0, U1, U2, and U3 power states. U0 is the functional state. U1 and U2 are lower power states compared to U0. U1 is a low power state with fast exit to U0; U2 is a low power state which saves more power than U1 with slower exit to U0. U3 is suspend state, which is the most power-saving state, with tens of milliseconds exit to U0. Unlike USB 2.0, SuperSpeed packet traffic is unicast rather than broadcast. Packet only travels the direct path in-between host and the target device. SuperSpeed traffic will not reach an unrelated device. When enabled for U1/U2 entry, and there is no pending traffic within comparable exit latency, GL3523 will initiate U1/U2 entry to save the power. On the other hand, the link partner of GL3523 may also initiate U1/U2 entry. In this case, GL3523 will accept or reject low power state entry according to its internal condition.

4.3.11 Router/Aggregator Engine

Router/Aggregator Engine implements the control logic defined in Chapter10 of USB 3.1 specification. Router/Aggregator Engine uses smart method for route packet to device or aggregate packet to host.

4.3.12 REPEATER

Repeater logic implements the control logic defined in Section 11.4 and Section 11.7 of USB specification revision 2.0. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

4.3.13 TT

TT (Transaction Translator) implements the control logic defined in Section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL3523 adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively.

4.3.13.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

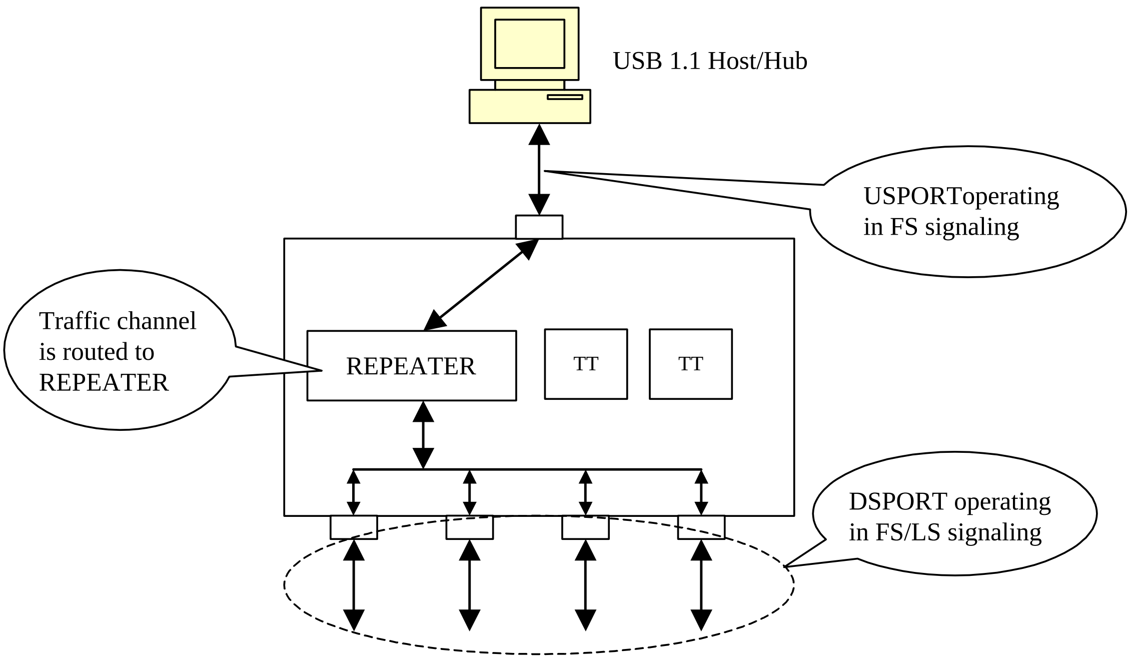


Figure 4.3 - Operating in USB 1.1 Schemes

4.3.13.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

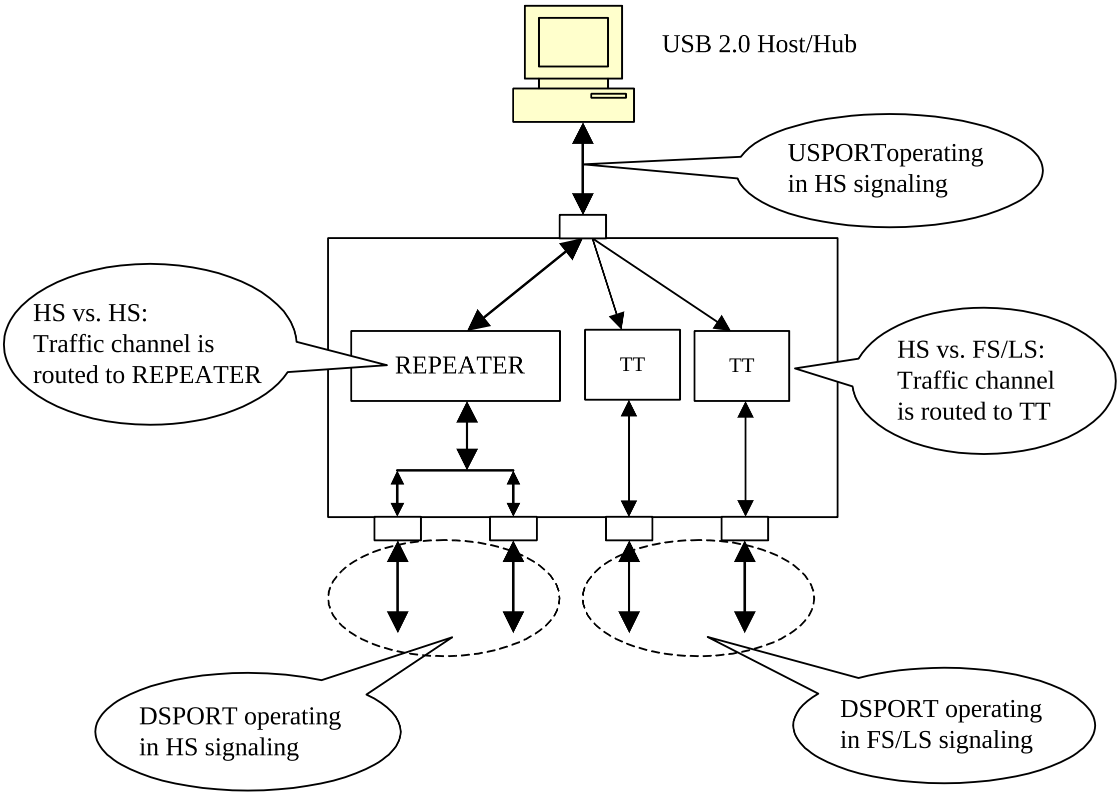


Figure 4.4 - Operating in USB 2.0 Schemes

4.3.14 CDP Control Logic

CDP (charging downstream port) control logic implements the logic defined in USB Battery charging specification revision 1.2. The major function of it is to control DSPORT Transceiver to make handshake with a portable device which is compliant with USB Battery charging spec rev1.2 as well. After recognizing charging detection each other, portable device will draw up to 1.5A from VBUS to fast charge its battery.

4.3.15 USB 3.1 Gen 1/USB 2.0 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

4.4 Configuration and I/O Settings

4.4.1 RESET Setting

GL3523's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL3523's internal reset is designed to monitor silicon's internal core power (1.2V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 40 µS after power good. GL3523's reset circuit as depicted in the picture.

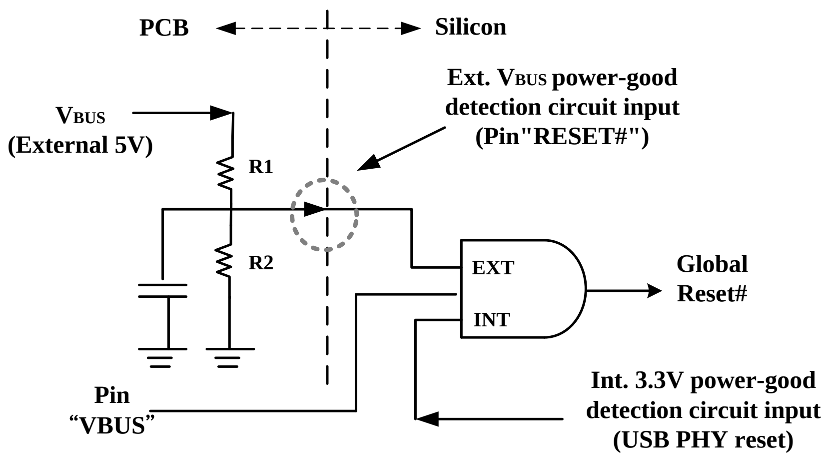


Figure 4.5 - Power on Reset Diagram

To fully control the reset process of GL3523, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit. Timing of POR is illustrated as below figure.

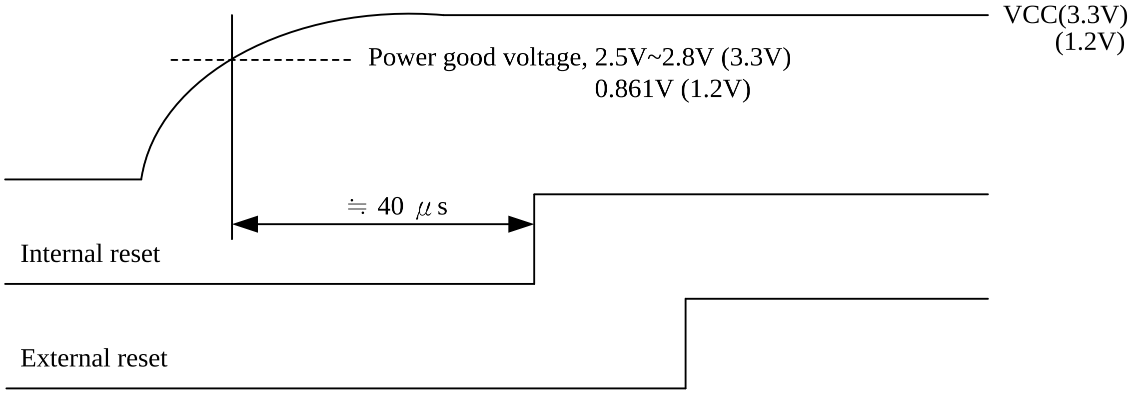


Figure 4.6 - Power on Sequence of GL3523

4.4.2 PGANG Setting

To save pin count, GL3523 uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 21us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL3523 outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a greater than 100KΩ pull high resister should be placed. In figure 4.7, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

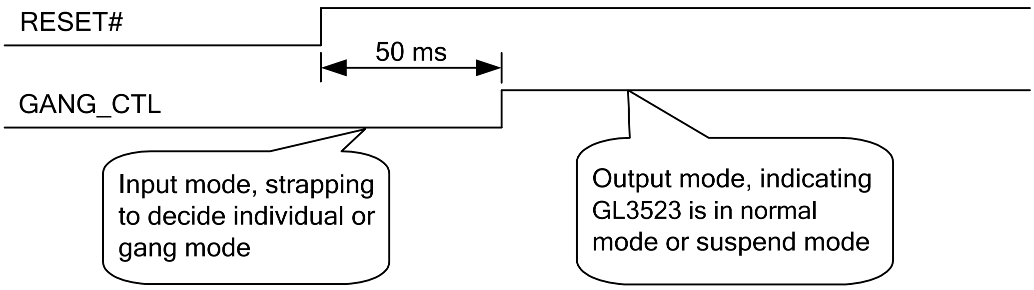


Figure 4.7 - Timing of PGANG Strapping

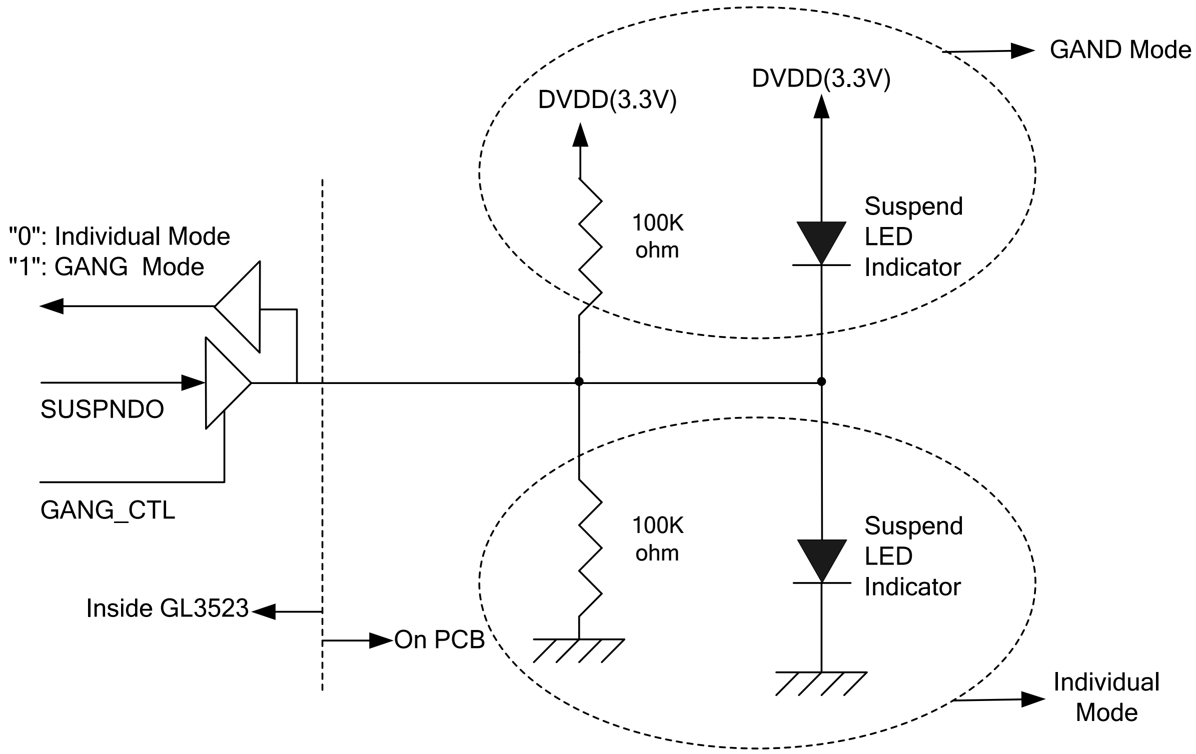


Figure 4.8 - GANG Mode Setting

4.4.3 SELF/BUS Power Setting

By setting PSELF, GL3523 can be configured as a bus-power or a self-power hub.

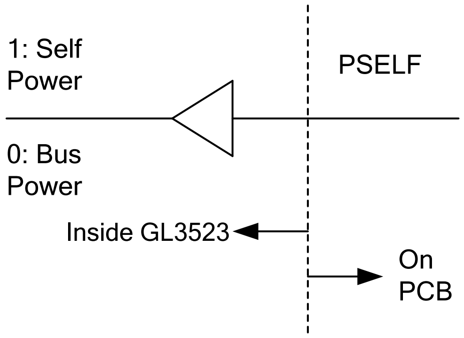


Figure 4.9 - SELF/BUS Power Setting

4.4.4 LED Connections

GL3523 controls the LED lighting according to the flow defined in Section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL3523. When GL3523 is globally suspended, GL3523 will turn off the LED to save power.

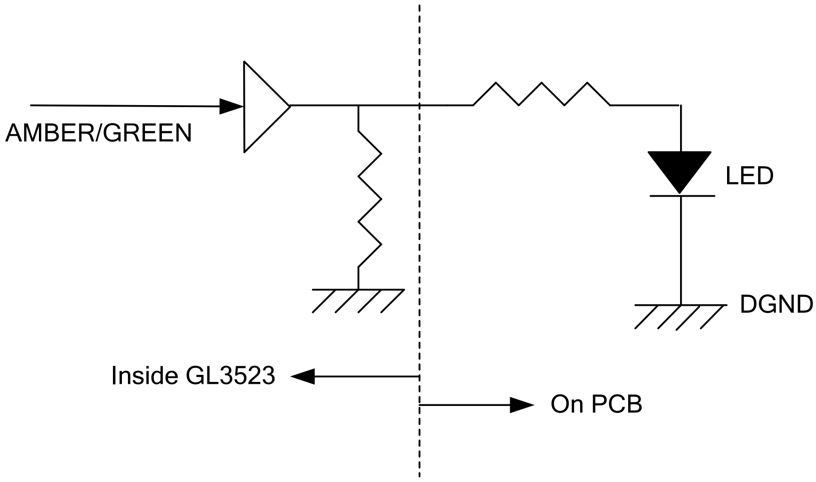


Figure 4.10 - LED Connection

4.4.5 Power Switch Enable Polarity

Both low/high-enabled power switches are supported. It is determined by jumper setting.
The power switch polarity will be configured by the state of pin AMBER2, as the following table:

Table 4.1 - Configuration by Power Switch Type

AMBER2	Power Switch Enable Polarity
0	Low-active
1	High-active

Note: When AMBER2=1, the external resistor of PWREN1~4 need pull down

4.4.6 Port Configuration

Each specific downstream port can be disabled individually by firmware, SMBus or vendor command, which extends the flexibility for PCB design and fits more applications.
In GL3523-S series of Hub, multiple upstream ports are also allowed for special applications. For further usage information, please contact Genesys FAE or sales team.

4.4.7 Non-removable Port Setting

For compound applications or embedded systems, downstream ports that always connect inside the system can be set as non-removable by firmware configuration, EEPROM, and pin strapping. Please refer to **Genesys USB3.1 Hub FW ISP Tool User Guide** for the detailed setting information.

4.4.8 SMBUS Mode (SMBUS Slave Address=0x25)

GL3523 enters SMBUS mode since Power-On occurs, and RESET# pin is asserted as well. After that, GL3523 will define OVCUR3J as SMC and OVCUR4J as SMD. GL3523 will exit the SMBUS mode since the RESET# pin is de-asserted. The more complicated settings such as PID, VID, power saving, port number, port non/removable, and downstream port electrical tuning can be configured by SMBUS.

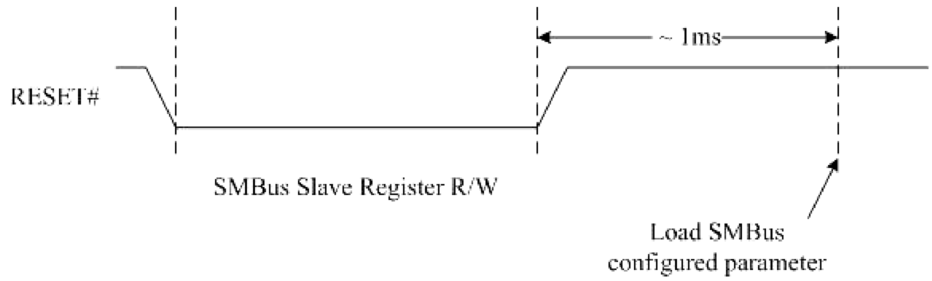


Figure 4.11 - SMBus Timing Diagram

CHAPTER 5 FAST CHARGING SUPPORT

5.1 Introduction to Battery Charging Specification Rev.1.2

The USB ports on personal computers are convenient places for portable devices to draw current for charging their batteries. This convenience has led to the creation of dedicated chargers that simply expose a USB standard-A receptacle. This allows portable devices to use the same USB cable to charge from either a PC or from a dedicated charger.

If a portable device is attached to a USB host or hub, then the USB 2.0 specification requires that after connecting, a portable device must draw less than:

- 2.5 mA average if the bus is suspended
- 100 mA maximum if bus is not suspended and not configured
- 500 mA maximum if bus is not suspended and configured for 500 mA

If a portable device is attached to a charging host or hub, it is allowed to draw a current up to 1.5A, regardless of suspend. In order for a portable device to determine how much current it is allowed to draw from an upstream USB port, the USB-IF Battery Charging specification defines the mechanisms that allow the portable device to distinguish between a USB standard host, hub or a USB charging host. Since portable devices can be attached to USB charging ports from various manufactures, it is important that all USB charging ports behave the same way. This specification also defines the requirements for a USB chargers and charging downstream ports.

5.2 Standard Downstream Port (SDP)

GL3523 complies with Battery Charging Specification rev1.2, which defines three charging ports: SDP, CDP and DCP. The SDP is a standard USB port which can transfer data and provide maximum 500mA current.

5.3 Charging Downstream Port (CDP)

GL3523 supports battery charging detection, turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP). GL3523 will make physical layer handshaking when a portable device that complies with BC rev1.2 attaches to its downstream port. After physical layer handshaking, a portable device is allowed to draw more current up to 1.5A.

Once the charging downstream port of GL3523 is enabled, it will monitor the V_{DP_SRC} on D+ line anytime. When a portable device, which is compliant with BC rev1.2, is attached to the downstream port, it will drive V_{DP_SRC} on D+ line to initiate the handshake with charging downstream port. GL3523 will response on its D- line by V_{DM_SRC} and keep in a certain period of time and voltage level. The portable device will accept this handshaking on its D- line in correct timing period and voltage level, and then turns off its V_{DP_SRC} on D+ line. GL3523 will recognize that charging negotiation is finished by counting time between the portable device turning on and off its V_{DP_SRC}. After that, the portable device can start to draw more current from VBUS to charge its battery more rapidly. It can draw current up to 1.5A.

If there is no response from D- line, the portable device will recognize that it is attached to a standard downstream port, not a charging port.

5.4 Dedicated Charging Port (DCP)

GL3523 also supports dedicated charging port, which is a downstream port on a device that outputs power through a USB connector, but it is not capable of enumerating a downstream device. With the adequate system circuit design, GL3523 will turn its downstream port from a standard downstream port (SDP) into dedicated charging port (DCP), i.e short the D+ line to the D- line, to let the portable device draws current up to 1.5A. Please refer to the **USB3.1 Hub Design Guide** document for the detailed information.

5.5 ACA-Dock

An ACA-Dock is a docking station that has one upstream port, and zero or more downstream ports. The upstream port can be attached to a portable device (PD), and is capable of sourcing ICDP to the PD, which means that the upstream port can charge and have data communication with the PD at the same time. Please refer to Battery Charging Spec v1.2 for more details.

5.6 Apple and Samsung Devices

GL3523 Hub not only supports BC1.2, but also supports fast-charging for Apple 1A/2.4A and Samsung Galaxy devices.

5.7 Charging Downstream Port Configuration

Fast-charging capability can be disabled/enabled by each specific downstream port. Please refer to the **Genesys USB3.1 Hub FW ISP Tool User Guide** document for the detailed setting information.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
VDDcore	1.2VPower Supply	-0.5	+1.32	V
V_{IN}	3.3V Input Voltage for digital I/O(EE_DO) pins*	-0.5	+5	V
Vincore	1.2V	-0.5	+1.32	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-60	+100	^oC
F_{OSC}	Frequency	25 MHz ± 0.03%		

*Please refer to the reference design schematic.

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
VDDcore	1.2V Power Supply	1.15	1.2	1.32	V
V_{IND}	Input Voltage for digital I/O pins	-0.5	3.3	3.6	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	3.3	3.6	V
T_A	Ambient Temperature	0	-	70	^oC
T_J	Absolute maximum junction temperature	0	-	125	^oC

6.3 DC Characteristics

6.3.1 DC Characteristics except USB Signals

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	1	V
V_{IH}	HIGH level input voltage	1.4	-	-	V
V_{TLH}	Schmitt trigger PAD*-LOW to HIGH threshold voltage	1.7	-	-	V
V_{THL}	Schmitt trigger PAD*- HIGH to LOW threshold voltage	-	-	0.7	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	μA
R_{DN}	Pad internal pull down resister	232	378	647	KΩ
R_{UP}	Pad internal pull up resister	276	435	718	KΩ

* Schmitt trigger pads are VBUS, RESET

6.3.2 USB 2.0 Interface DC Characteristics

GL3523 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to the specification for more information.

6.3.3 USB 3.1 Gen 1 Interface DC Characteristics

GL3523 conforms to DC characteristics for Universal Serial Bus 3.1 specification. Please refer to the specification for more information.

6.4 Power Consumption

GL3523 integrates 5V-to-3.3V and 5V-to-1.2V regulators. If supplying 5V power, internal regulators convert 5V to 3.3V and 1.2 V, and power consumed in 5V domain in the following table already includes 1.2V and 3.V power consumption and conversion loss. In other words, if using 5V as input power, 1.2V and 3.3V power can be ignored; if using external 1.2V and 3.3V power as input sources, the total power consumption will be the sum of 1.2V and 3.3V.

Number of Active USB 3.1 Ports	Using 5V power input		Using 1.2V and 3.3V power input				Unit
	5V		1.2V		3.3V		
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Chip Disabled (Standby)	880		0		40		µW
Reset	6		1.9		2		mW
Suspend	12.5		5		3.3		mW
0	140	-	16	-	79	-	mW
1	442	444	285	286	80	80	mW
2	563	564	389	391	80	80	mW
3	688	691	494	496	80	80	mW
4	821	825	599	600	80	80	mW

Number of Active USB 2.0 Ports	Using 5V power input		Using 1.2V and 3.3V power input				Unit
	5V		1.2V		3.3V		
	Config.	Read/ Write	Config.	Read/ Write	Config.	Read/ Write	
Chip Disabled (Standby)	880		0		40		µW
Reset	6		1.9		2		mW
Suspend	12.5		5		3.3		mW
0	140	-	16	-	79	-	mW
1	171	212	16	16	98	125	mW
2	201	273	16	16	117	164	mW
3	231	310	16	16	138	188	mW
4	261	342	16	16	158	210	mW

Note:

Test result represents silicon level operating current without considering additional power consumption contributed by external over-current protection circuit. The power consumption could be different depending on configurations.

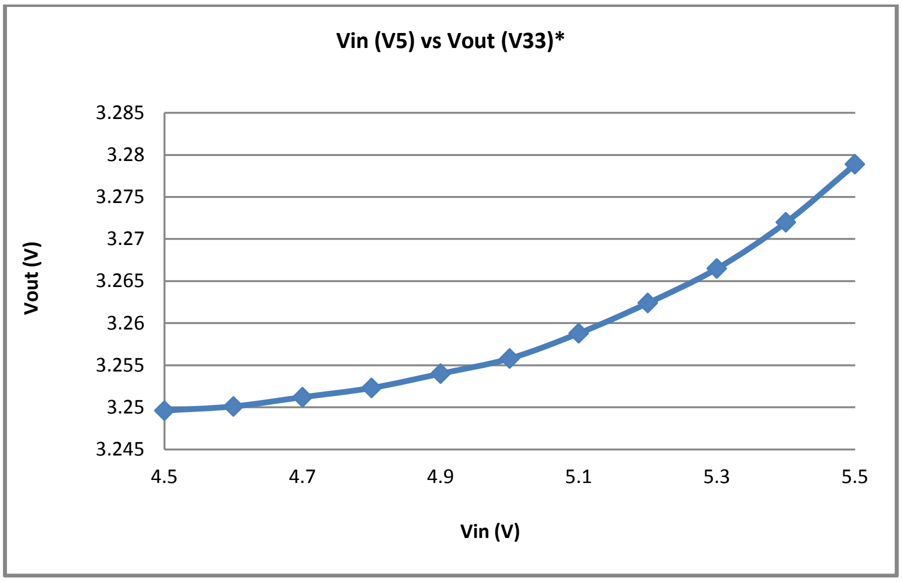
6.5 On-Chip Power Regulator

GL3523 requires 3.3V and 1.2V source power for normal operation of internal core logic and USB physical layer (PHY). There are two kinds of regulators integrated in GL3523; one is low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source; another one is DC-DC switching regulator converts 5V to 1.2 V. The 3.3V and 1.2V power output are guaranteed by internal voltage reference circuits to prevent unstable 5V power compromise USB data integrity. The regulators' maximum currents loading are 250mA (5-3.3V) and 0.8A (5-1.2V), which provide enough tolerance for normal GL3523 operation (below 100mA).

6.5.1 5V to 3.3V Regulator

5V to 3.3V On-chip Power Regulator features are described as follows.

- 5V to 3.3V low-drop power regulator
- 250mA maximum output driving capability
- Provide stable 3.3V output when Vin = 4.5V~5.5V
- 125uA maximum quiescent current (typical 80uA).



*Note: Measured environment: Ambient temperature = 25℃,
Current Loading = 250mA

Figure 6.1 - Vin(V5) vs Vout(V33)*

6.5.2 5V to 1.2V Regulator

5V to 1.2V DC-DC Switching Regulator features are described as follows.

- 5V to 1.2V DC-DC switching regulator
- 0.8A maximum output driving capability

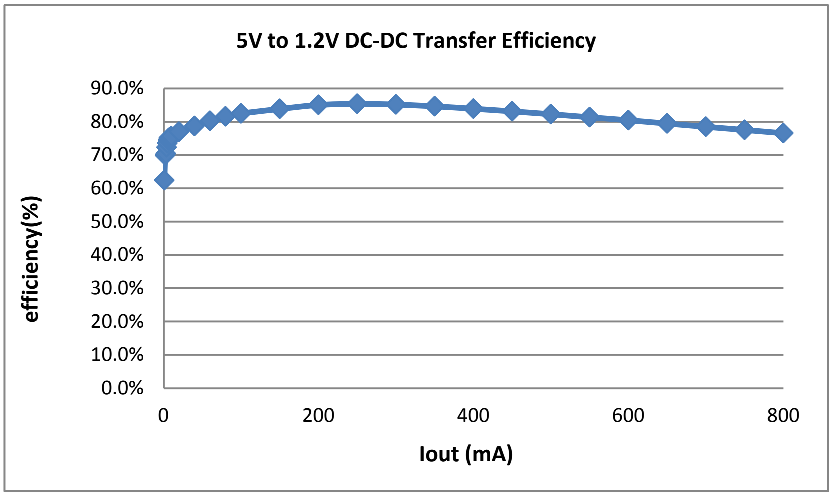


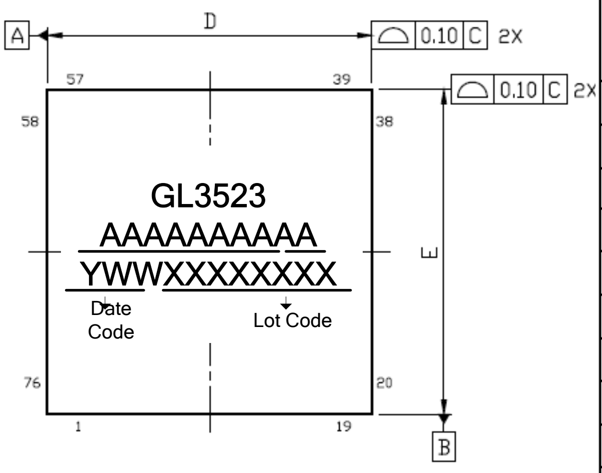
Figure 6.2 - Vin (V5) vs. Vout (V1.2)

6.6 External Clock

XOUT: 25MHz crystal oscillator output. It should be left open if an external clock source is used.

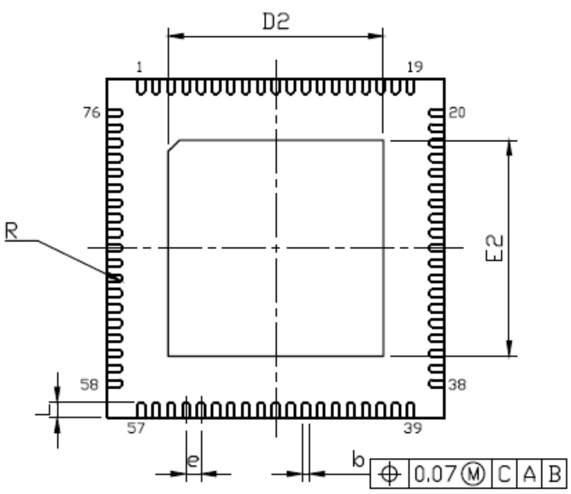
XIN: 25MHz crystal oscillator input. If an external 3.3V clock source is used, its frequency has to be 25MHz +/-300ppm with a peak-to-peak jitter less than 50ps..

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.80 (31.5)	0.90 (35.4)
A1	0.00 (0.00)	0.035 (1.4)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.2 (7.9)	0.25 (9.8)
D	9.00 (354.3) BSC		
D2	5.10 (200.8)	5.75 (226.4)	6.40 (252)
E	9.00 (354.3) BSC		
E2	5.10 (200.8)	5.75 (226.4)	6.40 (252)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)
R	0.075 (3.0)	-	-

Note: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.



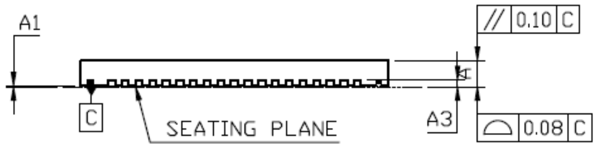
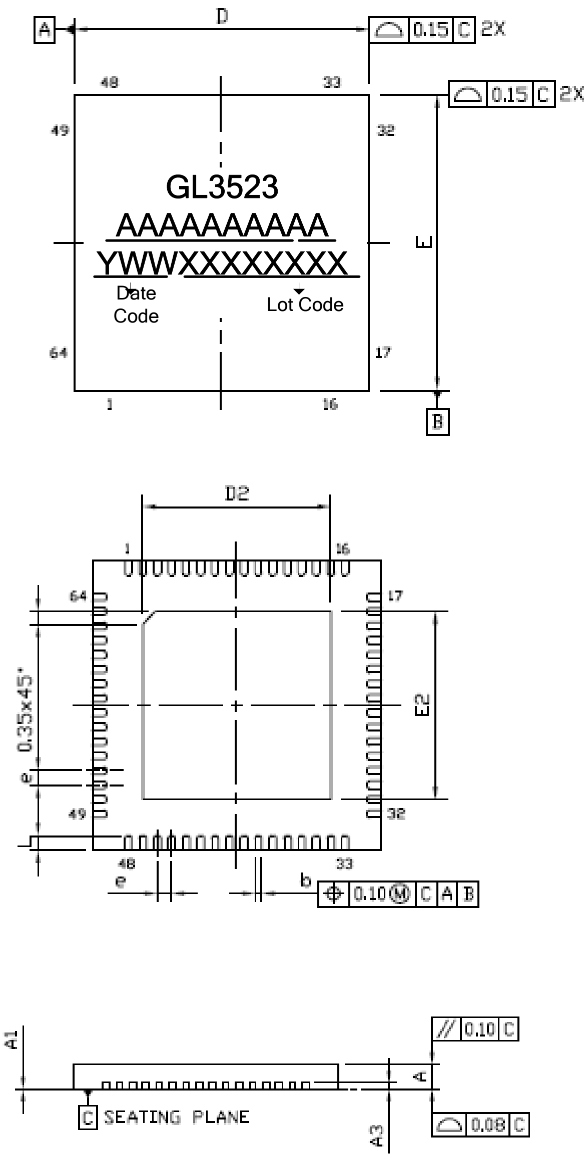


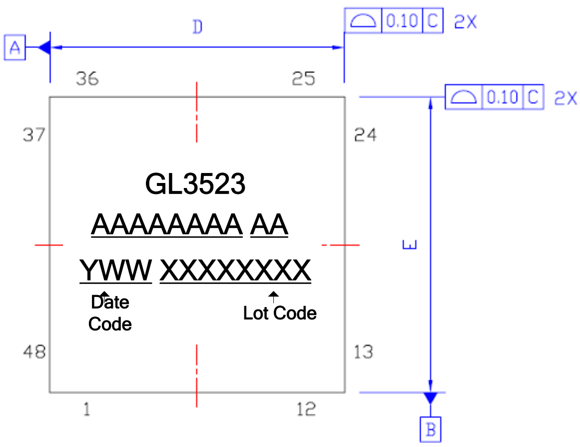
Figure 7.1 - QFN76 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	8.00 (315.0) BSC		
D2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
E	8.00 (315.0) BSC		
E2	4.10 (161.4)	5.35 (210.6)	6.60 (259.8)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.2 - QFN64 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.13 (5.1)	0.18 (7.1)	0.25 (9.8)
D	6.00 (236.2) BSC		
D2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
E	6.00 (236.2) BSC		
E2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

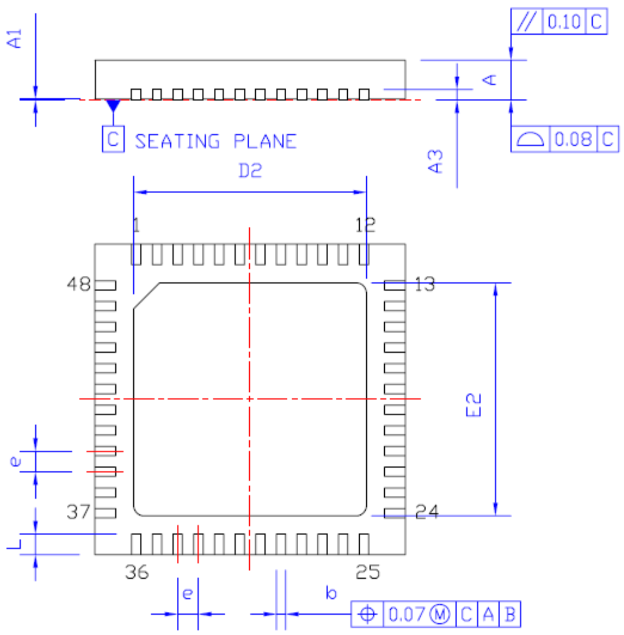
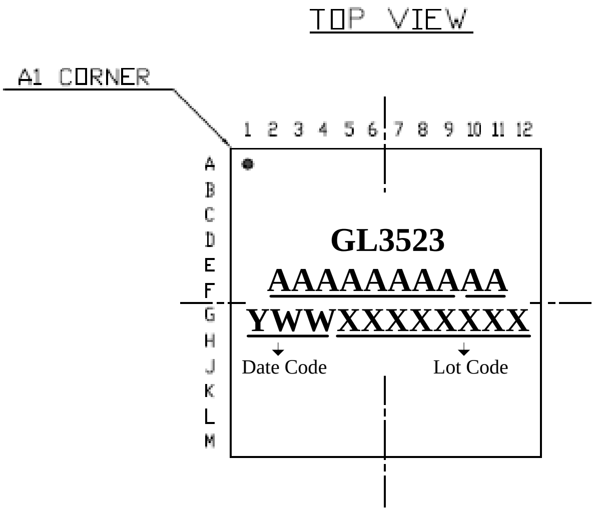
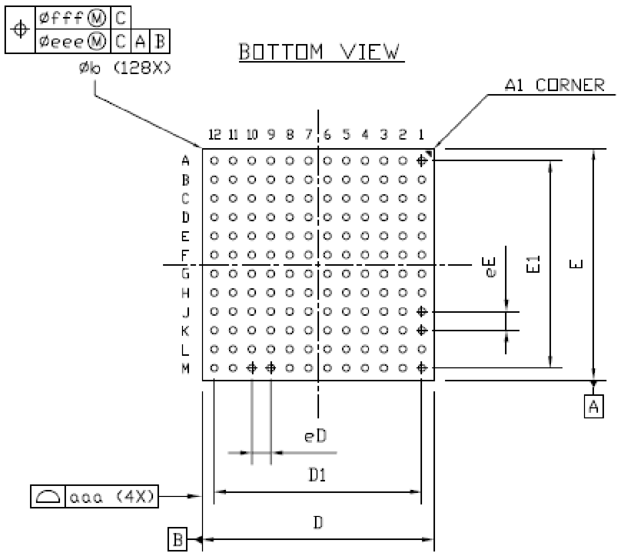


Figure 7.3 - QFN48 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.00 (39.4)
A1	0.12 (4.7)	---	0.20 (7.9)
A2	0.26 (10.2) REF		
A3	0.45 (17.7) REF		
b	0.20 (7.9)	0.25 (9.8)	0.30 (11.8)
D	8.00 (315.0) BSC		
E	8.00 (315.0) BSC		
eD	0.65 (25.6) BSC		
D1	7.15 (281.5) BSC		
eE	0.65 (25.6) BSC		
E1	7.15 (281.5) BSC		
aaa	0.10 (3.9)		
bbb	0.10 (3.9)		
ddd	0.08 (3.1)		
eee	0.15 (5.9)		
fff	0.08 (3.1)		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.



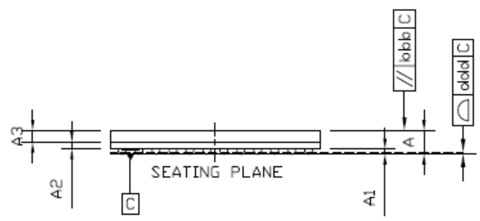
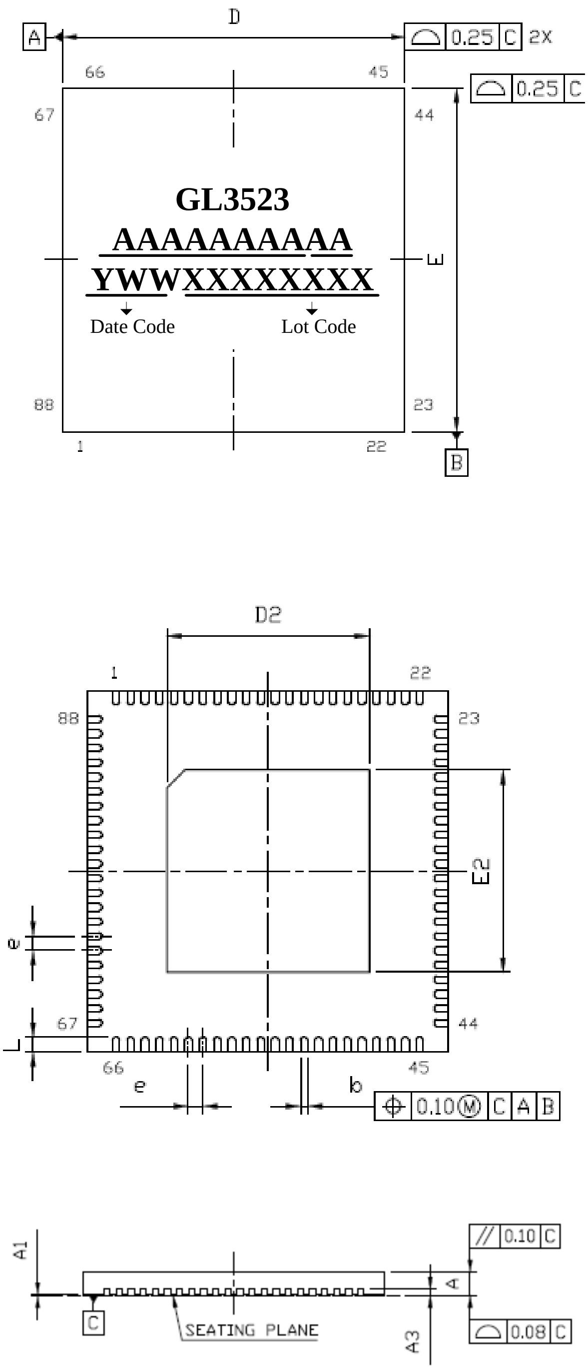


Figure 7.4 - VFBGA144 Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
D	10.00 (393.7) BSC		
D2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
E	10.00 (393.7) BSC		
E2	5.45 (214.5)	5.60 (220.5)	5.75 (226.4)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.5 - QFN88 Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Material	Version	Status
GL3523-OTY30	QFN 76	Green Package	30	Available
GL3523-OSY30	QFN 64	Green Package	30	Available
GL3523-ONY30	QFN 48	Green Package	30	Available
GL3523-VBYS3	VFBGA144	Green Package	S3	Available
GL3523-OV2S3	QFN88 (2C3A)	Green Package	S3	Available
GL3523-OV1S3	QFN88 (1C4A)	Green Package	S3	Available
GL3523-OTYS3	QFN76	Green Package	S3	Available
GL3523-OSYS3	QFN64	Green Package	S3	Available