7-inch LCD Touch Screen Module AN970

User Manual

ALINX

Version Record

Version	Date	Release By	Description
Rev 1.0	2022-04-30	Rachel Zhou	First Release

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Part 1: 7-inch LCD Touch Screen Module Description

ALINX 7-inch LCD screen module (AN970) is Tianma's 7-inch TFT LCD screen, the model of the LCD screen is TM070RDH13, and the touch chip of the touch screen is Goodix GT911 chip.

The AN970 LCD screen module consists of TFT LCD screen, touch screen and driver board. The actual photos of AN970 are as follows:

Figure 1-1: AN970 Module Product Photo

Part 1.1: AN970 LCD Touch Screen Module Detail Parameter

7”LCD display LCD Touch Screen module detail parameter listed:

- 7”LCD display module size dimension: detailed as Figure 1-2
- LCD screen size: 7.0 inches (diagonal)
- Display pixels: 800 (horizontal) x 480 (vertical)

- Color depth: 16.7M colors (RGB 24-bit color)
- Power and power consumption: single power supply 5V, power consumption is 1.8 watts

Figure 1-3: AN970 Module Form Factors

Part 1.2: AN970 LCD Drive Timing

Horizontal Input Timing

The LCD screen display mode starts from the top left corner of the screen and is displayed point by point from left to right. Each time a line is displayed, it returns to the start position of the next line on the left side of the screen. During this time, the rows need to be blanked, and at the end of each line, the line sync signal is used for synchronization. There are two ways to drive the LCD, one is HV mode and the other is DE mode, both of which can drive the LCD screen, and the data is sampled on the rising edge of DCLK.

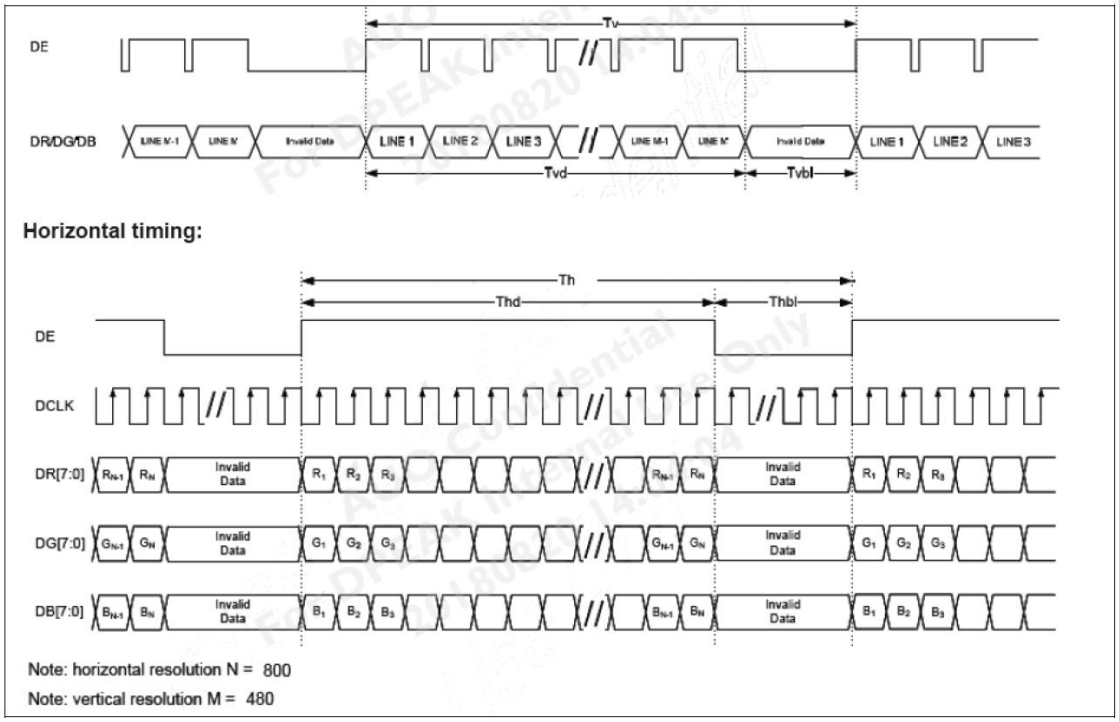

Figure 1-4: Horizontal Input Timing

b. Input timing Setting (DE Mode only)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remark
DCLK frequency	F_{DCLK}	30.3	33.26	37.8	MHz	
Hsync period (= Thd + Thbl)	Th	1000	1056	1112	T_{DCLK}	Note 1,2
Active Area	Thd	--	800	--	T_{DCLK}	
Horizontal blanking (= Thf+ The)	Thbl	200	256	312	T_{DCLK}	
Vsync period (= Tvd + Tvbl)	Tv	517	525	532	Th	
Active lines	Tvd	--	480	--	Th	
Vertical blanking (=Tvf + Tve)	Tvbl	37	45	52	Th	

Table 1-1: The Parameters of Horizontal Input Timing

Part 1.3: Touch Screen Drive Timing

For the driver of the touch screen, please refer to the "**GT911 编程指南文件 .pdf** (GT911 Programming Guide File.pdf)" document in the datasheet directory. Now the routine of touch screen is only applicable to ALINX ZYNQ7000 series development board and MPSOC development board.

Part 2: Hardware Connection

40-pin 0.1”spacing female header P4, connect directly to the expansion port of the development board with a 40-pin female header, so that the connection is simple and reliable.

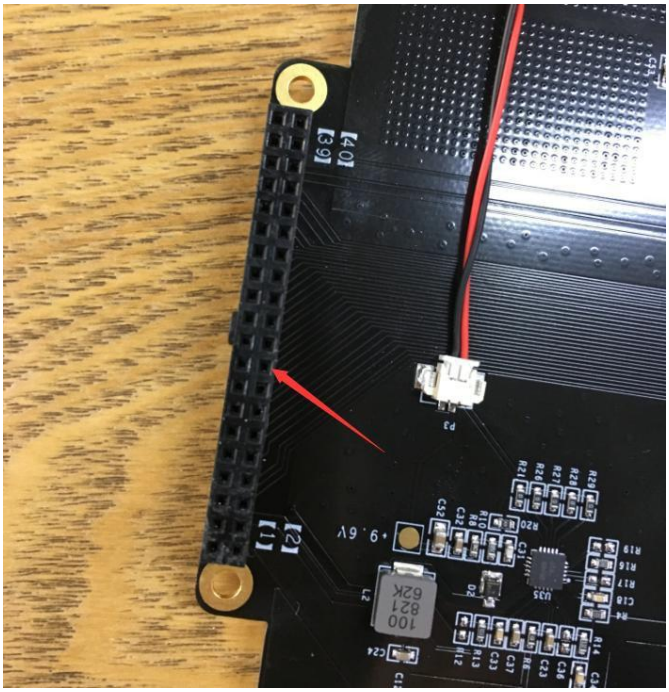

Figure 2-1: The 7-inch LCD Touch Screen Module Connection Interfaces

40-pin female header connection

The signal definition of the female header pin is compatible with the 40-pin expansion port on the ALINX FPGA development board, and the user can directly insert it into the FPGA development board for use (the gap is aligned). The following is a schematic diagram of the hardware connection between the ax7020 development board and the 7-inch touch screen:

AN970 LCD Module Connected to the J11 expansion port of the FPGA Development Board.
Download the programs, and there will be the color bar in the LCD Module

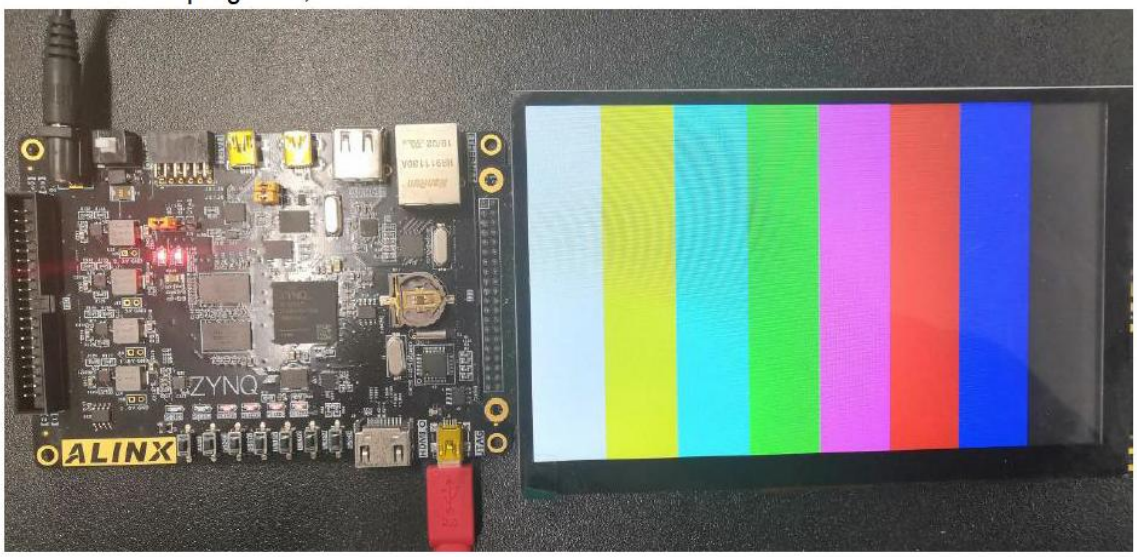

Figure 2-2: Hardware connection

The signal definition of the 40-pin 0.1”spacing female headers on the 7-inch LCD touch screen module is shown in the figure 2-3 and Table 2-1

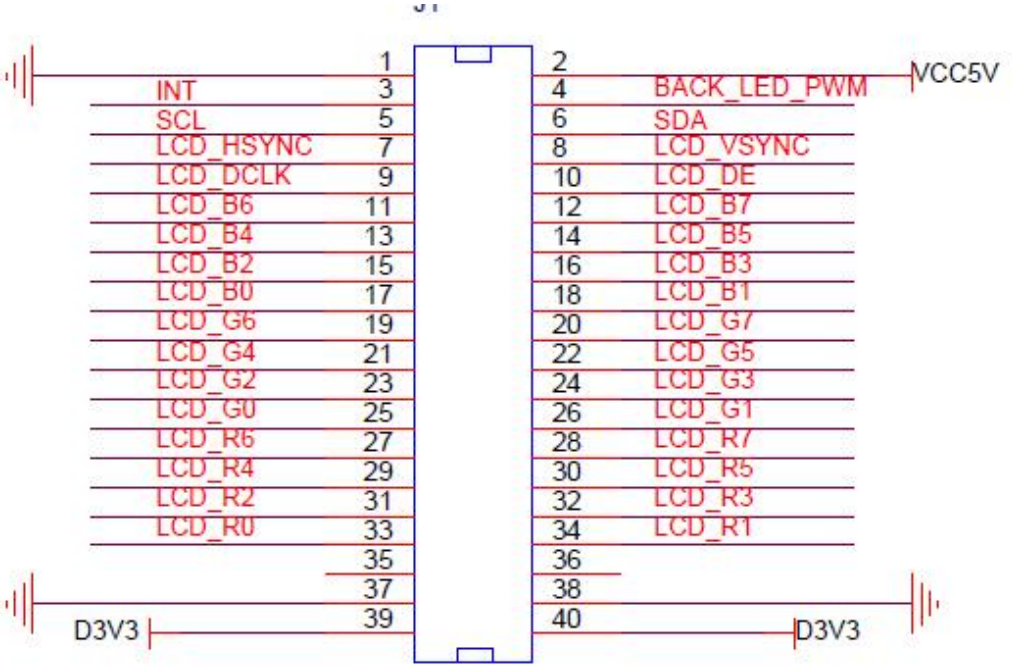

Figure 2-3: 40-pin female headers on the LCD Module

Pin Name	Pin of P4	Description	Pin Name	Pin of P4	Description
GND	Pin1	Reference Ground	VCC5V	Pin2	5V Power Input
INIT	Pin3	Screen interrupt	BACK_LED_PWM	Pin4	Back LCD PWM Control
SCL	Pin5	Screen I2C Clock	SDA	Pin6	Touch I2C Data
LCD_HSYNC	Pin7	Horizontal Synchronize	LCD_VSYNC	Pin8	Vertical Synchronize
LCD_DCLK	Pin9	Pixel Clock	LCD_DE	Pin10	Date Enable
LCD_B6	Pin11	Bit 6 of blue data	LCD_B7	Pin12	Bit 7 of blue data
LCD_B4	Pin13	Bit 4 of blue data	LCD_B5	Pin14	Bit 5 of blue data
LCD_B2	Pin15	Bit 2 of blue data	LCD_B3	Pin16	Bit 3 of blue data
LCD_B0	Pin17	Bit 0 of blue data	LCD_B1	Pin18	Bit 1 of blue data
LCD_G6	Pin19	Bit6 of green data	LCD_G7	Pin20	Bit 7 of green data
LCD_G4	Pin21	Bit4 of green data	LCD_G5	Pin22	Bit 5 of green data
LCD_G2	Pin23	Bit2 of green data	LCD_G3	Pin24	Bit 3 of green data
LCD_G0	Pin25	Bit0 of green data	LCD_G1	Pin26	Bit 1 of green data
LCD_R6	Pin27	Bit 6 of red data	LCD_R7	Pin28	Bit 7 of red data
LCD_R4	Pin29	Bit 4 of red data	LCD_R5	Pin30	Bit 5 of red data
LCD_R2	Pin31	Bit 2 of red data	LCD_R3	Pin32	Bit 3 of red data
LCD_R0	Pin33	Bit 0 of red data	LCD_R1	Pin34	Bit 1 of red data
--	--	--	--	--	--
GND	Pin37	Reference Ground	GND	Pin38	Reference Ground
D3V3	Pin39	3.3V(Reserved）	D3V3	Pin40	3.3V(Reserved）

Table 2-1: Signal Definition of the 40-pin female header

Part 3: 7-inch LCD Screen Display Experiment

For specific demos, refer to the projects in the ZYNQ FPGA development board or MPSOC FPGA development board documentation.

Experiment 1: LCD displays color bars and character images:

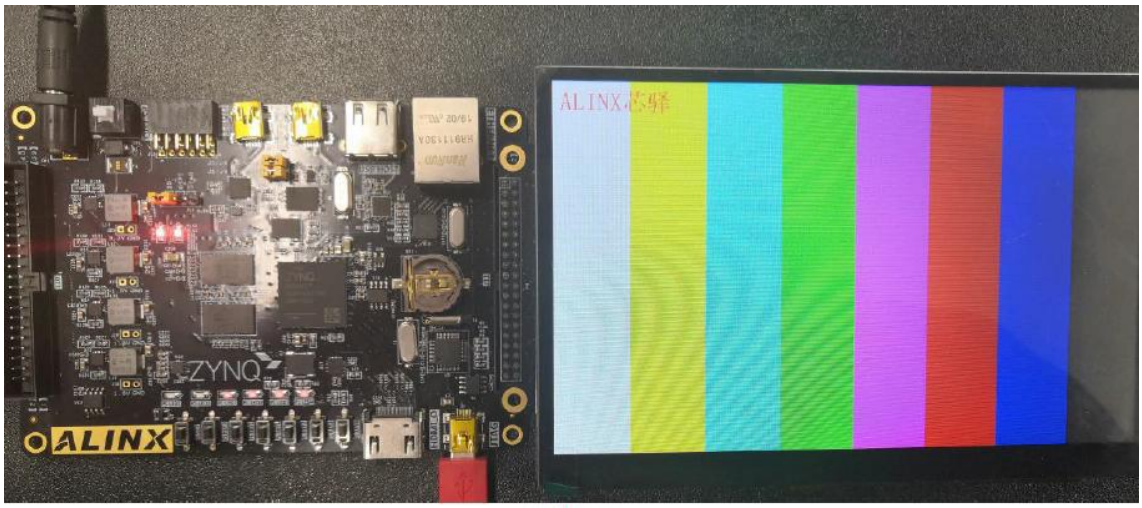

Figure 3-1: Character display

Experiment 2: Picture Display

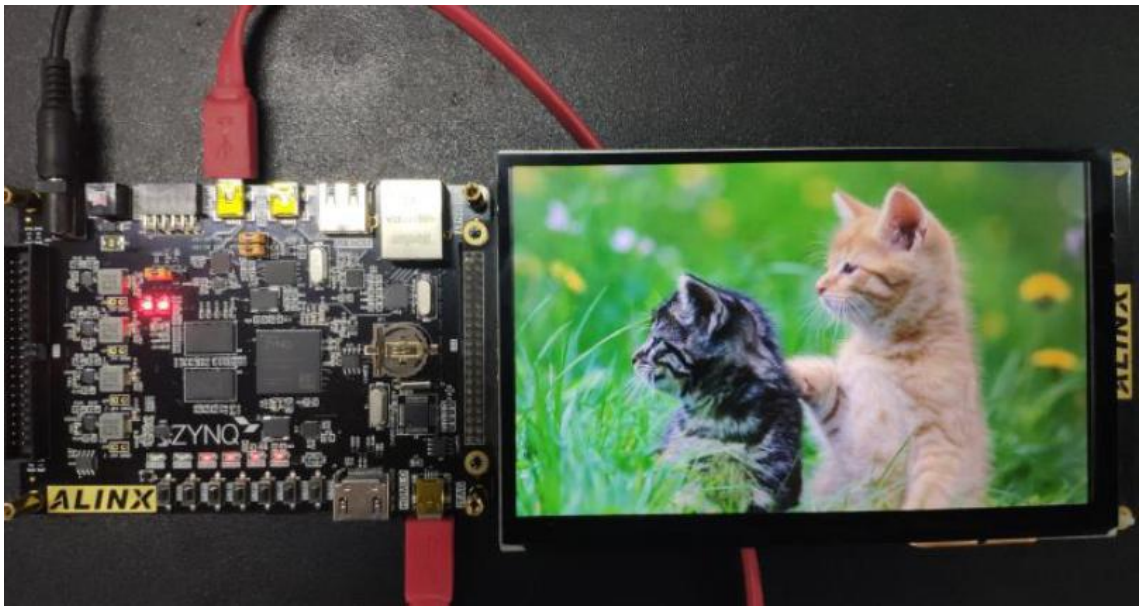

Figure 3-2: Picture display

Experiment 3: Touch Display

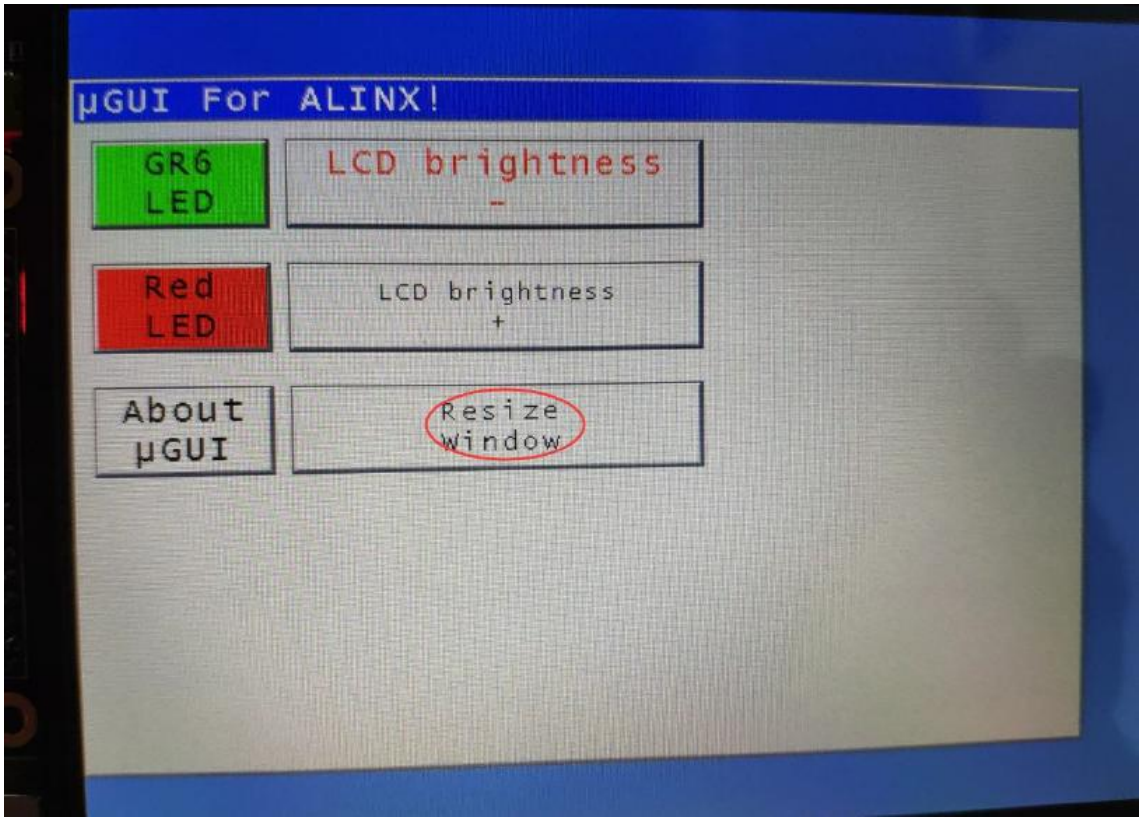

Figure 3-3: touch screen display