High Speed AD/DA Module AN108 User Manual

ALINX

Version Record

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Rev 1.3	2022-04-30	Rachel Zhou	First Release

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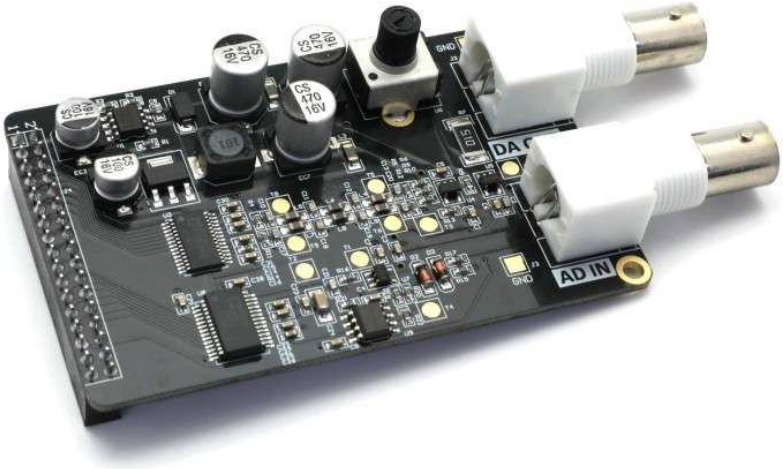

Figure 1-1: AN108 module product photo (front side)

Part 2 Hardware Block Diagram

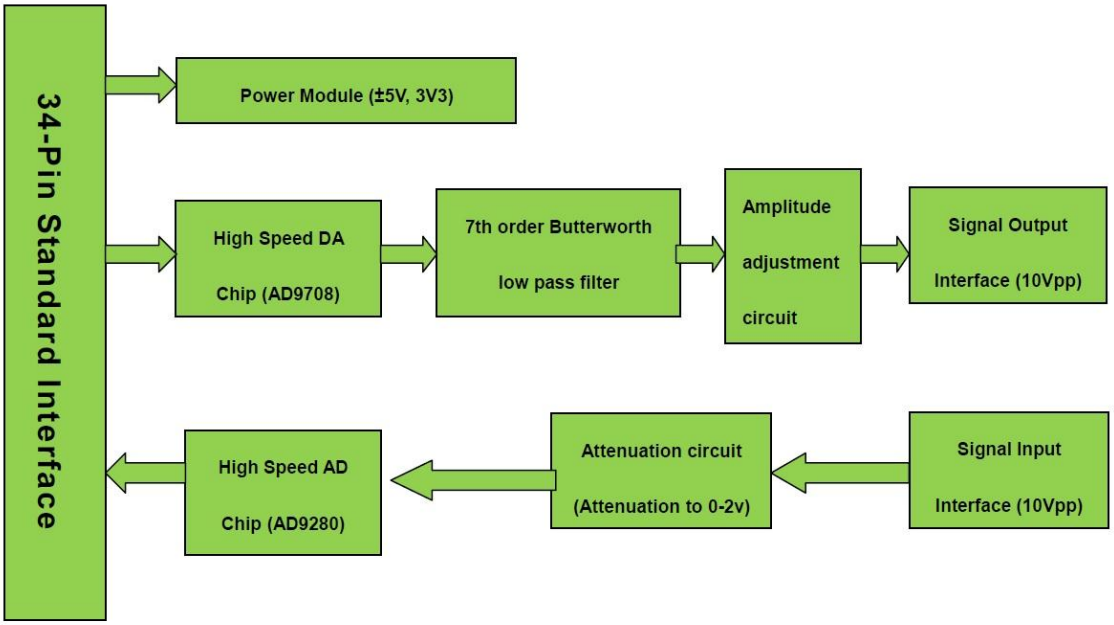

Figure 2-1: AN108 Module Hardware Block Diagram

Part 3: Digital to Analog Conversion Circuit

As shown in Figure 2-1 the hardware block diagram, the DA circuit consists of a high-speed DA chip, a 7th-order Butterworth low-pass filter, an amplitude adjustment circuit, and a signal output interface.

The high-speed DA chip we use is the AD9708 from AD. The AD9708 is a 8-bit, 125MSPS DA conversion chip with a built-in 1.2V reference and differential current output. Figure 3-1 is the functional block diagram of chip AD9708.

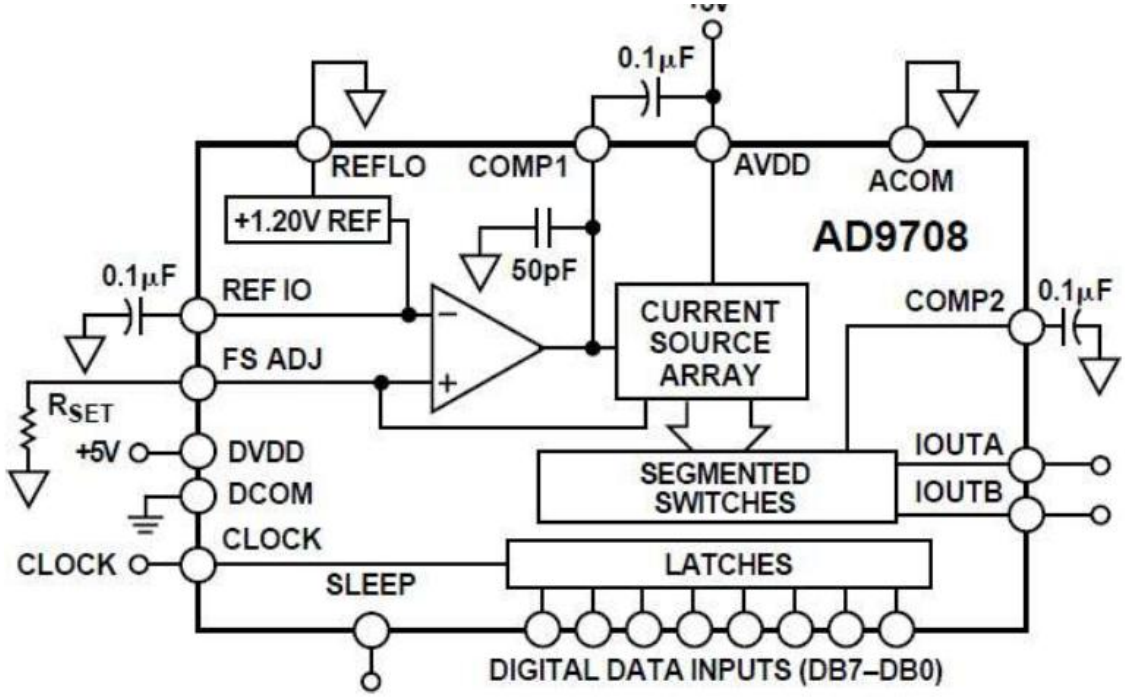

Figure 3-1: The Functional Block Diagram of Chip AD9708

After the differential output of the AD9708 chip, in order to prevent noise interference, a 7th-order Butterworth low-pass filter is connected to the circuit with a bandwidth of 40MHz. The frequency response is shown in the figure 3-2 below:

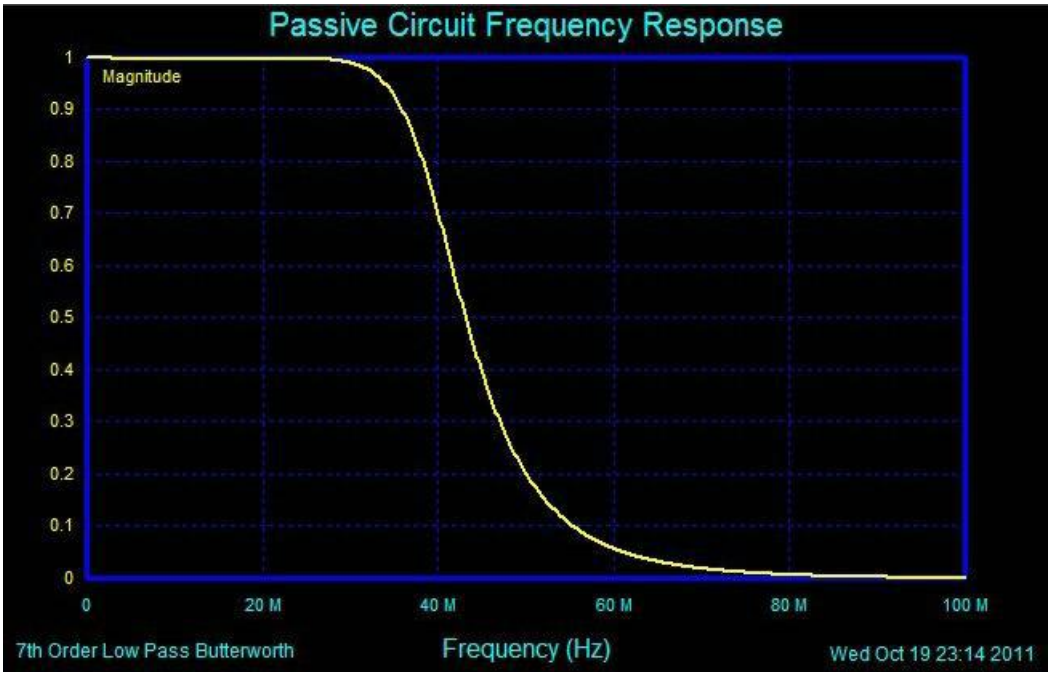

Figure 3-2: Passive Circuit Frequency Response

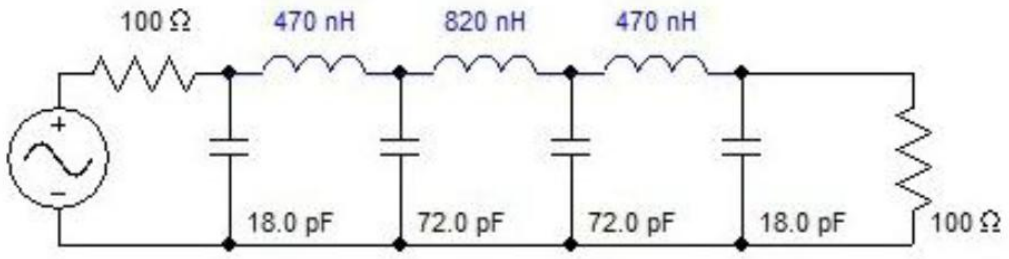

Figure 3-3: 7th-order Butterworth low-pass filter parameter

After the filter, we used two high-performance 145MHz bandwidth op amp AD8056 to achieve differential convert to single-ended, amplitude adjustment and other functions, so that the overall circuit performance has been maximized. The amplitude is adjusted using a 5K potentiometer and the final output range is -5V to 5V (10Vpp).

Note: Since the accuracy of the potentiometer is not very accurate, the final output has a certain error. It is possible that the waveform amplitude cannot reach 10Vpp, and there may be problems such as waveform clipping. These are normal conditions

Part4: Waveform Display

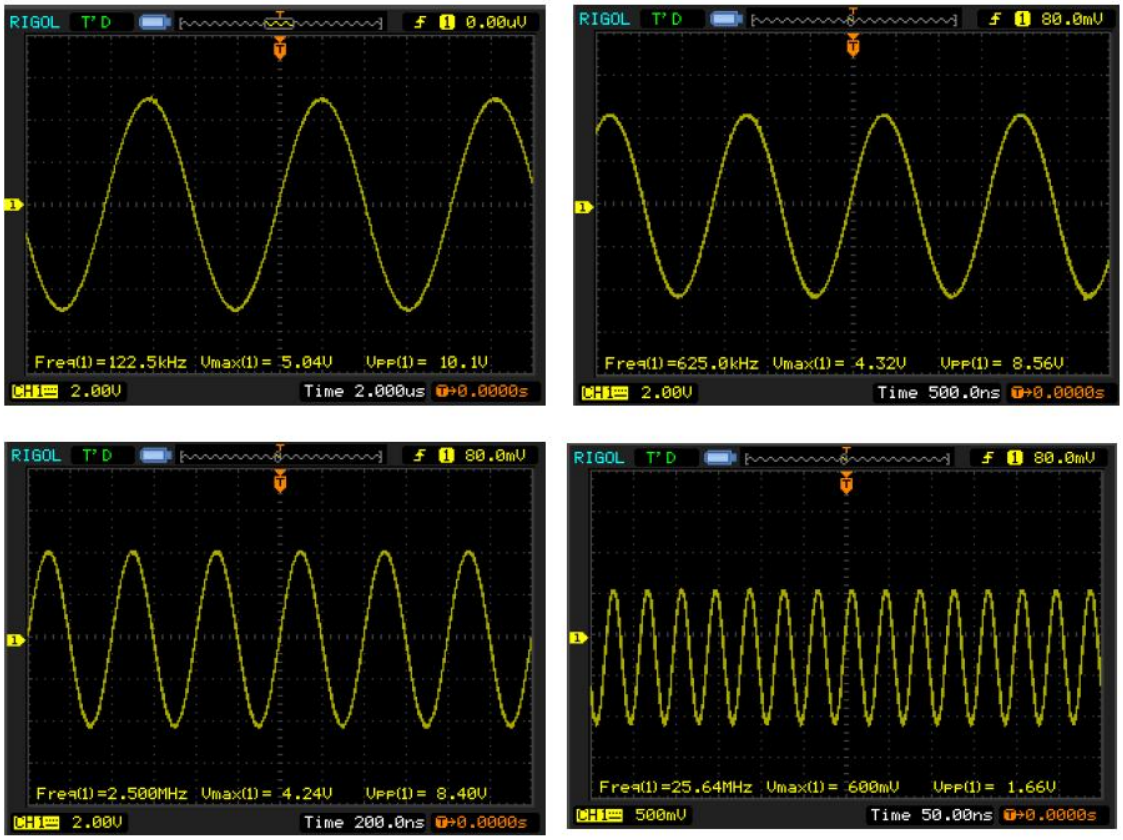

Figure 4-1: The Waveform Display

Part 5: Analog to Digital Conversion Circuit

As shown in Figure 2-1 the hardware block diagram, the AD circuit consists of a high speed AD chip, an attenuation circuit, and a signal input interface.

The high-speed AD chip used in the high speed AD/DA module AN108 is an 8-bit, maximum sampling rate of 32MSPS, ADMS280 chip of AD. Figure 5-1 is the functional block diagram of chip ADMS280.

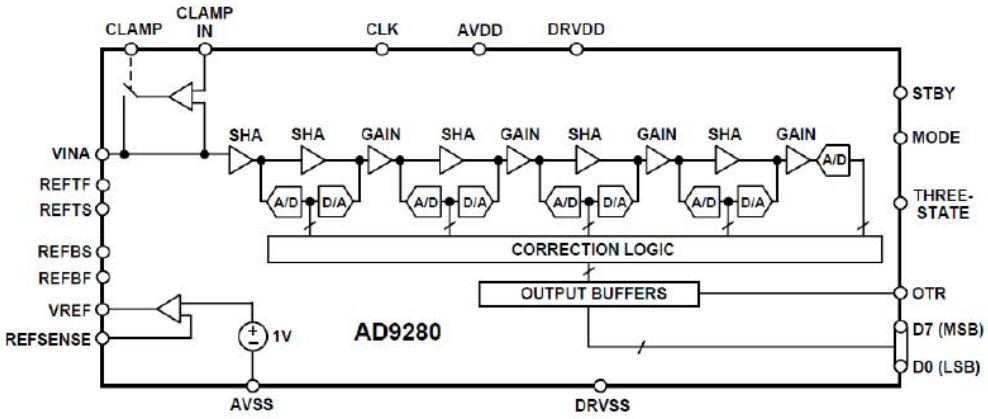

Figure 5-1: The Functional Block Diagram of Chip ADMS280

According to the configuration shown in figure 5-2 below, we set the AD voltage input range to: 0V~2V.

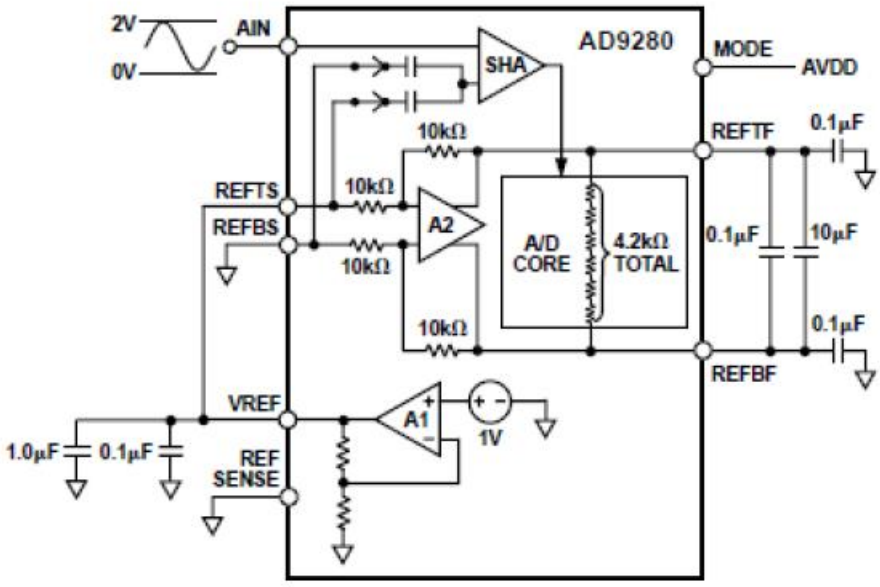

Figure 5-2: Set the AD voltage input range to: 0V~2V

Before the signal enters the AD chip, an attenuation circuit is constructed with a piece of AD8056 chip. The input range of the interface is -5V~+5V (10Vpp). After attenuation, the input range meets the input range of the AD chip (0~2V). The conversion formula is as follows:

$$V_{AD} = \frac{1}{5}V_{IN} + 1$$

When the input signal Vin=5(V), the signal input to AD Vad=2(V);

When the input signal Vin=-5(V), the signal input to AD Vad=0(V);

Part 6: SignalTap II Waveform

The waveform in Figure 6-1 below is the data waveform acquired with the tool SignalTap II in the Quartus II software.

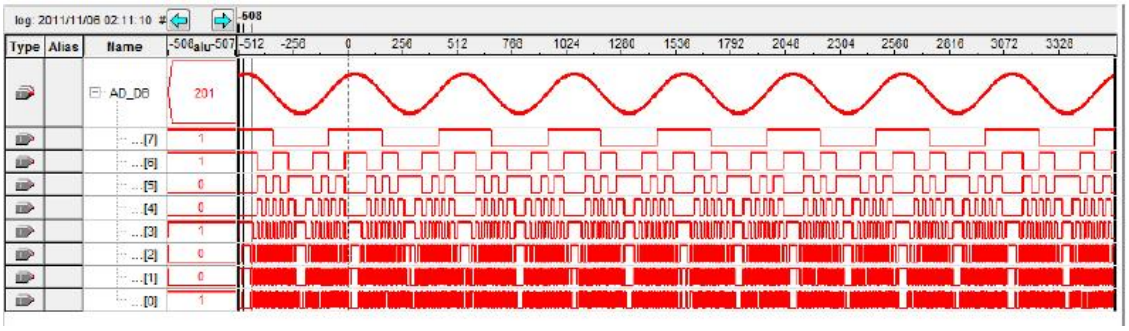

Figure 6-1: The Data Waveform Acquired with the Tool SignalTap II

Part 7: Interface definition

(J4 in the schematic diagram, the square pin the PCB labeled is pin 1)

Pin	Pin Name	Description	Pin	Pin Name	Description
1	DCOM	Ground	2	VCC	+5V
3			4		
5	DACLK	DA Clock Line	6	DADB7	DA Data Line
7	DADB6	DA Data Line	8	DADB5	DA Data Line

9	DADB4	DA Data Line	10	DADB3	DA Data Line
11	DADB2	DA Data Line	12	DADB1	DA Data Line
13	DADB0	DA Data Line	14		
15			16		
17			18		
19			20		
21	ADDB0	AD Data Line	22	ADDB1	AD Data Line
23	ADDB2	AD Data Line	24	ADDB3	AD Data Line
25	ADDB4	AD Data Line	26	ADDB5	AD Data Line
27	ADDB6	AD Data Line	28	ADDB7	AD Data Line
29	ADCLK	AD Clock Line	30		
31			32		
33			34		

Part 8: DA Experiment Steps

1) First, connect the high speed AD/DA module AN108 to the 34-pin standard expansion port of the ALINX sereis FPGA development board. (in case of power off)
2) When doing DA experiments, you need an oscilloscope to match the AD output port (near potentiometer BNC interface J2) is connected to the oscilloscope interface via the cable provided
3) Download the program to the FPGA using the Quartus II software (the test

program provided)

4) Adjust the oscilloscope to display the full waveform correctly.
5) Manually adjust the amplitude of the waveform with a potentiometer (U6)

Part 9: AD Experiment Steps

1) First, connect the high speed AD/DA module AN108 to the 34-pin standard expansion port of the ALINX sereis FPGA development board. (in case of power off)
2) This experiment requires the cooperation of the DA experiment, which means that we need to pass the DA output signal to the AD input port. Of course, if you have a signal source, it is better. Use the cable provided to connect the output interface of the signal source to the AD input interface (J3) (Note: AD port input range: -5V~+5V)
3) Download the program to the FPGA using the Quartus II software (the test program provided)
4) Real-time data collection with SignalTap II