

HW-Z1-ZCU106 Evaluation Board

(XCZU7EV-2FFVC1156)

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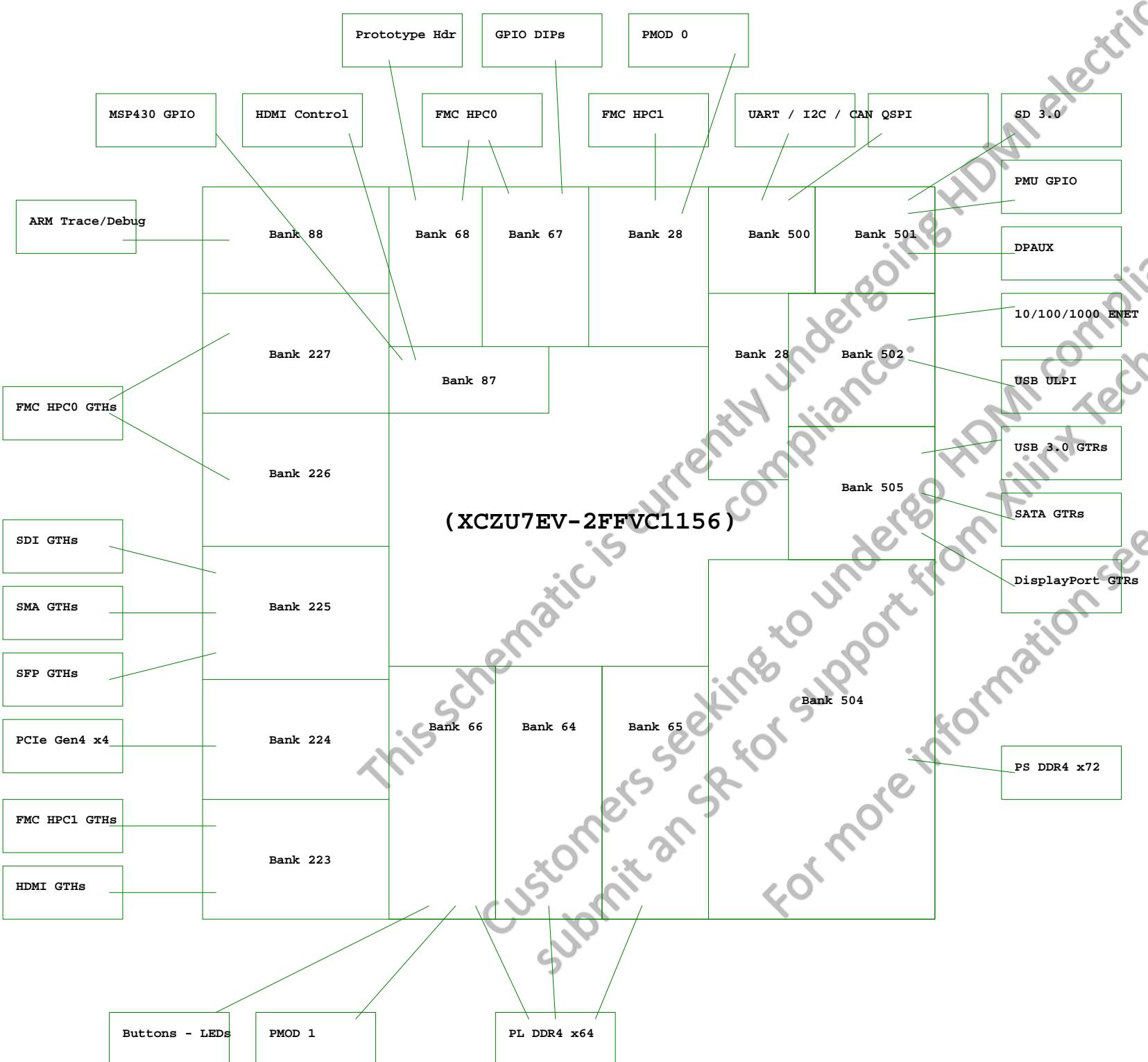
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		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
TITLE: Title Page SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		DATE: 01/08/2018:10:16
SHEET SIZE: B		VER: 1.0 REV: 01
SHEET	1 OF 95	DRAWN BY: BF



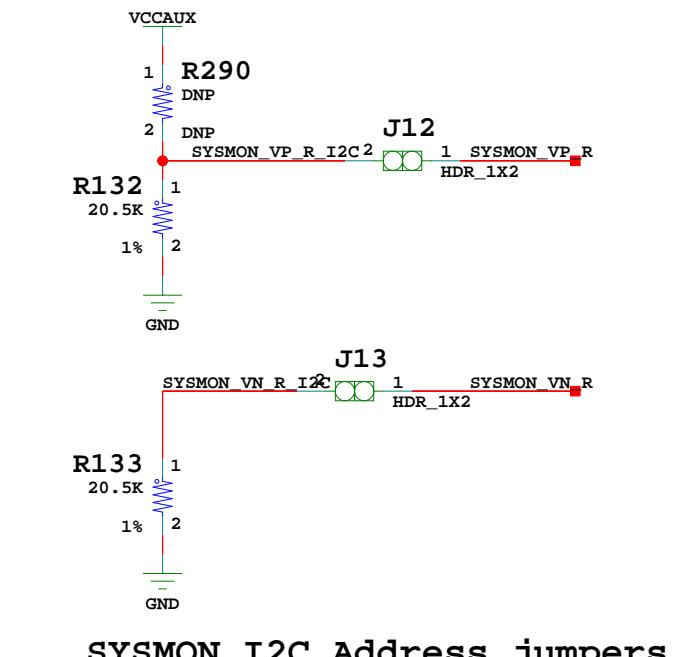
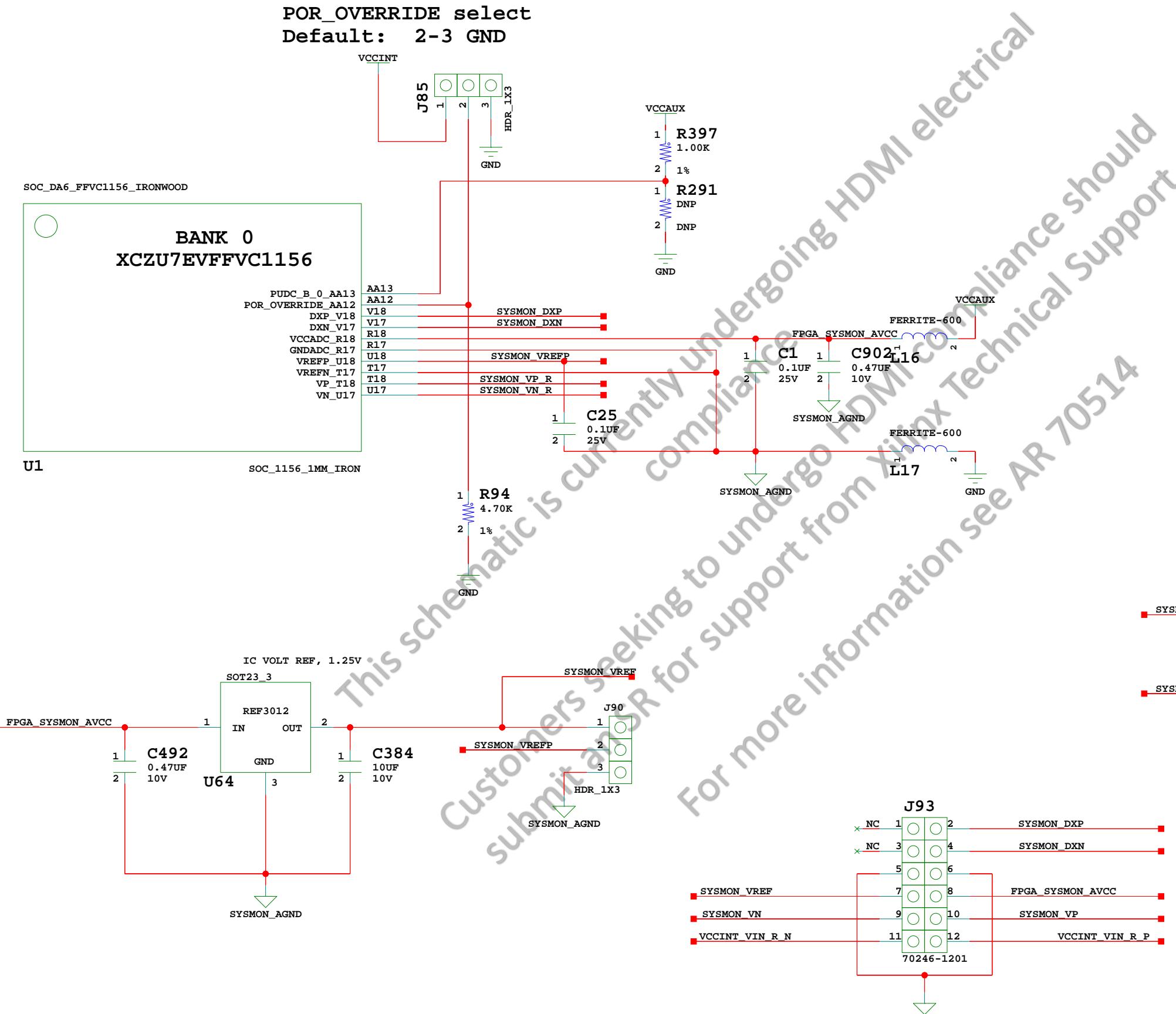
This schematic is currently undergoing HDMI compliance testing by Xilinx Technical Support.
Customers seeking to support from Xilinx Technical Support should submit an SR for more information see AR 70514



TITLE: Block Diagram
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

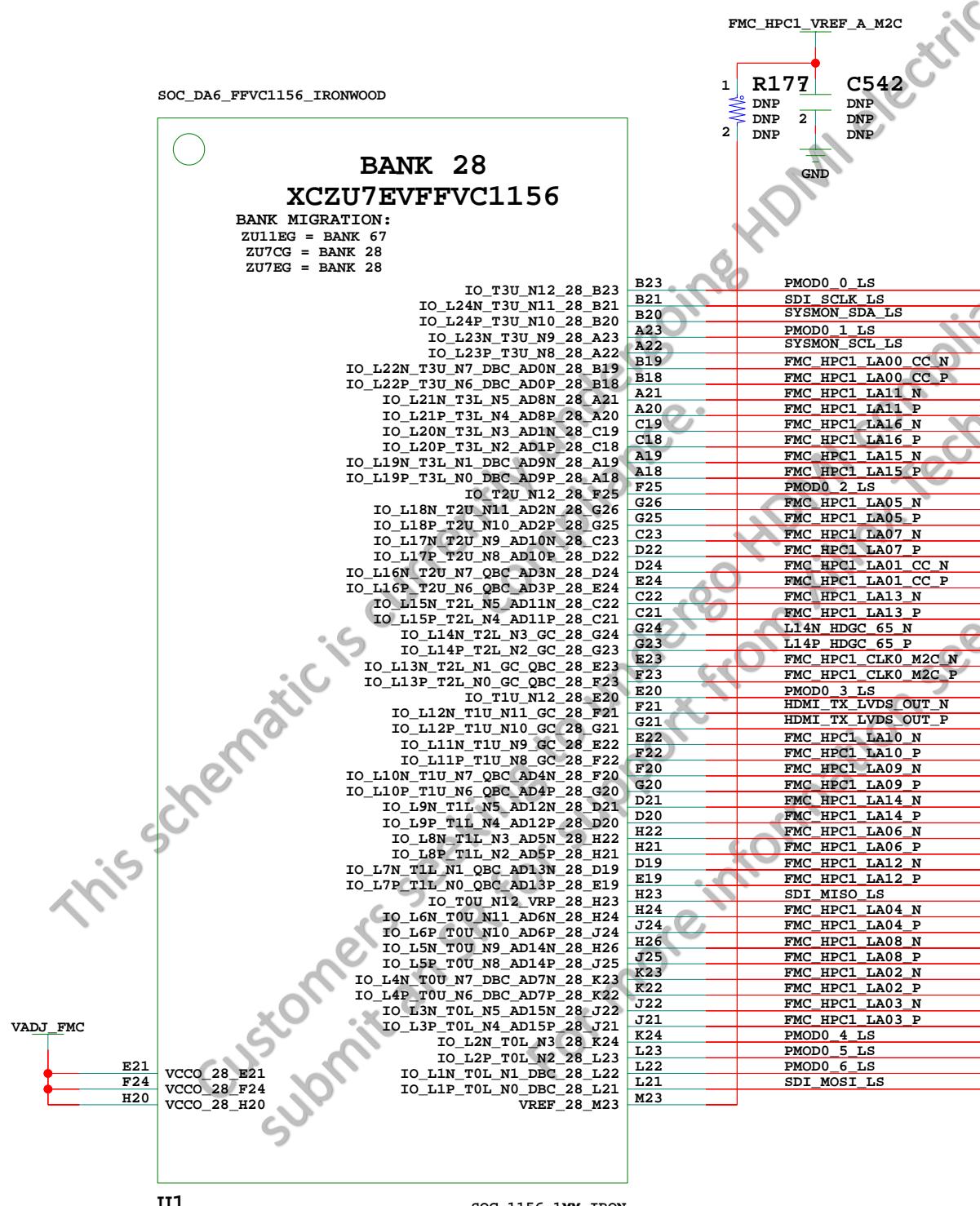
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PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 2 OF 95	DRAWN BY: BF



Zynq Bank 0

TITLE: Zynq Bank 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16		VER: 1.0
SHEET SIZE: B		REV: 01
SHEET 3 OF 95		DRAWN BY: BF

**Zynq Banks 28**

TITLE: Zynq Banks 28
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

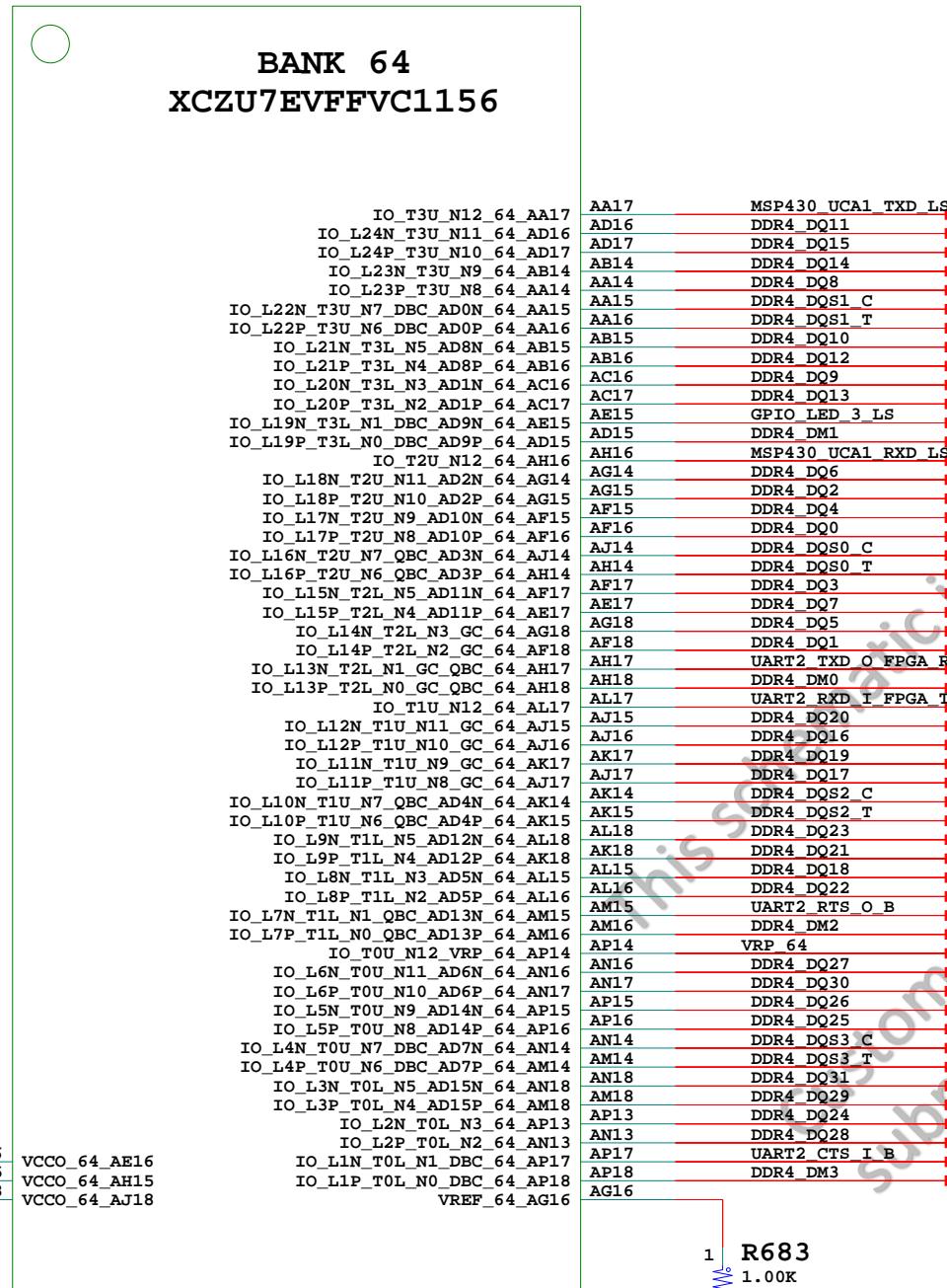
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PCB P/N: 1280937
SCH P/N: 0381770
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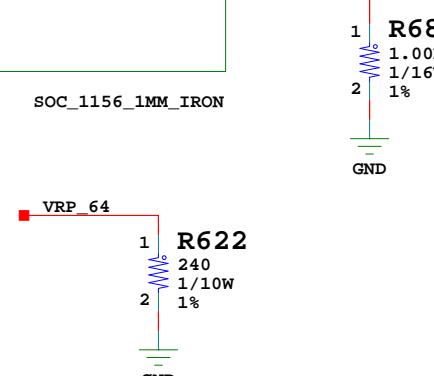
Layout: Place resistor and capacitor for VREF

Underneath the FPGA via array
right next to the via

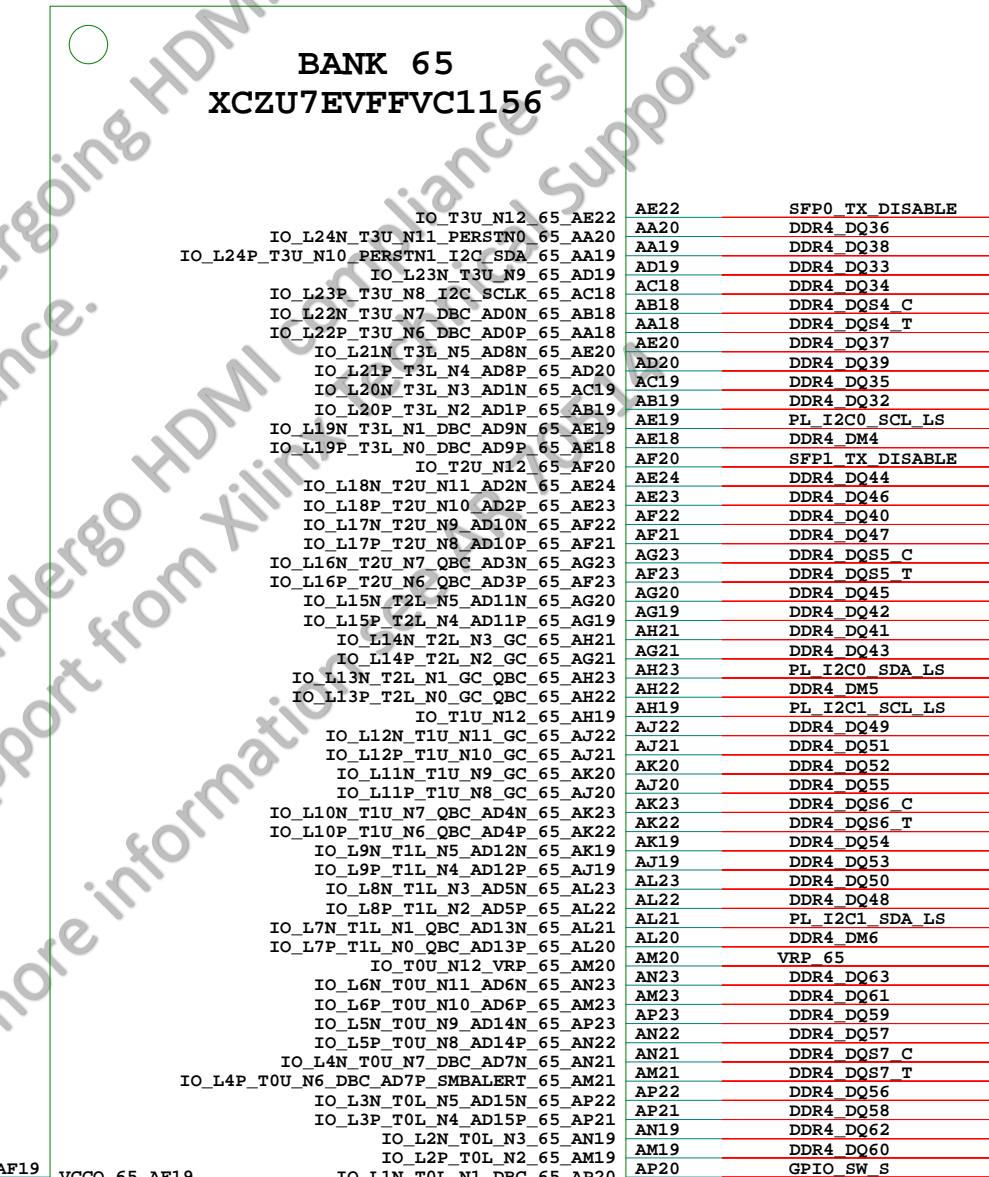
SOC_DA6_FFVC1156_IRONWOOD



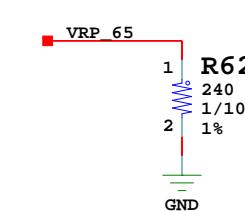
U1 SOC_1156_1MM_IRON



SOC_DA6_FFVC1156_IRONWOOD

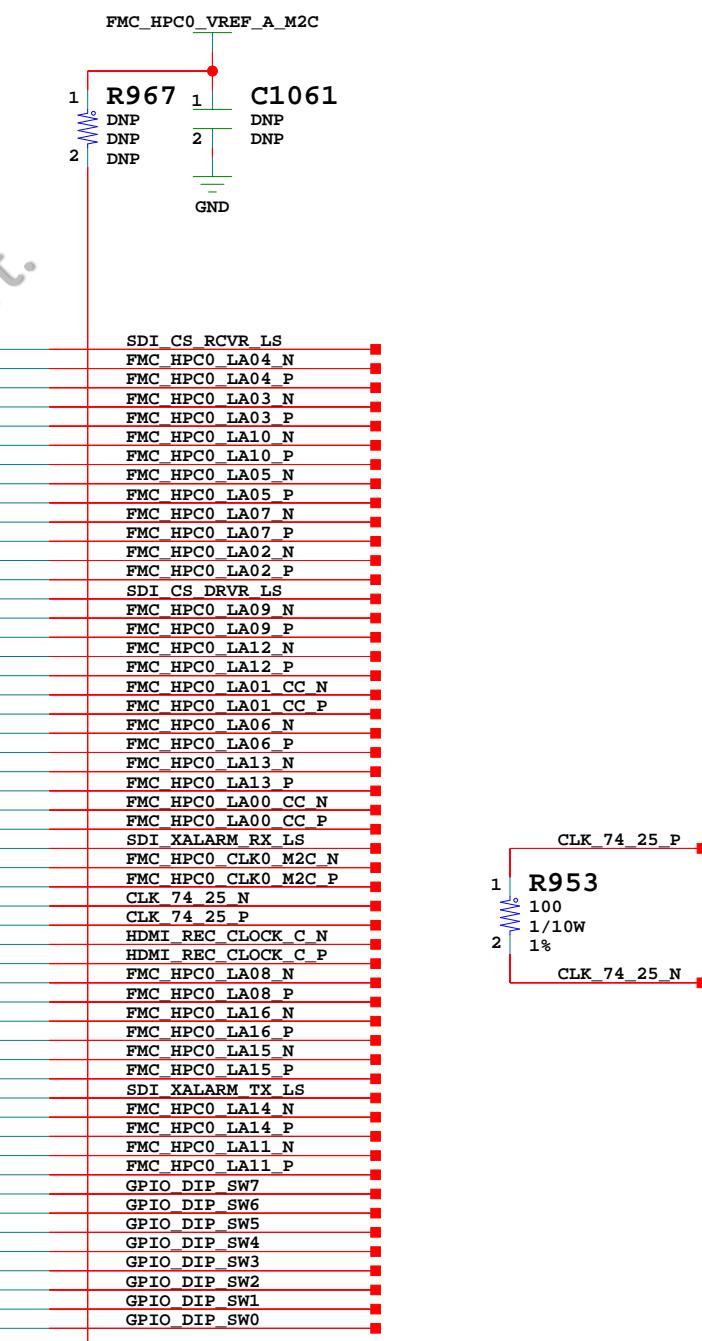
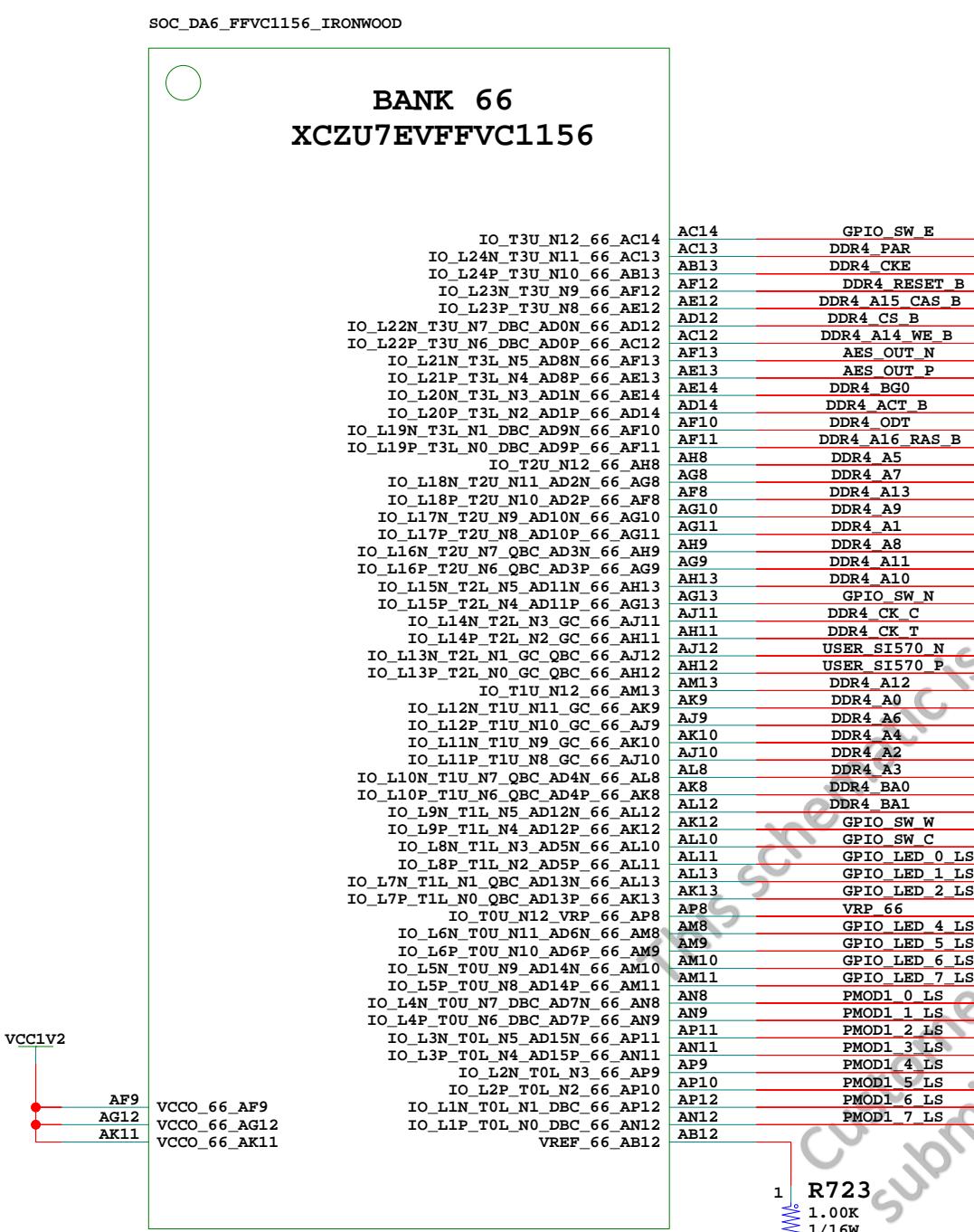


U1 SOC_1156_1MM_IRON



Zynq Banks 64 65

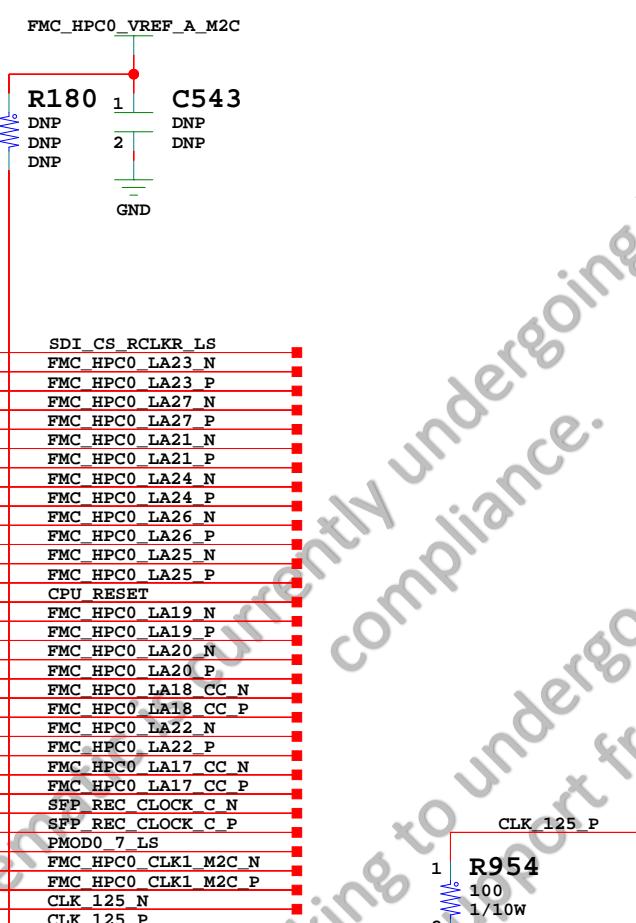
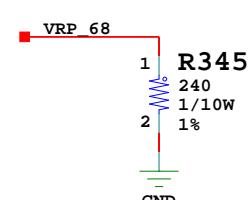
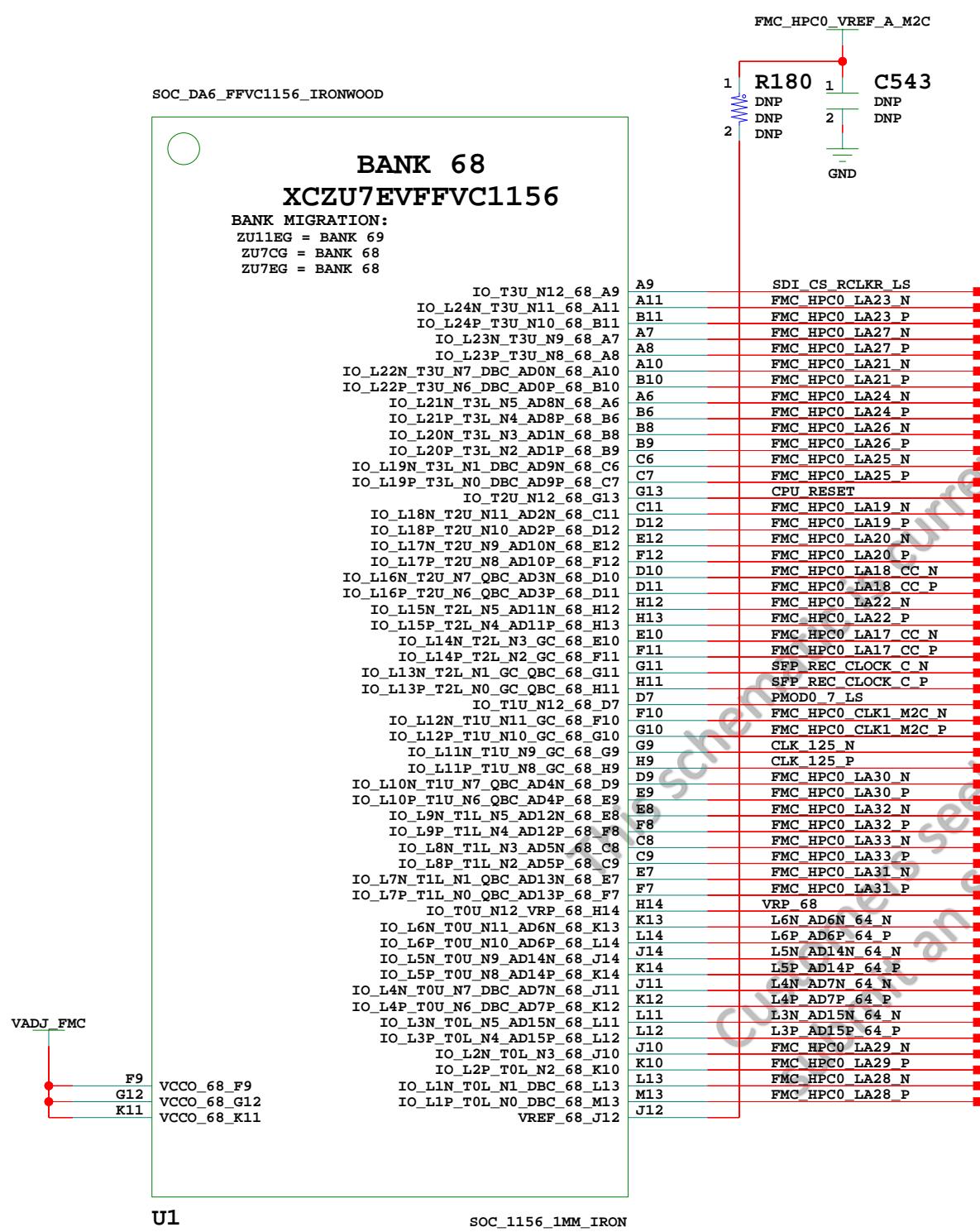
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DATE: 01/08/2018:10:16		VER: 1.0
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SHEET 5 OF 95		DRAWN BY: BF



Zyng Banks 66 67

SUMINX

TITLE: Zynq Banks 66 67 SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER:	1.0
SHEET SIZE: B	REV:	01
SHEET 6	OF 95	DRAWN BY: BF



Currently undergoing HDMI electrical compliance.
For more information see AR 70514

Zynq Banks 68



TITLE: Zynq Banks 68
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

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PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

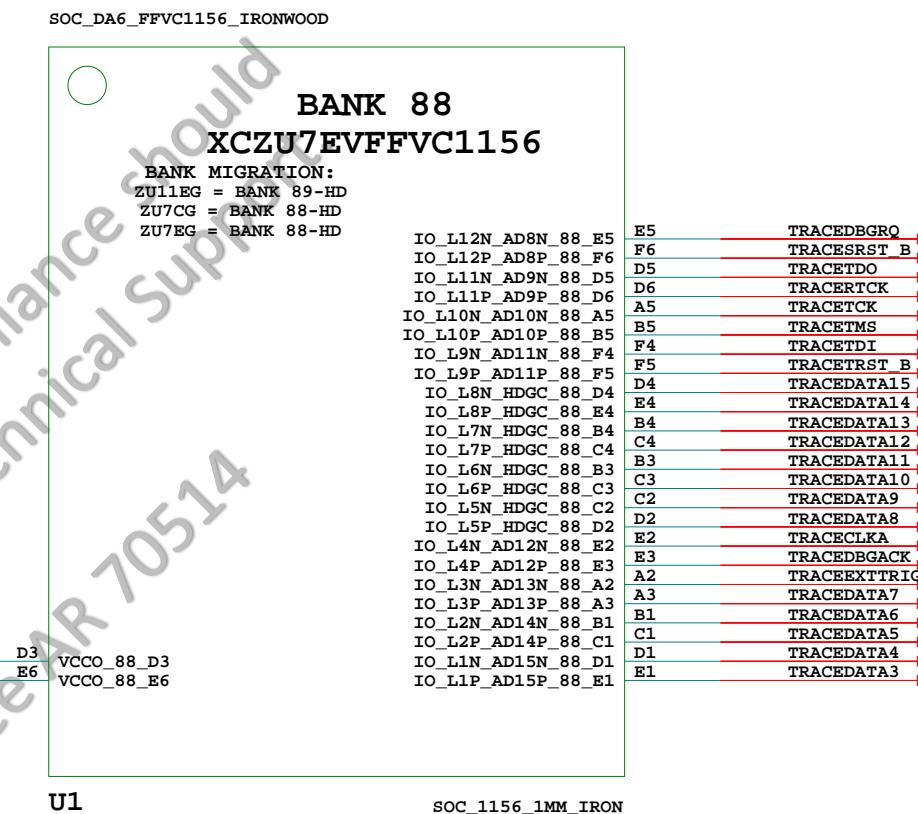
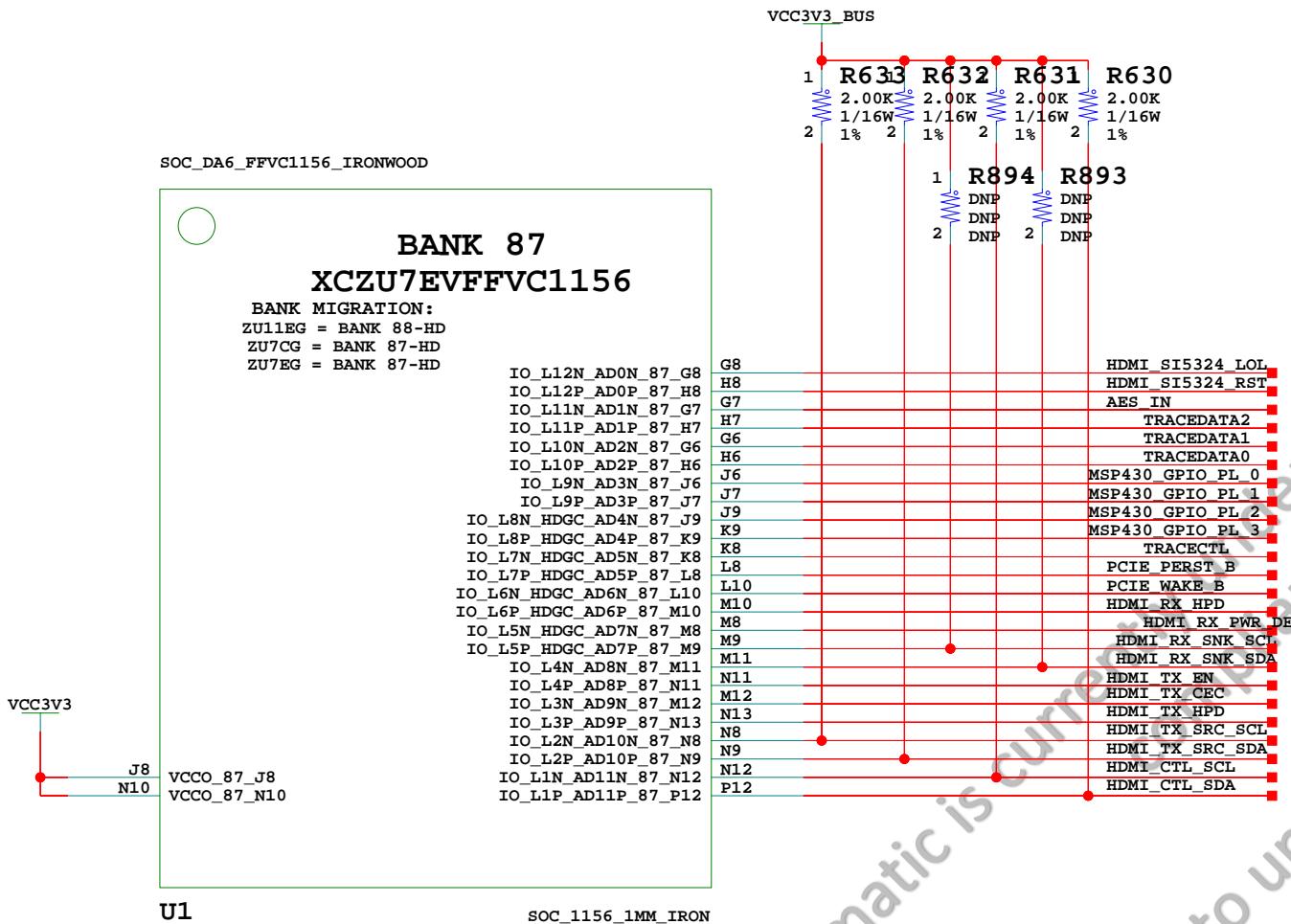
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REV: 01

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BF



Zynq Banks 87 88



TITLE: Zynq Banks 87 88 SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 8 OF 95	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD

BANK 223
XCZU7EVFFVC1156

BANK MIGRATION:
 ZU11EG = BANK 224
 ZU7CG = BANK 223
 ZU7EG = BANK 223

AN6	HDMI TX0_P
AN5	HDMI TX0_N
AP4	HDMI RX0_C_P
AP3	HDMI RX0_C_N
AM4	HDMI TX1_P
AM3	HDMI TX1_N
AN2	HDMI RX1_C_P
AN1	HDMI RX1_C_N
AL6	HDMI TX2_P
AL5	HDMI TX2_N
AL2	HDMI RX2_C_P
AL1	HDMI RX2_C_N
AJ6	FMC_HPC1_DP0_C2M_P
AJ5	FMC_HPC1_DP0_C2M_N
AK4	FMC_HPC1_DP0_M2C_P
AK3	FMC_HPC1_DP0_M2C_N
MGTREFCLKOP_223_AD8	
MGTREFCLKN_223_AD7	
MGTREFCLKP_223_AC10	
MGTREFCLKIN_223_AC9	

SOC_DA6_FFVC1156_IRONWOOD

BANK 224
XCZU7EVFFVC1156

BANK MIGRATION:
 ZU11EG = BANK 225
 ZU7CG = BANK 224
 ZU7EG = BANK 224

AH4	PCIE_TX3_P
AH3	PCIE_TX3_N
AJ2	PCIE_RX3_P
AJ1	PCIE_RX3_N
AG6	PCIE_TX2_P
AG5	PCIE_TX2_N
AG2	PCIE_RX2_P
AG1	PCIE_RX2_N
AE6	PCIE_TX1_P
AE5	PCIE_TX1_N
AF4	PCIE_RX1_P
AF3	PCIE_RX1_N
AD4	PCIE_TX0_P
AD3	PCIE_TX0_N
AE2	PCIE_RX0_P
AE1	PCIE_RX0_N
AB8	PCIE_CLK_P
AB7	PCIE_CLK_N
AA10	USER_SMA_MGT_CLOCK_C_P
AA9	USER_SMA_MGT_CLOCK_C_N
MGTRREF_R_AD10	
MGTAVTTRCAL_R_AA9	
AD10	MGTRREF_224[1] 1/10W
AD9	

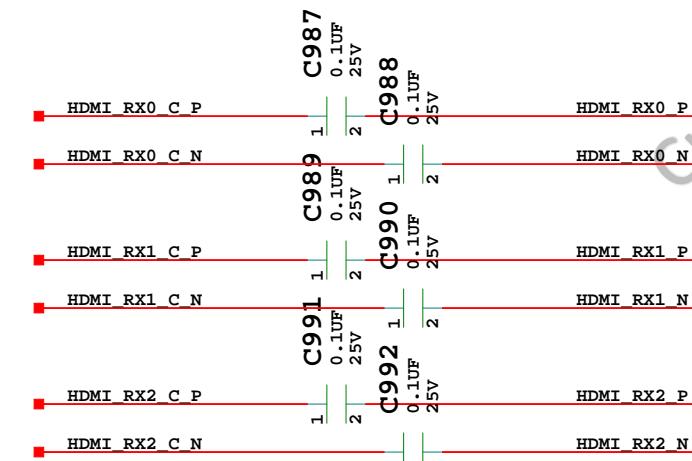
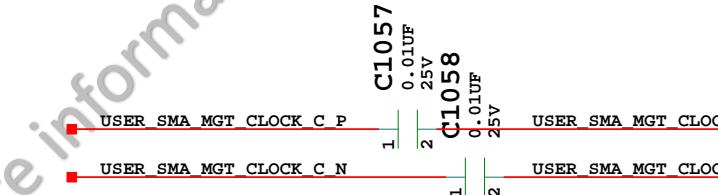
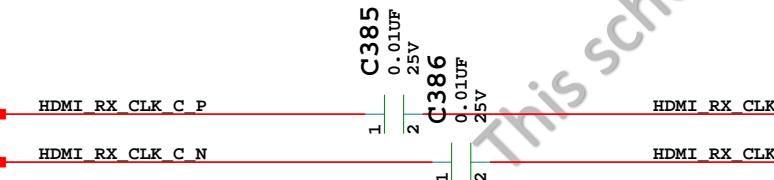
R214

U1

SOC_1156_1MM_IRON

U1

SOC_1156_1MM_IRON


Zynq Banks 223 224


TITLE: Zynq Banks 223 224
 SCHEM, ROHS COMPLIANT
 HW-Z1-ZCU106_REV1_0

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 PCB P/N: 1280937
 SCH P/N: 0381770
 TEST P/N: TSS0186

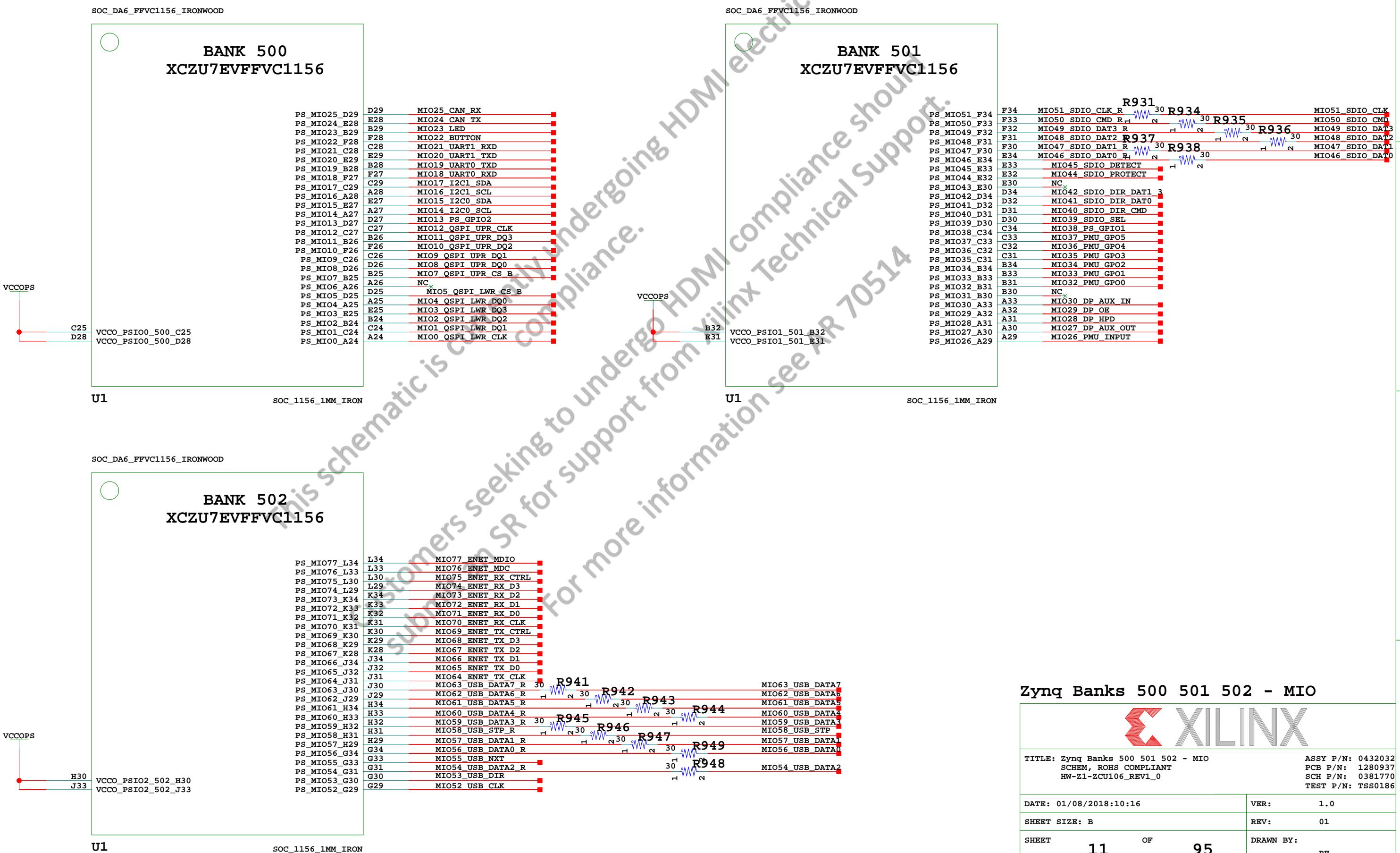
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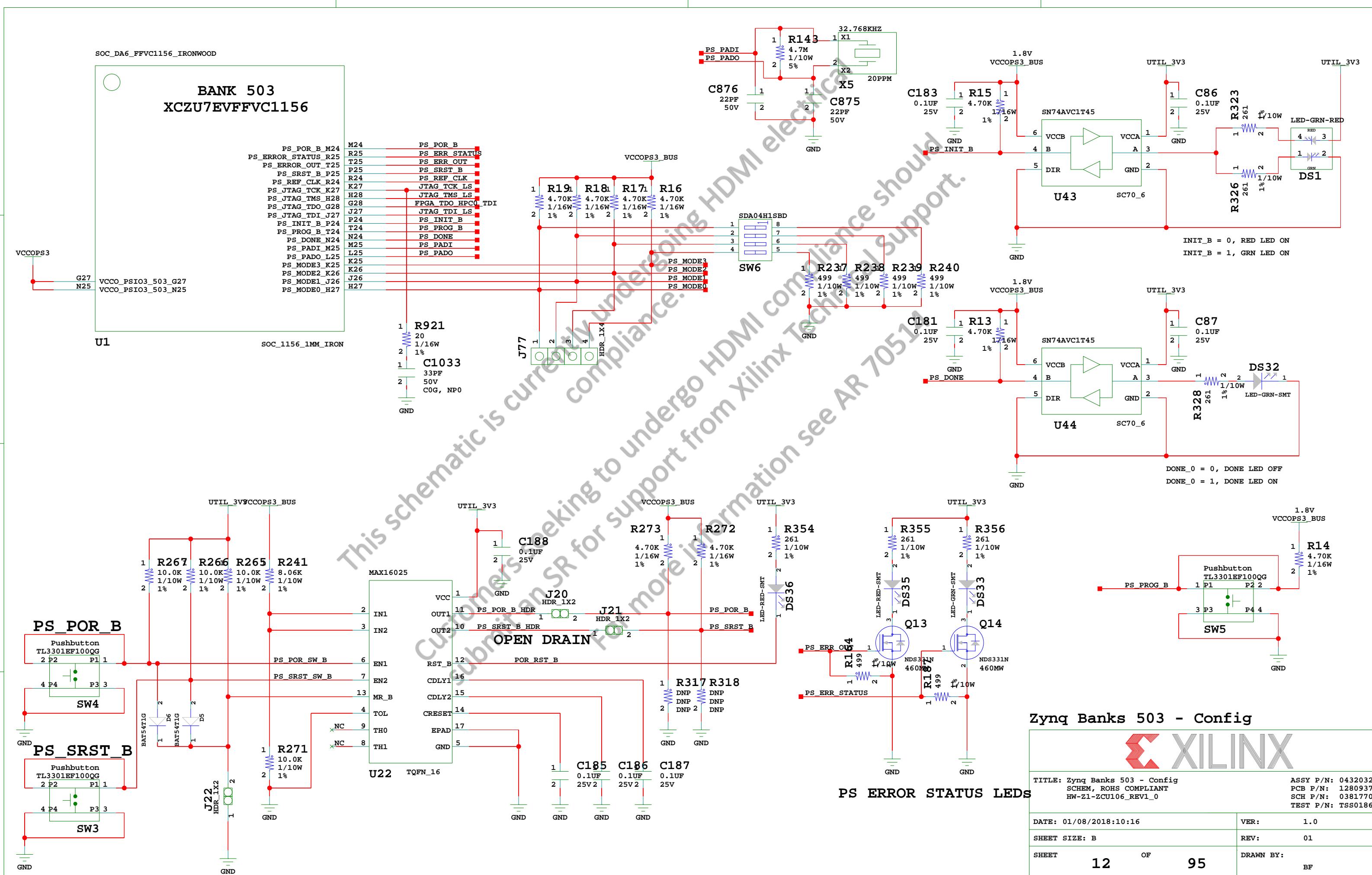
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 9 OF 95 DRAWN BY: BF





SOC_DA6_FFVC1156_IRONWOOD

BANK 504

XCZU7EVFFVC1156

DDR4_SODIMM_A0	AN34	PS_DDR_A0_AN34	AP27	DDR4_SODIMM_DQ0
DDR4_SODIMM_A1	AM34	PS_DDR_A1_AM34	AP25	DDR4_SODIMM_DQ1
DDR4_SODIMM_A2	AM33	PS_DDR_A2_AM33	AP26	DDR4_SODIMM_DQ2
DDR4_SODIMM_A3	AL34	PS_DDR_A3_AL34	AM26	DDR4_SODIMM_DQ3
DDR4_SODIMM_A4	AL33	PS_DDR_A4_AL33	PS_DDR_DQ3_AM26	DDR4_SODIMM_DQ4
DDR4_SODIMM_A5	AK33	PS_DDR_A5_AK33	PS_DDR_DQ4_AP24	DDR4_SODIMM_DQ5
DDR4_SODIMM_A6	AK30	PS_DDR_A6_AK30	PS_DDR_DQ5_AL25	DDR4_SODIMM_DQ6
DDR4_SODIMM_A7	AJ30	PS_DDR_A7_AJ30	PS_DDR_DQ6_AM25	DDR4_SODIMM_DQ7
DDR4_SODIMM_A8	AJ31	PS_DDR_A8_AJ31	PS_DDR_DQ7_AM24	DDR4_SODIMM_DQ8
DDR4_SODIMM_A9	AH31	PS_DDR_A9_AH31	PS_DDR_DQ8_AN28	DDR4_SODIMM_DQ9
DDR4_SODIMM_A10	AG31	PS_DDR_A10_AG31	PS_DDR_DQ9_AN28	DDR4_SODIMM_DQ10
DDR4_SODIMM_A11	AF31	PS_DDR_A11_AF31	PS_DDR_DQ10_AP29	DDR4_SODIMM_DQ11
DDR4_SODIMM_A12	AG30	PS_DDR_A12_AG30	PS_DDR_DQ11_AP28	DDR4_SODIMM_DQ12
DDR4_SODIMM_A13	AF30	PS_DDR_A13_AF30	PS_DDR_DQ12_AM31	DDR4_SODIMM_DQ13
DDR4_SODIMM_WE_B	AG29	PS_DDR_A14_AG29	PS_DDR_DQ13_AP31	DDR4_SODIMM_DQ14
DDR4_SODIMM_CAS_B	AG28	PS_DDR_A15_AG28	PS_DDR_DQ14_AN31	DDR4_SODIMM_DQ15
DDR4_SODIMM_RAS_B	AF28	PS_DDR_A16_AF28	PS_DDR_DQ15_AM30	DDR4_SODIMM_DQ16
NC	AF26	PS_DDR_A17_AF26	PS_DDR_DQ16_AP25	DDR4_SODIMM_DQ17
DDR4_SODIMM_BA0	AE27	PS_DDR_BA0_AE27	PS_DDR_DQ17_AG25	DDR4_SODIMM_DQ18
DDR4_SODIMM_BA1	AE28	PS_DDR_BA1_AE28	PS_DDR_DQ18_AG26	DDR4_SODIMM_DQ19
DDR4_SODIMM_ACT_B	AE25	PS_DDR_ACT_N_AE25	PS_DDR_DQ19_AJ25	DDR4_SODIMM_DQ20
DDR4_SODIMM_ALERT_BA26		PS_DDR_ALERT_N_AB26	PS_DDR_DQ20_AG24	DDR4_SODIMM_DQ21
DDR4_SODIMM_PARITY_AA26		PS_DDR_PARITY_AA26	PS_DDR_DQ21_AK25	DDR4_SODIMM_DQ22
ZYNQ_DDR4_SODIMM_RESET_AB26		PS_DDR_RAM_RST_N_AD26	PS_DDR_DQ22_AJ24	DDR4_SODIMM_DQ23
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DDR4_SODIMM_ODT1	AJ32	PS_DDR_ODT1_AJ32	PS_DDR_DQ34_AC29	DDR4_SODIMM_DQ35
DDR4_SODIMM_DQS0_T	AN26	PS_DDR_DQS_P0_AN26	PS_DDR_DQ35_AD32	DDR4_SODIMM_DQ36
DDR4_SODIMM_DQS0_C	AN27	PS_DDR_DQS_N0_AN27	PS_DDR_DQ36_AC31	DDR4_SODIMM_DQ37
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VCCO_PSDDR_504		AJ33	PS_DDR_DQ62_W34	DDR4_SODIMM_DQ63
VCCO_PSDDR_504		AJ28	PS_DDR_DQ63_Y34	AF32
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VCCO_PSDDR_504		AG32	PS_DDR_DQ65_AB32	DDR4_SODIMM_CB1
VCCO_PSDDR_504		AG32	PS_DDR_DQ66_AH33	DDR4_SODIMM_CB2
VCCO_PSDDR_504		AG32	PS_DDR_DQ67_AE33	DDR4_SODIMM_CB3
VCCO_PSDDR_504		AG27	PS_DDR_DQ68_AP33	DDR4_SODIMM_CB4
VCCO_PSDDR_504		AG27	PS_DDR_DQ69_AH34	DDR4_SODIMM_CB5
VCCO_PSDDR_504		AE31	PS_DDR_DQ70_AJ34	DDR4_SODIMM_CB6
VCCO_PSDDR_504		AE31	PS_DDR_DQ71_AK34	DDR4_SODIMM_CB7
VCCO_PSDDR_504		AE26	PS_DDR_ZQ_AC26	AC26 UDIMM PS ZQ

U1

SOC_1156_1MM_IRON

1 R351
2 240
3 1/10W
4 1%
5 GND

Zynq Banks 504 - Memory



TITLE: Zynq Banks 504 - Memory
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

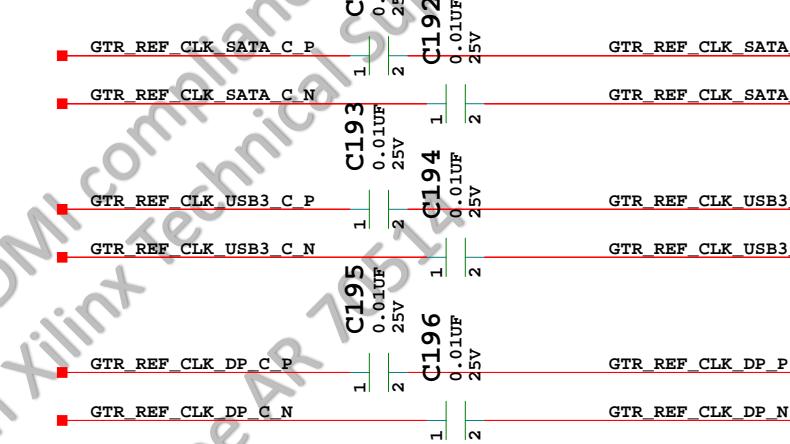
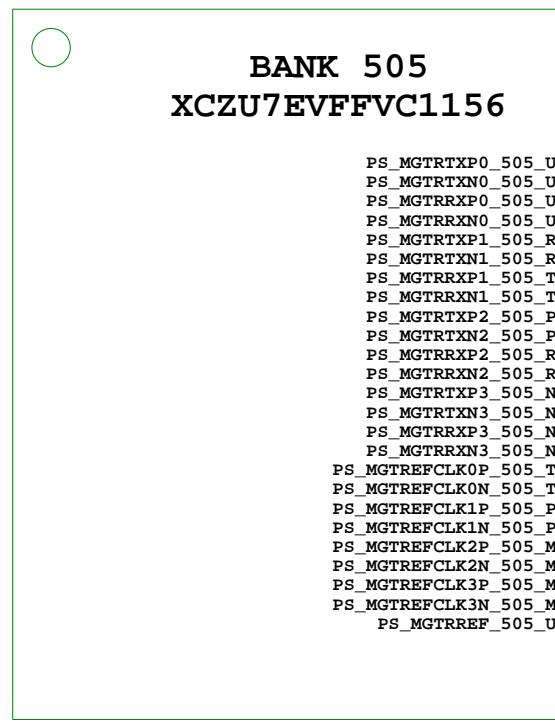
SHEET SIZE: B

REV: 01

SHEET 13 OF 95

DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD



This schematic is currently undergoing HDMI compliance support.
 Customers seeking to undergo HDMI compliance should submit an SR for support from Xilinx Technical Support.
 For more information see AP 701A.

Zynq Banks 505 - GTR

TITLE: Zynq Banks 505 - GTR
 SCHEM, ROHS COMPLIANT
 HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
 PCB P/N: 1280937
 SCH P/N: 0381770
 TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 14 OF 95	DRAWN BY: BF

SOC_DA6_FFVC1156_IRONWOOD

BANK MGTAVCC_R
XCZU7EVFFVC1156

 MGTAVCC_R_W8
 MGTAVCC_R_U8
 MGTAVCC_R_T10
 MGTAVCC_R_R8
 MGTAVCC_R_AC8
 MGTAVCC_R_AB10
 MGTAVCC_R_AA8

 W8
 U8
 T10
 R8
 AC8
 AB10
 AA8

MGTAVCC

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK MGTAVTT_R
XCZU7EVFFVC1156

 MGTAVTT_R_Y6
 MGTAVTT_R_V6
 MGTAVTT_R_T6
 MGTAVTT_R_P6
 MGTAVTT_R_M6
 MGTAVTT_R_AP6
 MGTAVTT_R_AM6
 MGTAVTT_R_AK6
 MGTAVTT_R_AH6
 MGTAVTT_R_AF6
 MGTAVTT_R_AD6
 MGTAVTT_R_AB6

 Y6
 V6
 T6
 P6
 M6
 AP6
 AM6
 AK6
 AH6
 AF6
 AD6
 AB6

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK MGTVCCAUX_R
XCZU7EVFFVC1156

 MGTVCCAUX_R_Y10
 MGTVCCAUX_R_V10

 Y10
 V10

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK VCCAUX
XCZU7EVFFVC1156

 VCCAUX_V23
 VCCAUX_U23
 VCCAUX_R23
 VCCAUX_P23

VCCAUX

U1

SOC_1156_1MM_IRON

SOC_DA6_FFVC1156_IRONWOOD

BANK VCCAUX_IO
XCZU7EVFFVC1156

 VCCAUX_IO_U22
 VCCAUX_IO_T22
 VCCAUX_IO_R22
 VCCAUX_IO_N22

VCCAUX

U1

SOC_1156_1MM_IRON

Zynq Power 1
 TITLE: Zynq Power 1
 SCHEM, ROHS COMPLIANT
 HW-Z1-ZCU106_REV1_0

 ASSY P/N: 0432032
 PCB P/N: 1280937
 SCH P/N: 0381770
 TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

SHEET SIZE: B

REV: 01

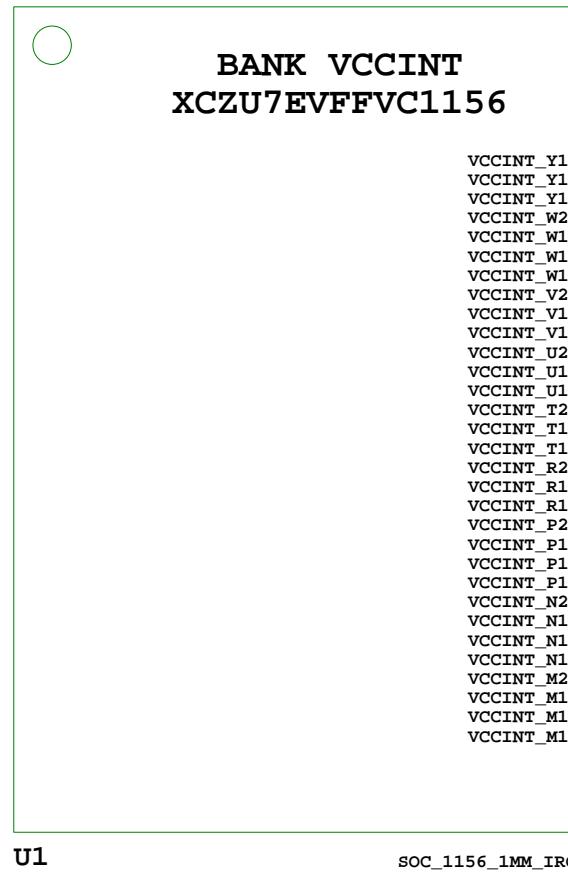
SHEET 15 OF 95

DRAWN BY:

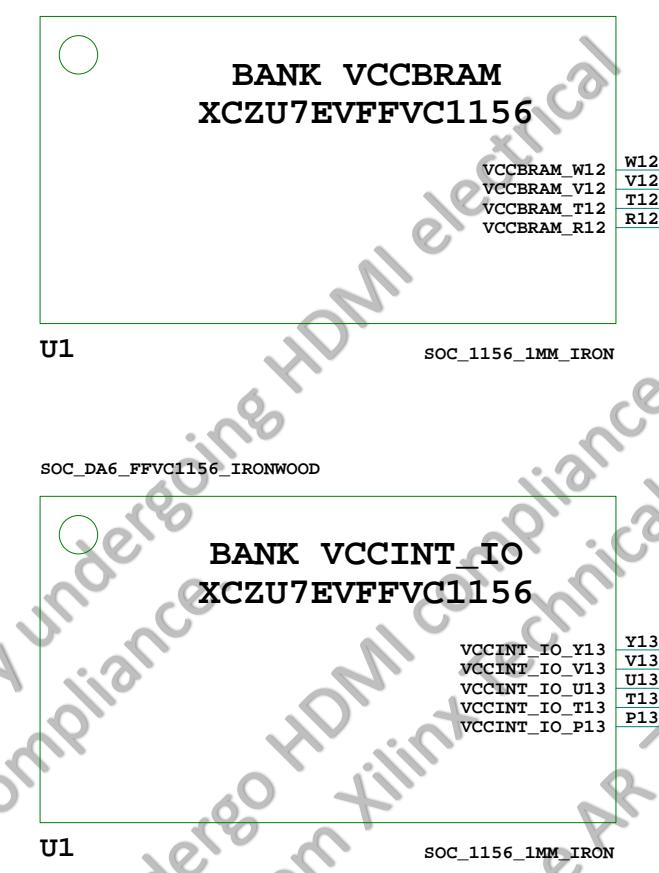
BF

This schematic is currently undergoing HDMI compliance should
 Customers seeking to undergo HDMI compliance should
 submit an SR for support from Xilinx Technical Support.
 For more information see AR 70514

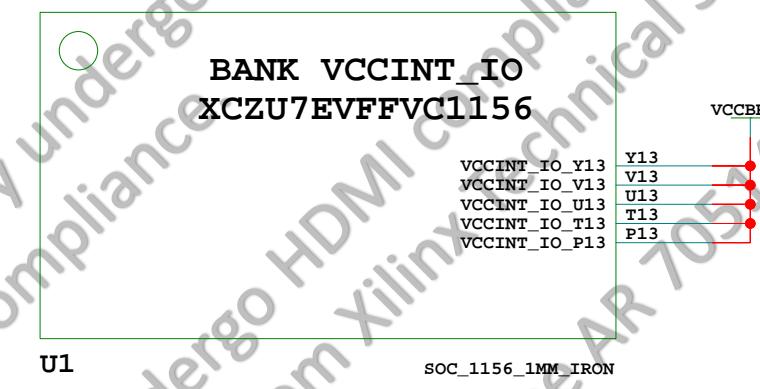
SOC_DA6_FFVC1156_IRONWOOD



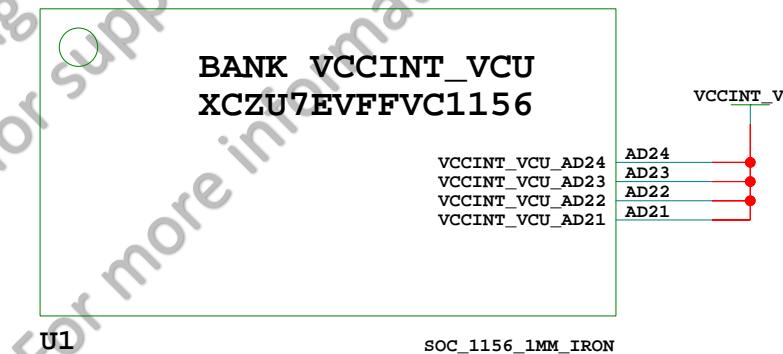
SOC_DA6_FFVC1156_IRONWOOD



SOC_DA6_FFVC1156_IRONWOOD



SOC_DA6_FFVC1156_IRONWOOD



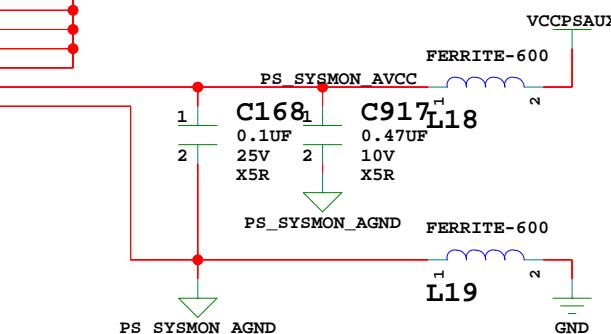
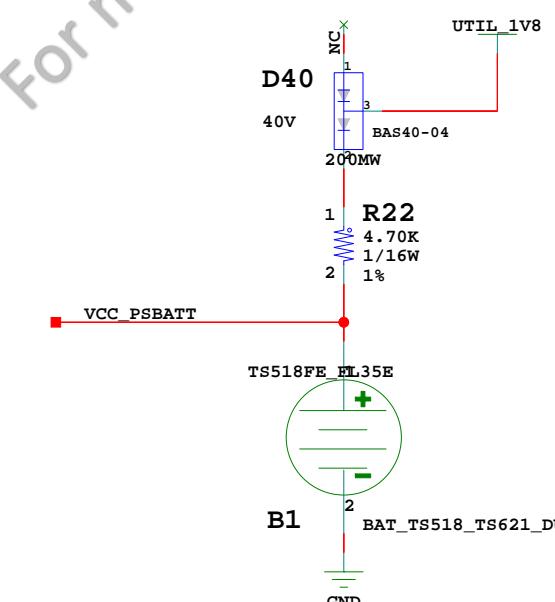
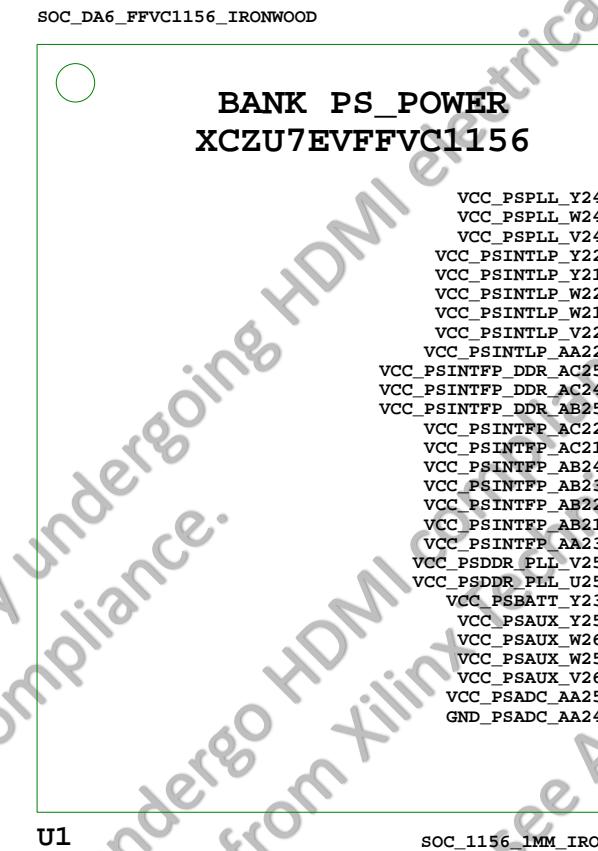
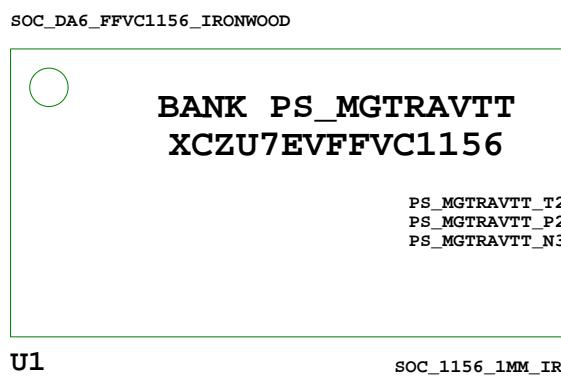
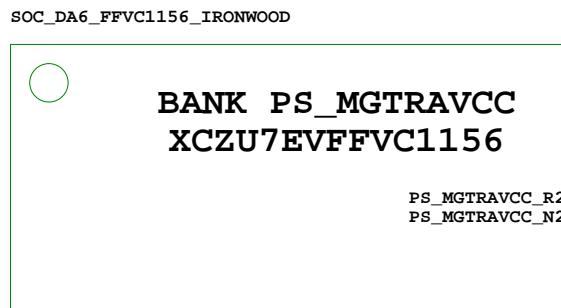
This schematic is currently undergoing HDMI electrical compliance testing. Customers seeking to undergo HDMI compliance should submit an SR for support from Xilinx Technical Support. For more information see AR 70514.

Zynq Power 2

TITLE: Zynq Power 2
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 16 OF 95	DRAWN BY: BF



Zynq Power 3



TITLE: Zynq Power 3
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

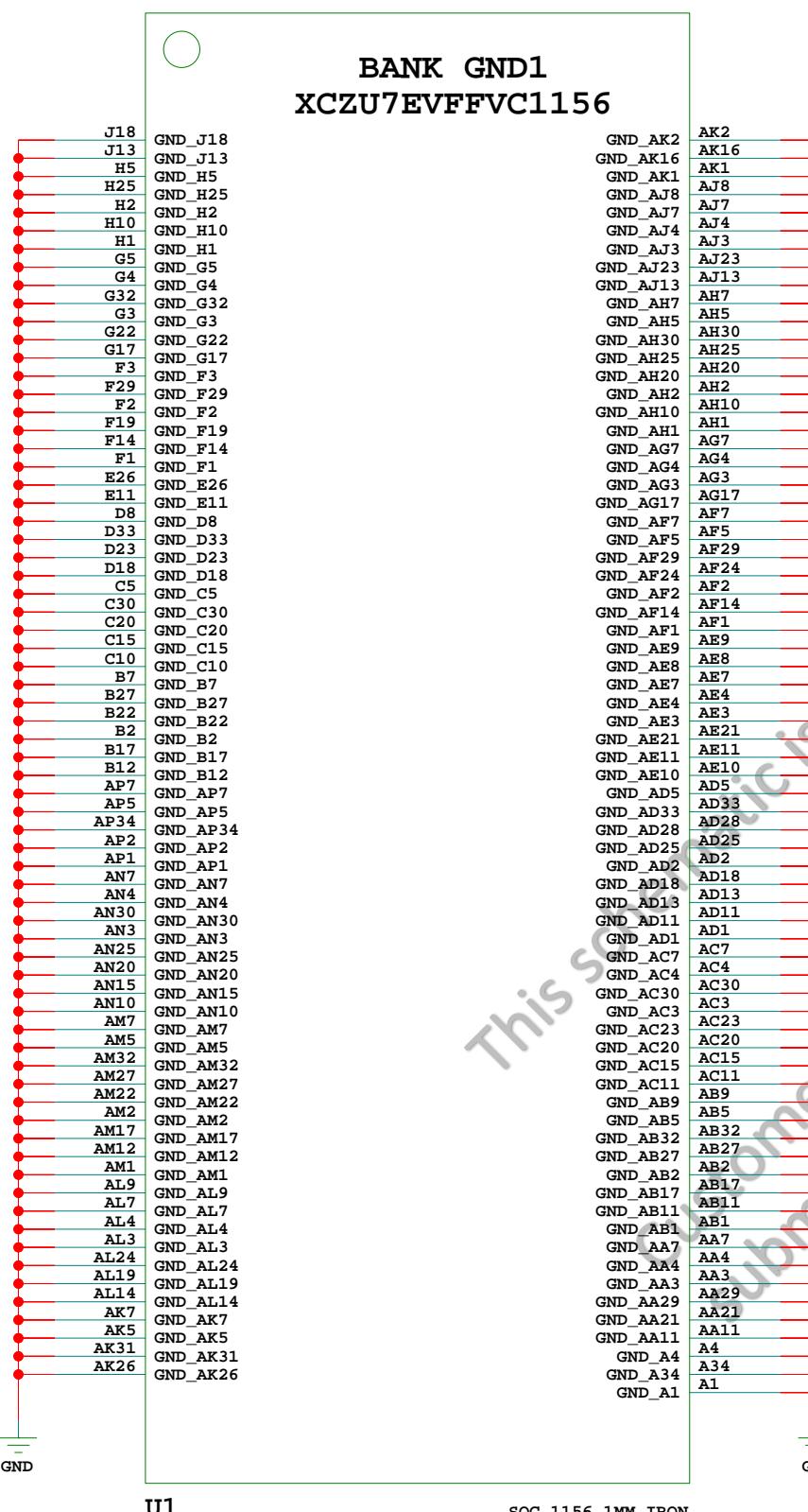
SHEET SIZE: B

REV: 01

SHEET 17 OF 95

DRAWN BY:
BF

SOC_DA6_FFVC1156_IRONWOOD



SOC_DA6_FFVC1156_IRONWOOD

**Zynq GND**

TITLE: Zynq GND
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

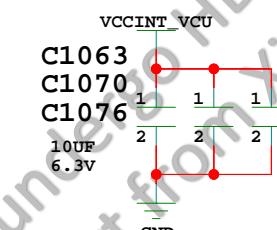
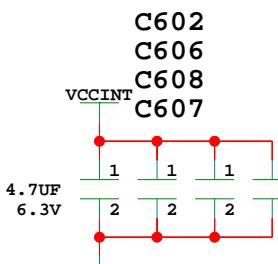
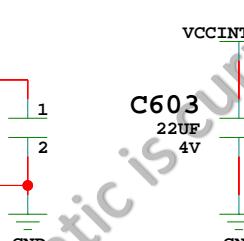
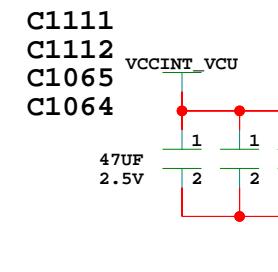
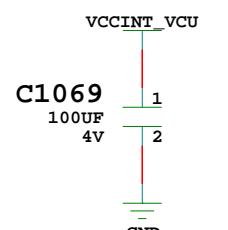
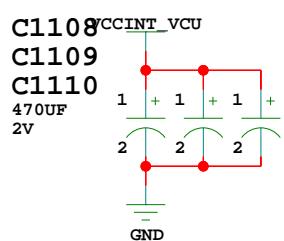
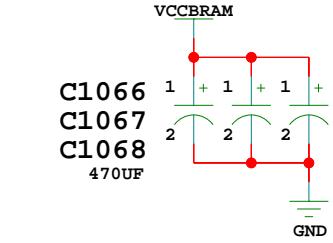
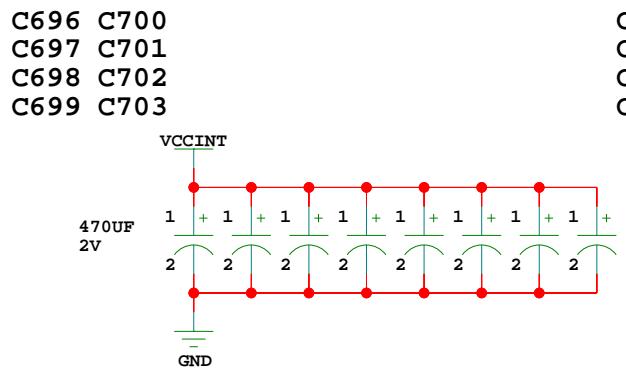
SHEET SIZE: B

REV: 01

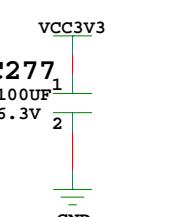
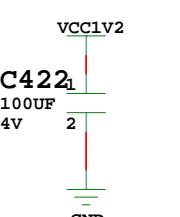
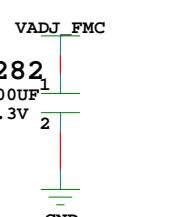
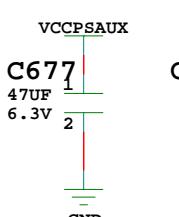
SHEET 18 OF 95

DRAWN BY:

BF



VCCO BANKS 0 28 64 65 66 67 68 87 88



VCCBRAM

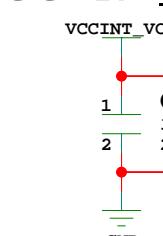
VCCINT

VCCINT_VCU

Place the **VCCINT_VCU** section in the **AR10514** area.

Place these 0201/0402 dual pad capacitors directly under UI near pins AD24/AD23/AD22/AD21

VCCINT VCU



**C1114
330UF
2.5V Place these 1210 capacitors
close to U1**

Zynq Decoupling 1



TITLE: Zynq Decoupling 1
SCHEM, ROHS COMPLIANT
HW-71-ZCU106 REV1.0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: T660180

DATE: 01/08/2018 10:16

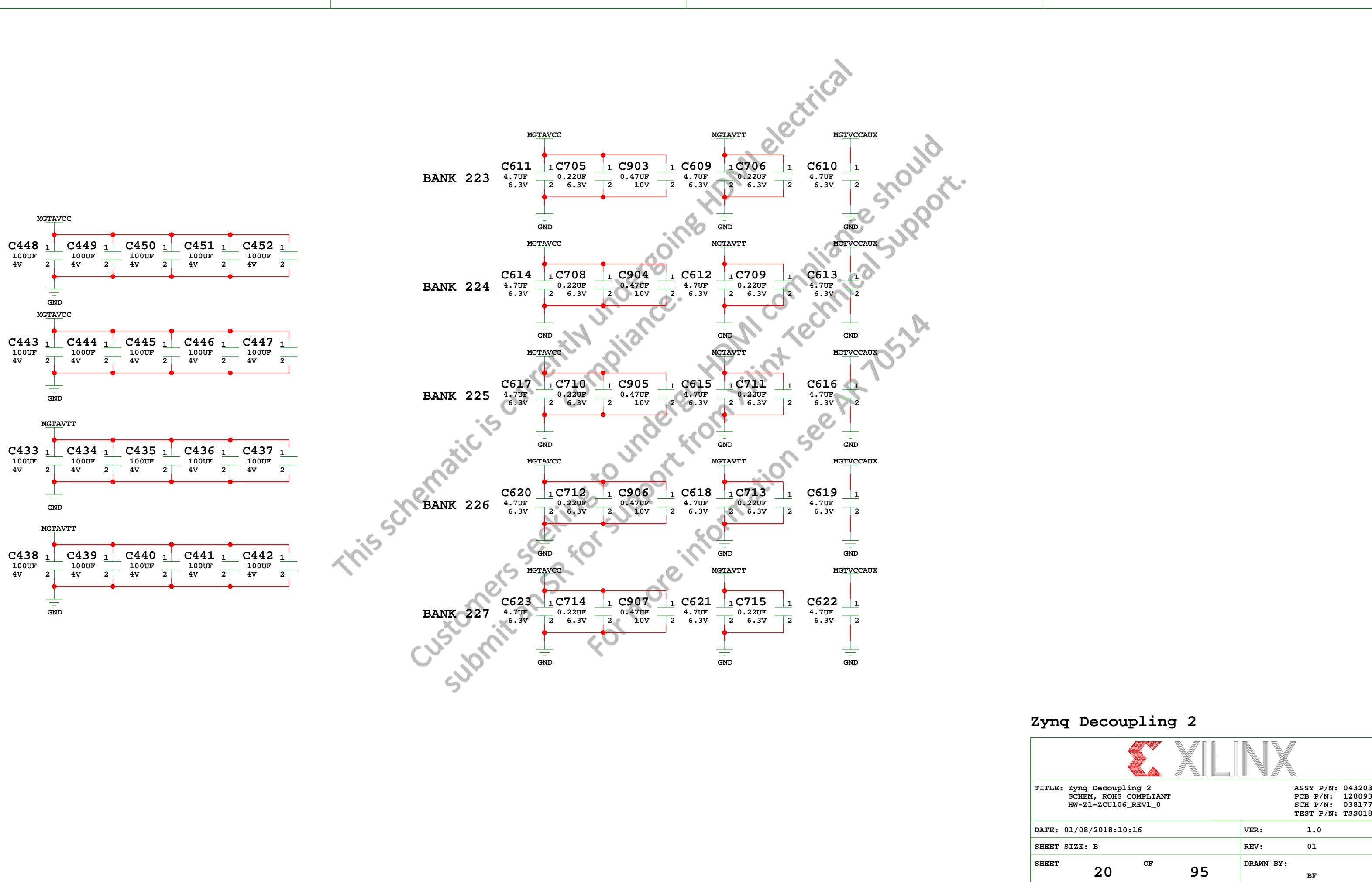
10

SHEET SIZE: B

01

SHEET 19 OF 95

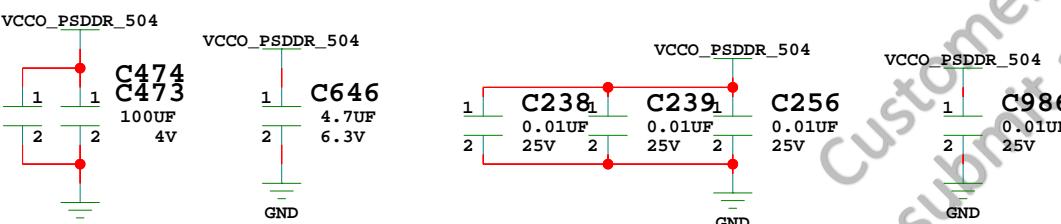
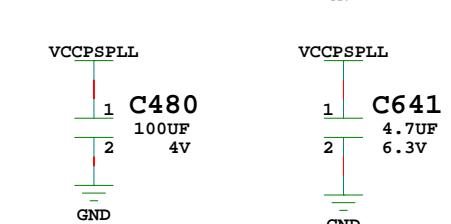
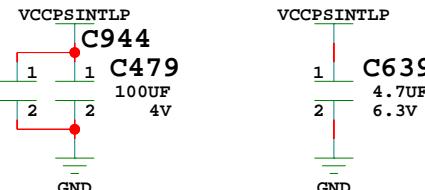
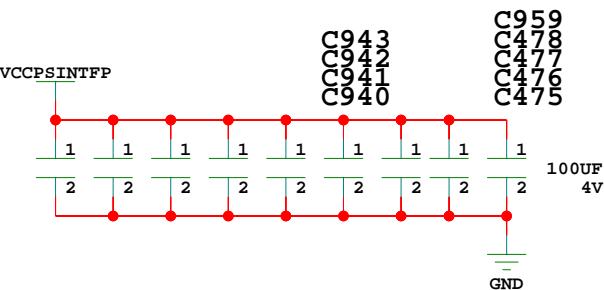
2



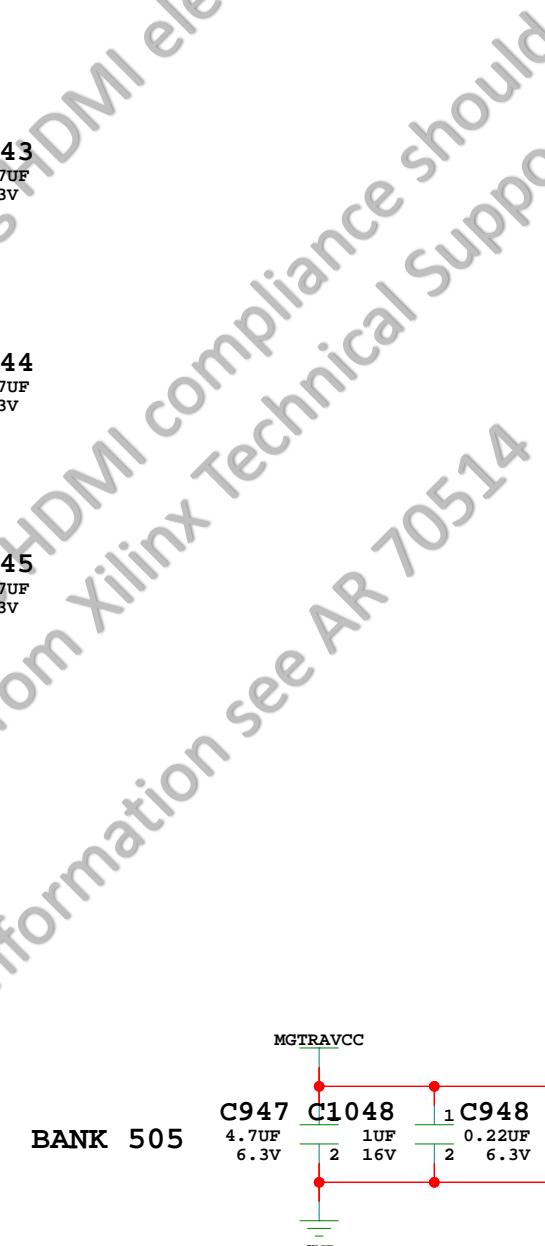
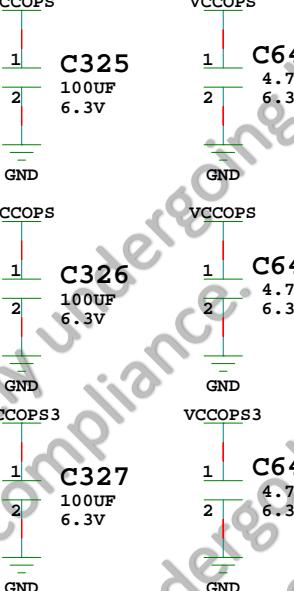
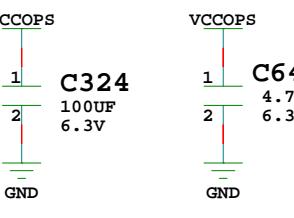
TITLE: Zynq Decoupling 2
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 20 OF 95	DRAWN BY: BF

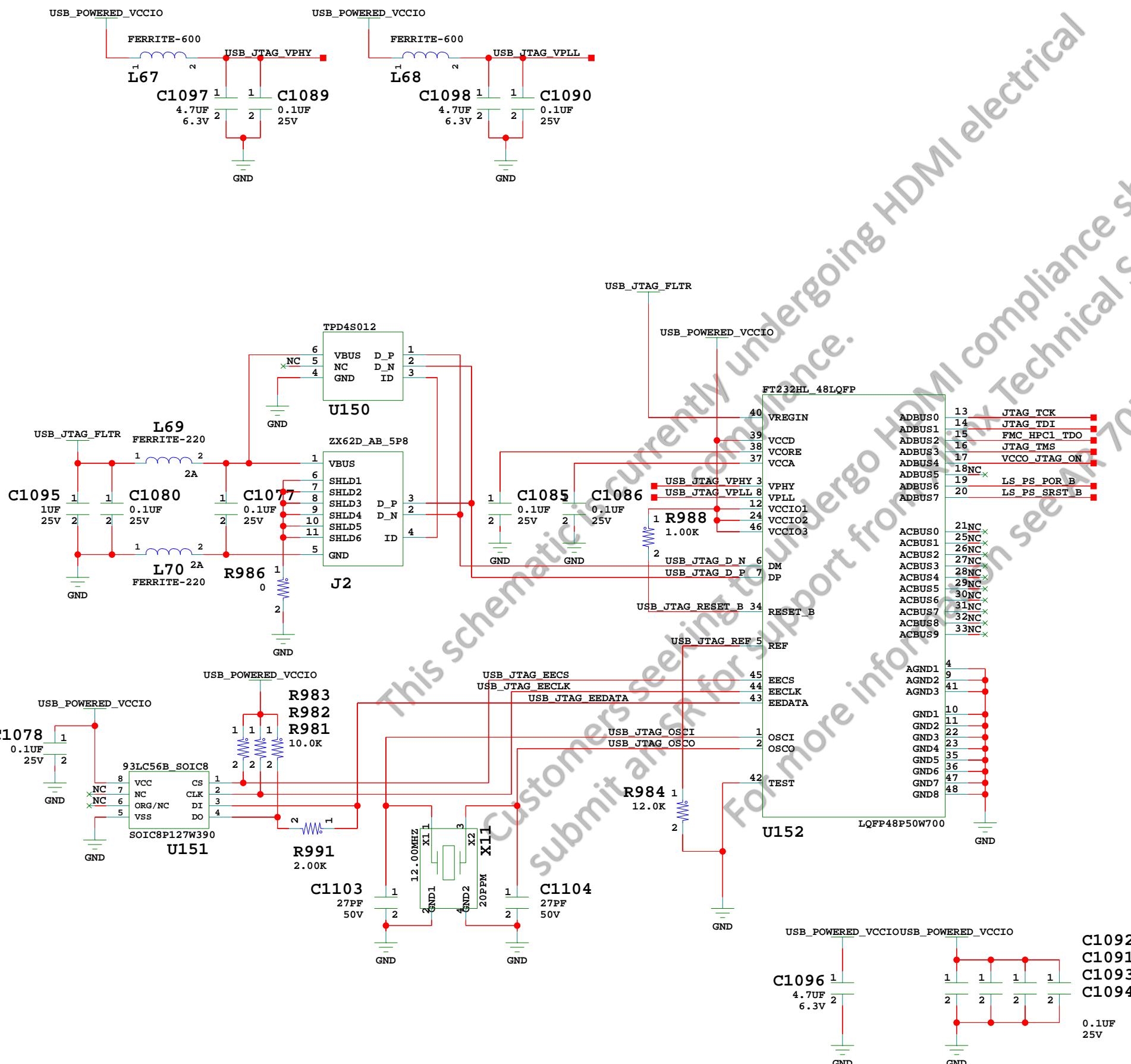


Place this round pad capacitor directly under U1



Zynq Decoupling 3

TITLE: Zynq Decoupling 3 SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 21 OF 95	DRAWN BY: BF



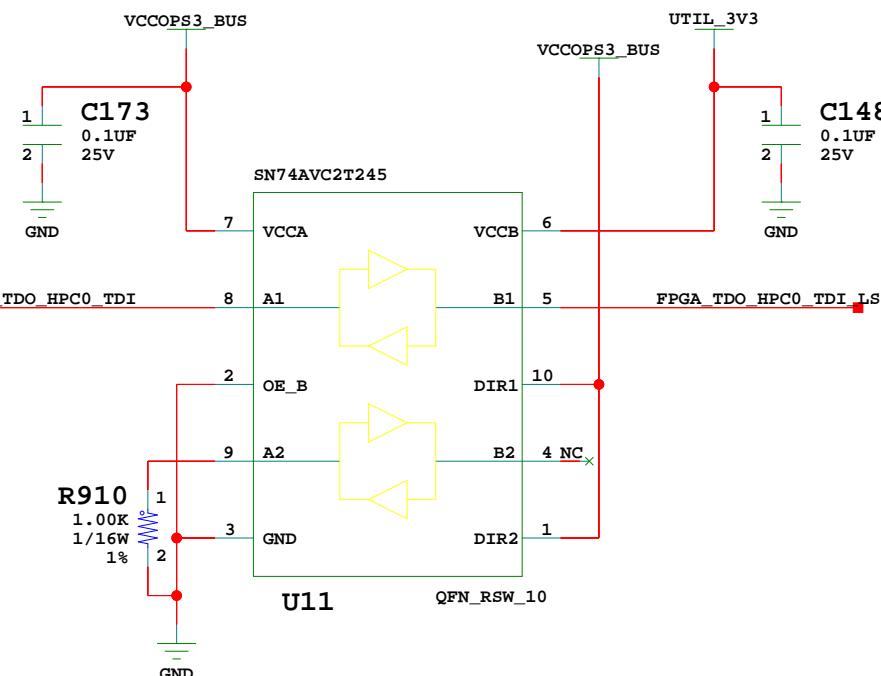
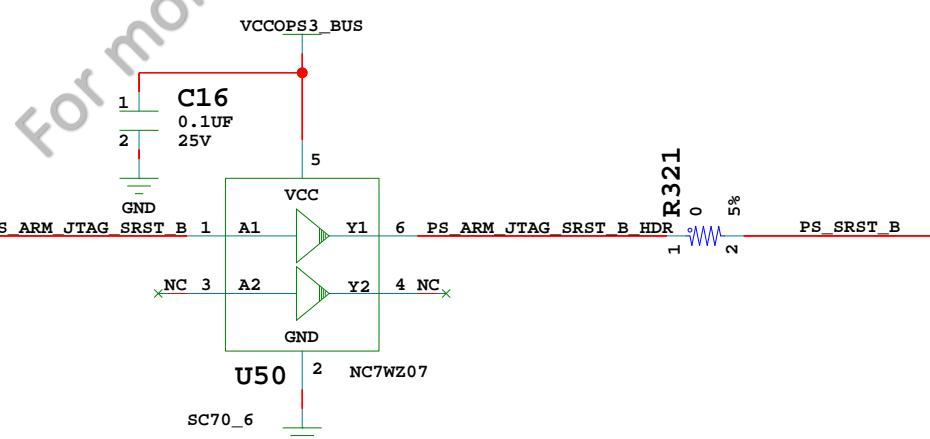
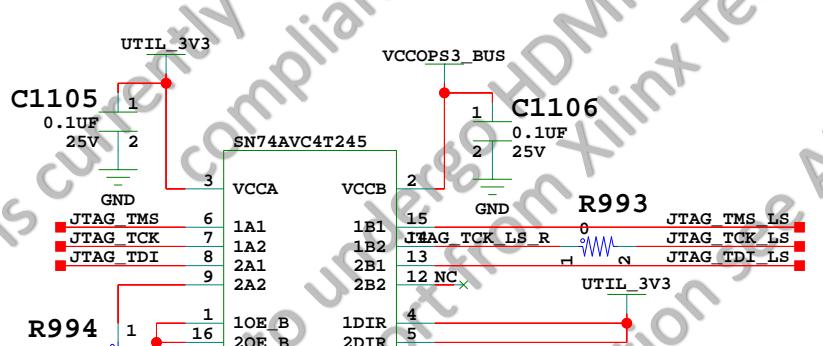
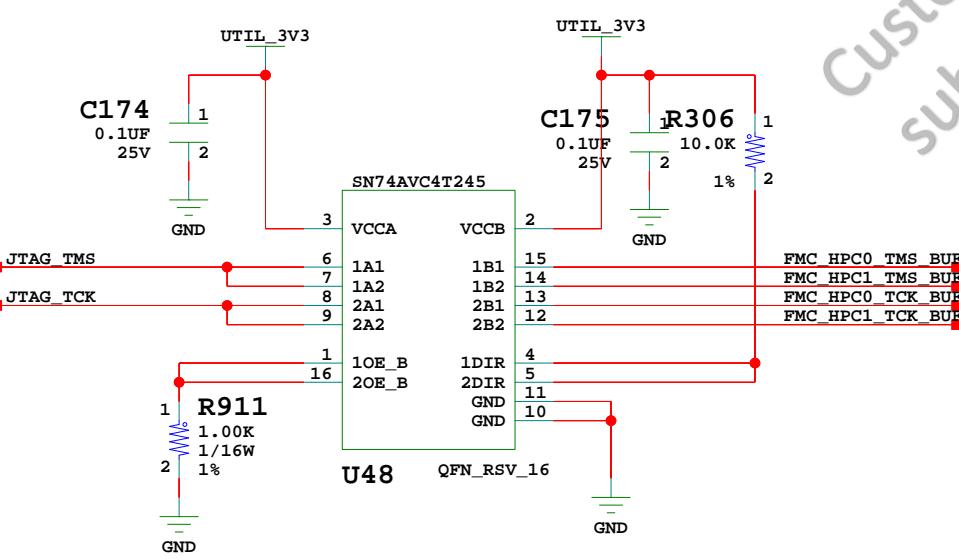
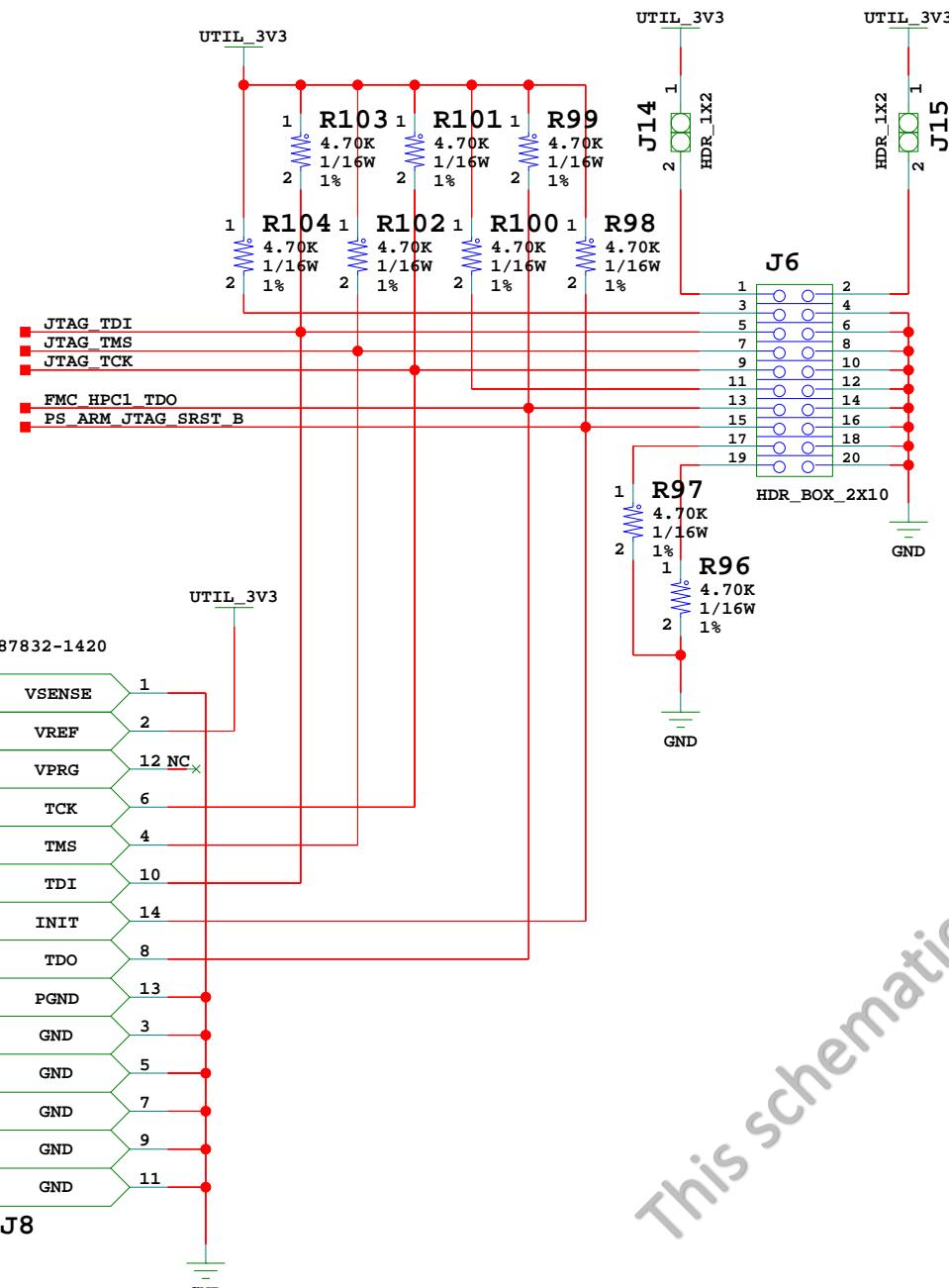
USB JTAG



TITLE: USB JTAG
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

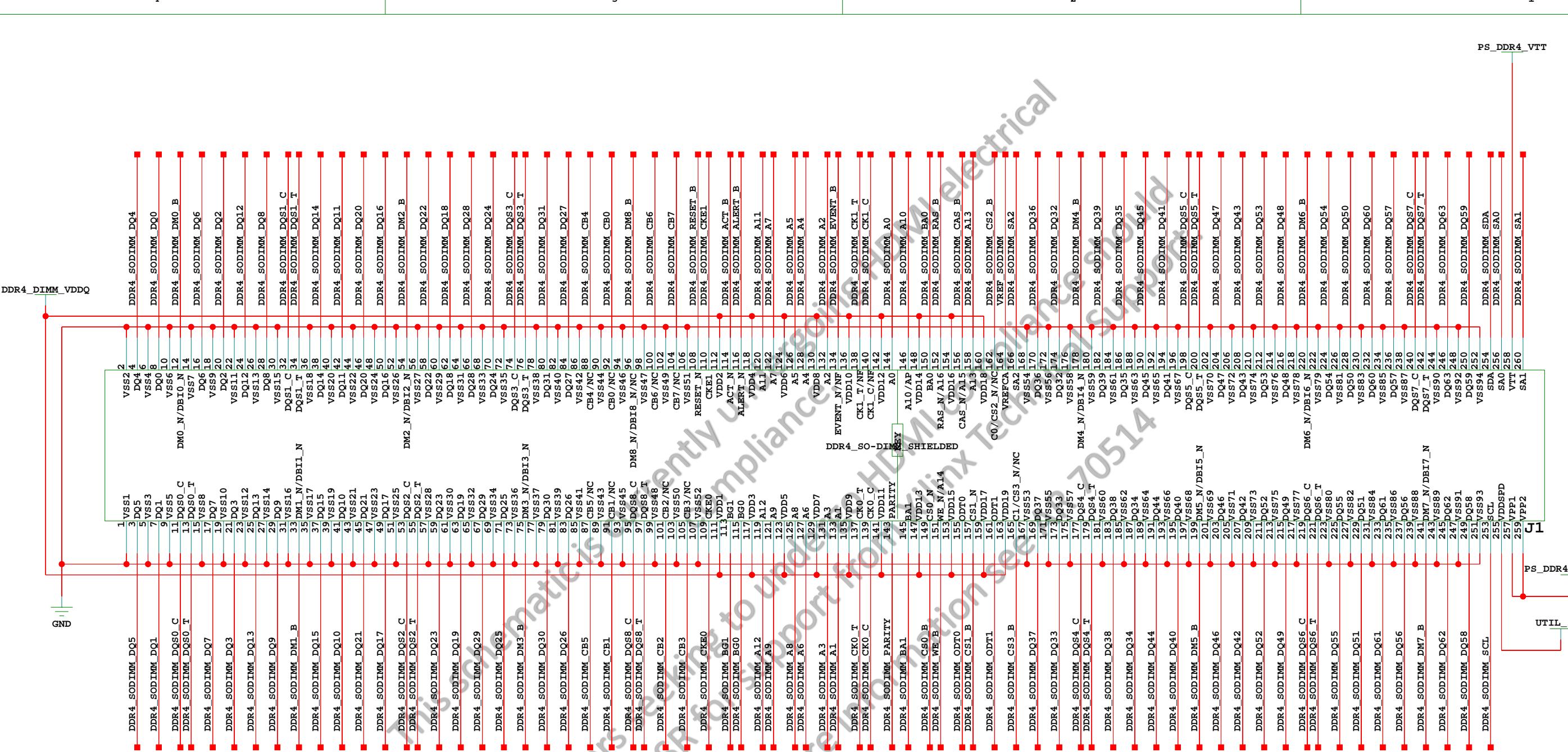
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 22 OF 95	DRAWN BY: BF



JTAG Headers

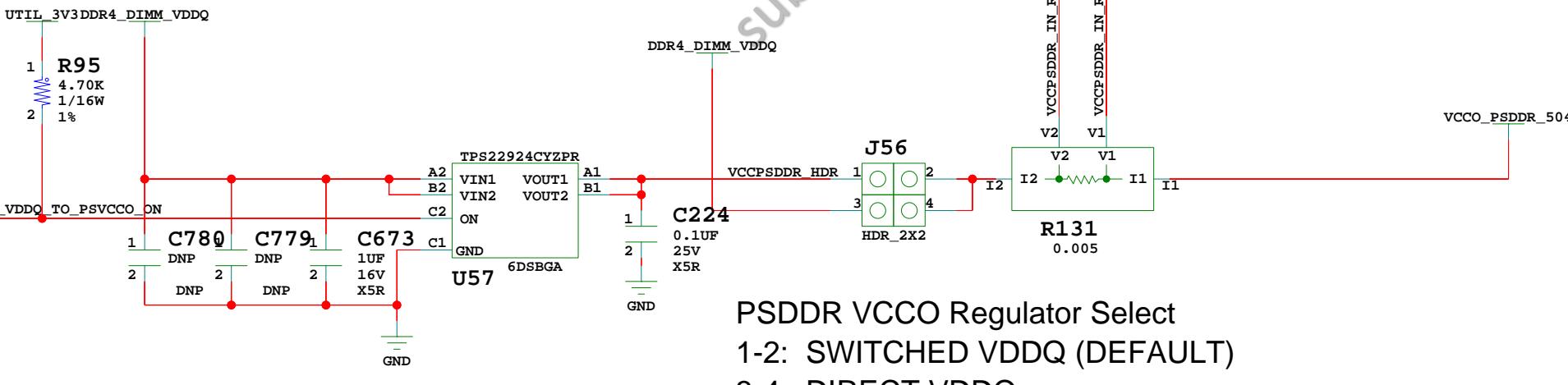
S XIII INX

TITLE: JTAG Headers SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16		VER: 1.0
SHEET SIZE: B		REV: 01
SHEET 23	OF 95	DRAWN BY: BF

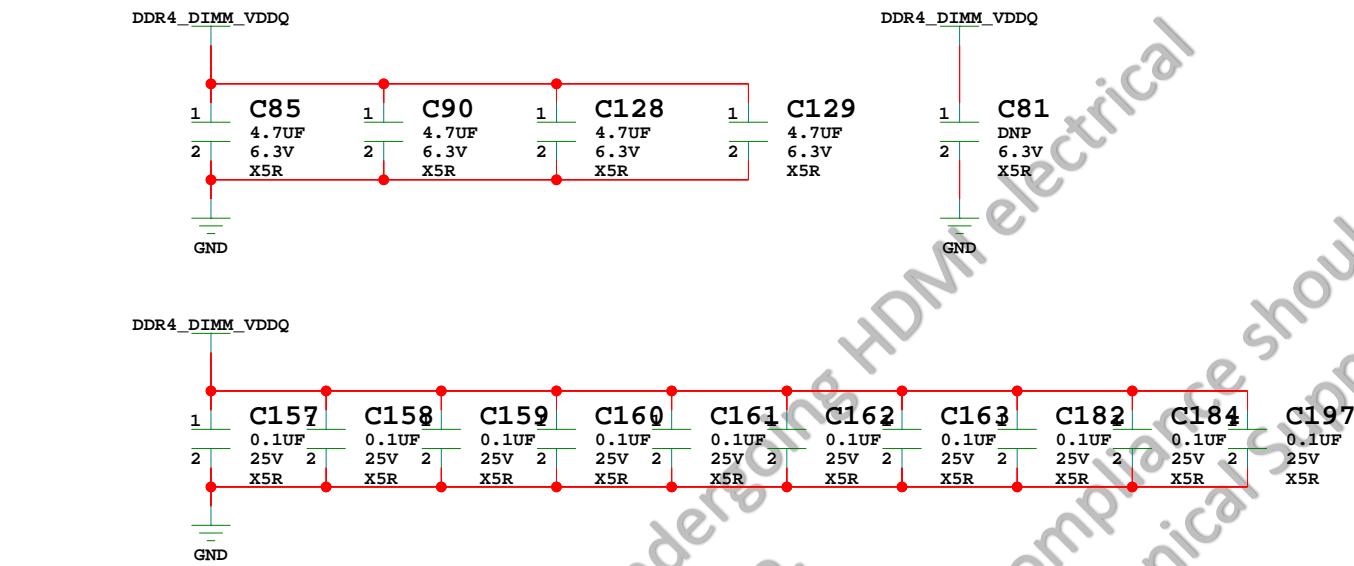
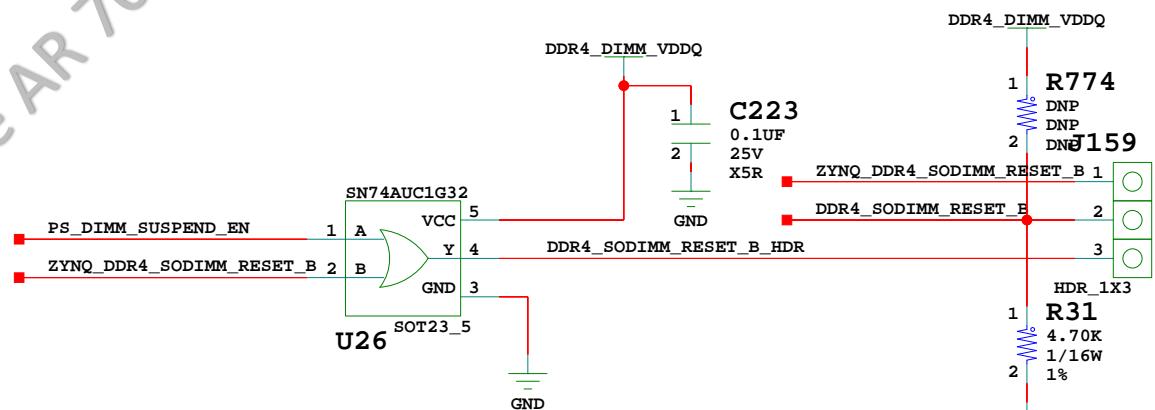


PLACE ABOVE CAPS BENEATH/CLOSE TO DIMM SOCKET

DDR DIMM VCCO DISABLE



DDR DIMM RESET_B CONTROL



XILINX

TITLE: PS DDR4 SODIMM Decoupling
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

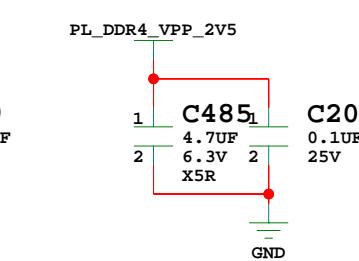
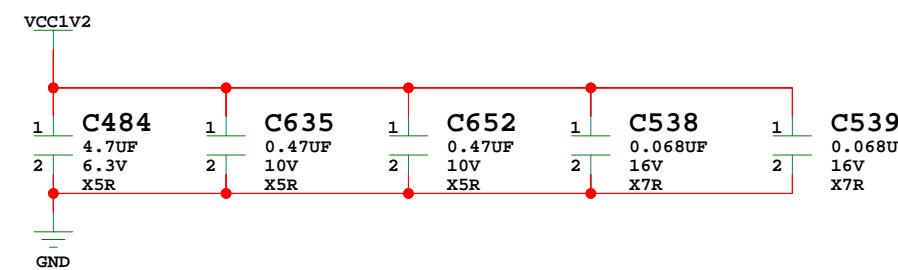
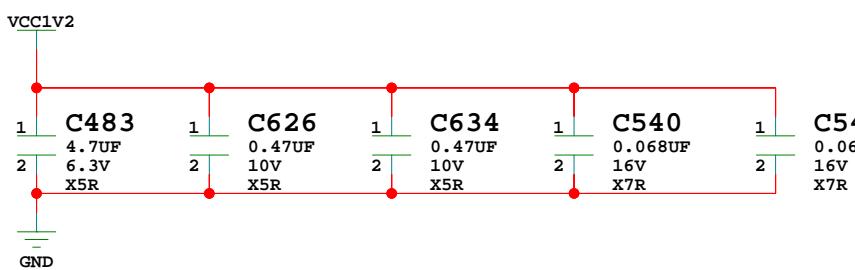
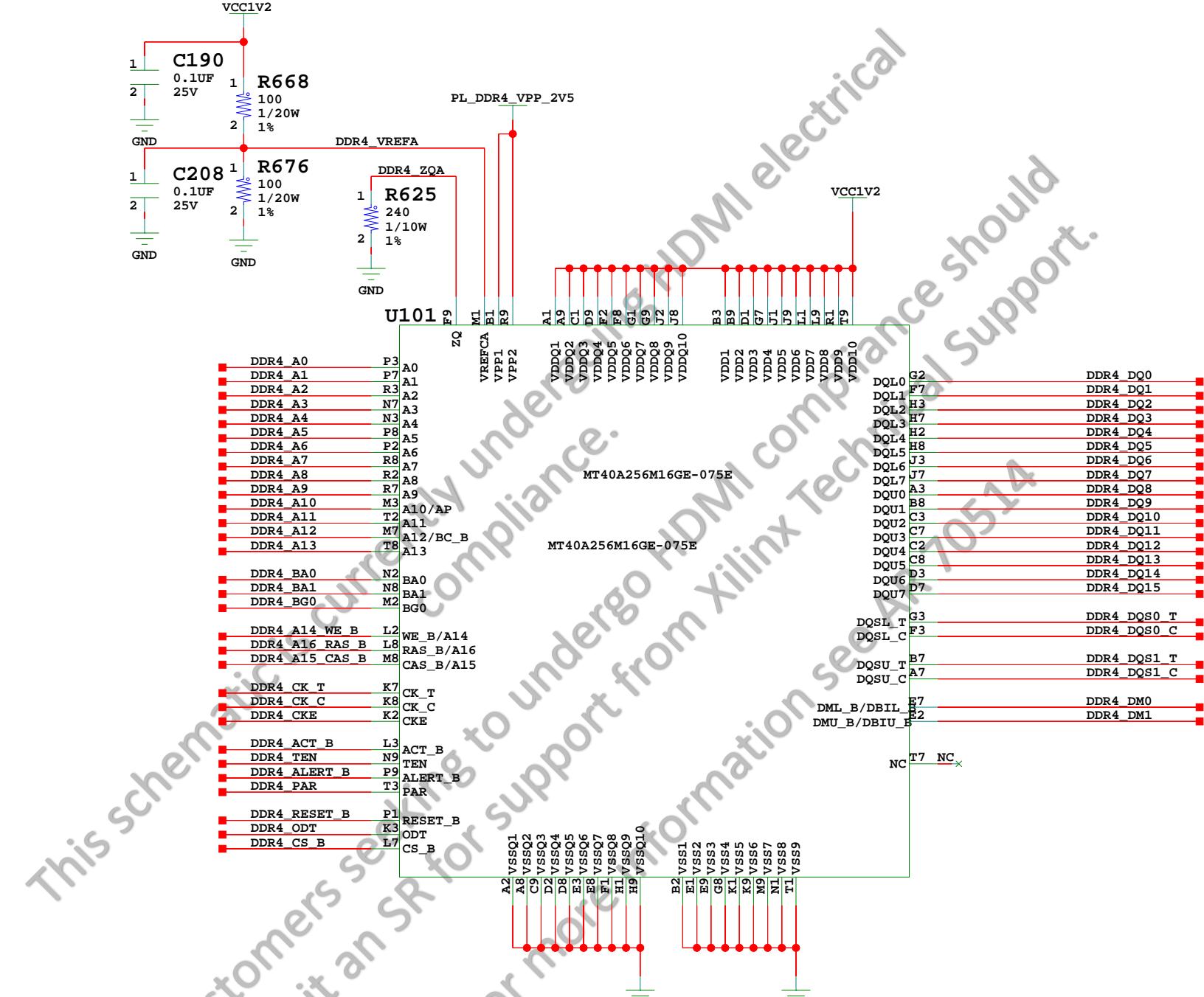
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 25 OF 95

DRAWN BY: BF



PL Component DDR4 Data [15-0]

TITLE: PL Component DDR4 Data [15-0]
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

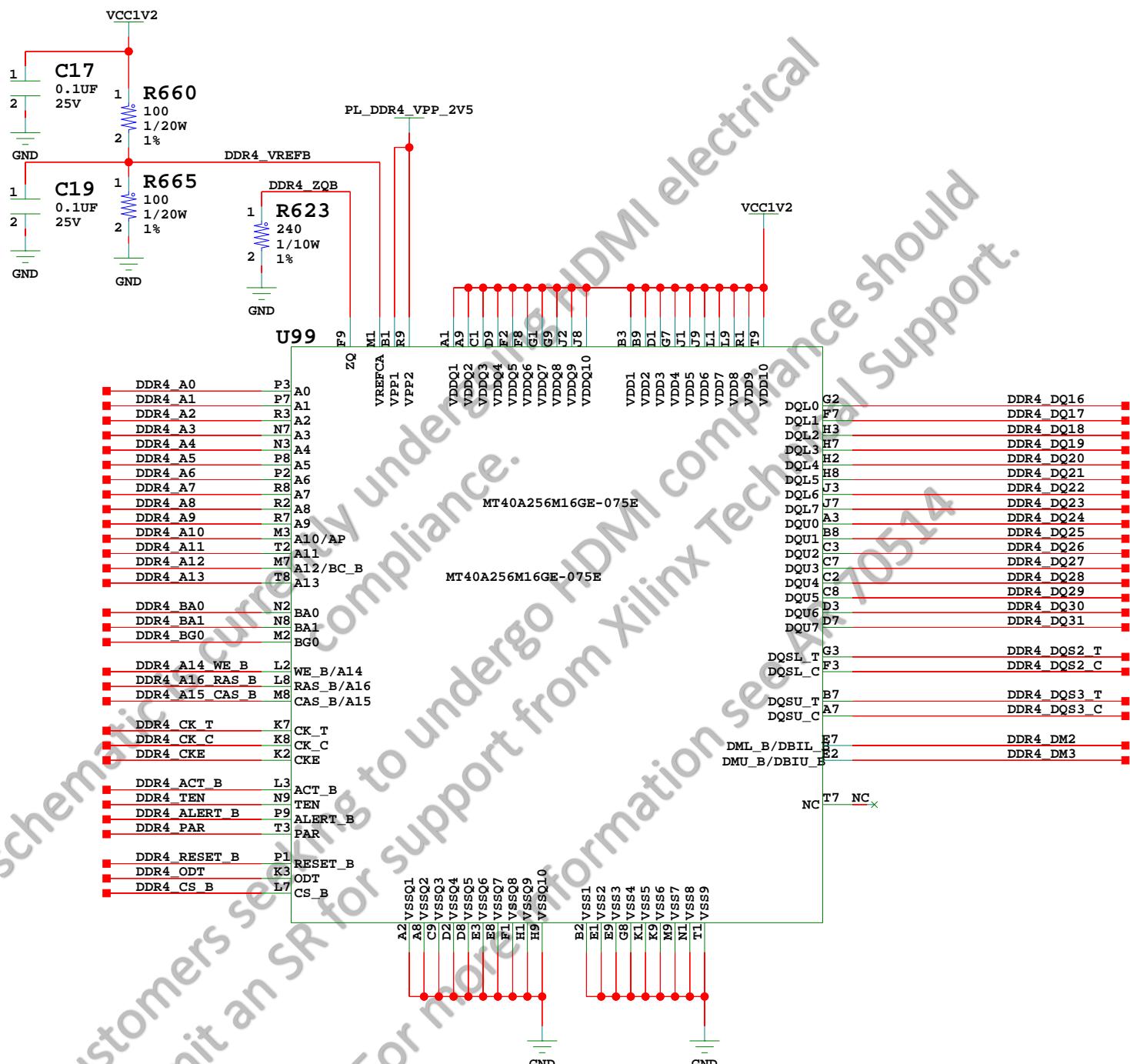
DATE: 01/08/2018:10:16

VER: 1.0

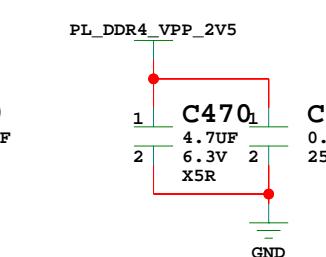
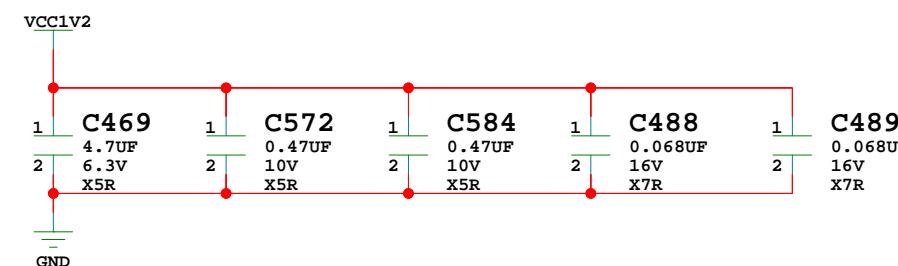
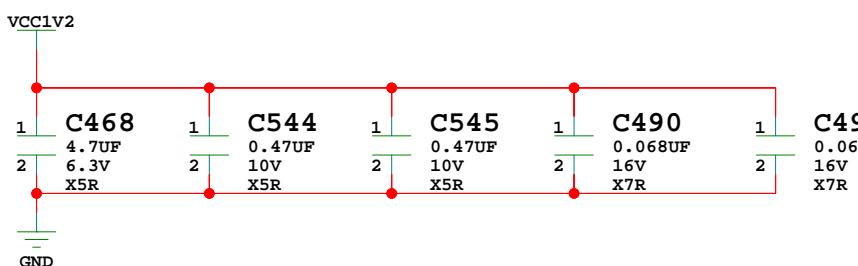
SHEET SIZE: B

REV: 01

SHEET 26 OF 95 DRAWN BY: BF



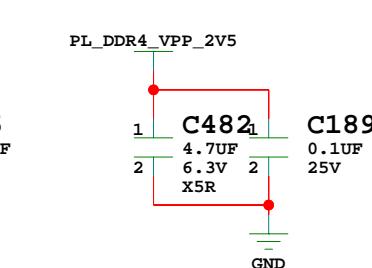
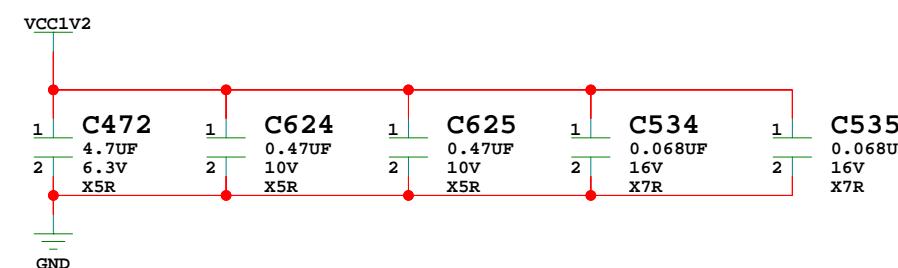
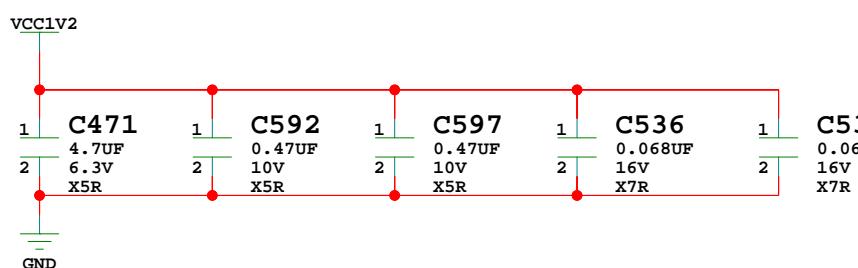
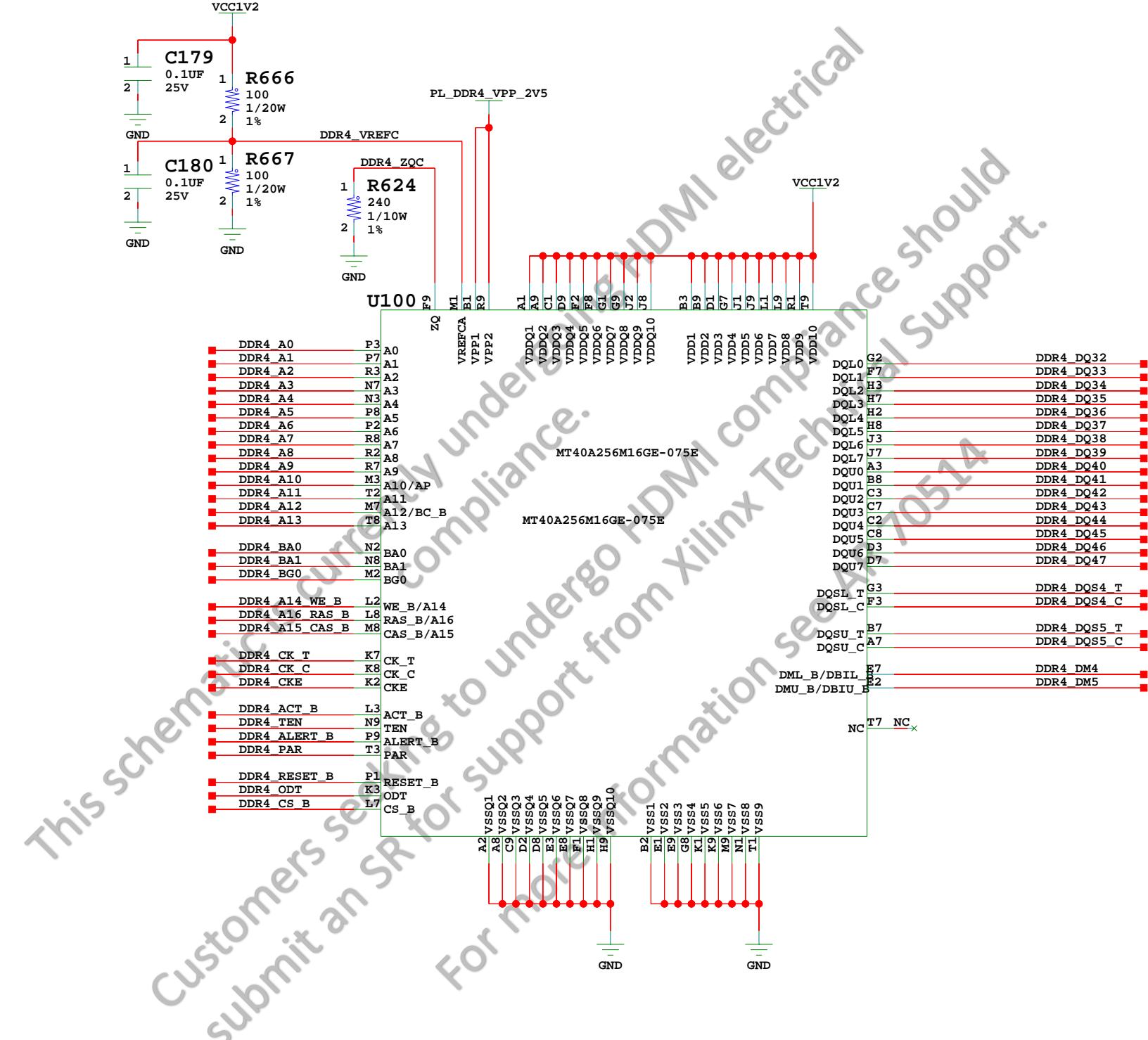
This schematic currently undergoes HDMI compliance testing.
Customers seeking to undergo HDMI compliance testing should submit an SR for support from Xilinx Tech Support.
For more information see MT-10514



PL Component DDR4 Data [31-16]



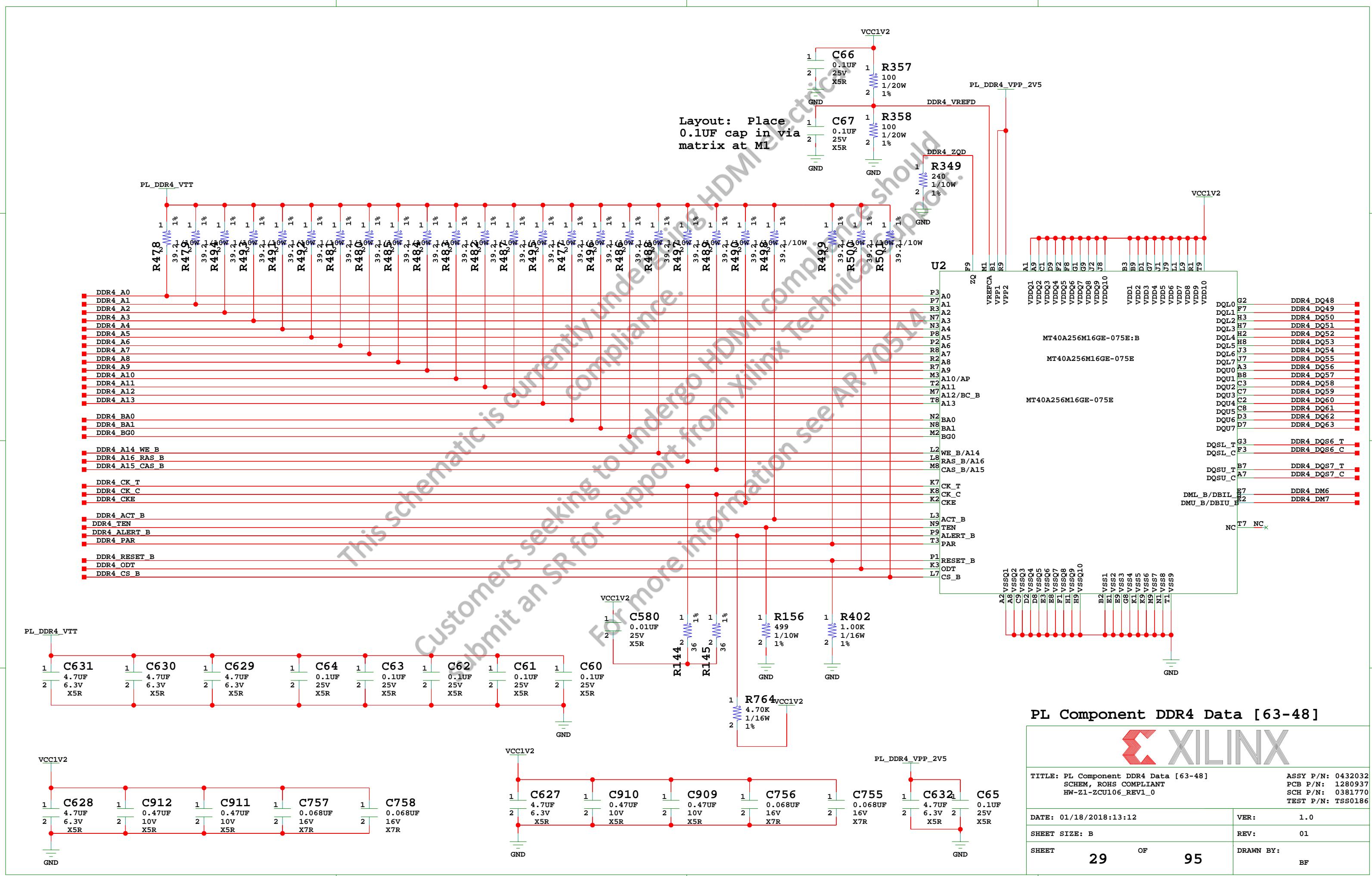
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DATE: 01/08/2018:10:16	VER: 1.0
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SHEET 27 OF 95	DRAWN BY: BF

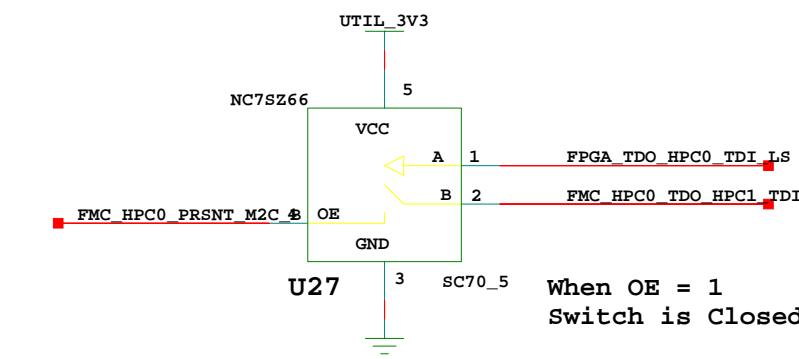
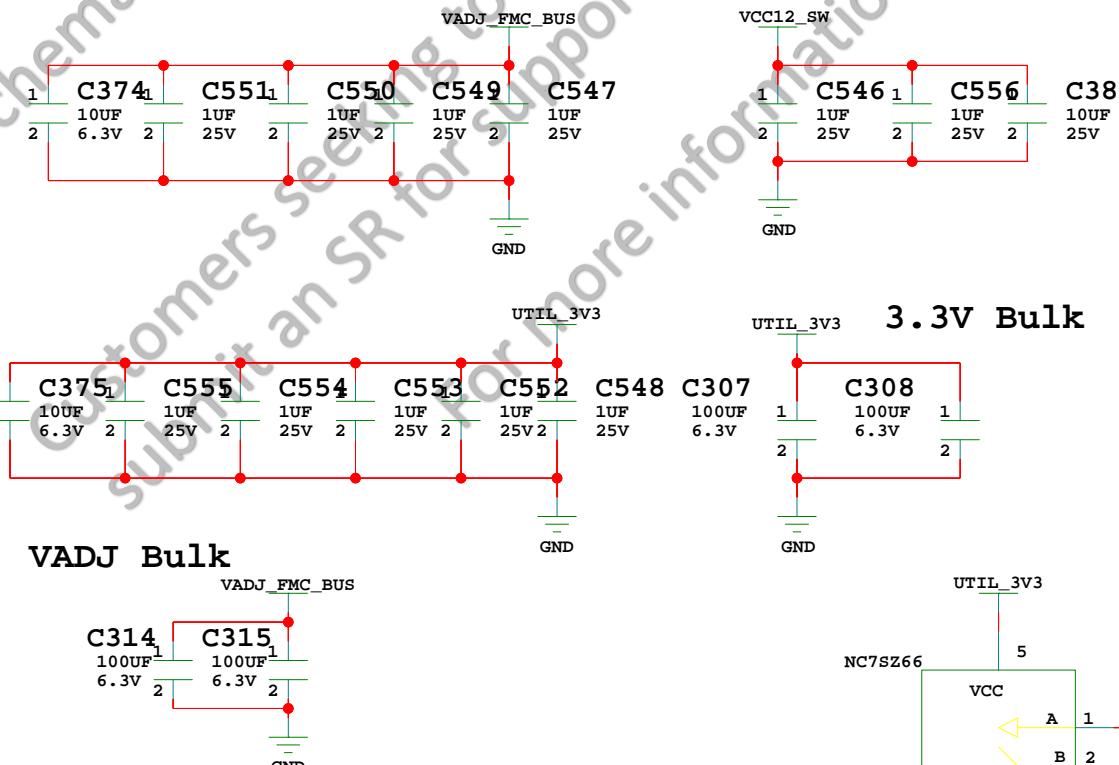
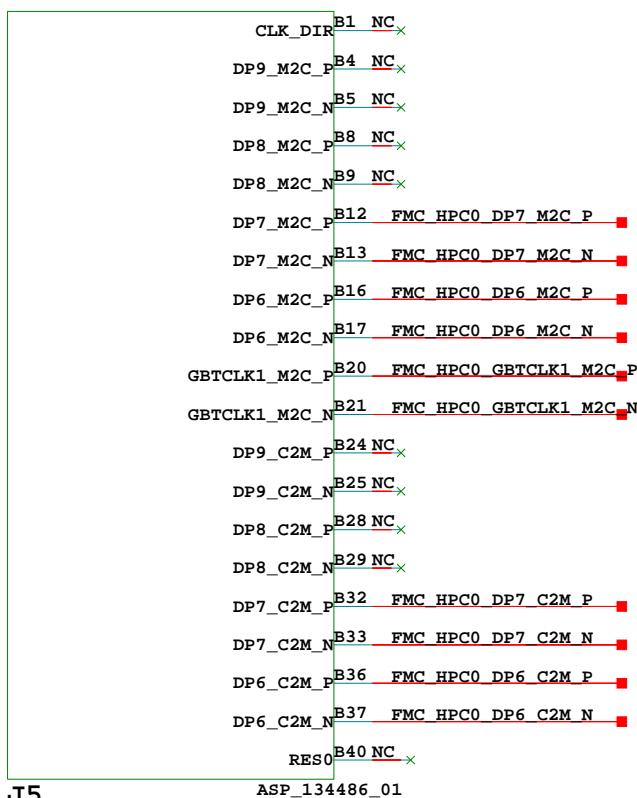
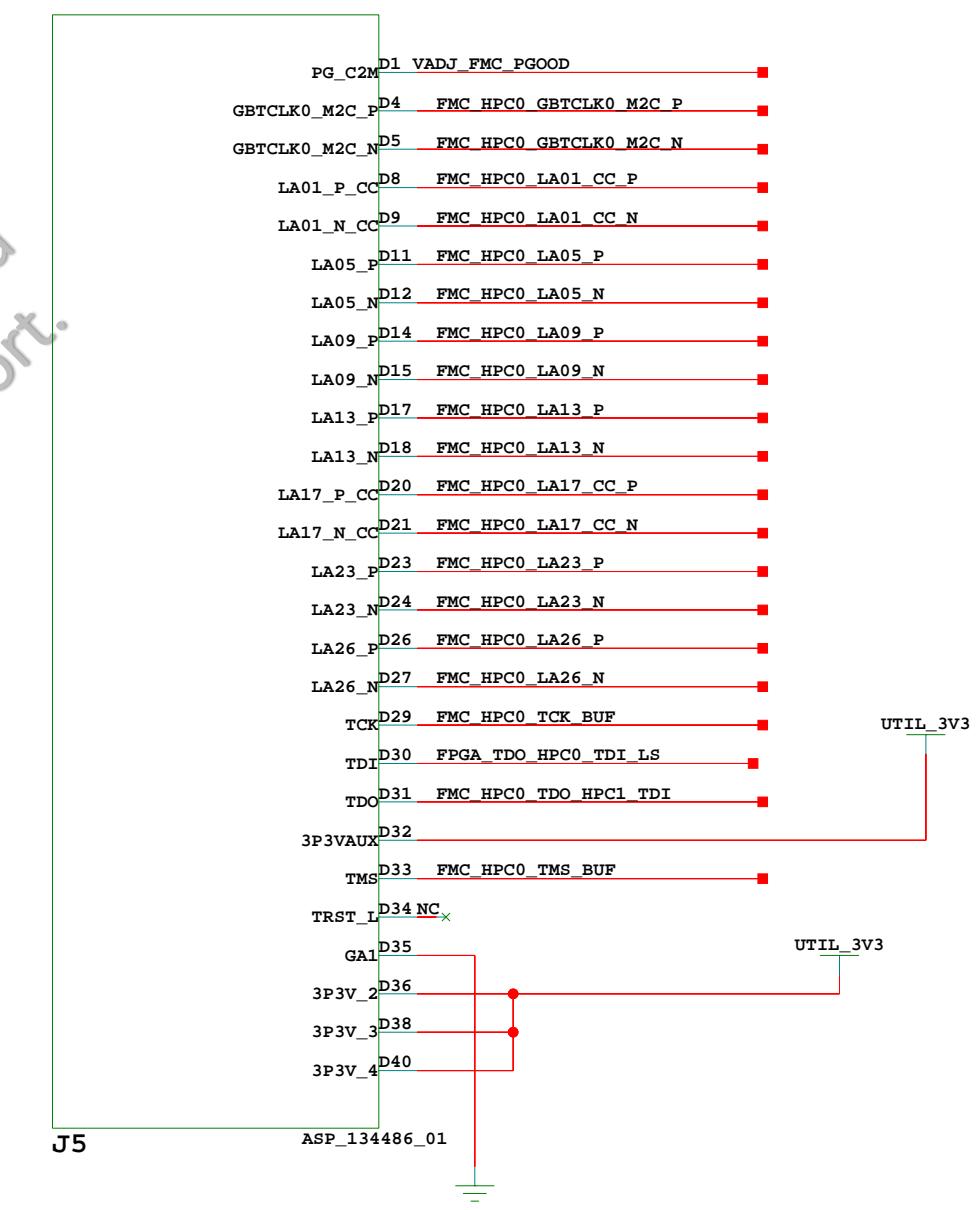
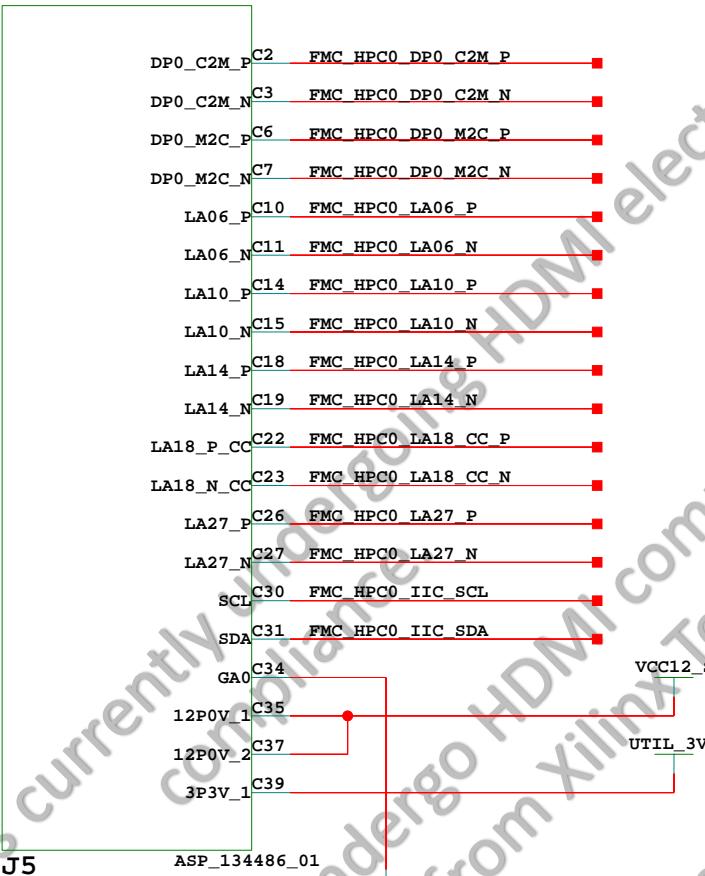
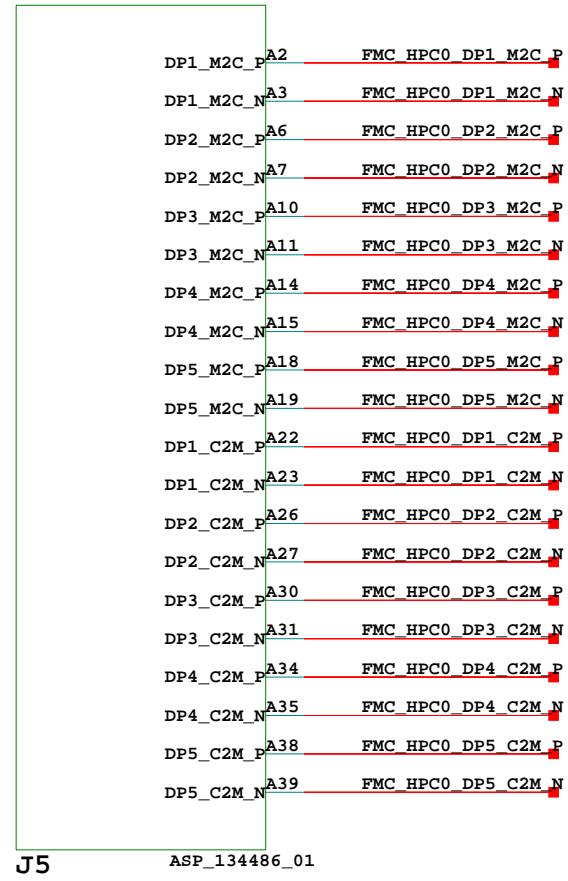


PL Component DDR4 Data [47-32]



TITLE: PL Component DDR4 Data [47-32] SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16		VER: 1.0
SHEET SIZE: B		REV: 01
SHEET 28 OF 95		DRAWN BY: BF





ANSI/VITA 57.1 - Revised 2010 PL FMC HPC0 Header Rows A B C D

XILINX

TITLE: PL FMC HPC0 Header Rows A B C D
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

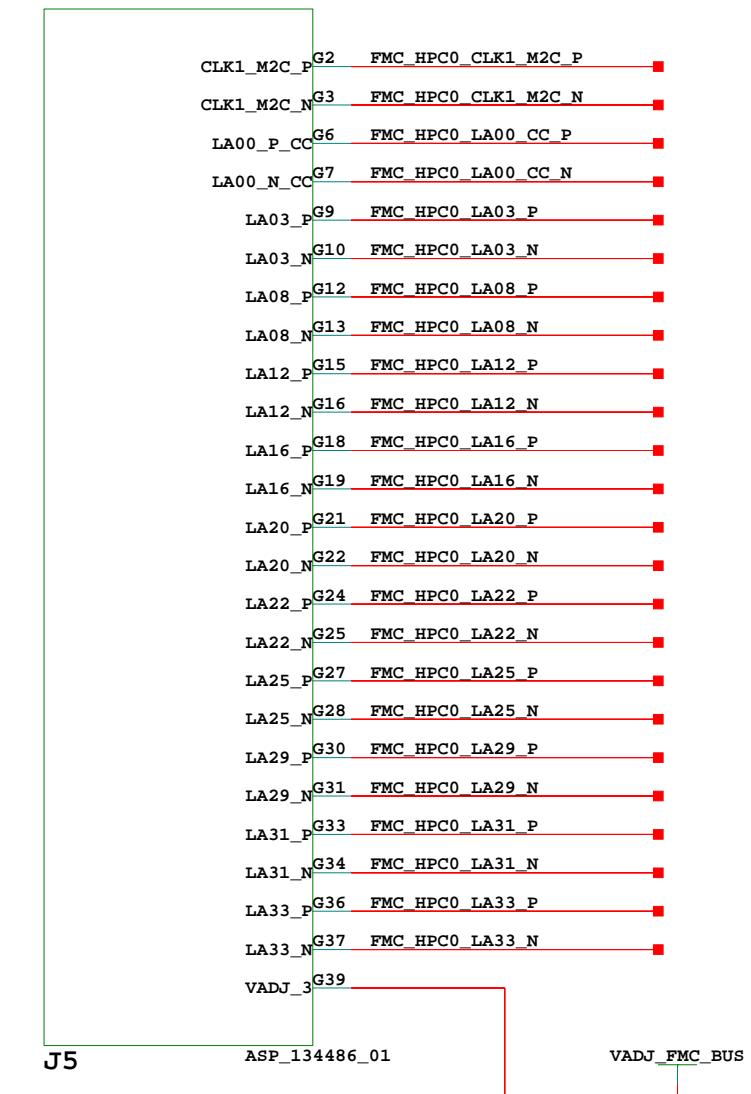
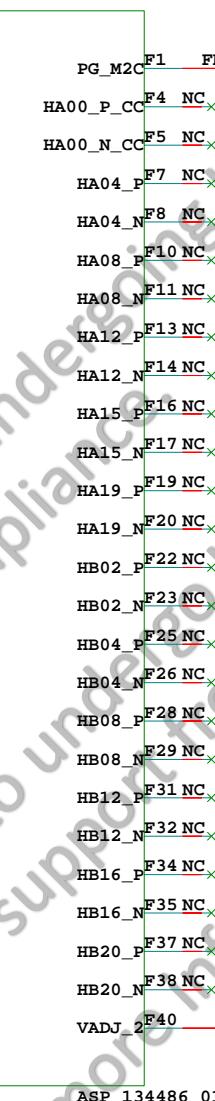
SHEET SIZE: B

REV: 01

SHEET 30 OF 95

DRAWN BY: BF

This Schematic is currently
compliant to undergo HDMI compliance should
customers see fit to submit an SR for support from Xilinx Technical Support.
For more information see AR 70514

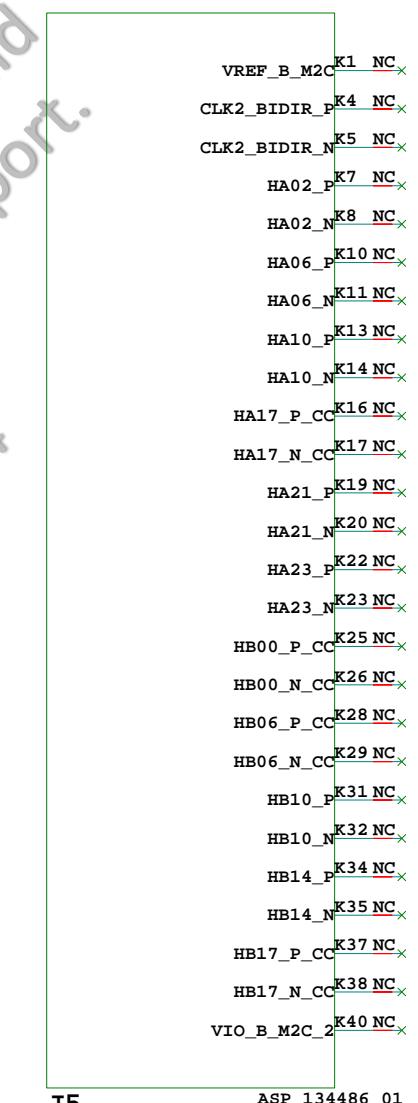


This schematic is currently under review for HDMI compliance.
Customers seeking to understand HDMI compliance should submit an SR for support from Xilinx Technical Support.
For more information see AR 70514

**ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows E F G**



TITLE: PL FMC HPC0 Header Rows E F G SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 31 OF 95	DRAWN BY: BF



ANSI/VITA 57.1 - Revised 2010
PL FMC HPC0 Header Rows H J K



TITLE: PL FMC HPC0 Header Rows H J K
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

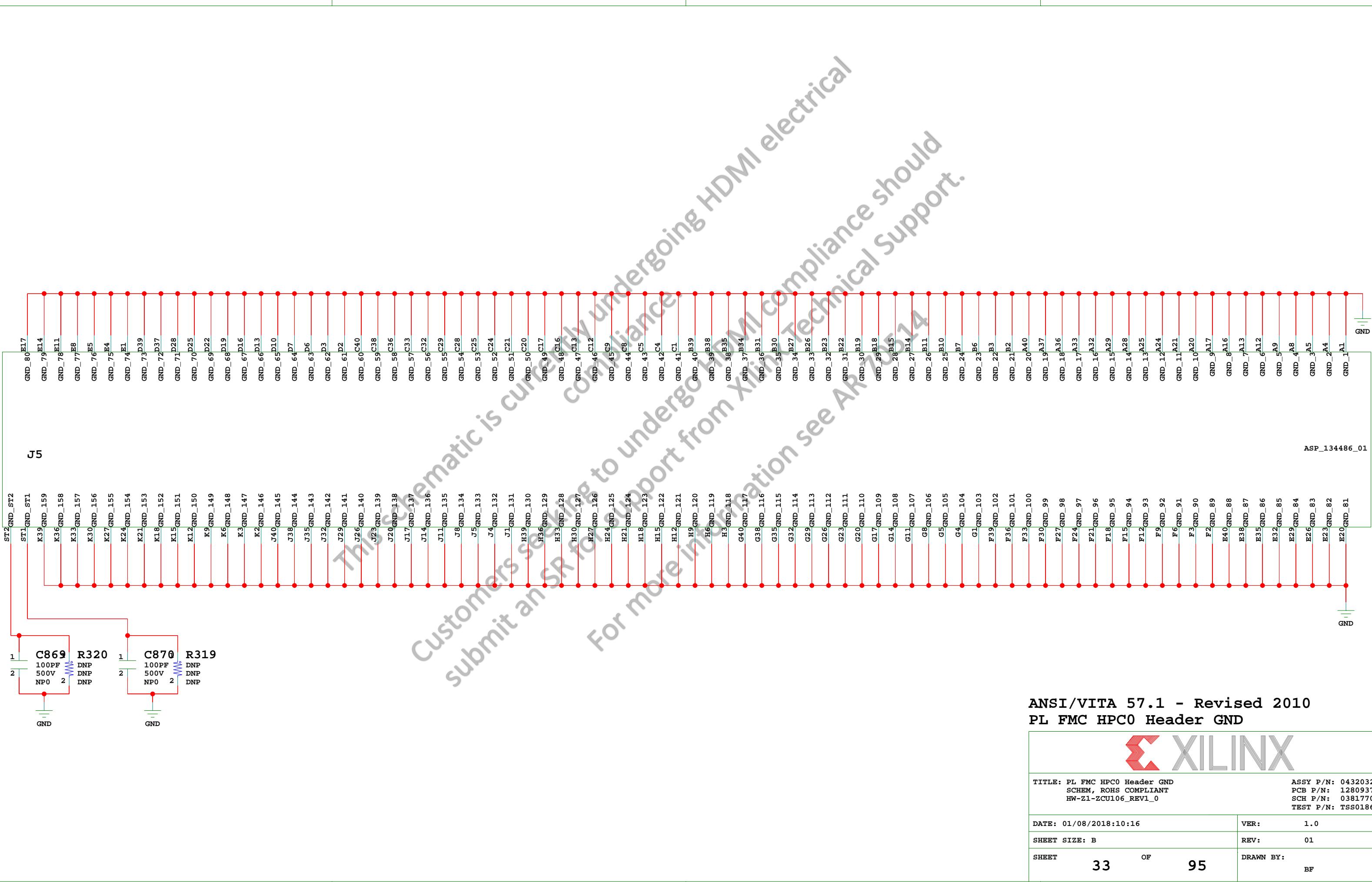
VER: 1.0

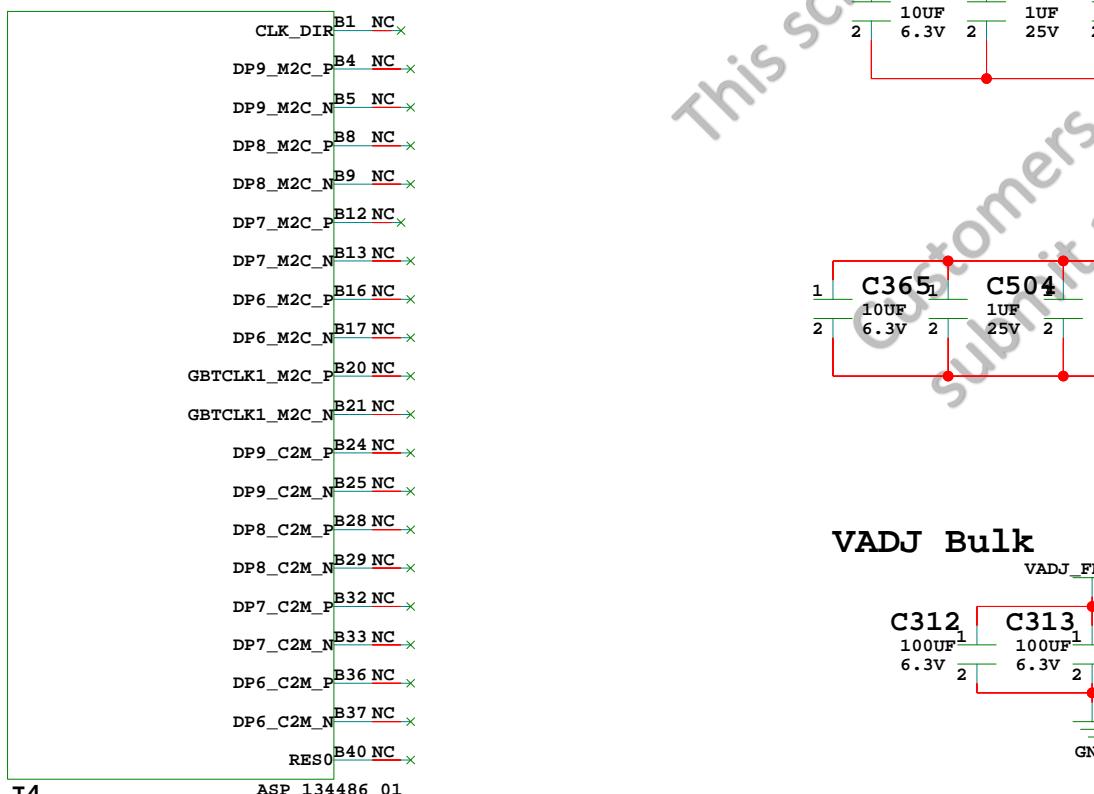
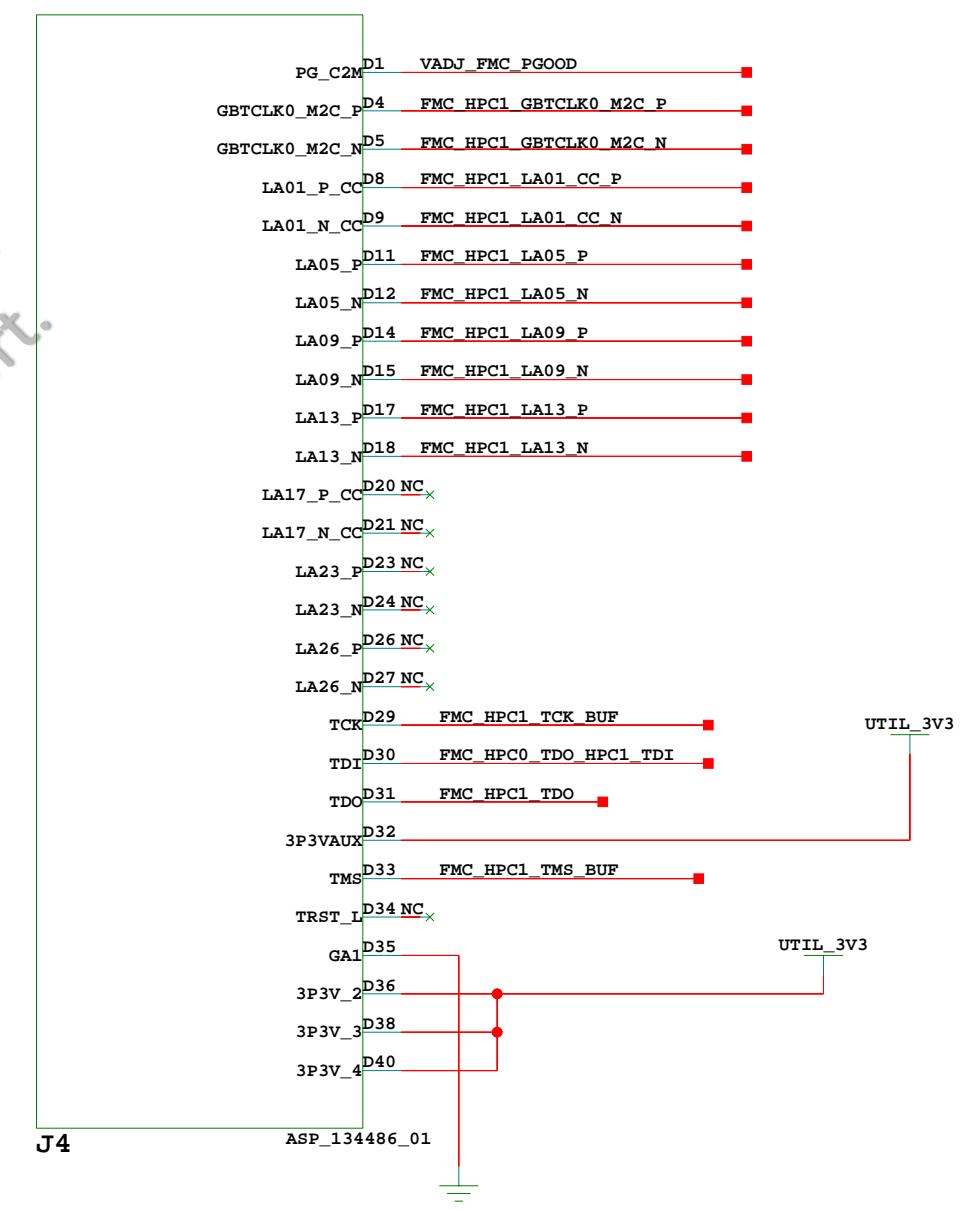
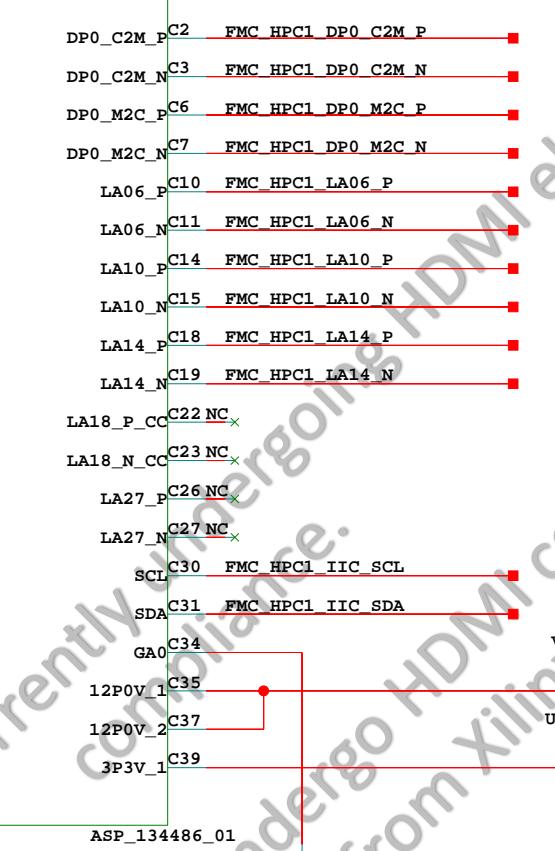
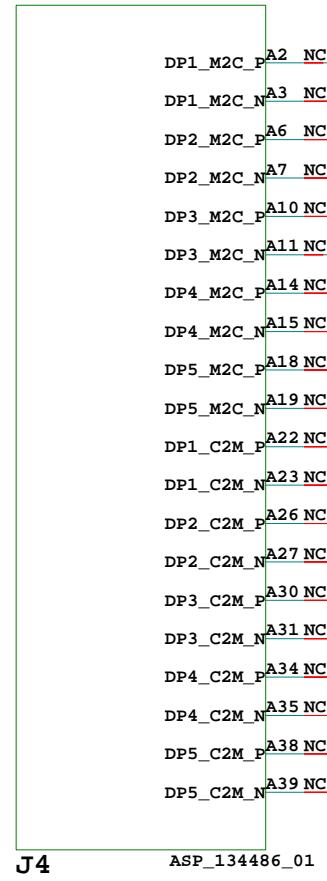
SHEET SIZE: B

REV: 01

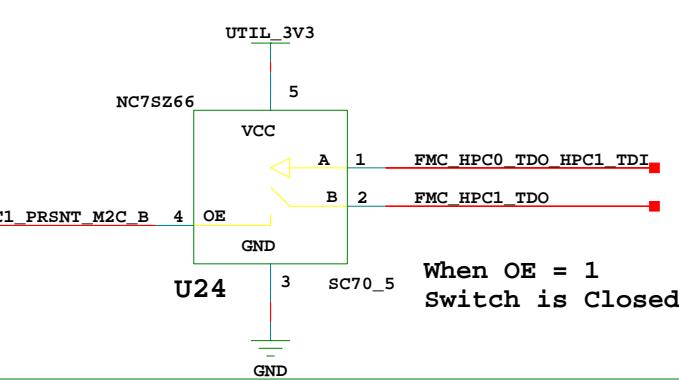
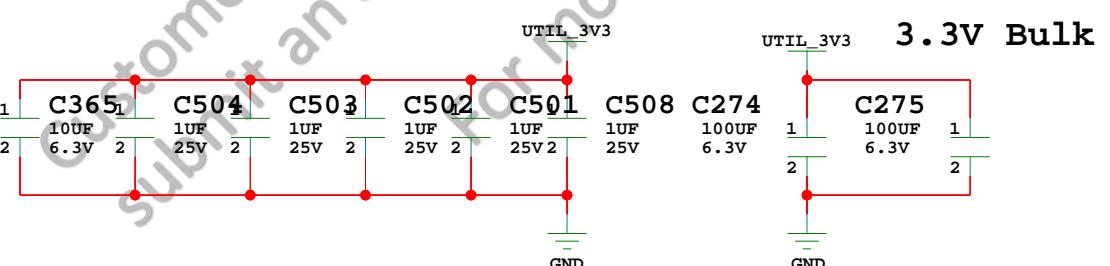
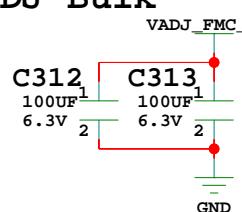
SHEET 32 OF 95

DRAWN BY:
BF





VADJ Bulk



ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows A B C D



TITLE: PL FMC HPC1 Header Rows A B C D
SCHEM, ROHS COMPLIANT
HW-21-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

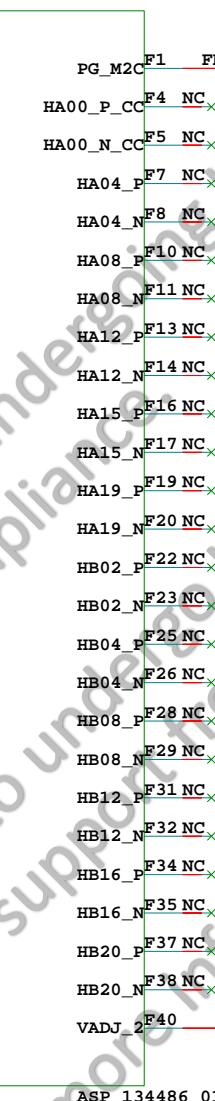
SHEET SIZE: B

REV: 01

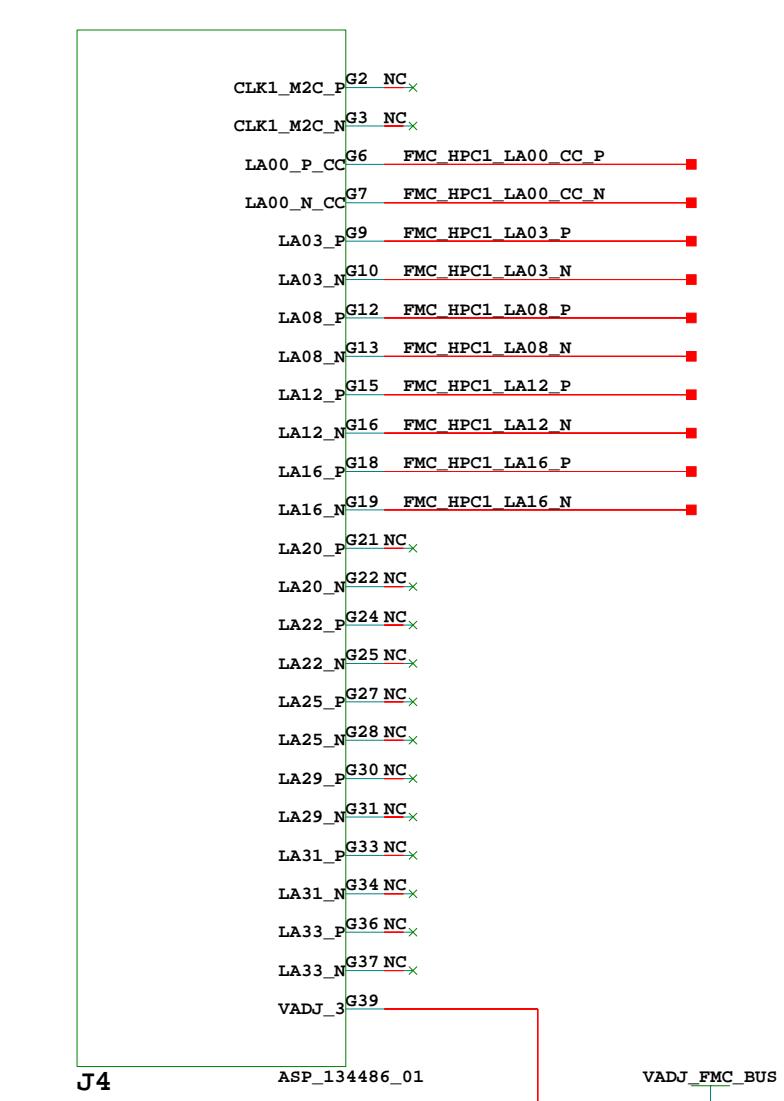
SHEET 34 OF 95

DRAWN BY: BF

This schematic is currently undergoing HDMI compliance should customers see fit to submit an SR for support from Xilinx Technical Support.



UTIL_3V3
R250
10.0K
1/10W
1%

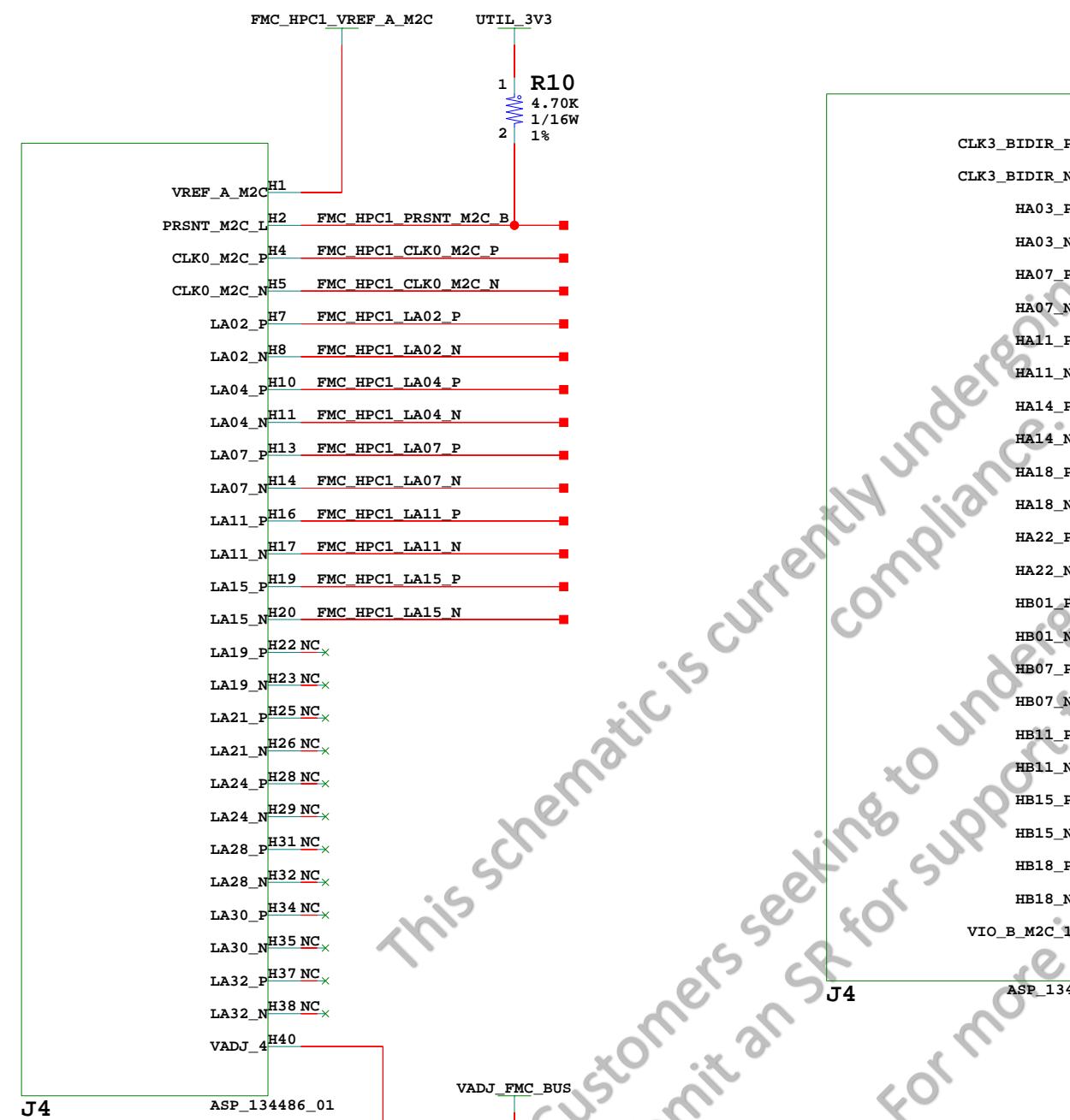


This schematic is currently under review for HDMI compliance.
Customers seeking to understand HDMI compliance should submit an SR for support. For more information see AR 70514.

ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows E F G



TITLE: PL FMC HPC1 Header Rows E F G SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 35 OF 95	DRAWN BY: BF



CLK3_BIDIR_P J2 NC
CLK3_BIDIR_N J3 NC
HA03_P J6 NC
HA03_N J7 NC
HA07_P J9 NC
HA07_N J10 NC
HA11_P J12 NC
HA11_N J13 NC
HA14_P J15 NC
HA14_N J16 NC
HA18_P J18 NC
HA18_N J19 NC
HA22_P J21 NC
HA22_N J22 NC
HB01_P J24 NC
HB01_N J25 NC
HB07_P J27 NC
HB07_N J28 NC
HB11_P J30 NC
HB11_N J31 NC
HB15_P J33 NC
HB15_N J34 NC
HB18_P J36 NC
HB18_N J37 NC
VIO_B_M2C_1 J39 NC
VIO_B_M2C_2 J40 NC

J4

ASP_134486_01

VREF_B_M2C K1 NC
CLK2_BIDIR_P K4 NC
CLK2_BIDIR_N K5 NC
HA02_P K7 NC
HA02_N K8 NC
HA06_P K10 NC
HA06_N K11 NC
HA10_P K13 NC
HA10_N K14 NC
HA17_P_CC K16 NC
HA17_N_CC K17 NC
HA21_P K19 NC
HA21_N K20 NC
HA23_P K22 NC
HA23_N K23 NC
HB00_P_CC K25 NC
HB00_N_CC K26 NC
HB06_P_CC K28 NC
HB06_N_CC K29 NC
HB10_P K31 NC
HB10_N K32 NC
HB14_P K34 NC
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HB17_N_CC K38 NC
VIO_B_M2C_2 K40 NC

J4

ASP_134486_01

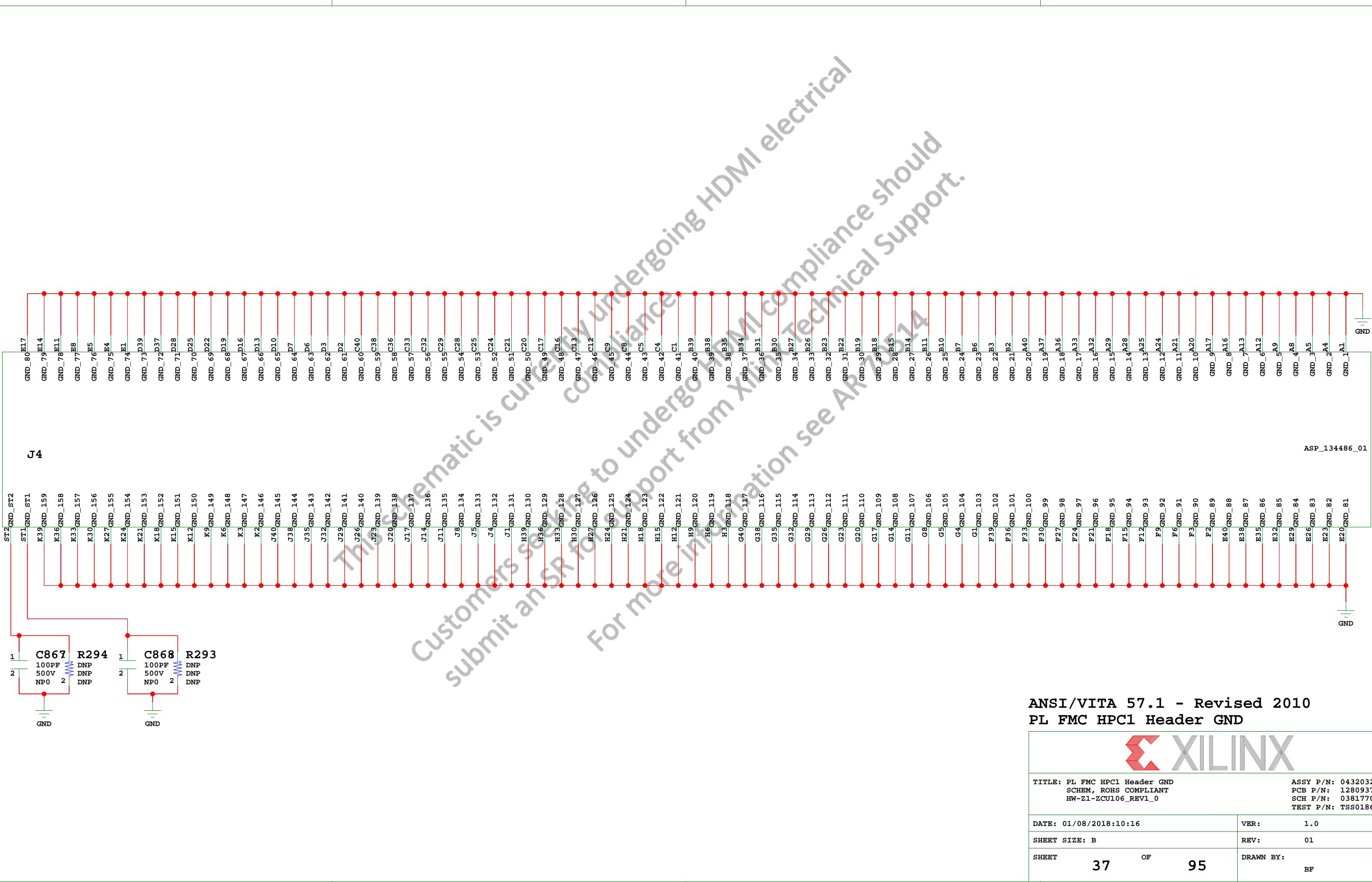
ANSI/VITA 57.1 - Revised 2010
PL FMC HPC1 Header Rows H J K

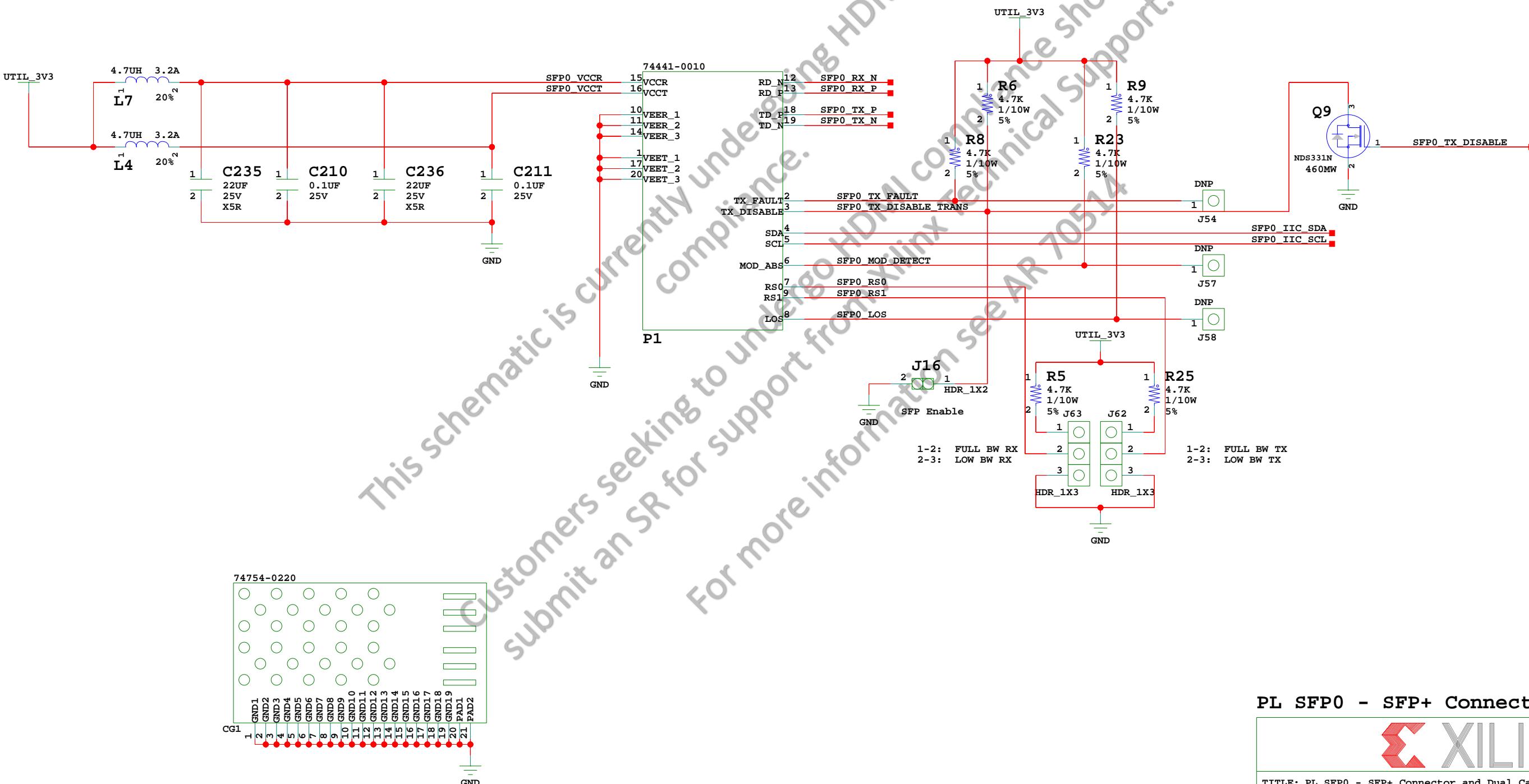


TITLE: PL FMC HPC1 Header Rows H J K
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 36 OF 95	DRAWN BY: BF

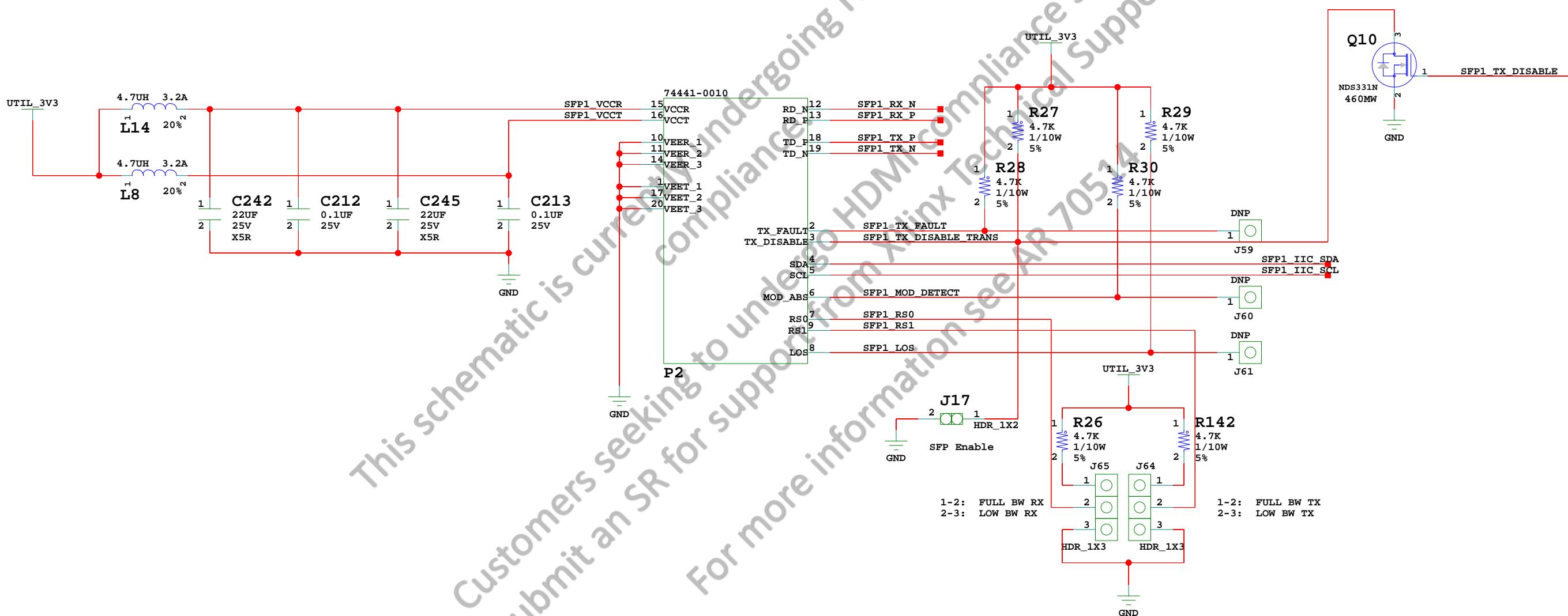




PL SFP0 - SFP+ Connector and Dual Cage



TITLE: PL SFP0 - SFP+ Connector and Dual Cage SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032
	PCB P/N: 1280937
	SCH P/N: 0381770
	TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 38 OF 95	DRAWN BY: BF



PL SFP1 - SFP+ Connector



TITLE: PL SFP1 - SFP+ Connector
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

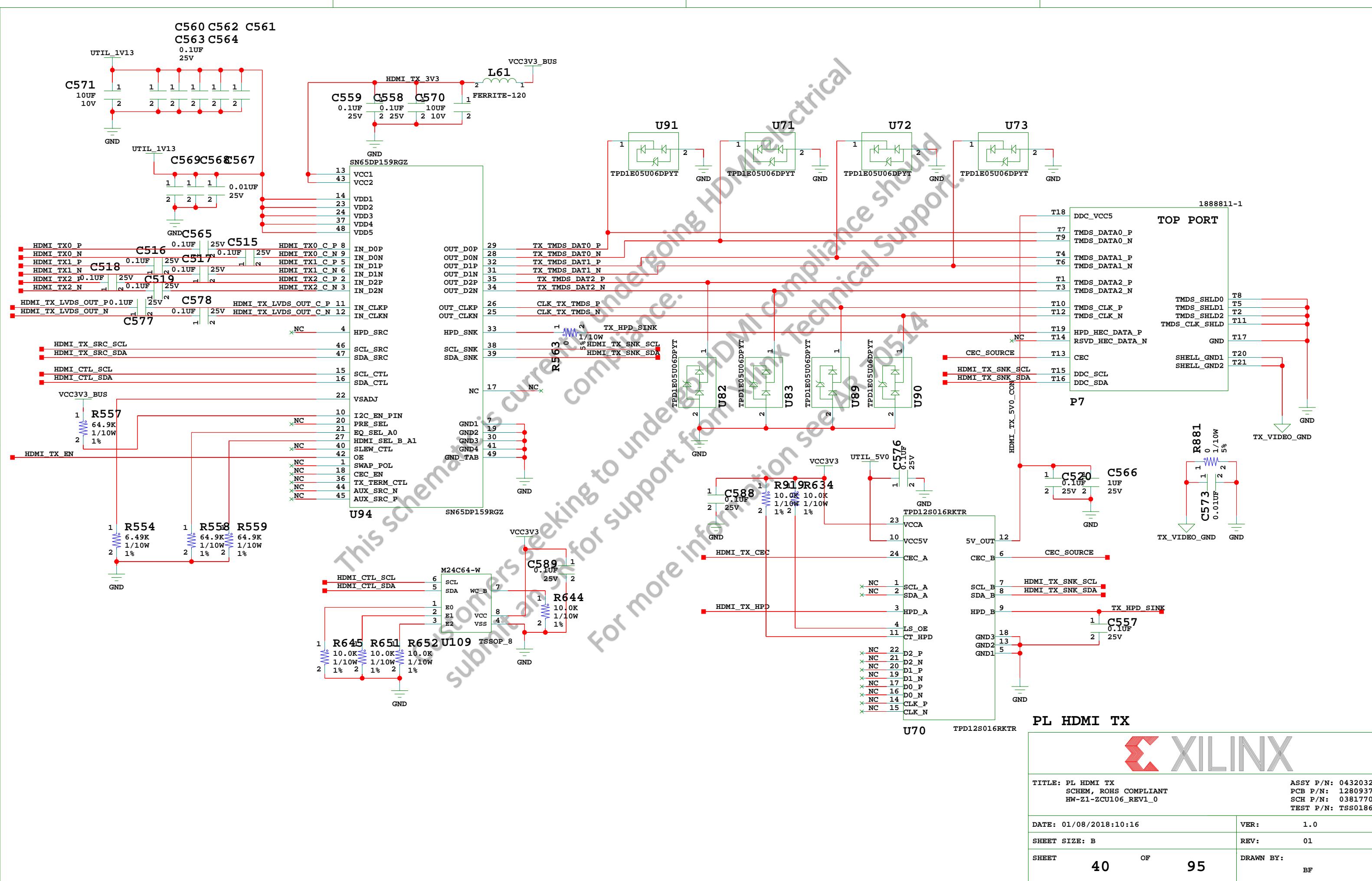
VER: 1.0

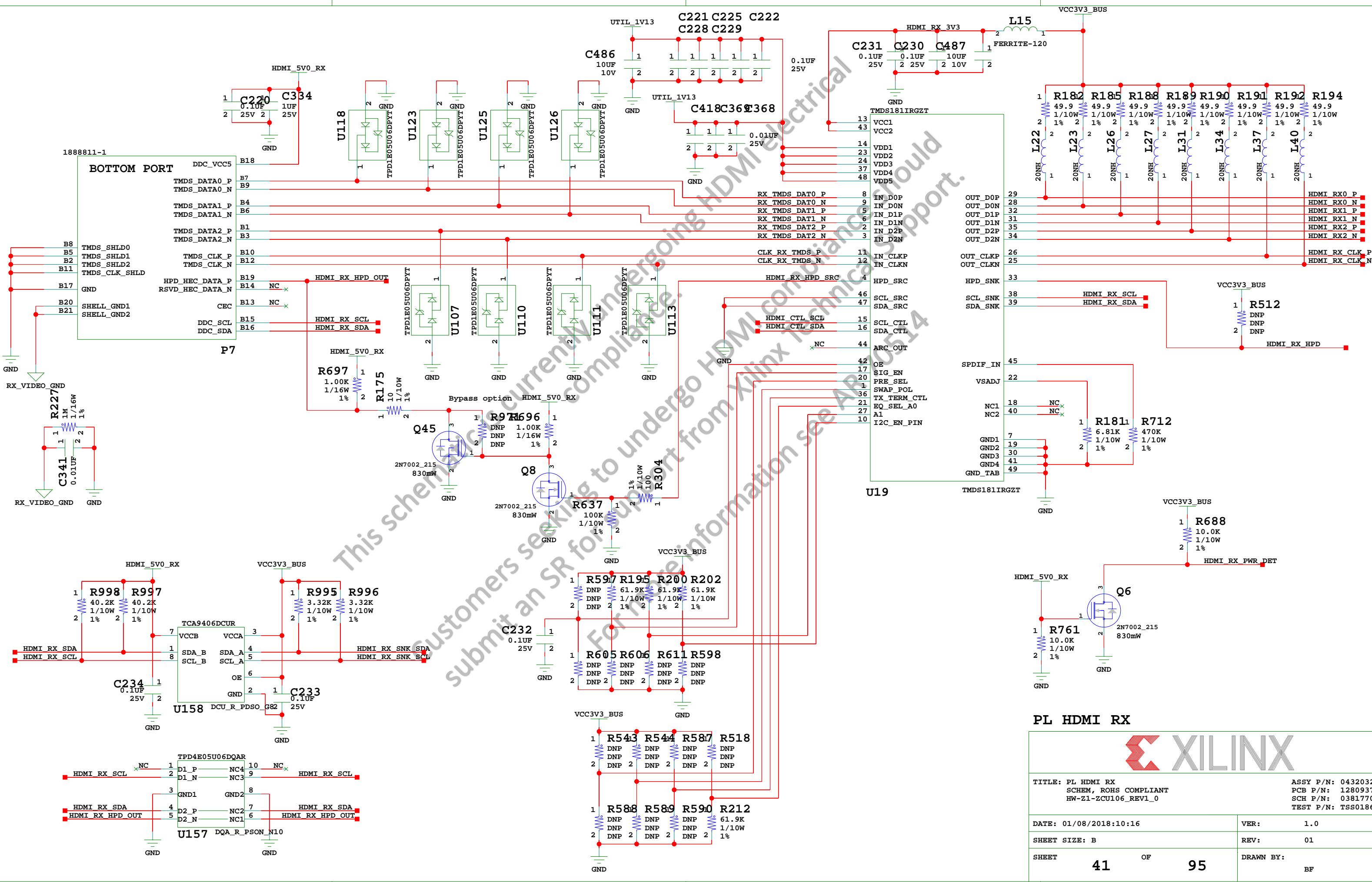
SHEET SIZE: B

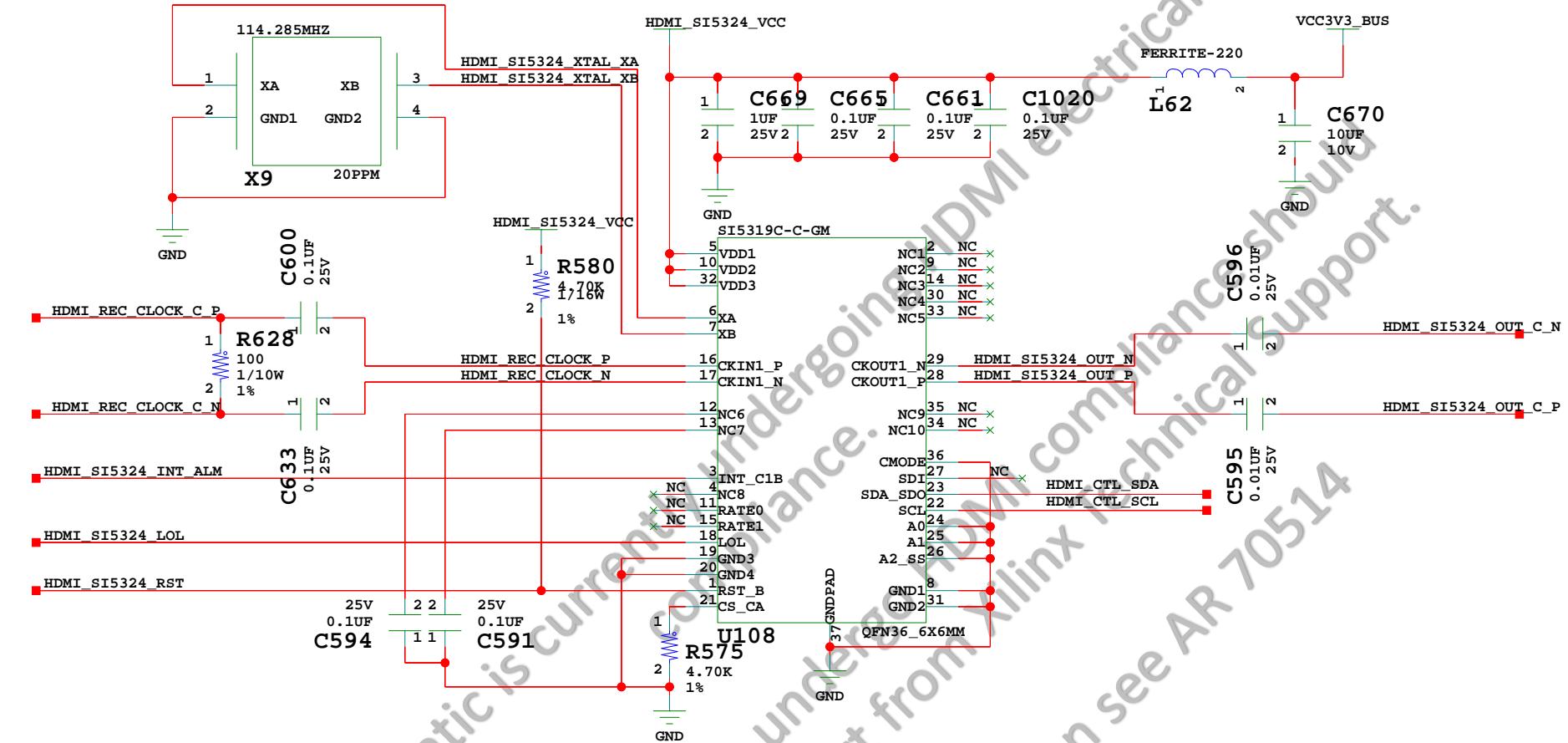
REV: 01

SHEET 39 OF 95

DRAWN BY:
BF







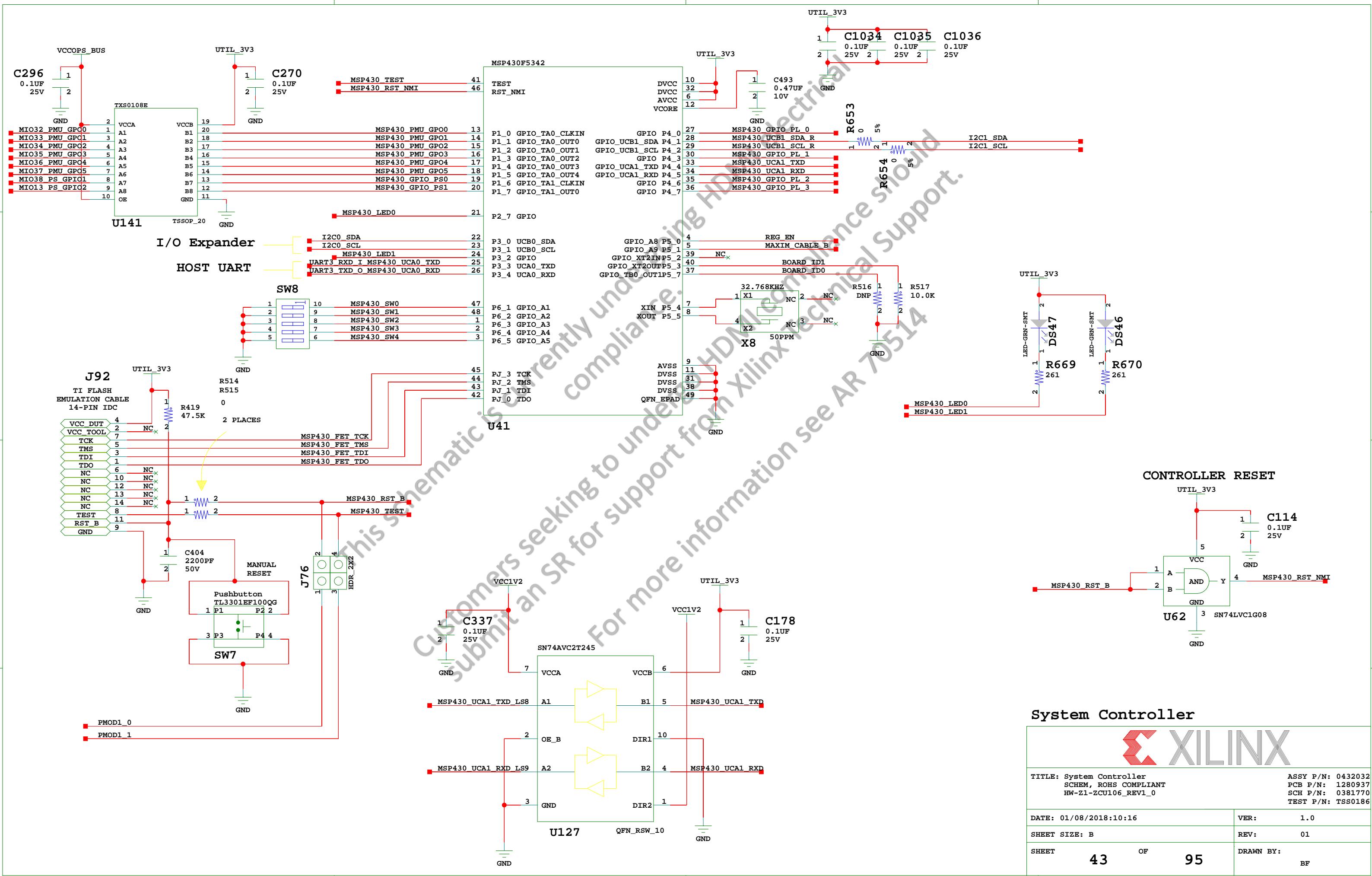
PL HDMI Clock Recovery

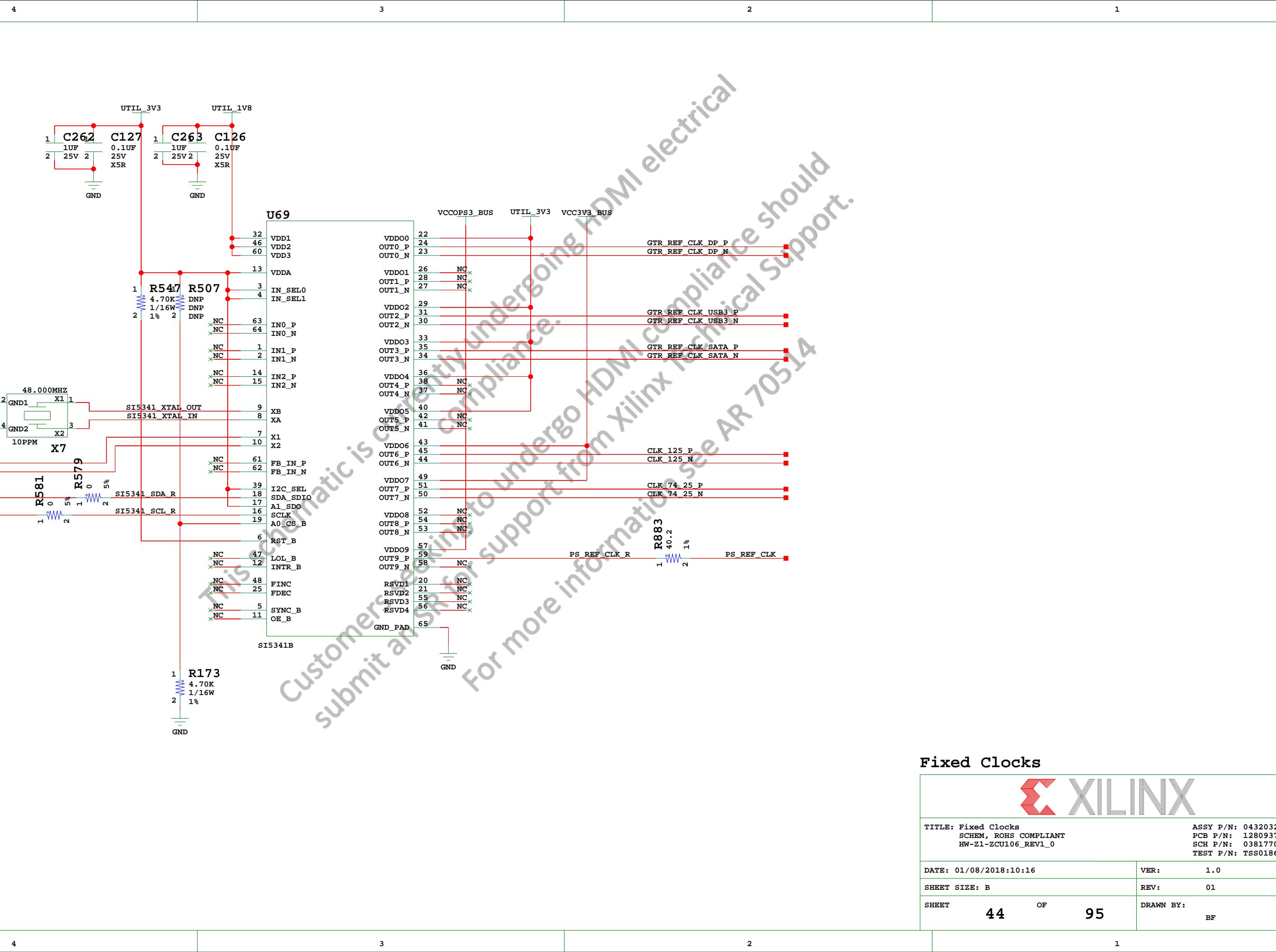


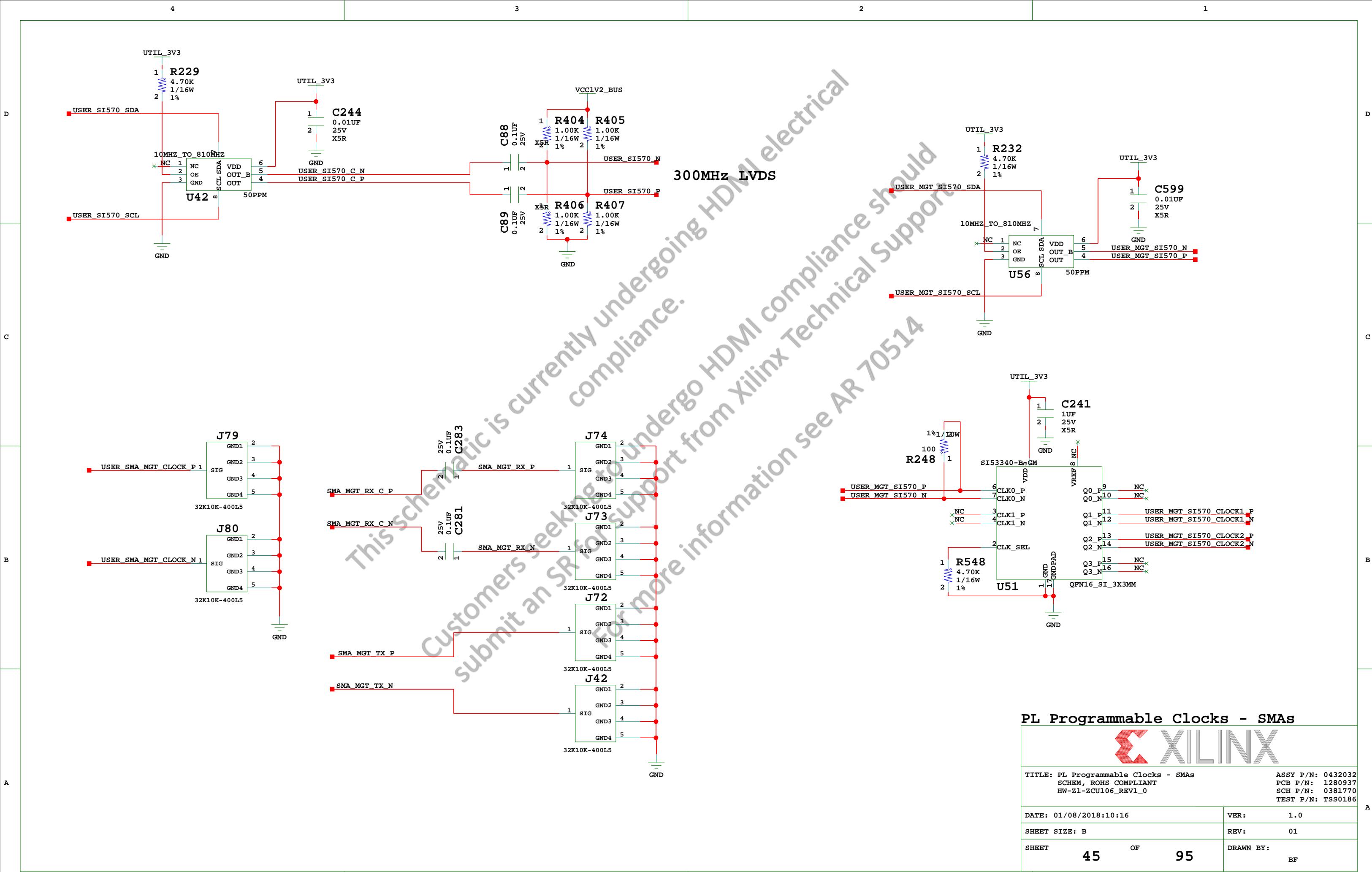
TITLE: PL HDMI Clock Recovery
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

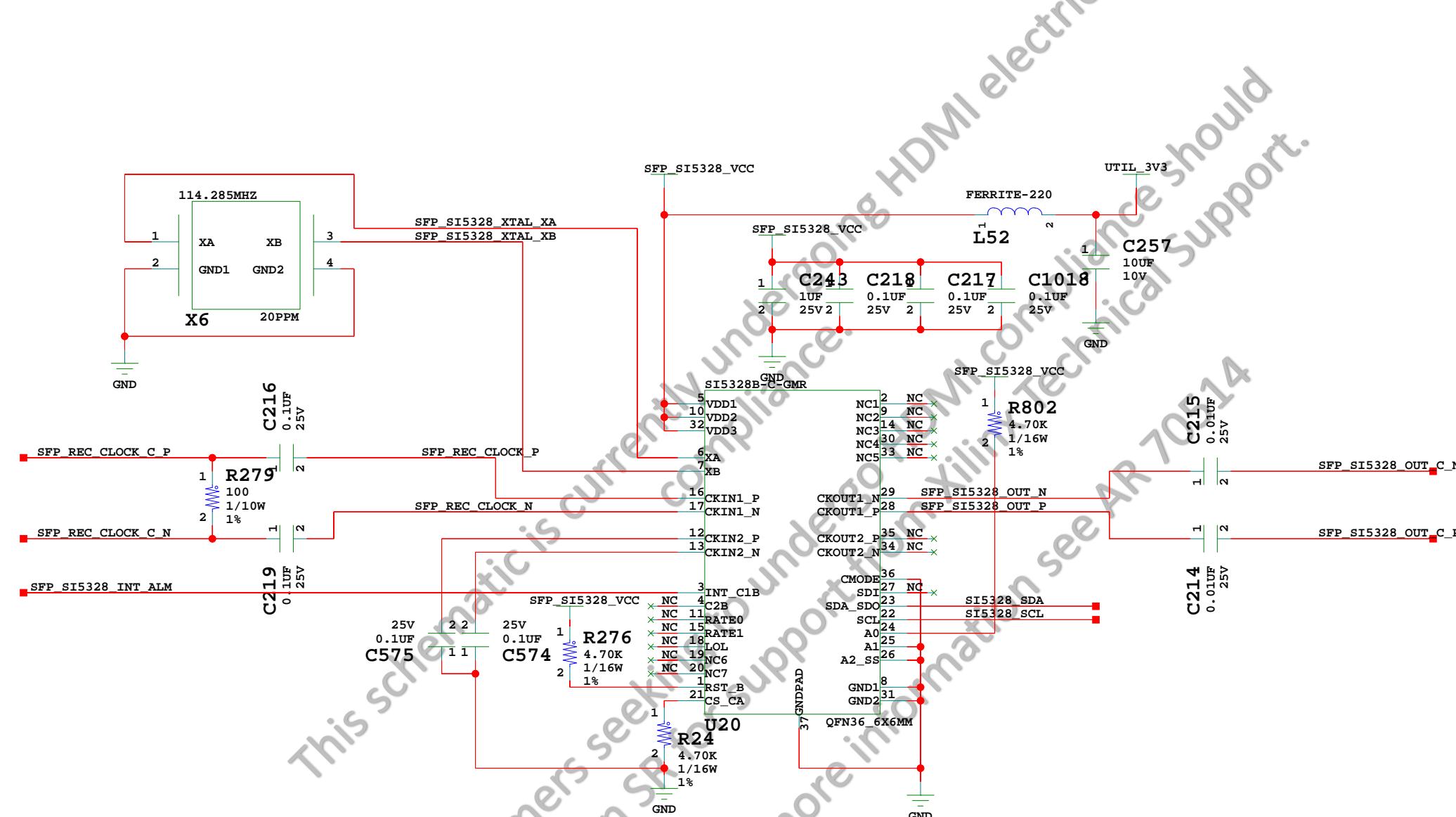
ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 42 OF 95	DRAWN BY: BF









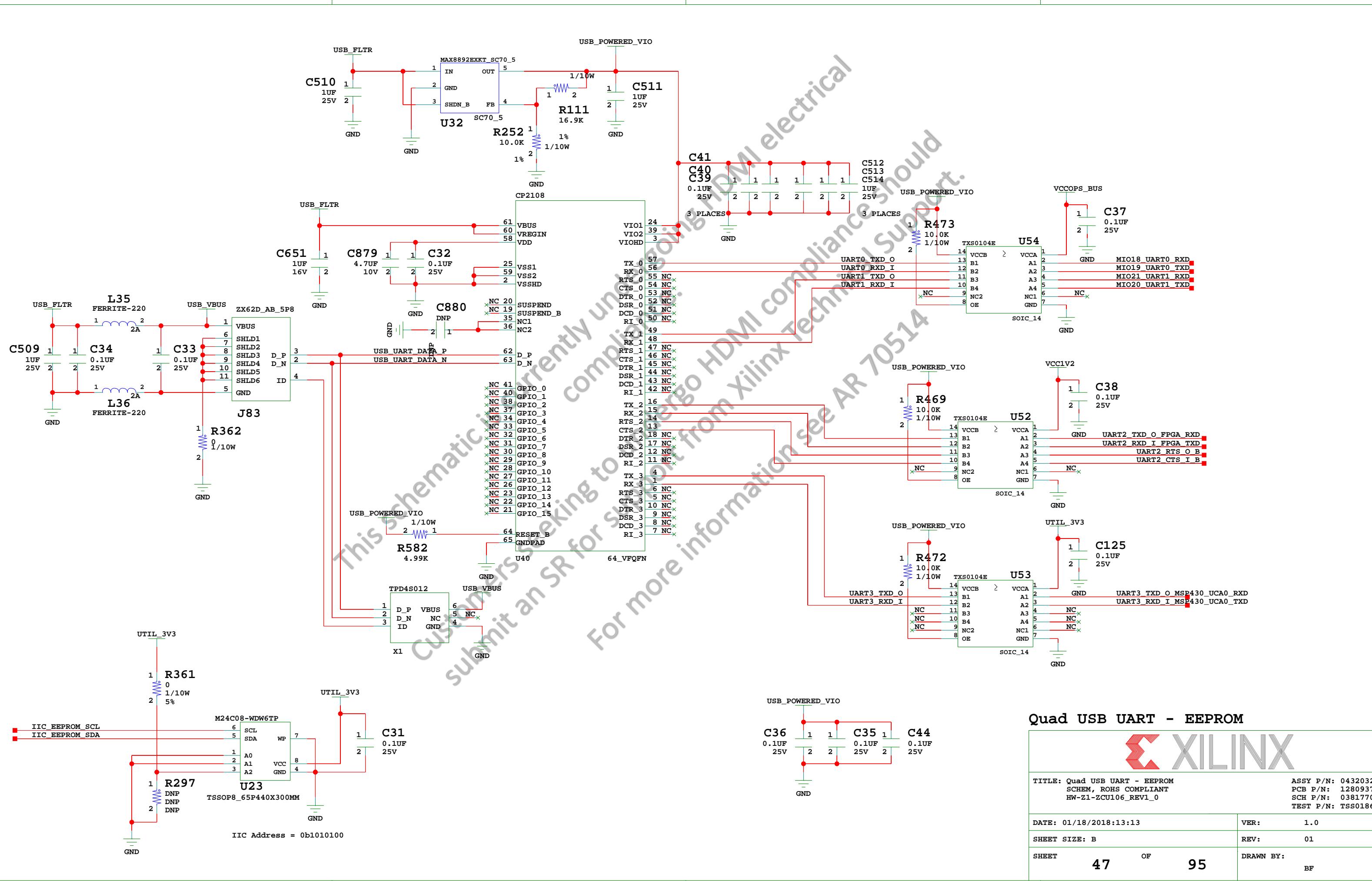
PL SFP Clock Recovery



TITLE: PL SFP Clock Recovery
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 46 OF 95	DRAWN BY: BF



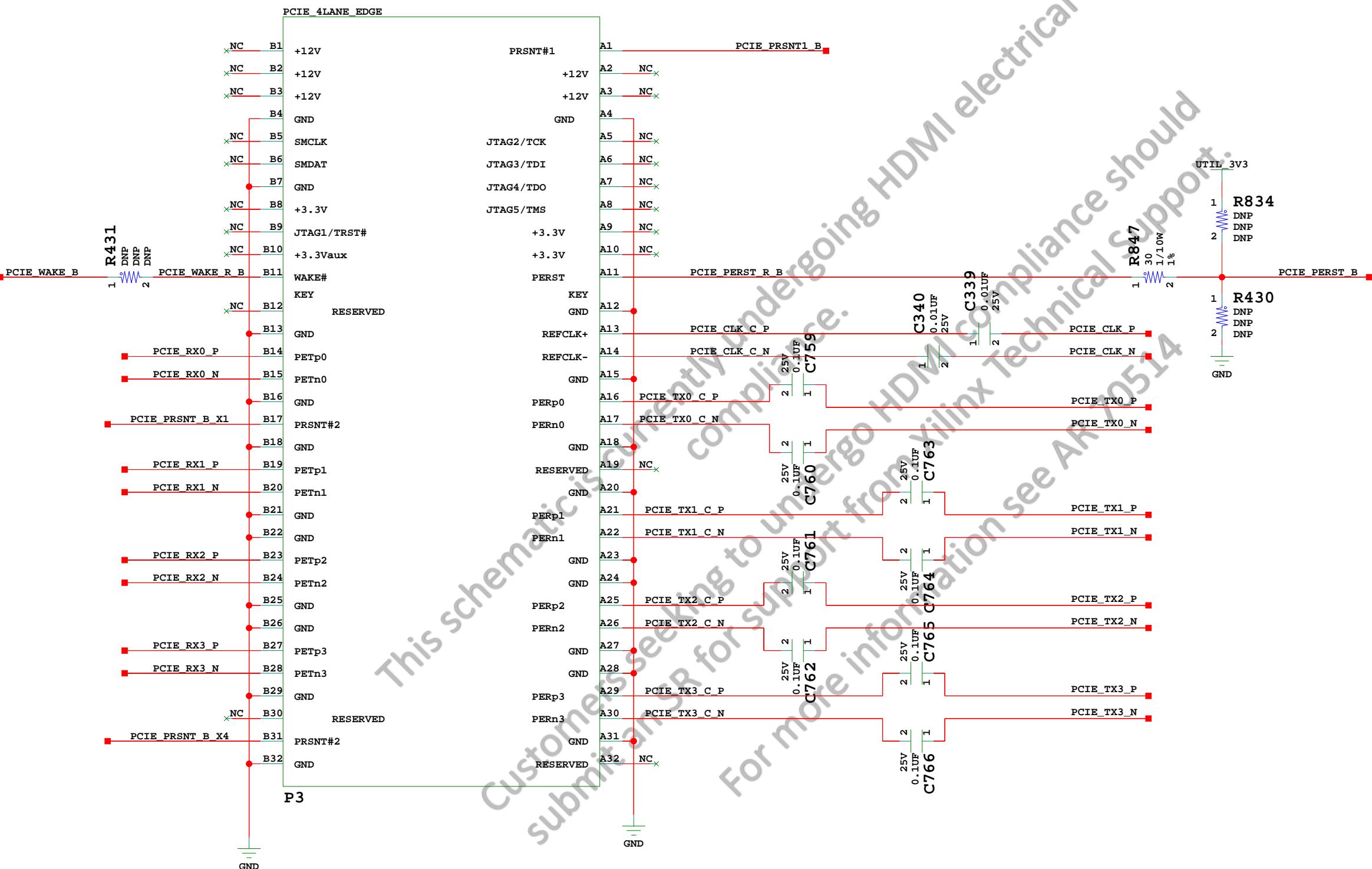
Quad USB UART - EEPROM



TITLE: Quad USB UART - EEPROM
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/18/2018:13:13	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 47 OF 95	DRAWN BY: BF

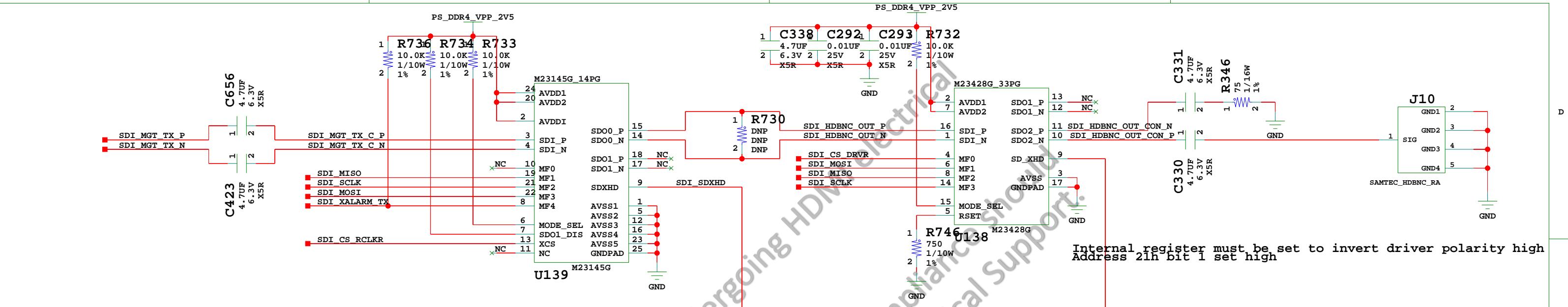


PL PCIe x4 Edge Connector

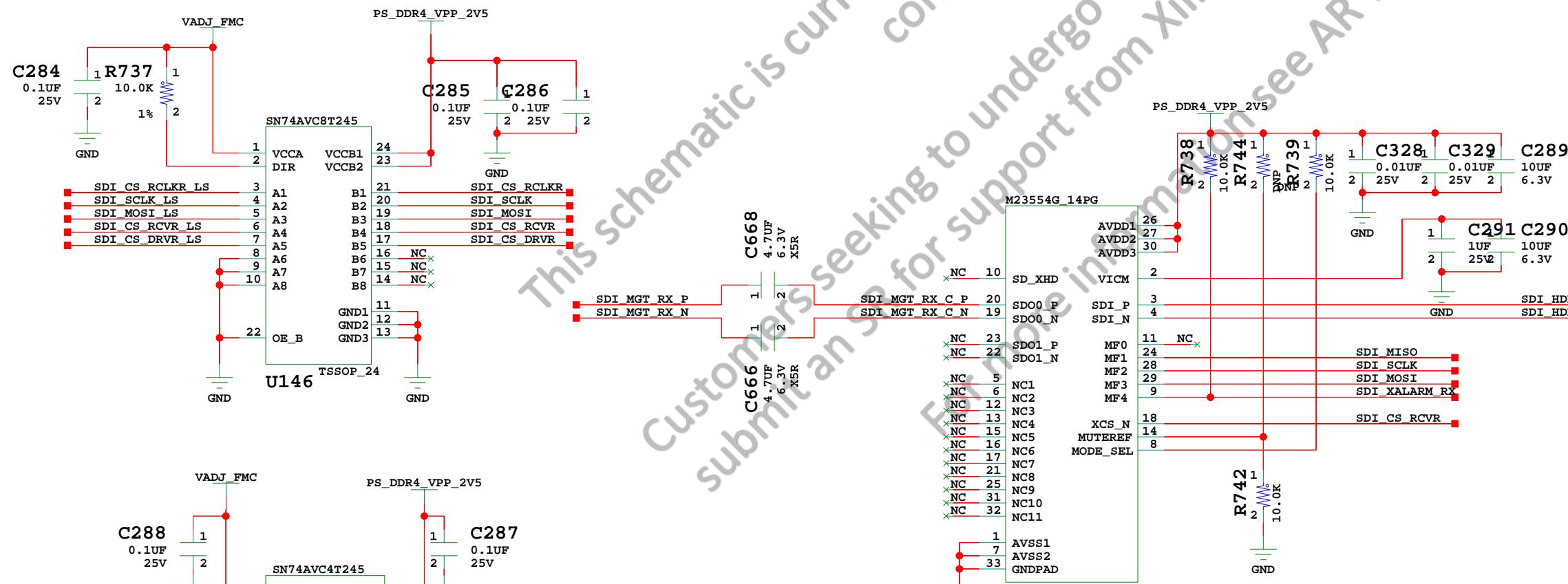


TITLE: PL PCIe x4 Edge Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 48 OF 95	DRAWN BY: BF

SDI VID OUT



SDI VID IN

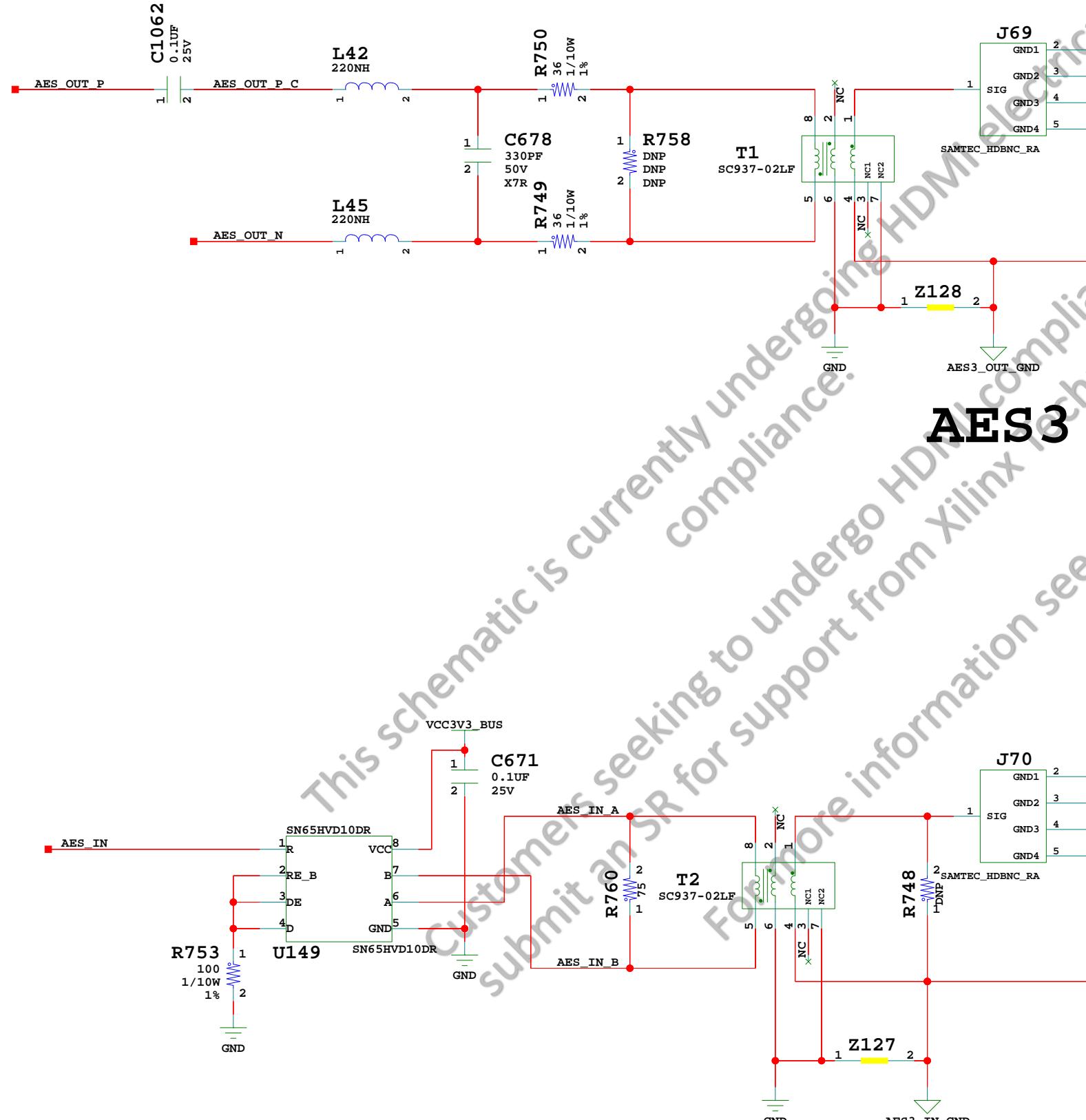


PL SDI Video Input - Output



TITLE: PL SDI Video Input - Output
ASSY P/N: 0432032
SCHEM, ROHS COMPLIANT
PCB P/N: 1280937
HW-Z1-ZCU106_REV1_0
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 49 OF 95	DRAWN BY: BF



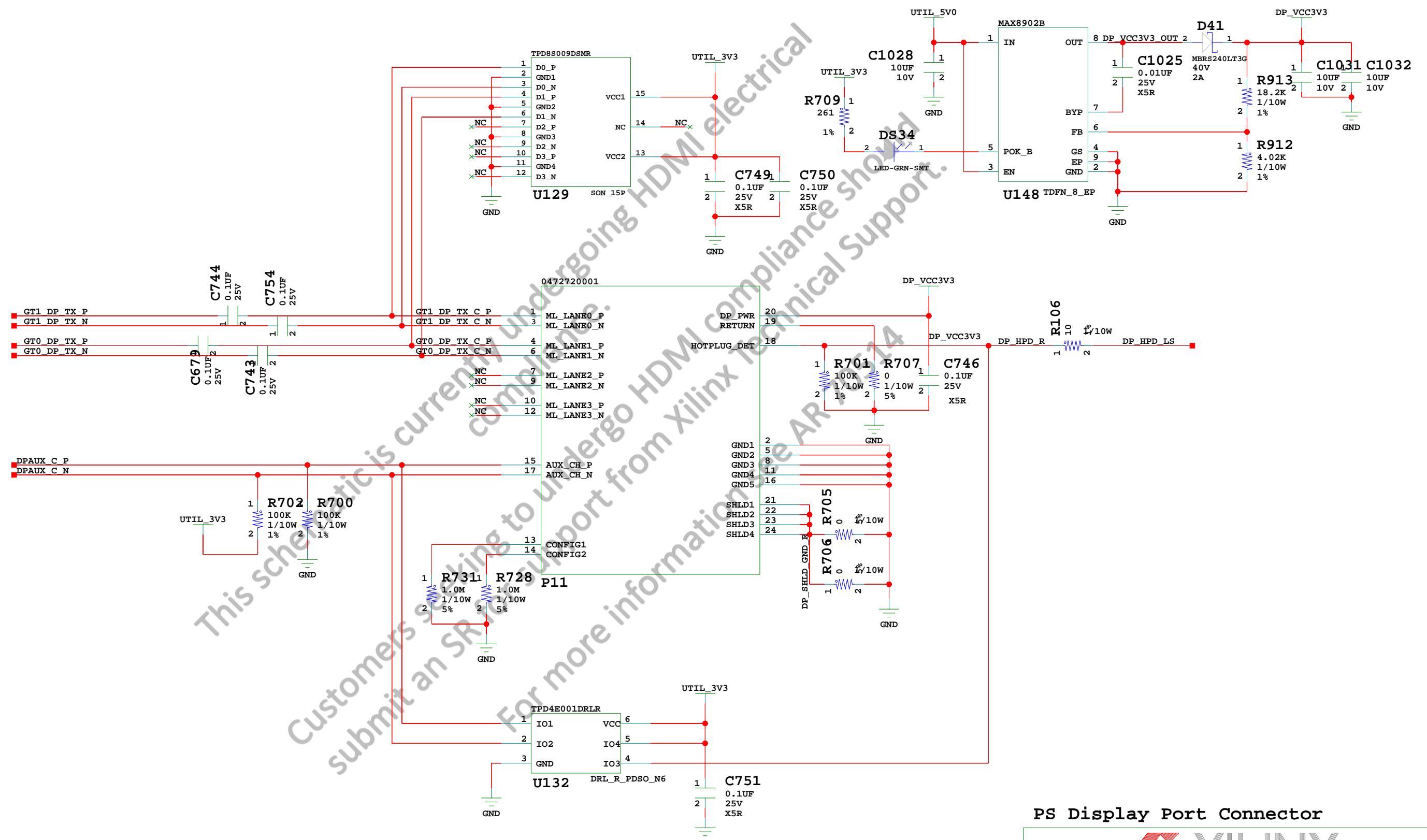
PL AES3 Audio Input - Output



TITLE: PL AES3 Audio Input - Output
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

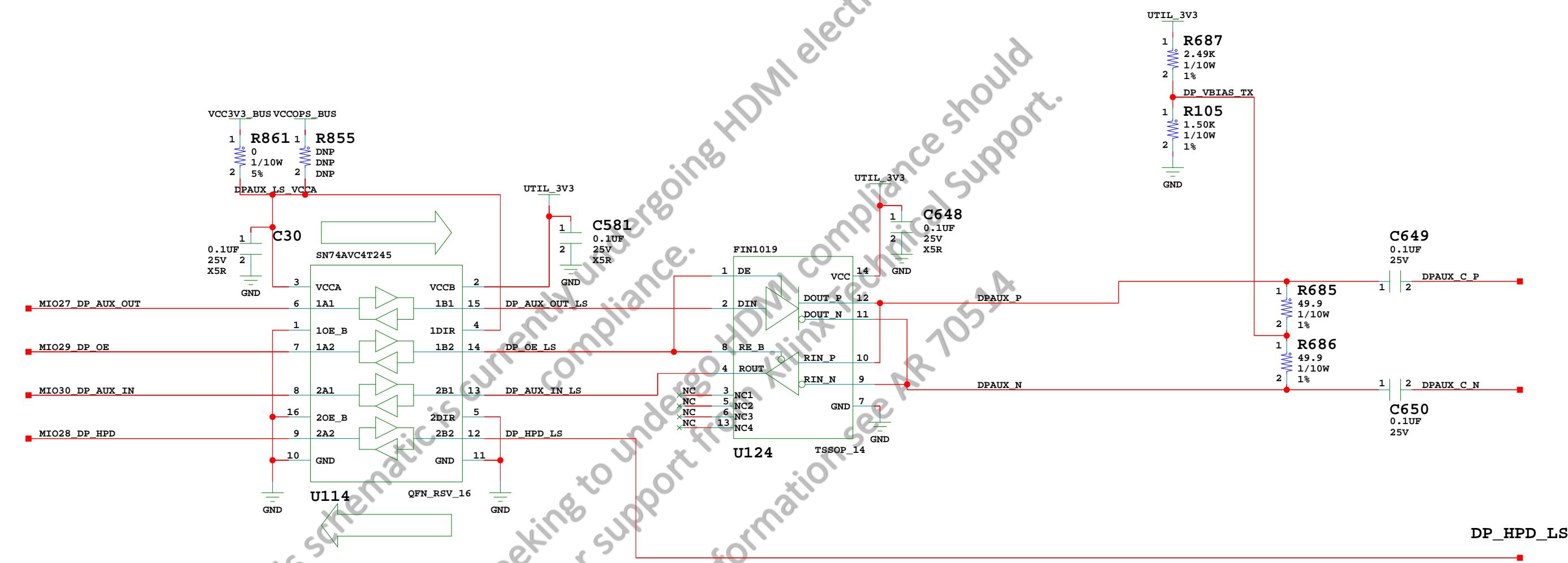
DATE: 01/18/2018:13:12	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 50 OF 95	DRAWN BY: BF



PS Display Port Connector



TITLE: PS Display Port Connector SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 51 OF 95	DRAWN BY: BF



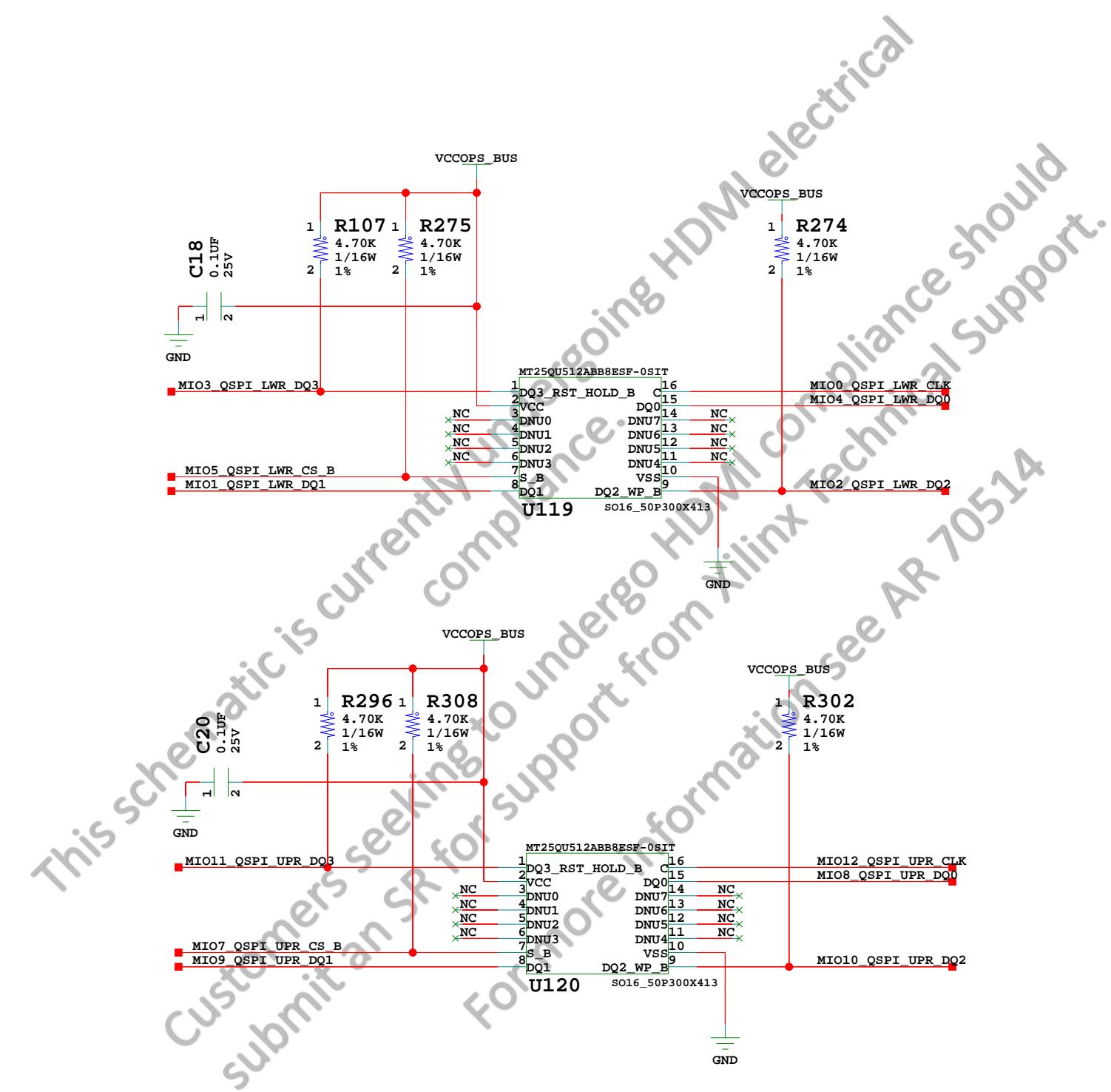
PS Display Port IO



TITLE: PS Display Port IO
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 52 OF 95	DRAWN BY: BF

**PS QSPI**

TITLE: PS_QSPI
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

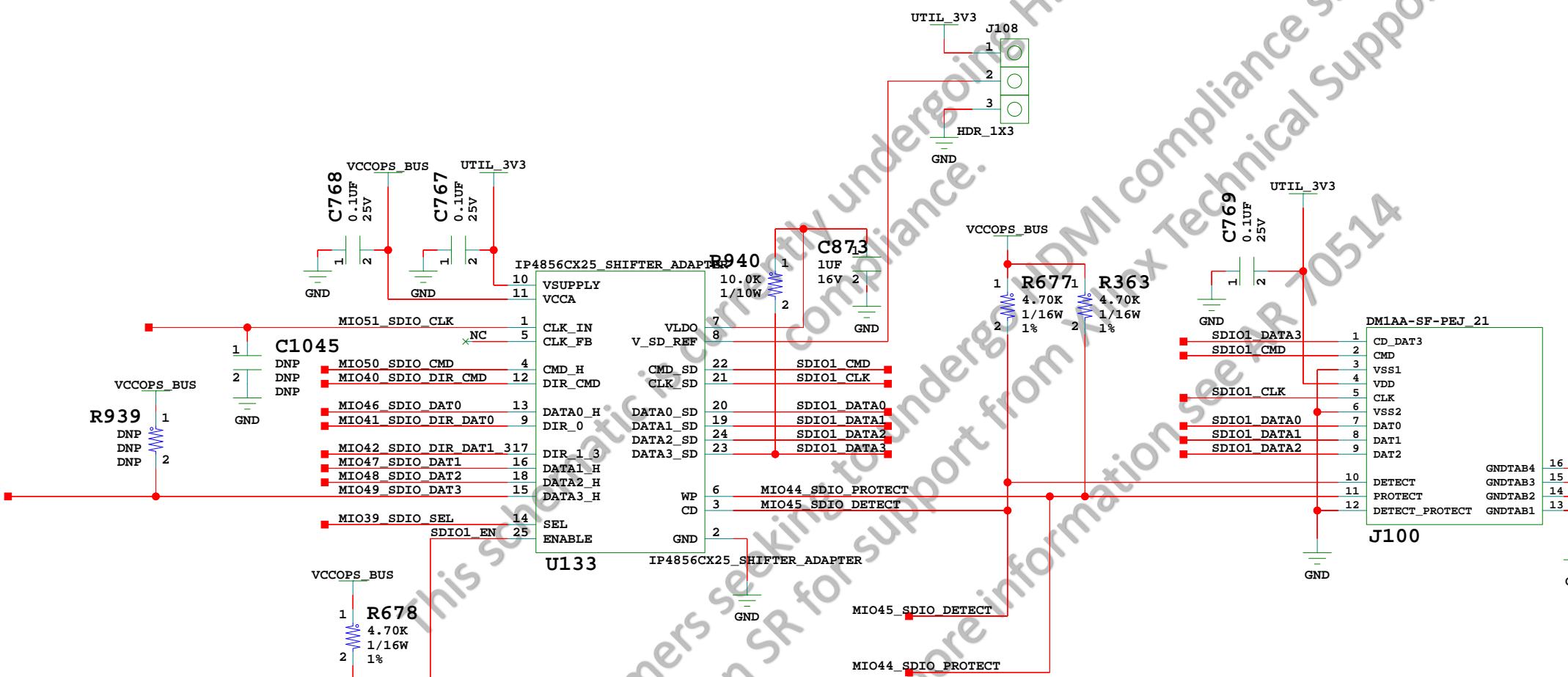
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 53 OF 95

DRAWN BY:
BF

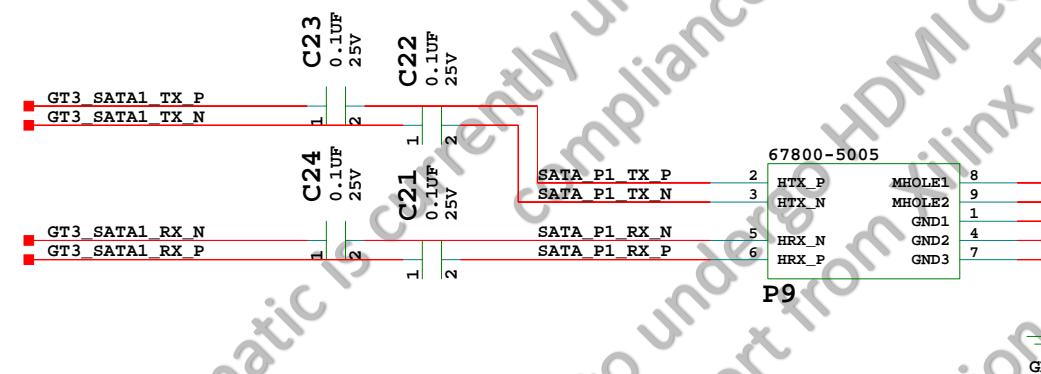


PS SD Card Connector

TITLE: PS SD Card Connector
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/18/2018:13:11	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 54 OF 95	DRAWN BY: BF



This schematic is currently undergoing HDMI electrical compliance.
 Customers seeking to undergo HDMI compliance should submit an SR for support from Xilinx Technical Support.
 For more information see AR 70514

PS SATA



TITLE: PS SATA
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

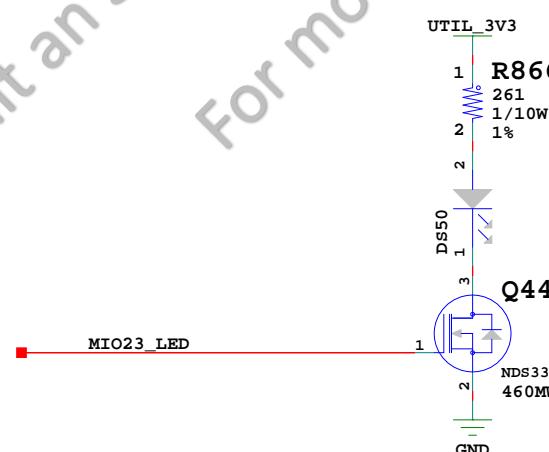
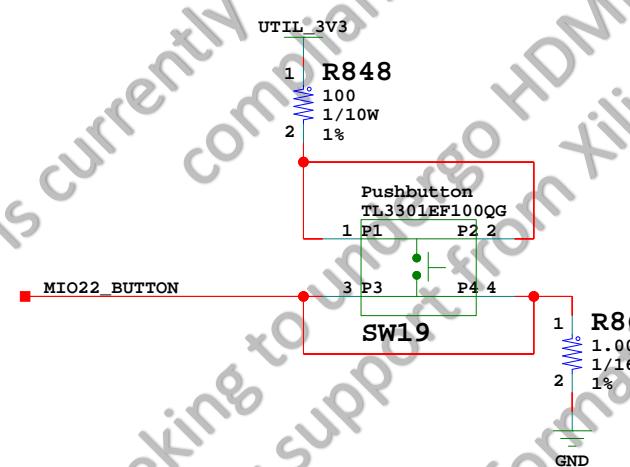
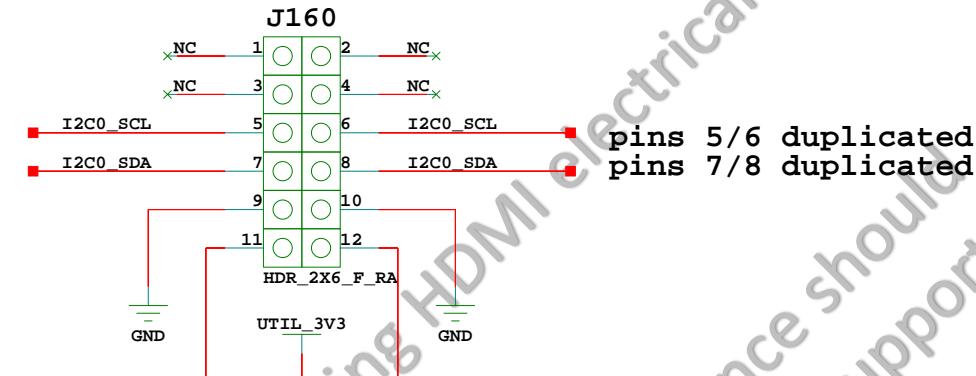
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 55 OF 95 DRAWN BY:
BF

Connects to R.A. Female 2x6 PMOD receptacle



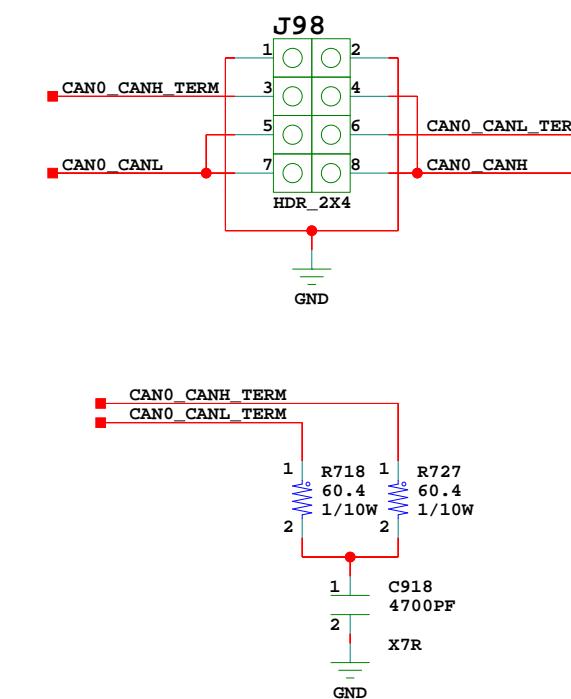
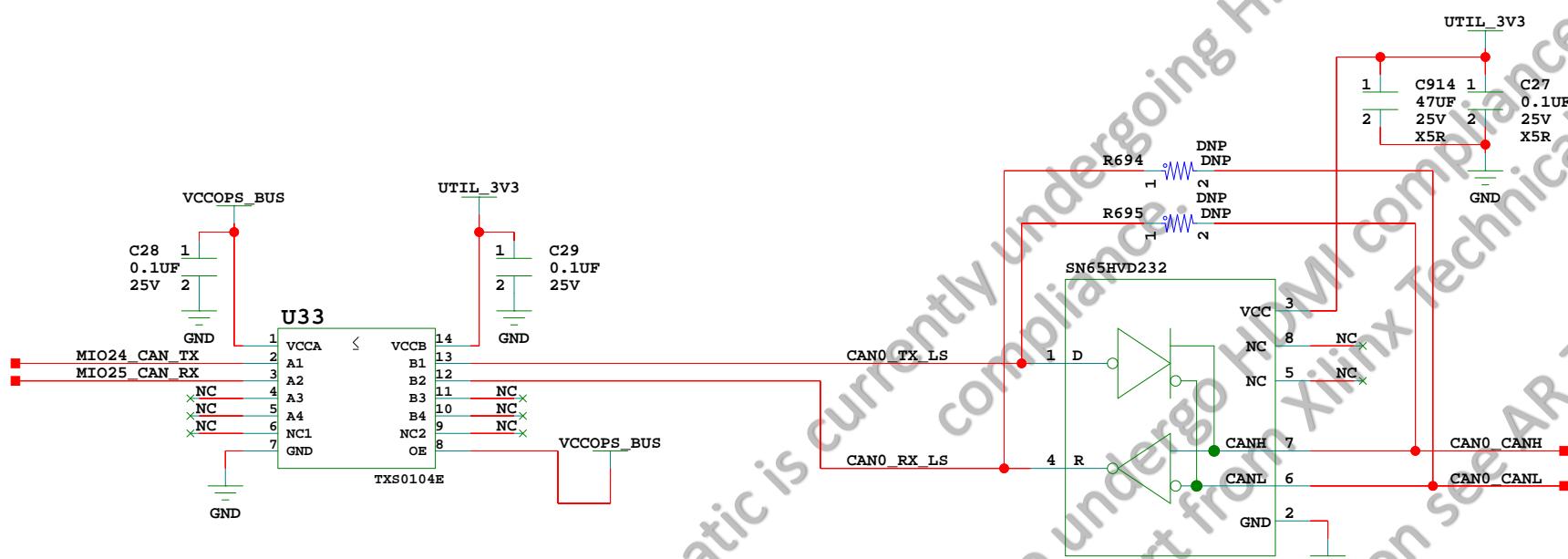
PS MIO PMOD - Button - LED



TITLE: PS MIO PMOD - Button - LED
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

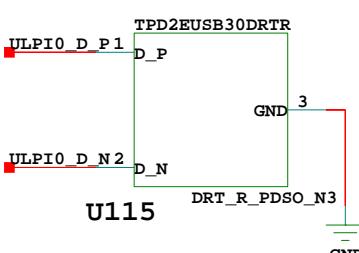
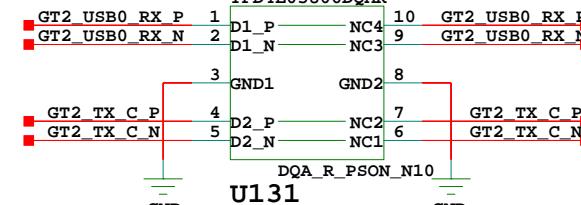
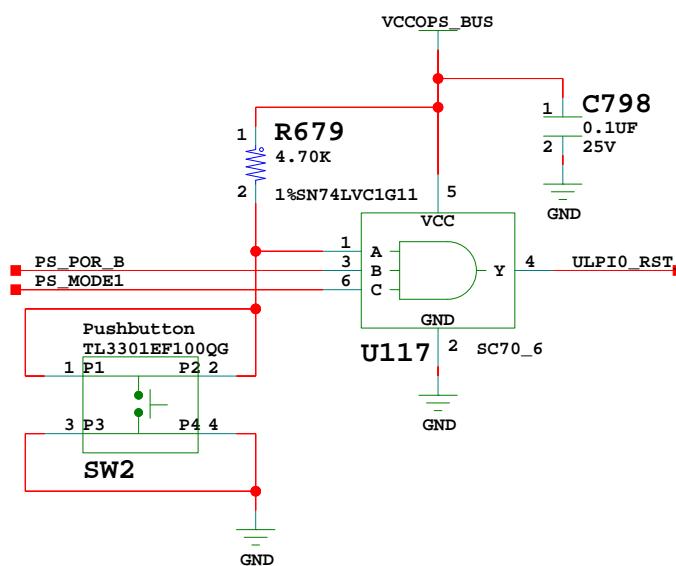
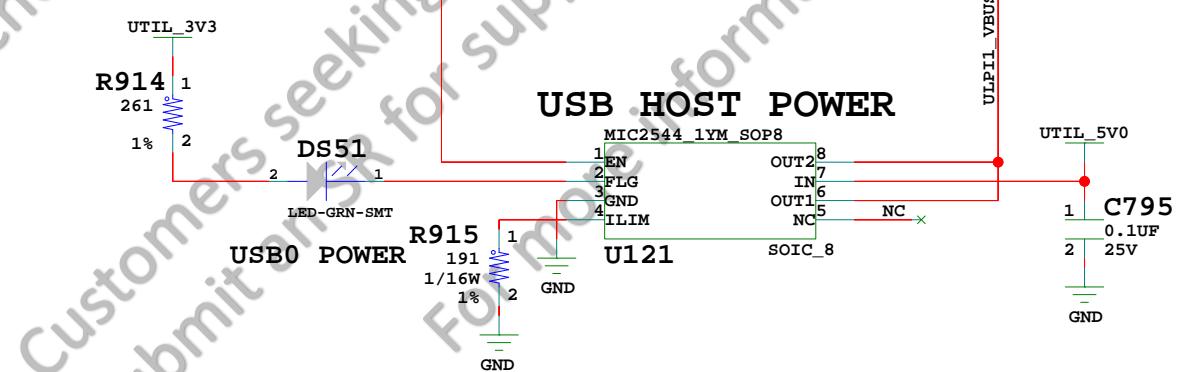
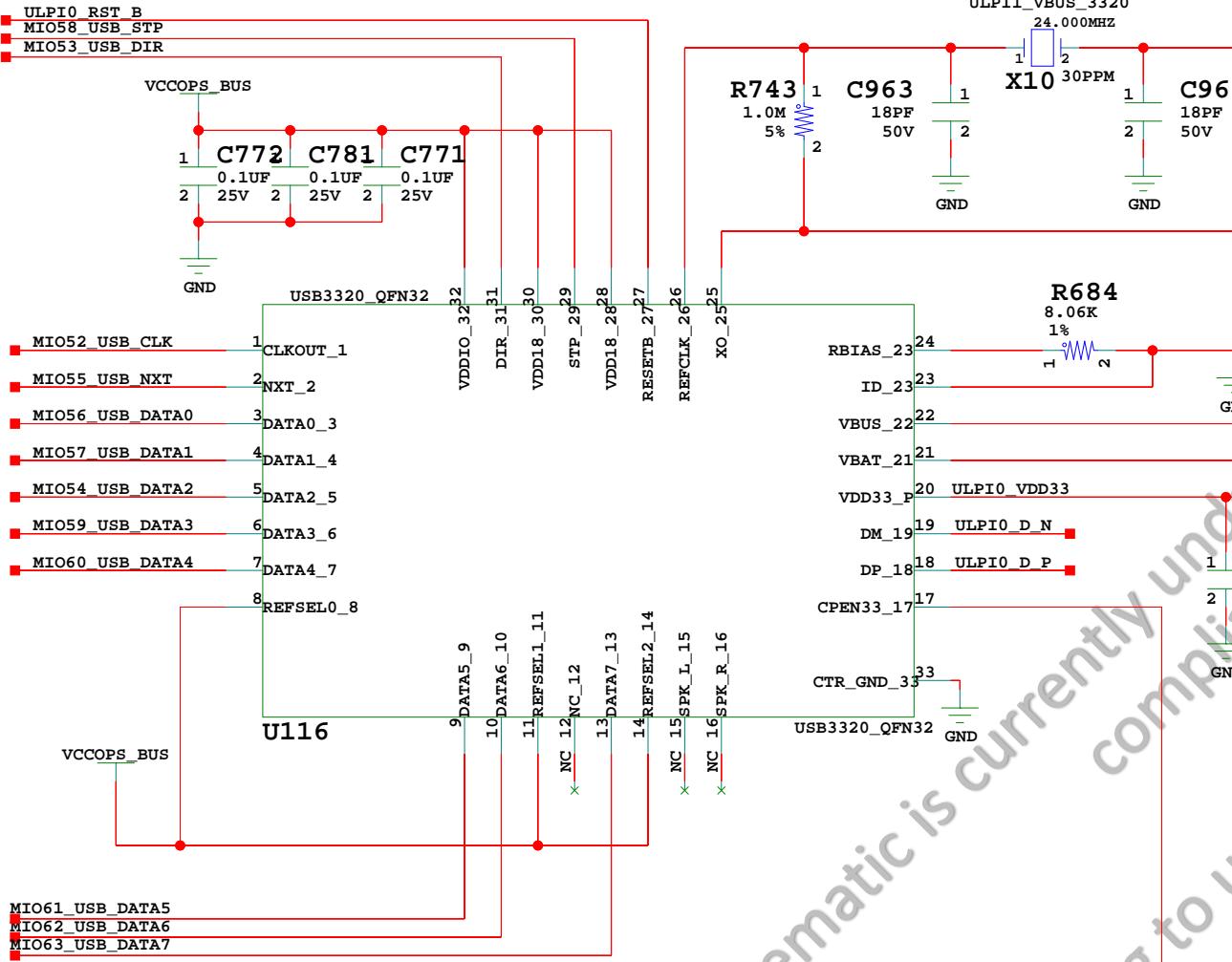
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 56 OF 95	DRAWN BY: BF



PS CAN Bus

XILINX	
TITLE: PS CAN Bus SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 57 OF 95	DRAWN BY: BF

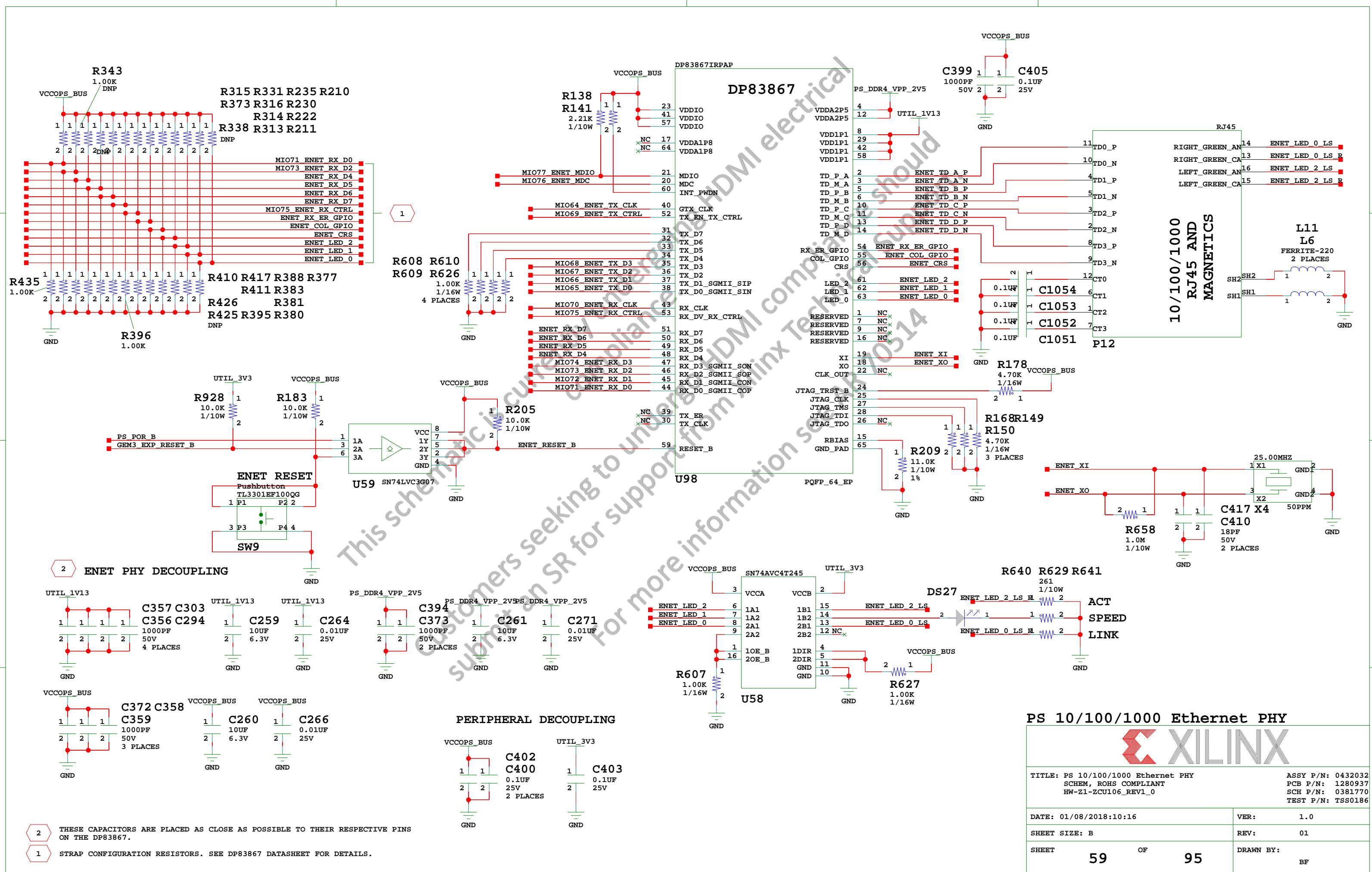
This schematic is currently undergoing HDMI electrical compliance testing.
Customers seeking to undergo HDMI compliance support should submit an SR for support from Xilinx Technical Support.
For more information see AR 70514

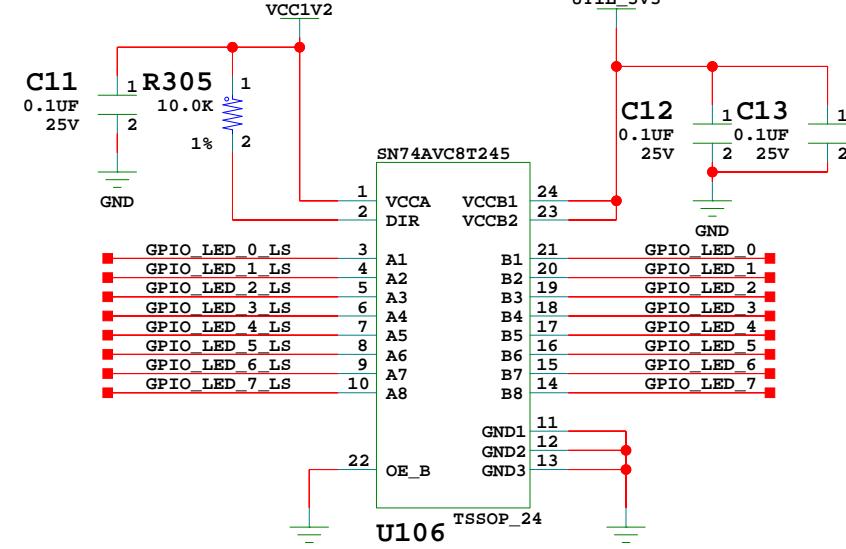


90 ohm impedance for USB 2.0 ULPI_D_P/N,
100 ohm for USB 3.0 USB_SSTX_P/N, USB_SS
Thick trace for ULPI VBUS SEL and related

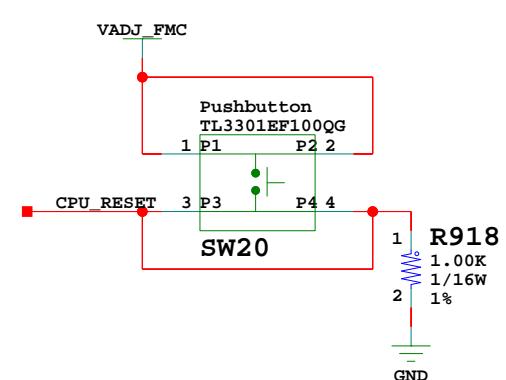
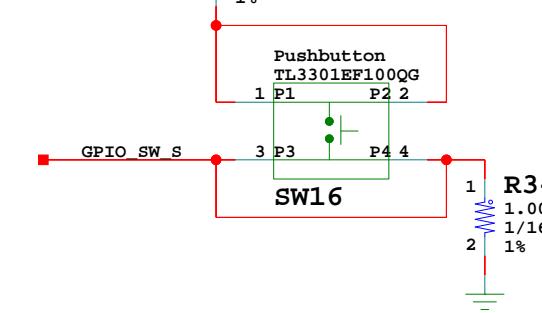
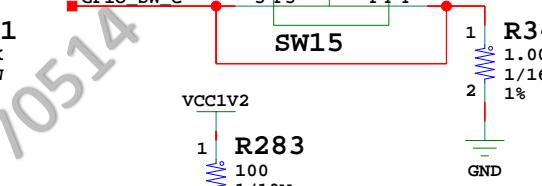
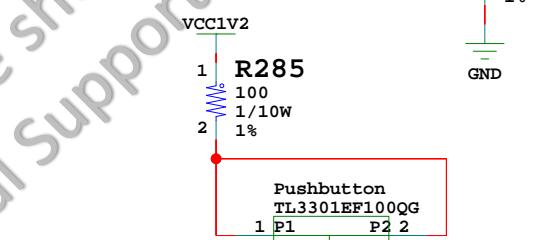
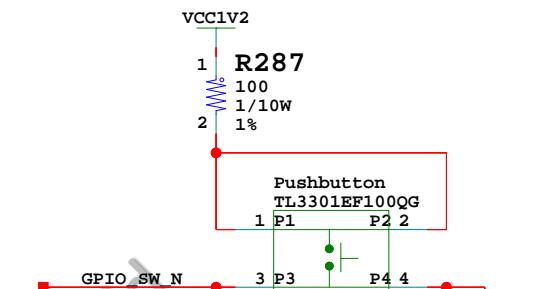
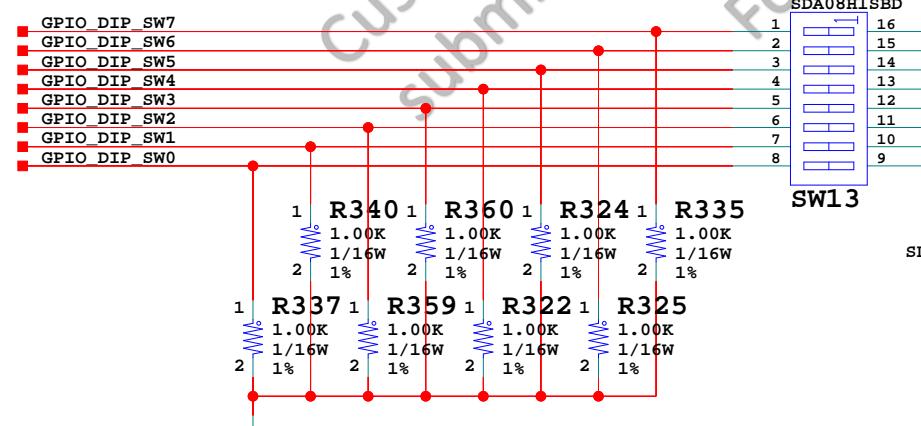
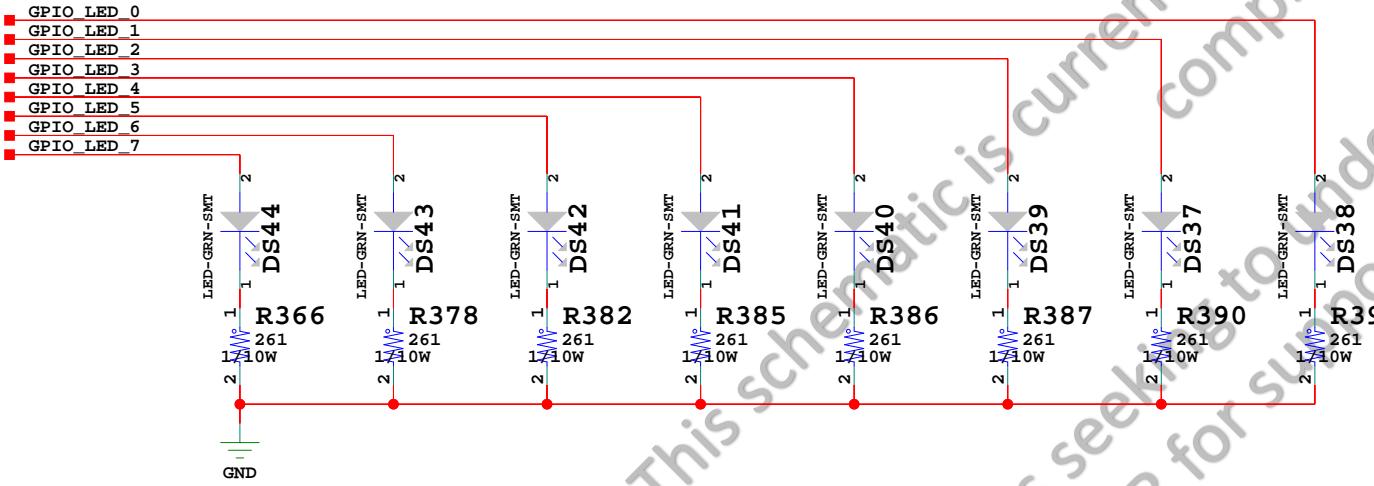
PS USB 3 0 ULPI 0

		
TITLE: PS USB 3_0 ULPI 0 SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		
ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186		
DATE: 01/08/2018:10:16	VER: 1.0	
SHEET SIZE: B	REV: 01	
 SHEET 58	 OF 95	DRAWN BY: BF





LEDs near top right edge



PL Buttons - Switches - LEDs



TITLE: PL Buttons - Switches - LEDs
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

SHEET SIZE: B

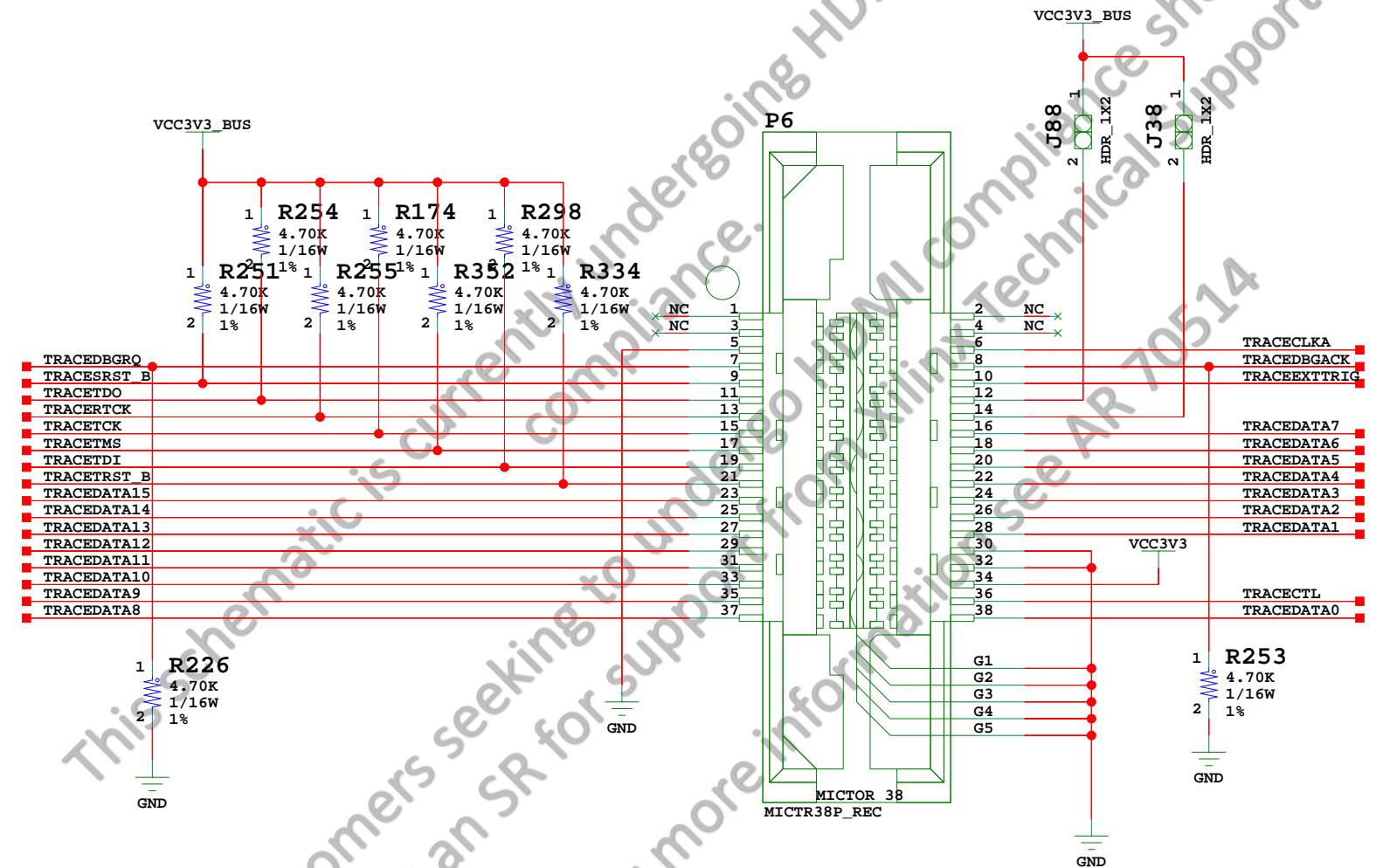
REV: 01

SHEET 60 OF 95

DRAWN BY:

BF

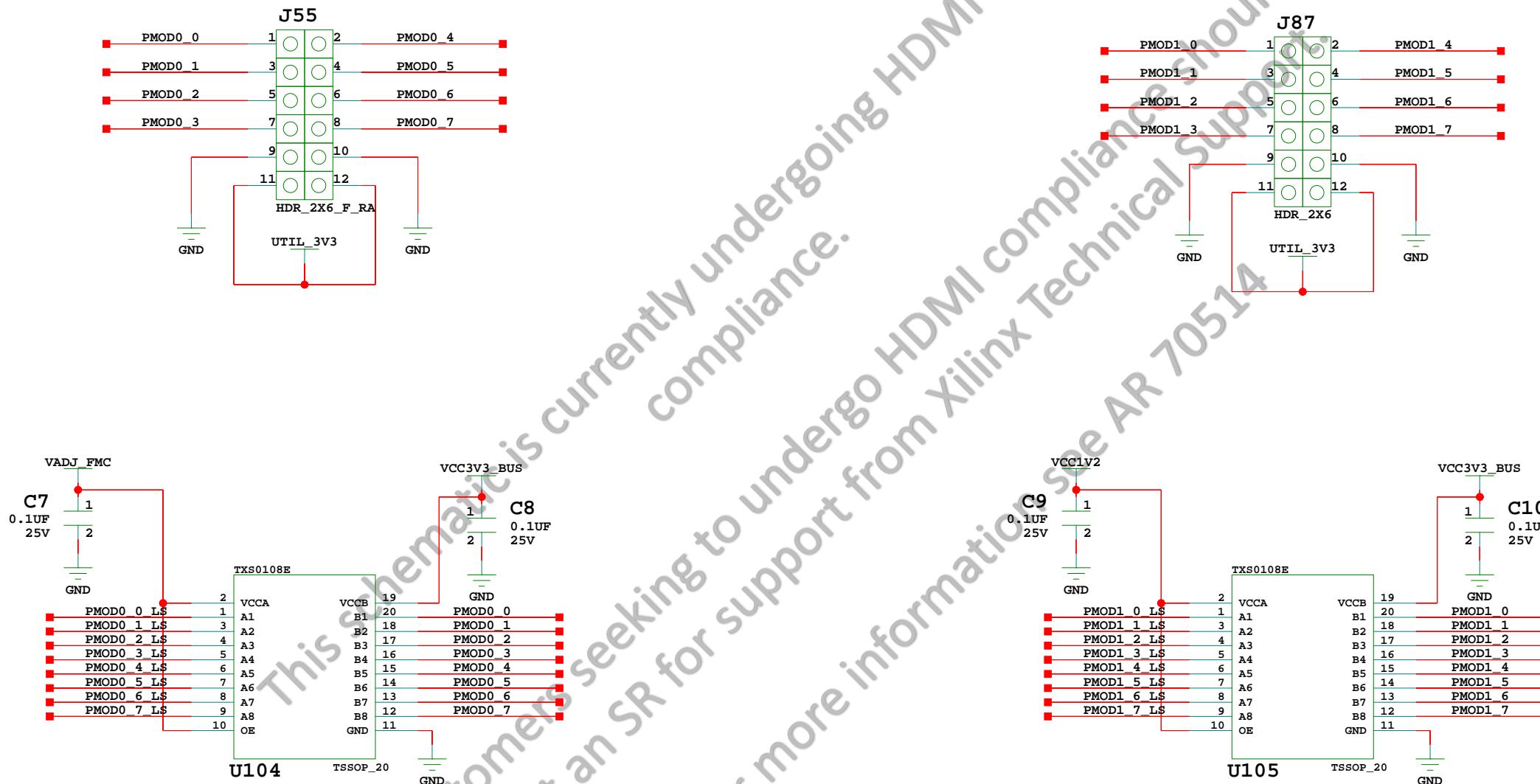
EMIO ARM Trace/Debug



PL EMIO ARM Trace Debug



TITLE: PL EMIO ARM Trace Debug SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0	
SHEET SIZE: B	REV: 01	
SHEET 61 OF 95	DRAWN BY: BF	



This schematic is currently undergoing HDMI compliance support. Customers seeking to undergo HDMI compliance should submit an SR for support from Xilinx Technical Support. For more information, see AR 70514

PL PMODs

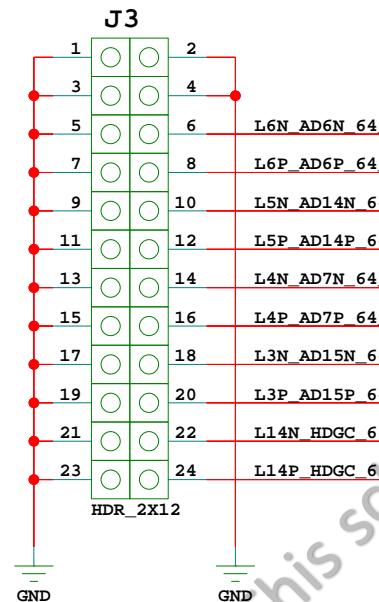


TITLE: PL PMODS
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

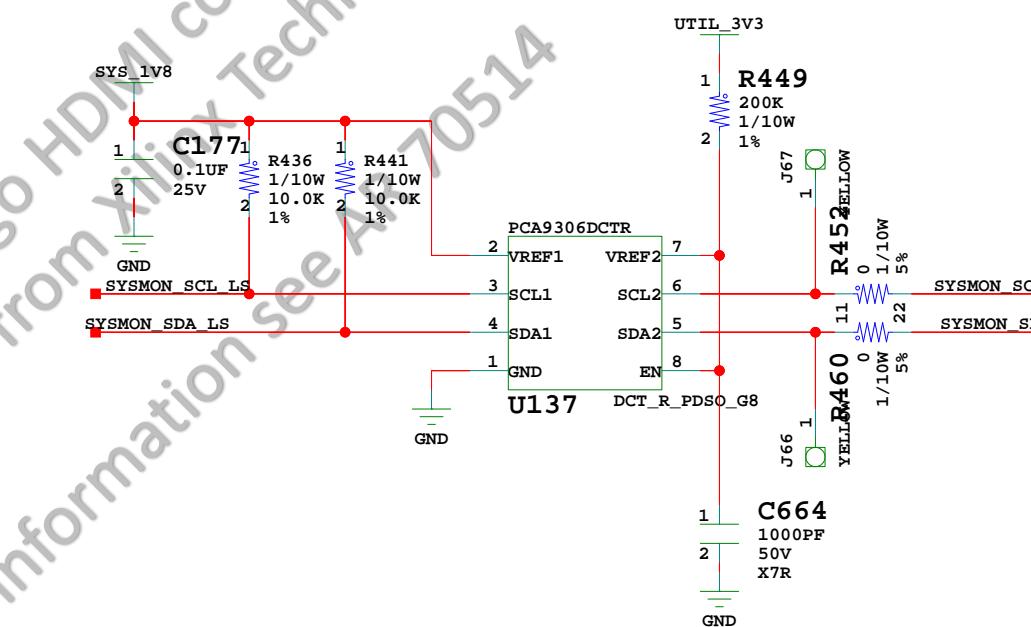
ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 62 OF 95	DRAWN BY: BF

Prototype Header



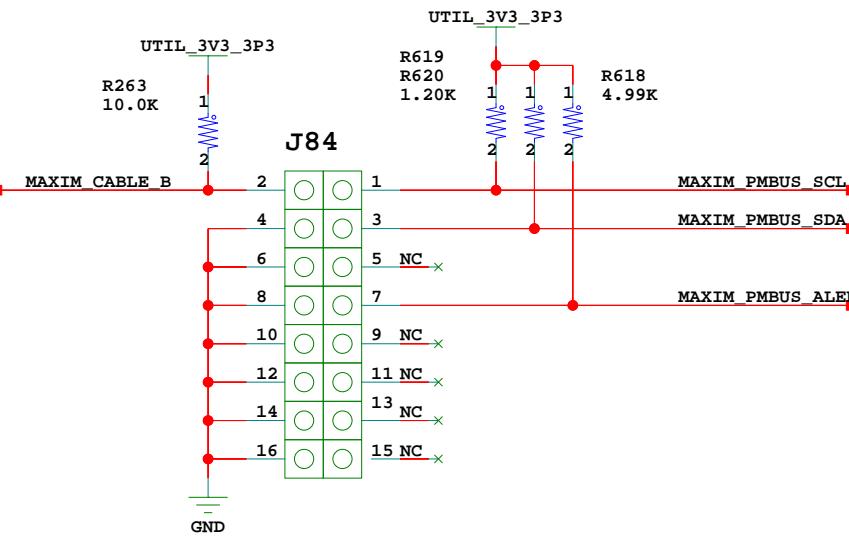
This schematic is currently undergoing HDMI electrical compliance. Customers seeking to undergo HDMI compliance should submit an SR for support from Xilinx Technical Support. For more information see Xilinx Part Number ZU0514



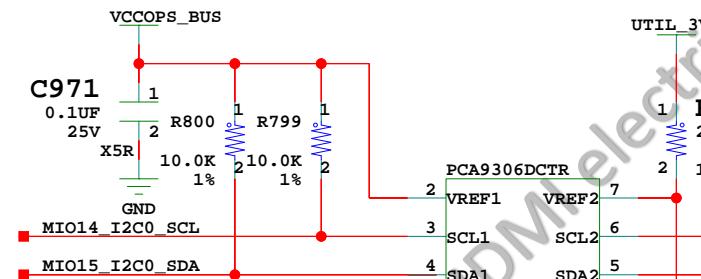
PL Prototype Header - SYSMON Level Shifter

TITLE: PL Prototype Header - SYSMON Level Shifter SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 63 OF 95	DRAWN BY: BF

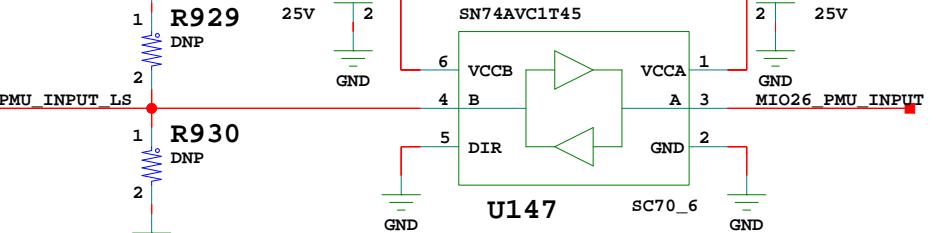
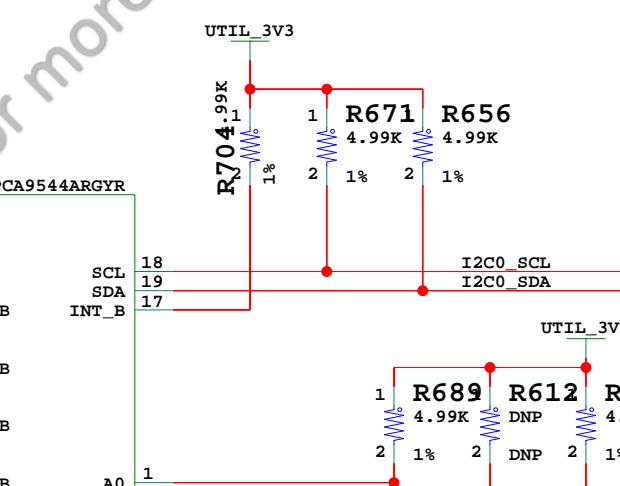
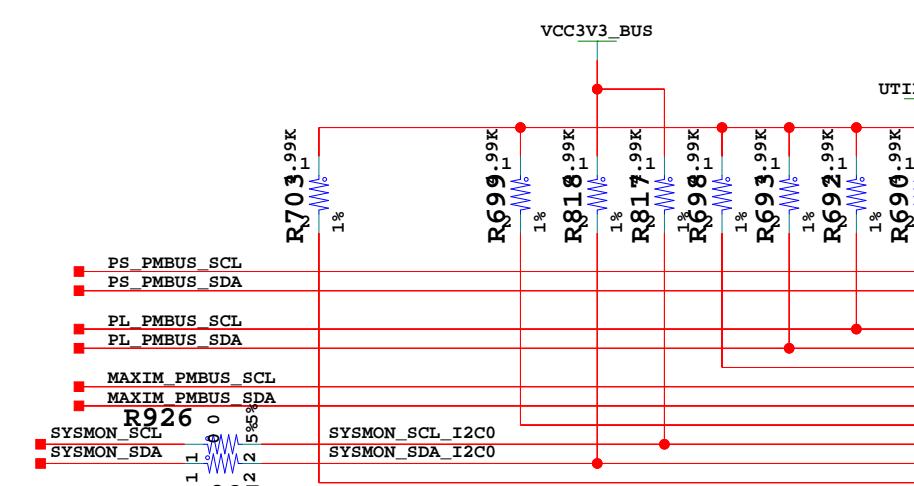
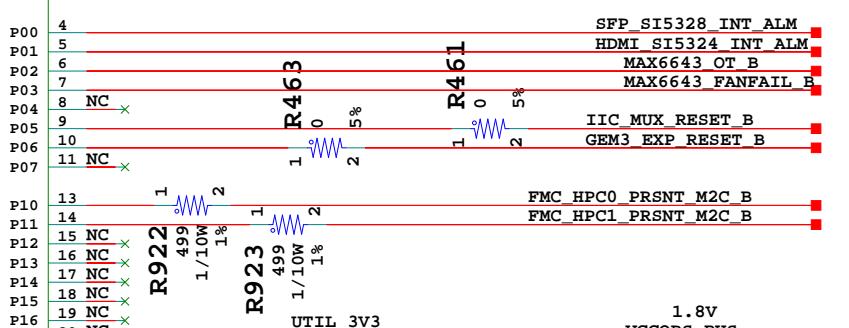
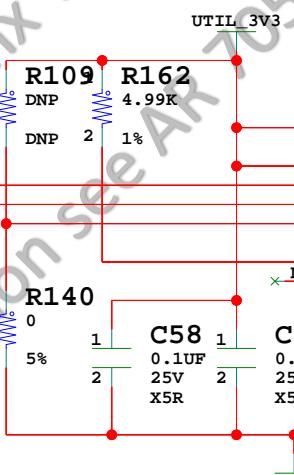
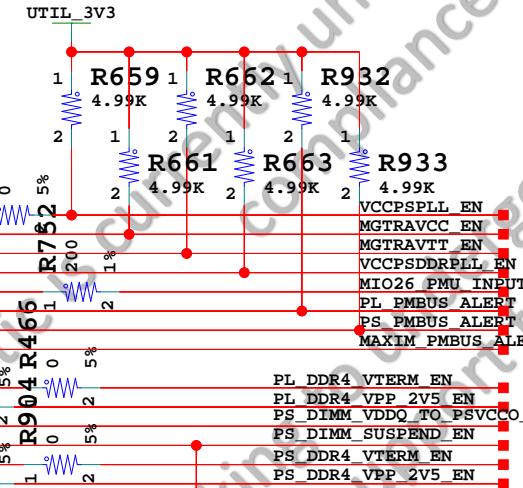
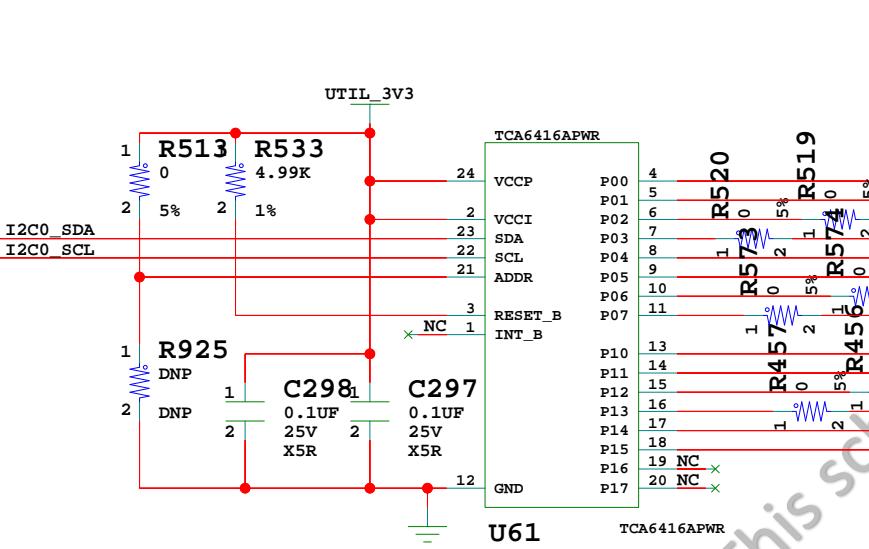
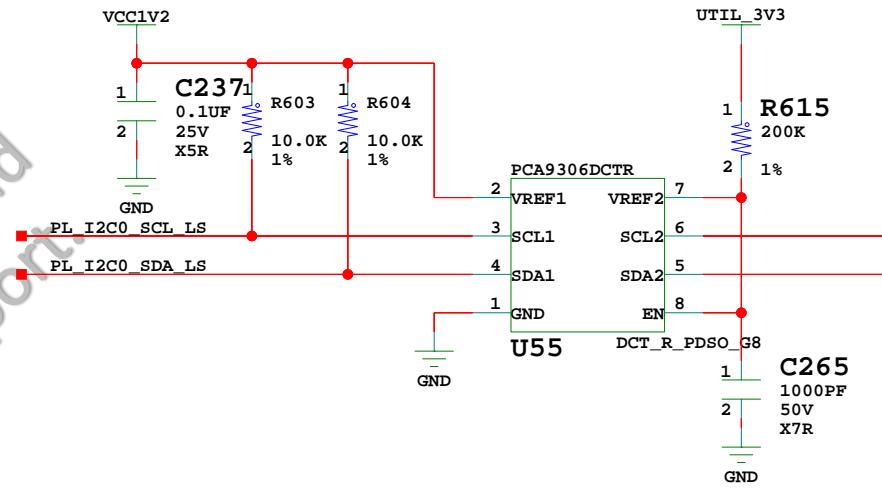
MAXIM PMBUS PROGRAMMING CABLE



PS I2C Level Shifter (I2C0)



PL I2C Level Shifter (disabled if VREF1 is off)



I2C0 MUXes Expanders Level Shifters PMBUS



TITLE: I2C0 MUXes Expanders Level Shifters PMBUS Header ASY P/N: 0432032
SCHEM., ROHS COMPLIANT PCB P/N: 1280937
HW-Z1-ZCU106_REV1_0 SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16 VER: 1.0

SHEET SIZE: B REV: 01

SHEET 64 OF 95 DRAWN BY: BF

IIC EEPROM SDA
IIC EEPROM SCL
SI5341 SDA
SI5341 SCL
USER SI570 SDA
USER SI570 SCL
USER MGT SI570 SDA
USER MGT SI570 SCL
SI5328 SDA
SI5328 SCL

R600 0.99K
R599.99K
R602.1
R601.99K
R596.99K
R595.99K
R594.99K
R593.99K
R592.99K
R591.99K

TCA9548APWR_TSSOP_24
SD0 23
SD1 22
SD2 7
SD3 8
SD4 9
SD5 10
SD6 11
SD7 12
SD8 13
SD9 14
SD10 15
SD11 16
SD12 17
SD13 18
SD14 19
SD15 20
RESET_B 3
A0 1
A1 2
A2 21
VCC 24
GND 12

UTIL_3V3
R299 1
DNP 2
R300 2
DNP 2
R586 4.99K
1/10W 1
R5851 4.99K
1/10W 2
R617 4.99K
1/10W 2
R616 4.99K
1/10W 1
I2C1_SDA
I2C1_SCL
IIC_MUX_RESET_B

FMC_HPC0_IIC_SDA
FMC_HPC0_IIC_SCL
FMC_HPC1_IIC_SDA
FMC_HPC1_IIC_SCL
SYSMON_SDA
SYSMON_SCL
DDR4_SODIMM_SDA
DDR4_SODIMM_SCL

R828.99K
R827.99K
R824.99K
R823.99K

R831.99K
R830.99K
R508 0.99K
R924 DNP
DNP

R816.99K
R815.99K
R814.99K
R813.99K

TCA9548APWR_TSSOP_24
SD0 23
SD1 22
SD2 7
SD3 8
SD4 9
SD5 10
SD6 11
SD7 12
SD8 13
SD9 14
SD10 15
SD11 16
SD12 17
SD13 18
SD14 19
SD15 20
RESET_B 3
A0 1
A1 2
A2 21
VCC 24
GND 12

R829 4.99K
1/10W 2
R806 4.99K
1/10W 2
R812 4.99K
1/10W 1
R811 4.99K
1/10W 1

I2C1_SDA
I2C1_SCL
IIC_MUX_RESET_B

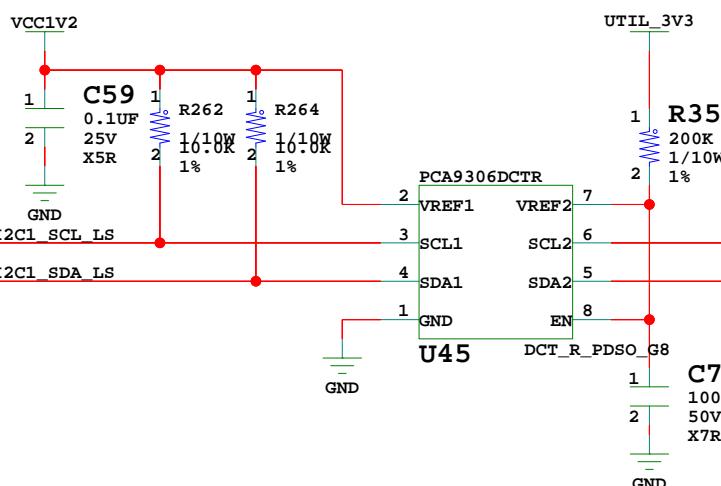
SFP1_IIC_SDA
SFP1_IIC_SCL
SFP0_IIC_SDA
SFP0_IIC_SCL

TCA9548APWR_TSSOP_24
SD0 23
SD1 22
SD2 7
SD3 8
SD4 9
SD5 10
SD6 11
SD7 12
SD8 13
SD9 14
SD10 15
SD11 16
SD12 17
SD13 18
SD14 19
SD15 20
RESET_B 3
A0 1
A1 2
A2 21
VCC 24
GND 12

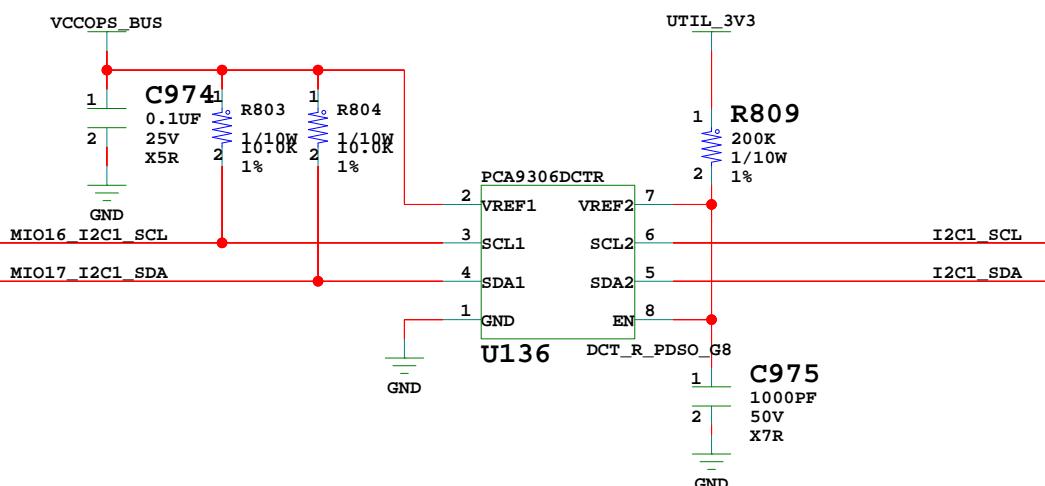
C973 0.1UF
25V X5R 2
R808 4.99K
1/10W 2
R810 4.99K
1/10W 2
R807 4.99K
1/10W 2

GND

PL I2C Level Shifter (disabled if VREF1 is off)



PS I2C Level Shifter (I2C1)



I2C1 MUXes and Level Shifters



TITLE: I2C1_MUXes and Level Shifters
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

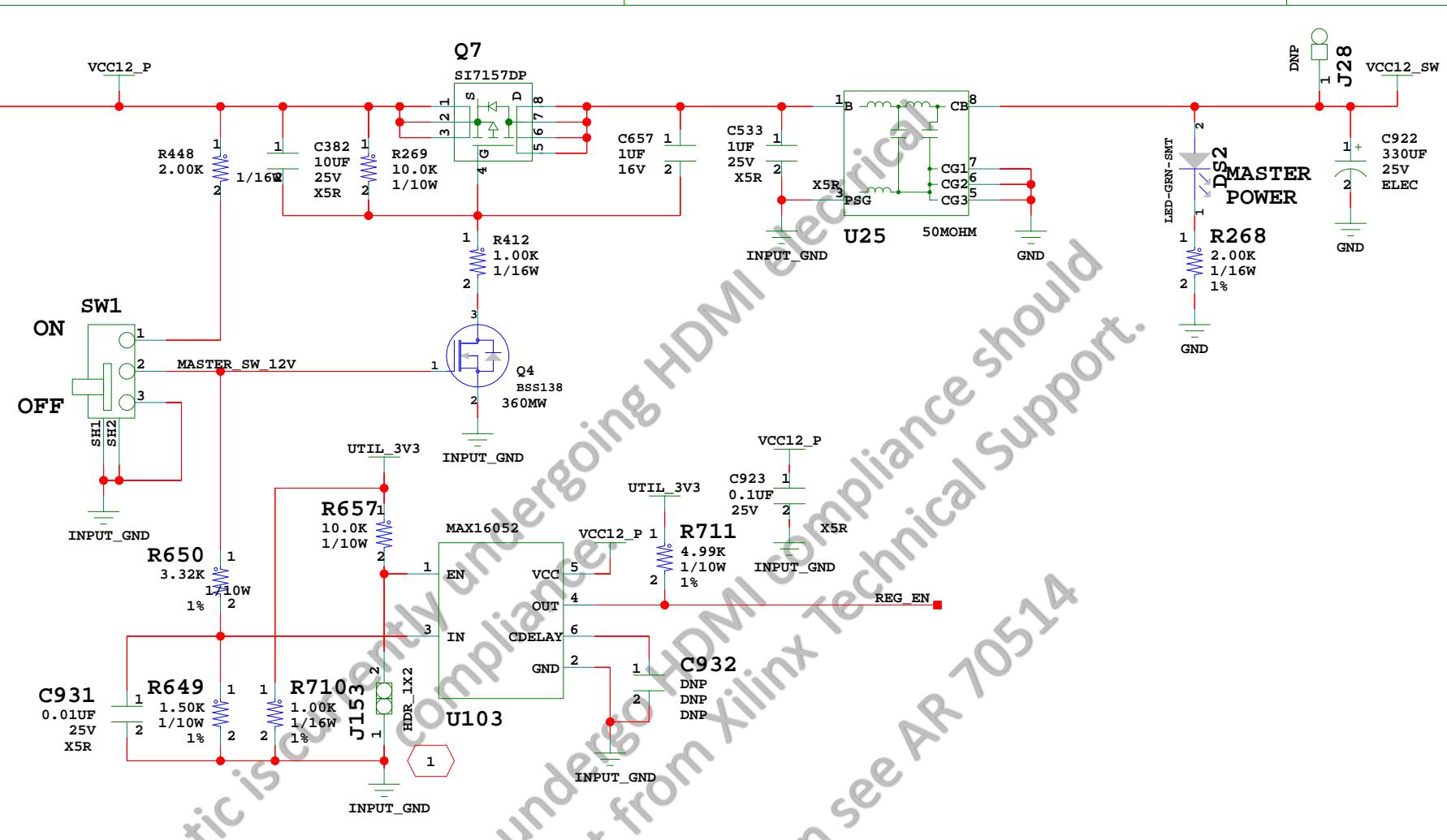
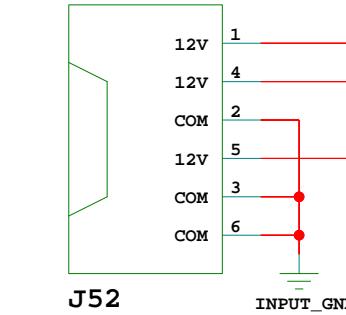
SHEET SIZE: B

REV: 01

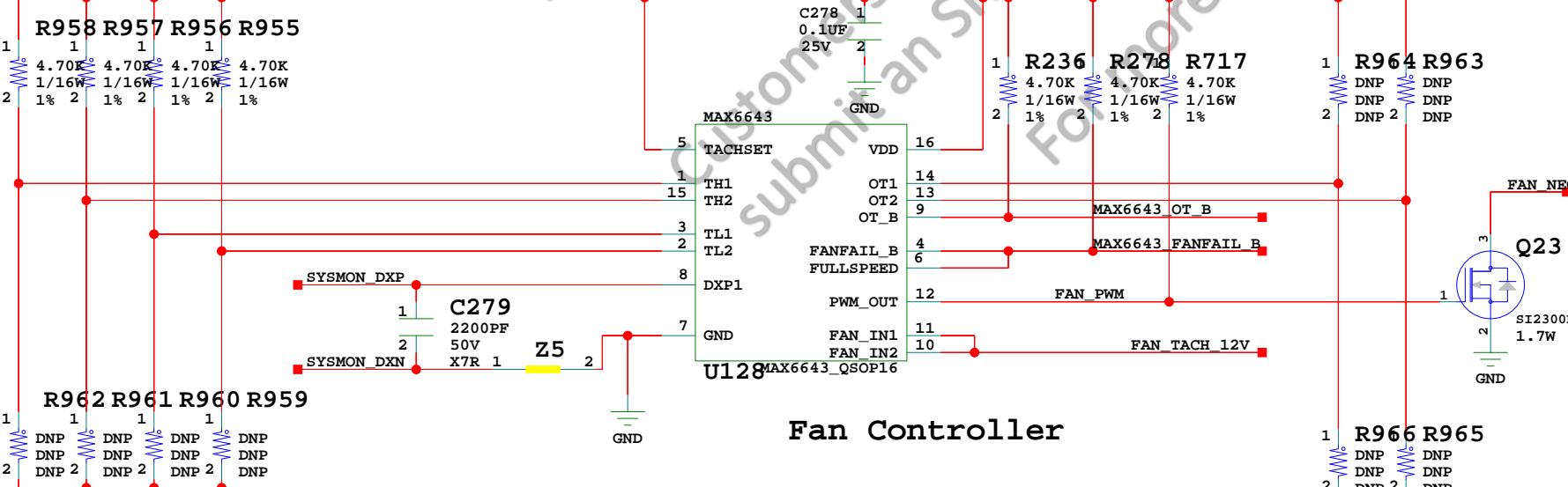
SHEET 65 OF 95

DRAWN BY:
BF

6-PIN MINI-FIT AC ADAPTER (BRICK)

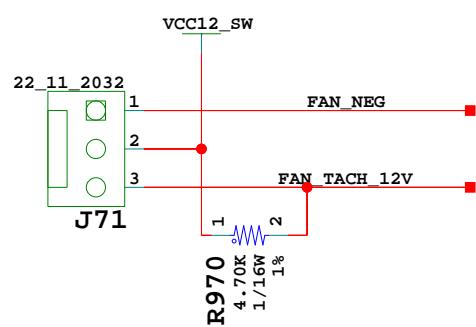


GND Test points



Fan Controller

Keyed Fan Header



12V Power Connectors Switch



TITLE: 12V Power Connectors Switch
SCHEM., ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

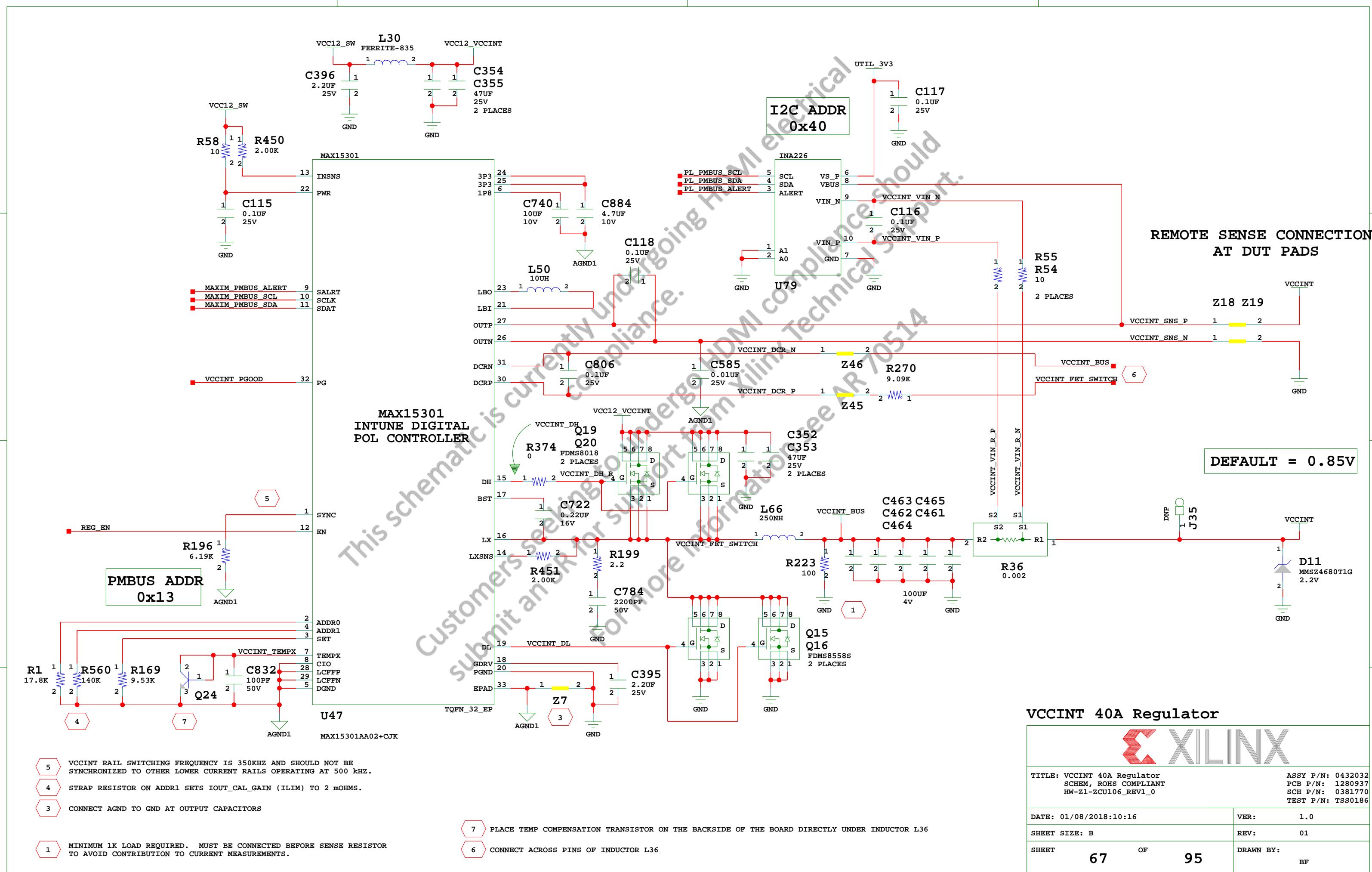
VER: 1.0

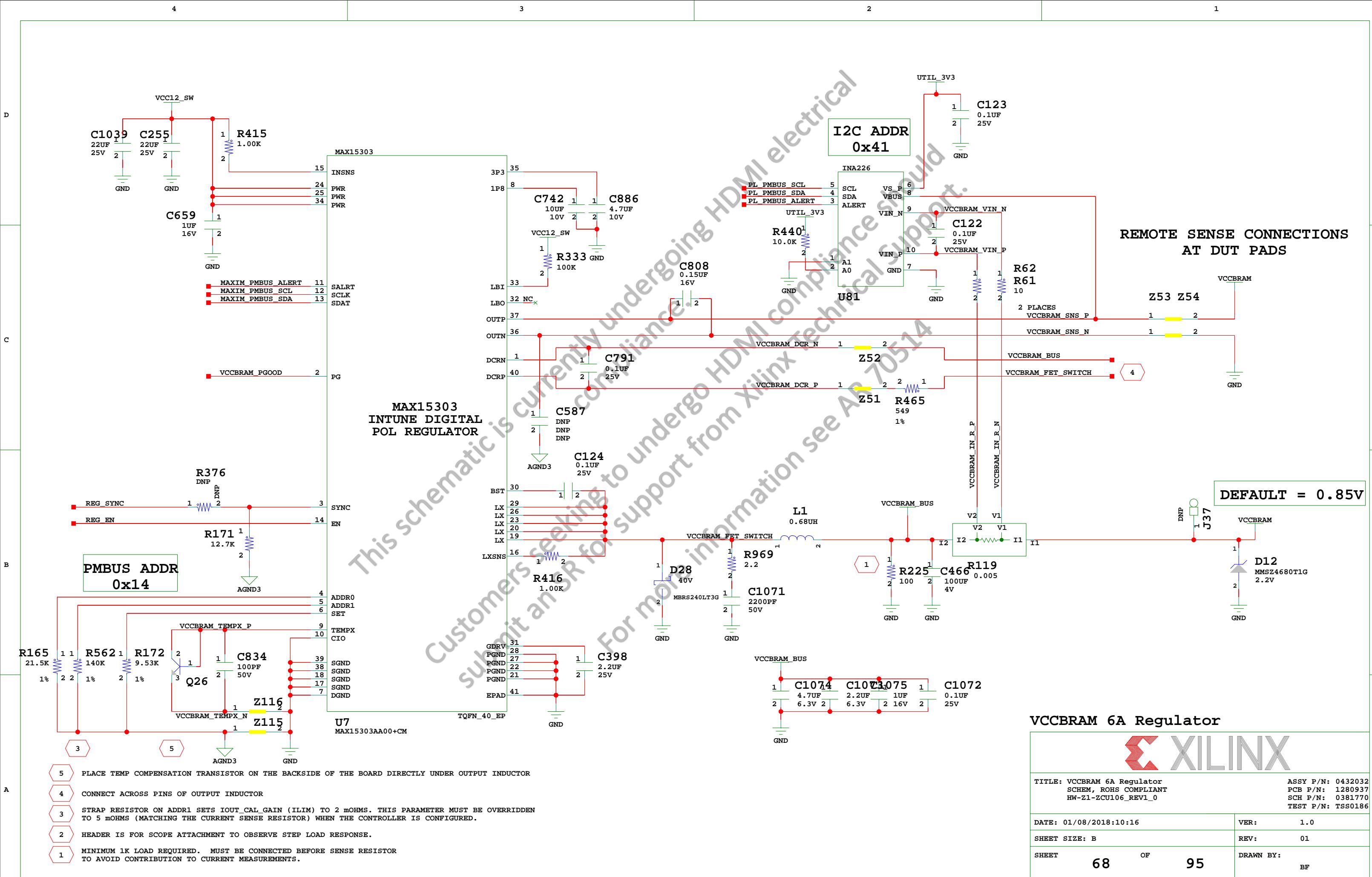
SHEET SIZE: B

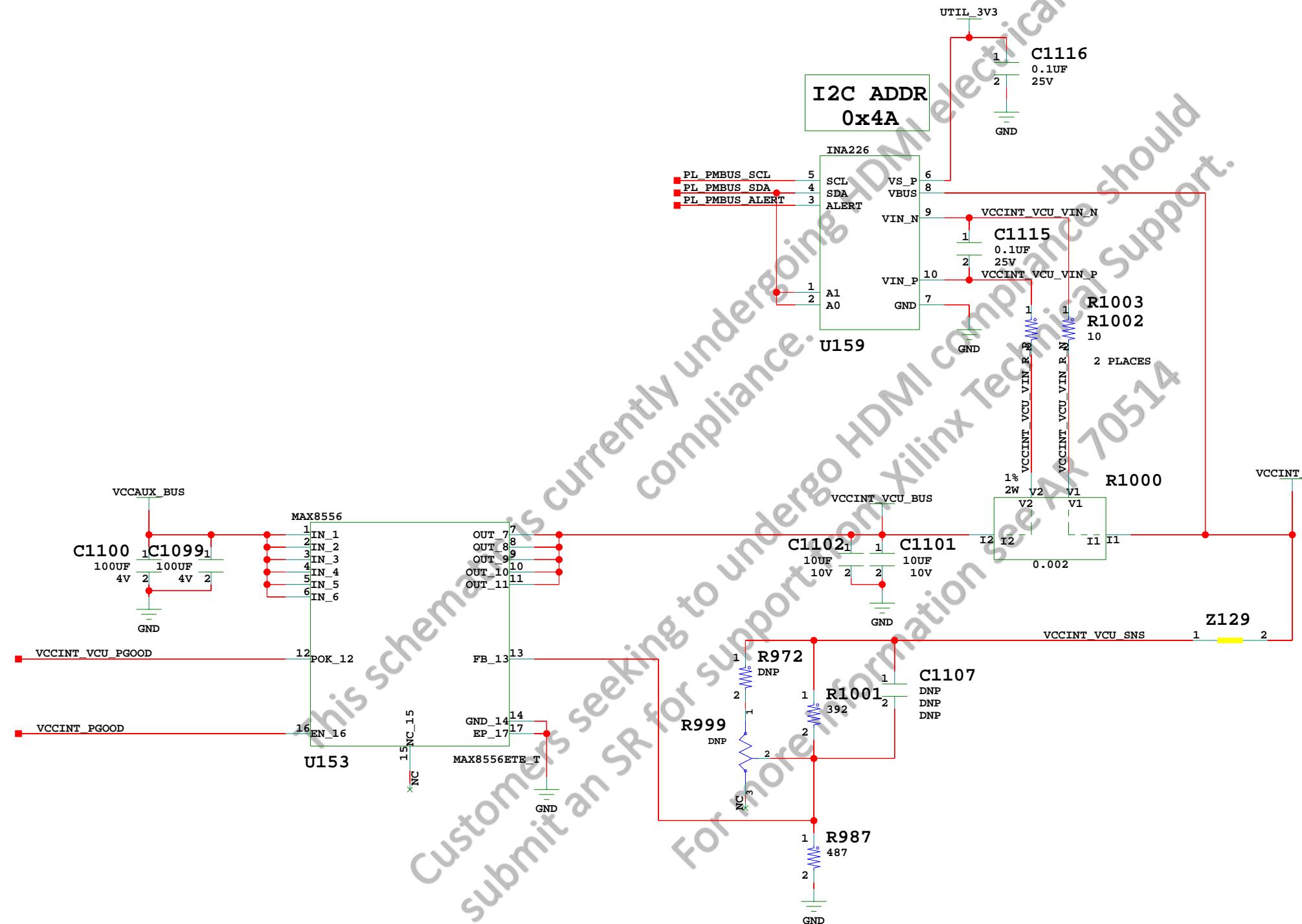
REV: 01

SHEET 66 OF 95

DRAWN BY:
BF







VCCINT_VCU 3A Regulator

TITLE: VCCINT_VCU 3A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

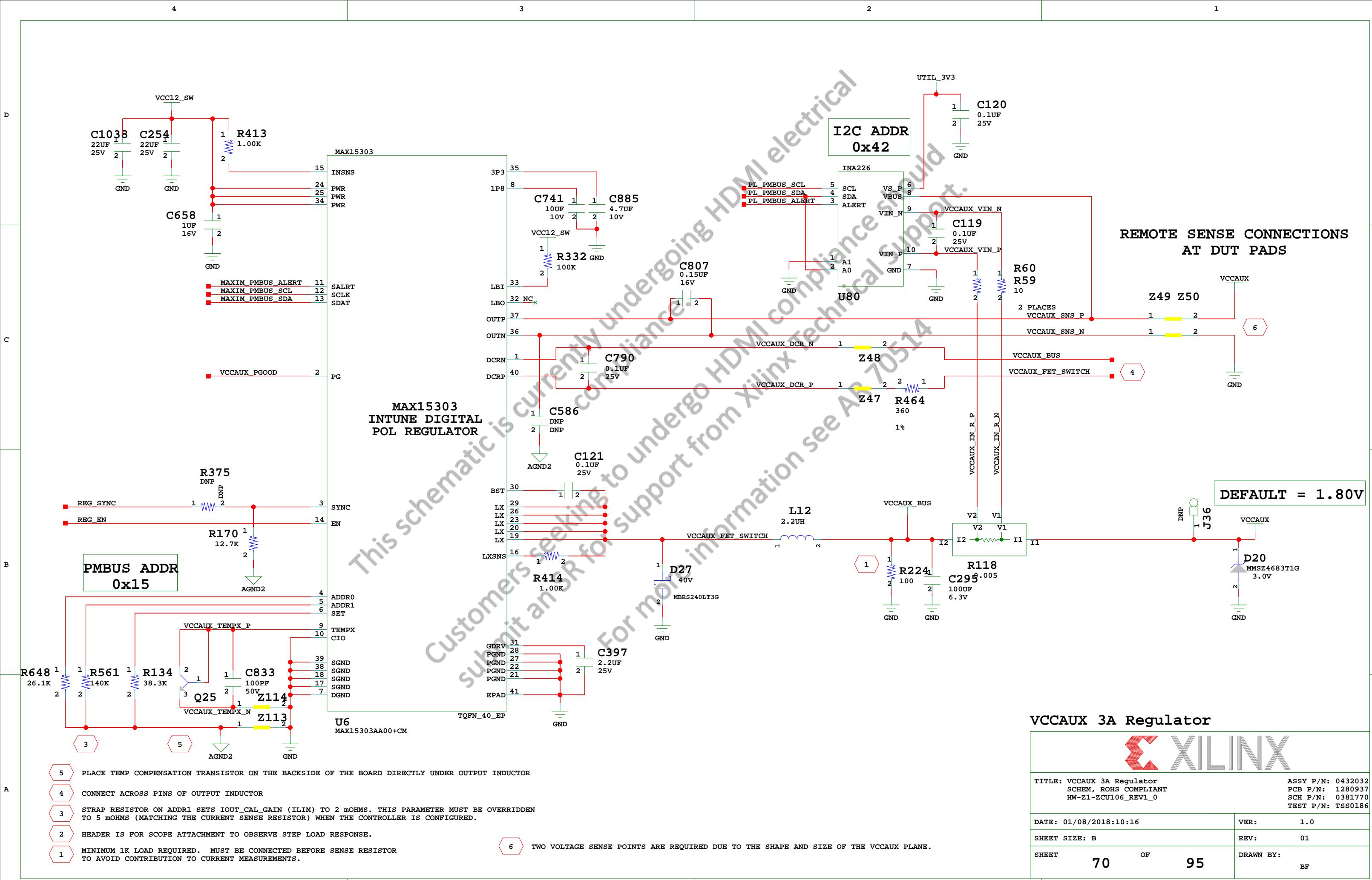
SHEET SIZE: B

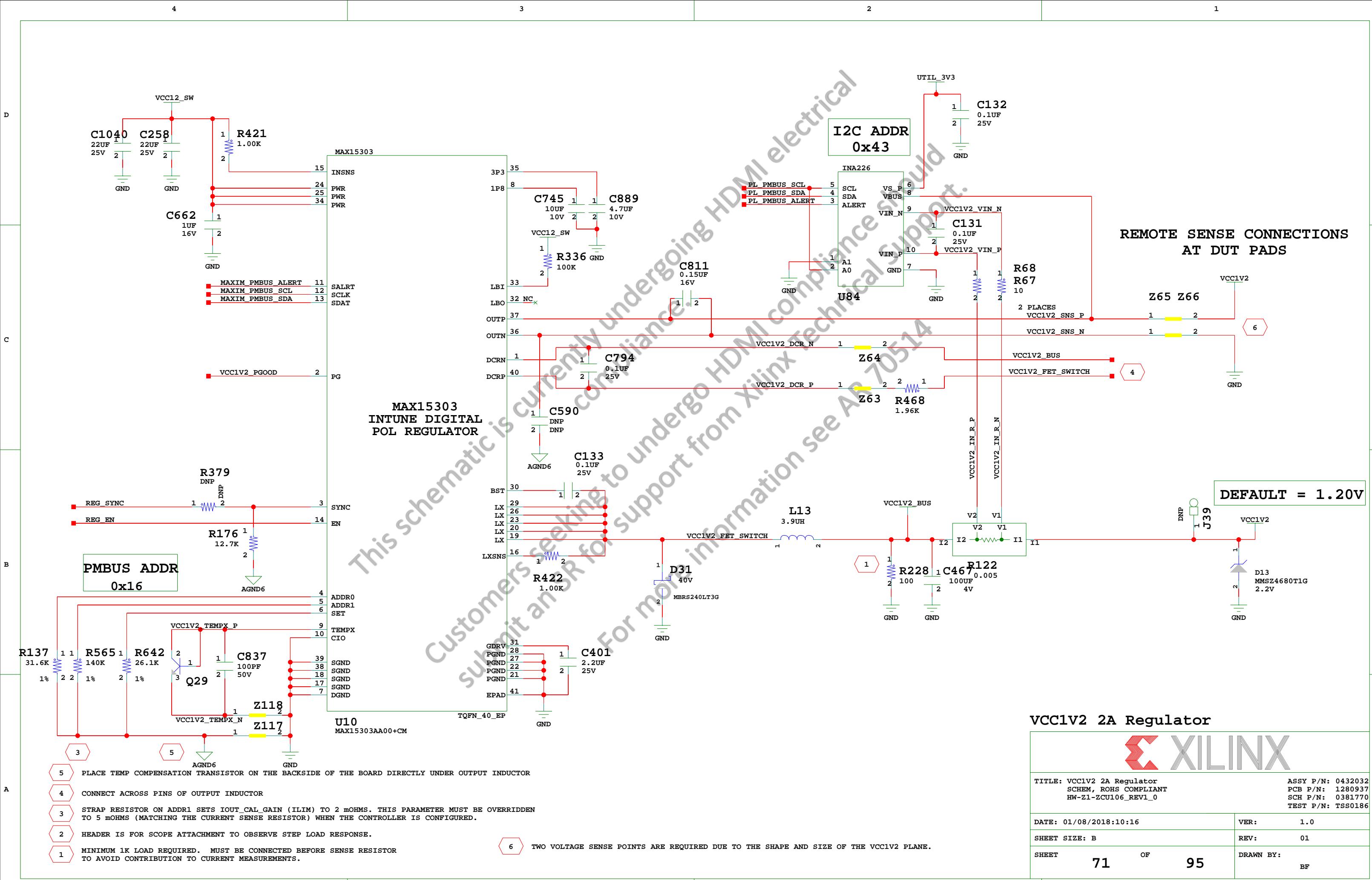
REV: 01

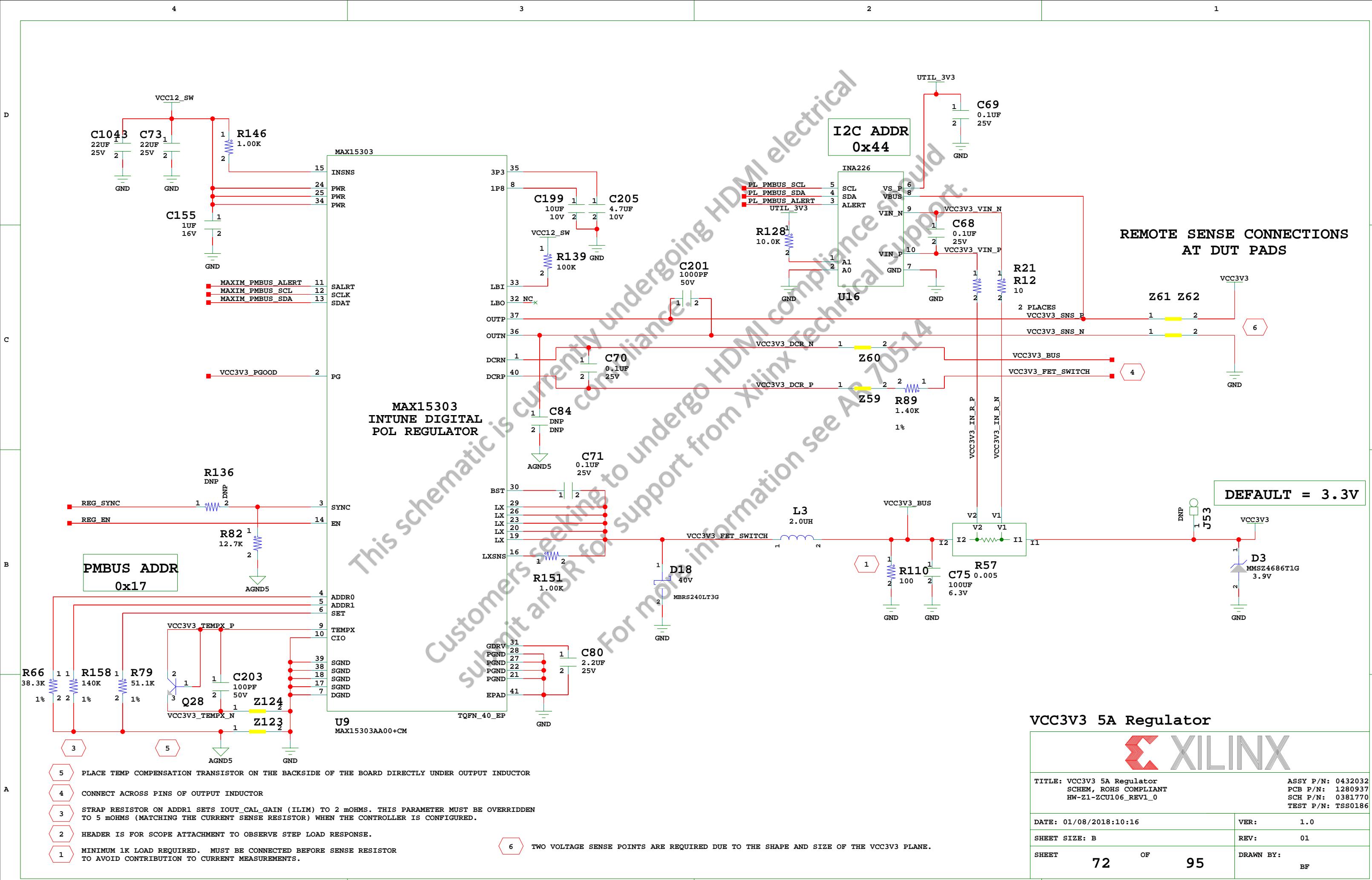
SHEET 69 OF 95

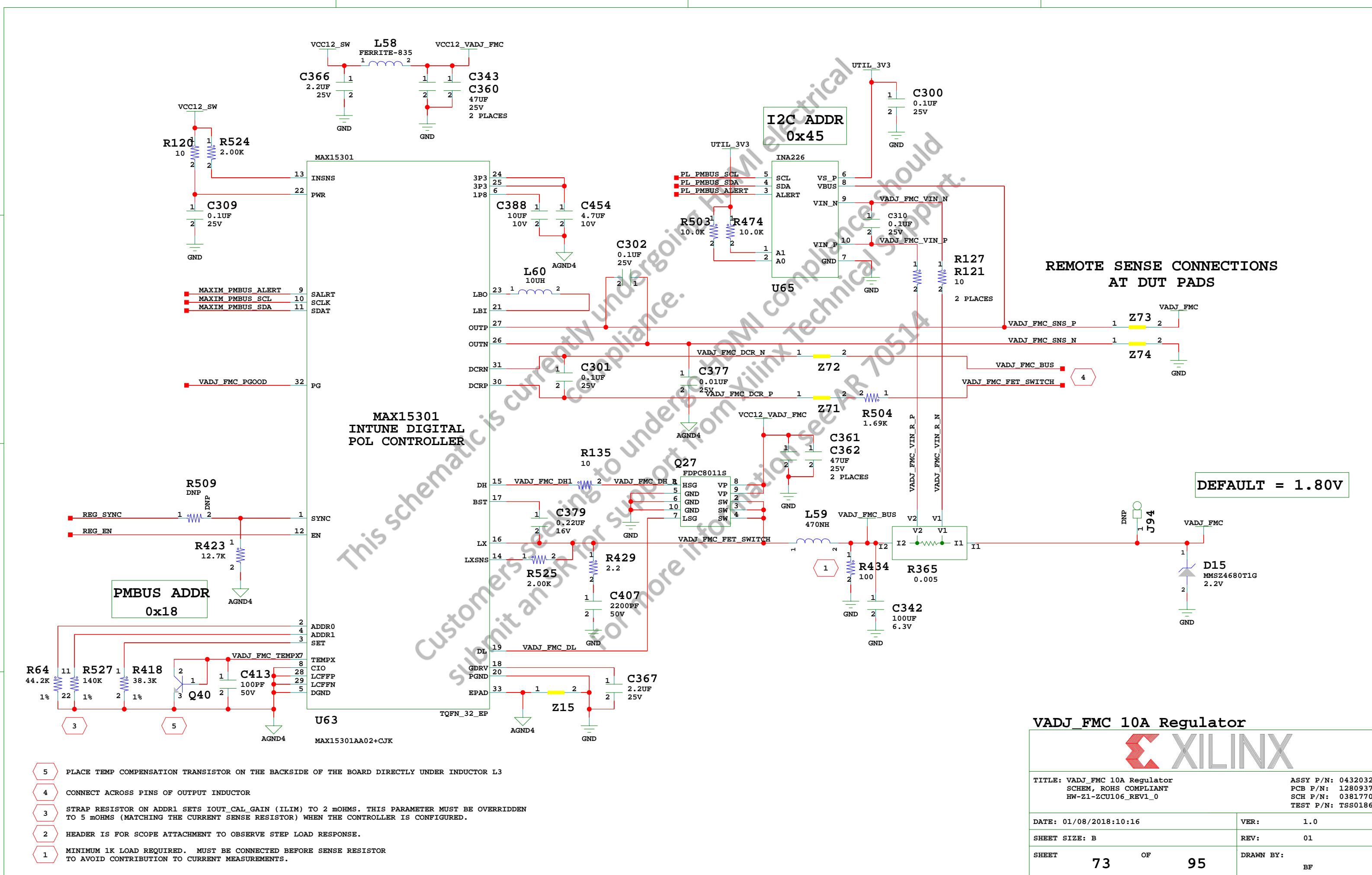
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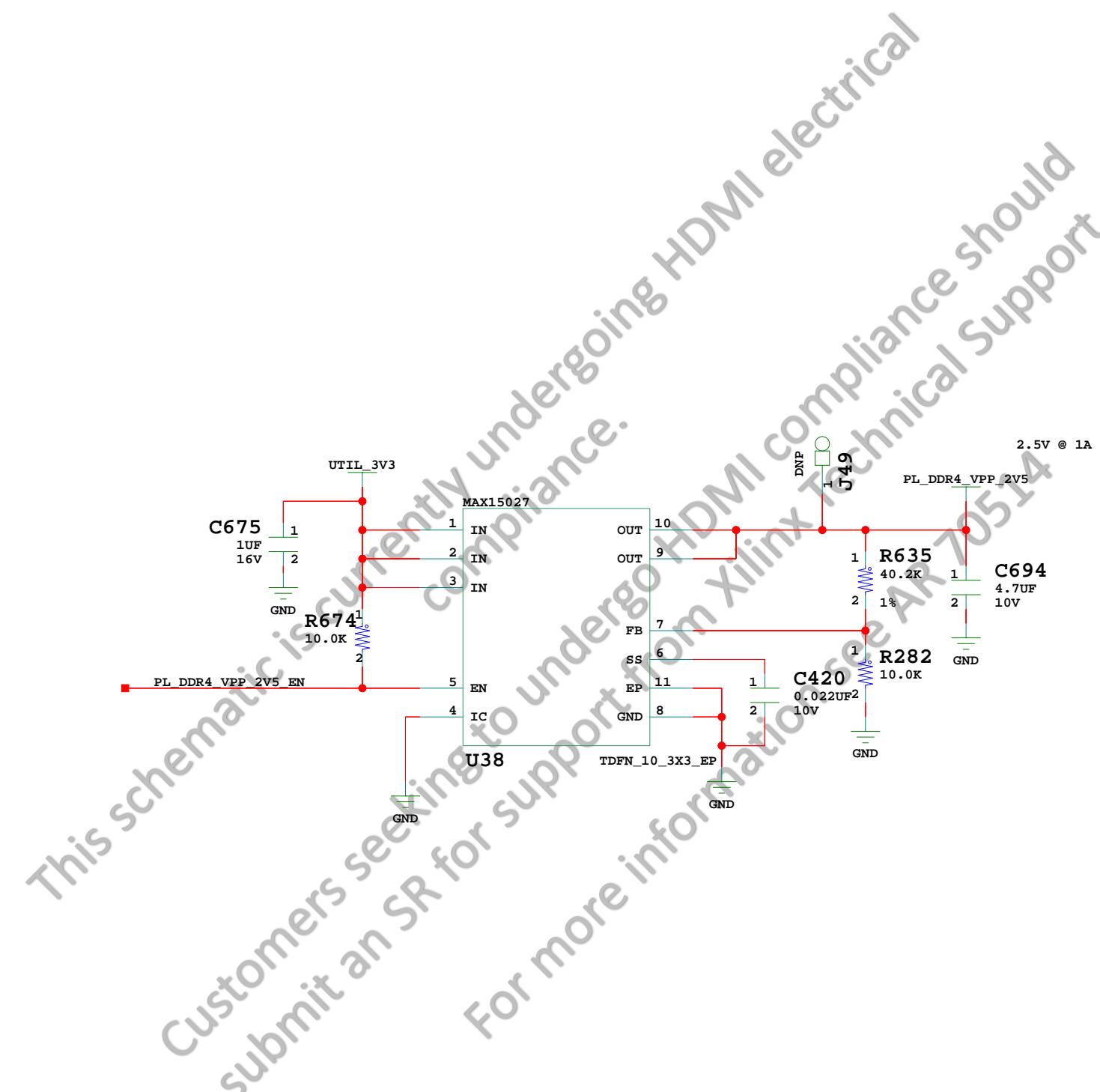
BF







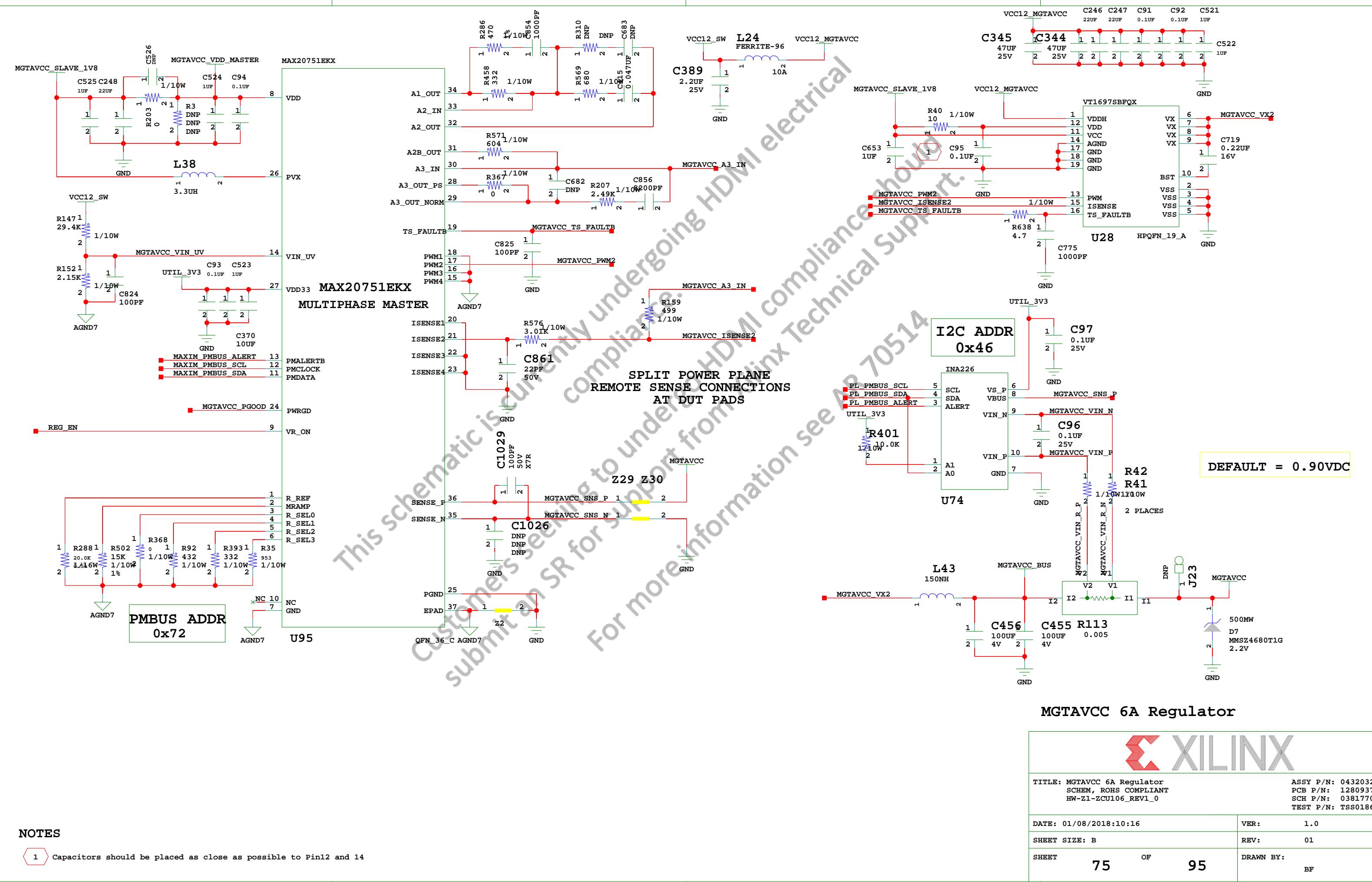


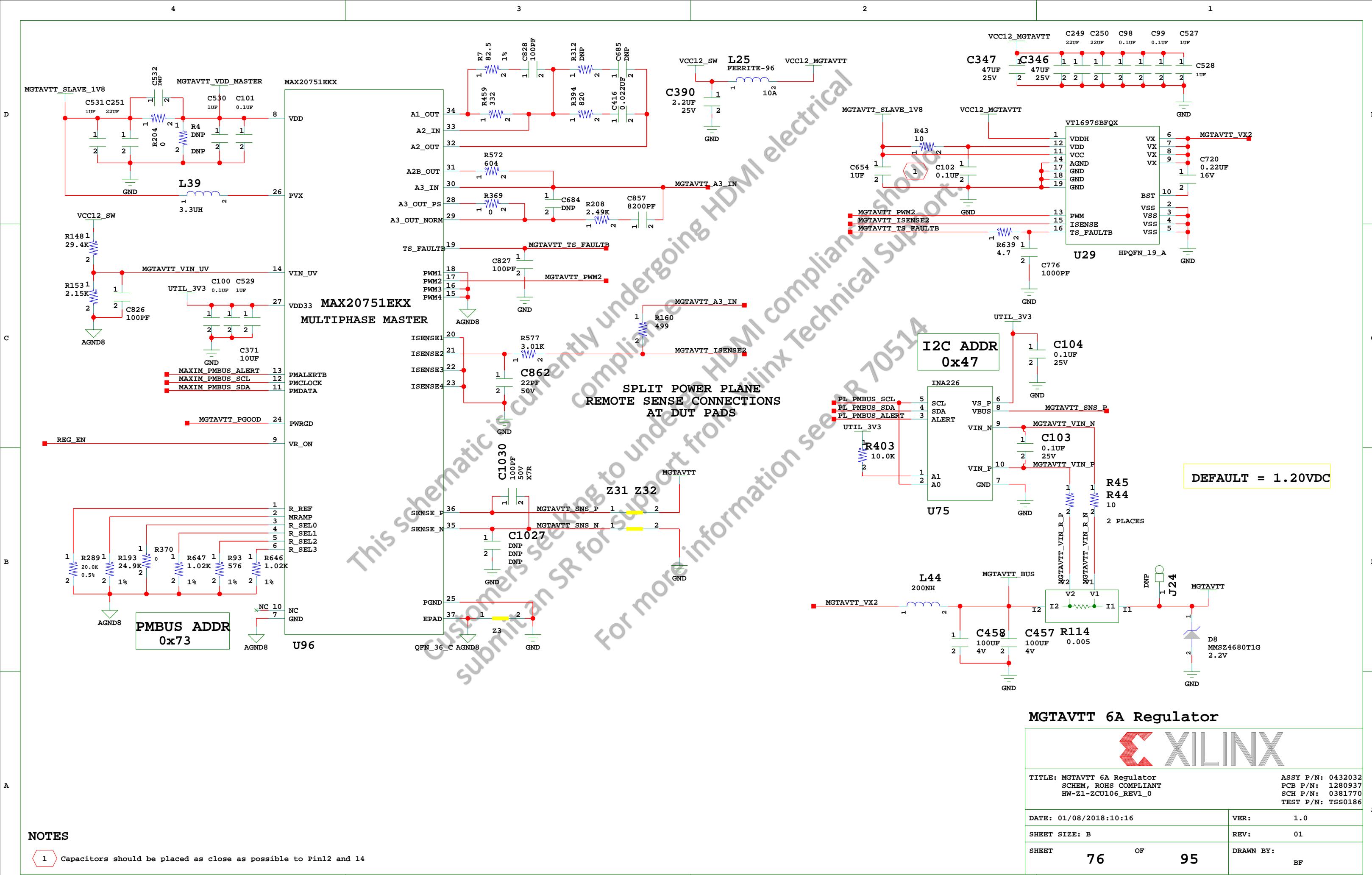


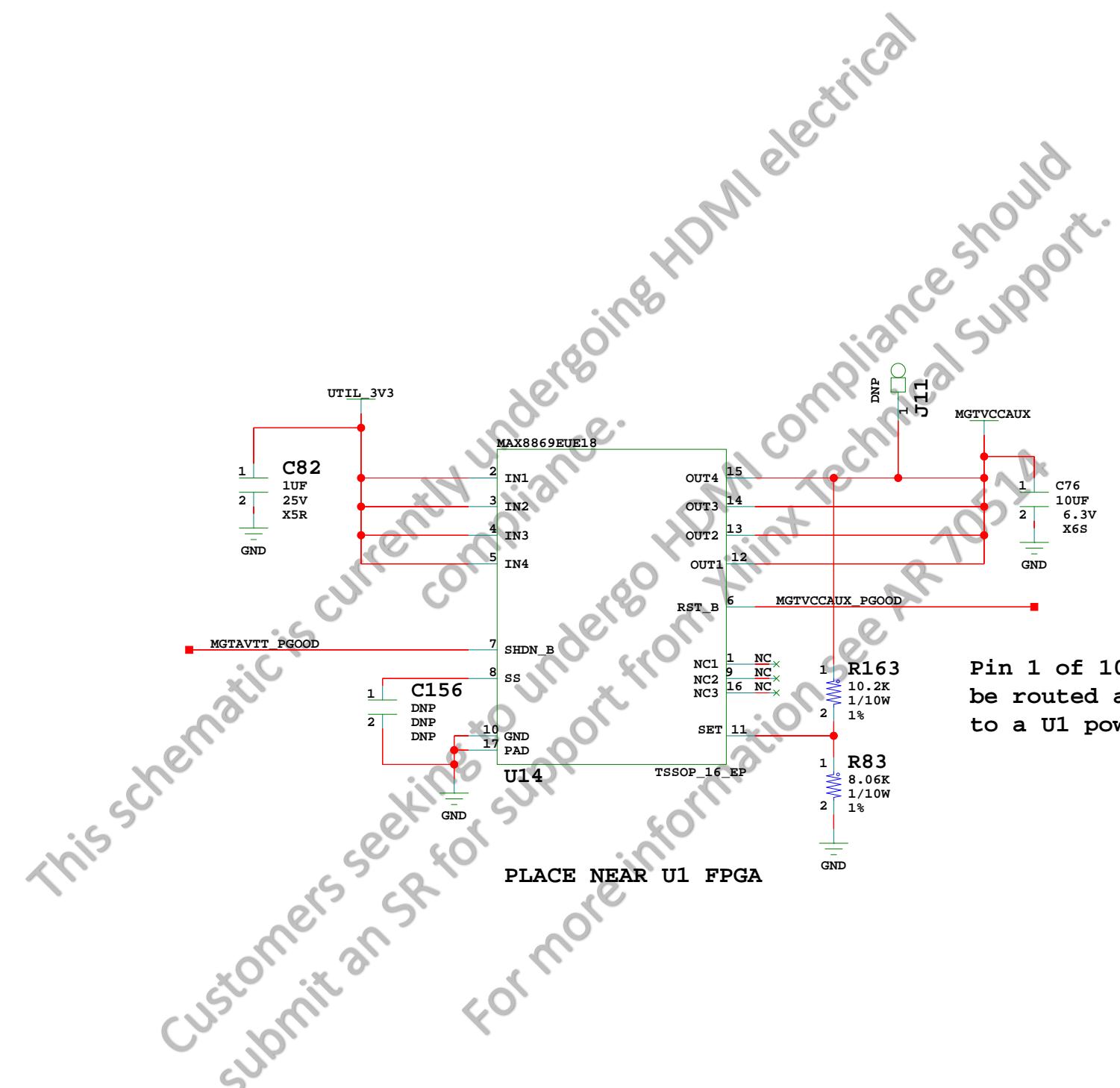
PL_DDR4_VPP_2V5 1A Regulator



TITLE: PL_DDR4_VPP_2V5 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 74 OF 95	DRAWN BY: BF







DEFAULT = 1.81VDC

MGTVCVCAUX 1A Regulator



TITLE: MGTVCVCAUX 1A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

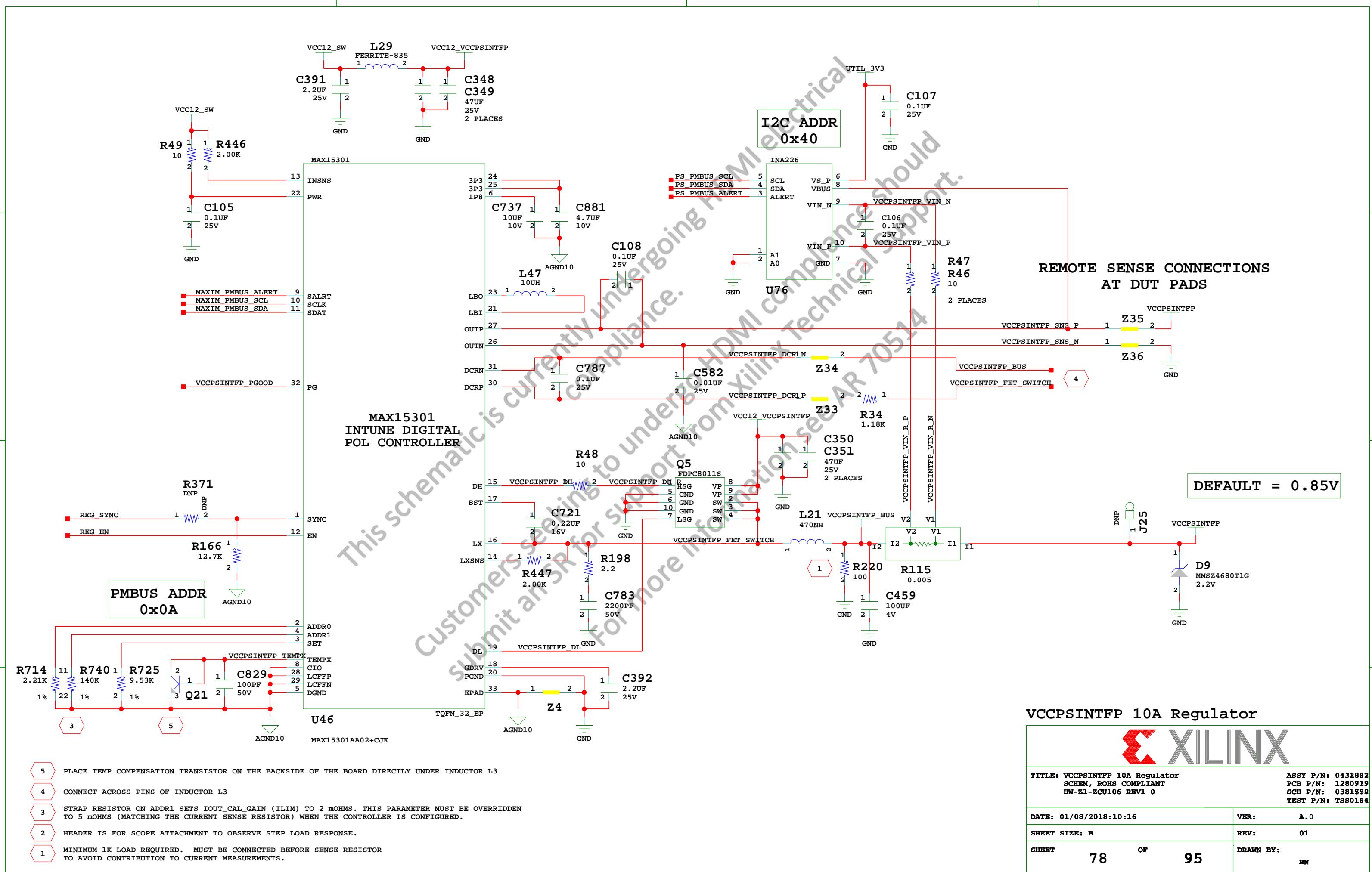
SHEET SIZE: B

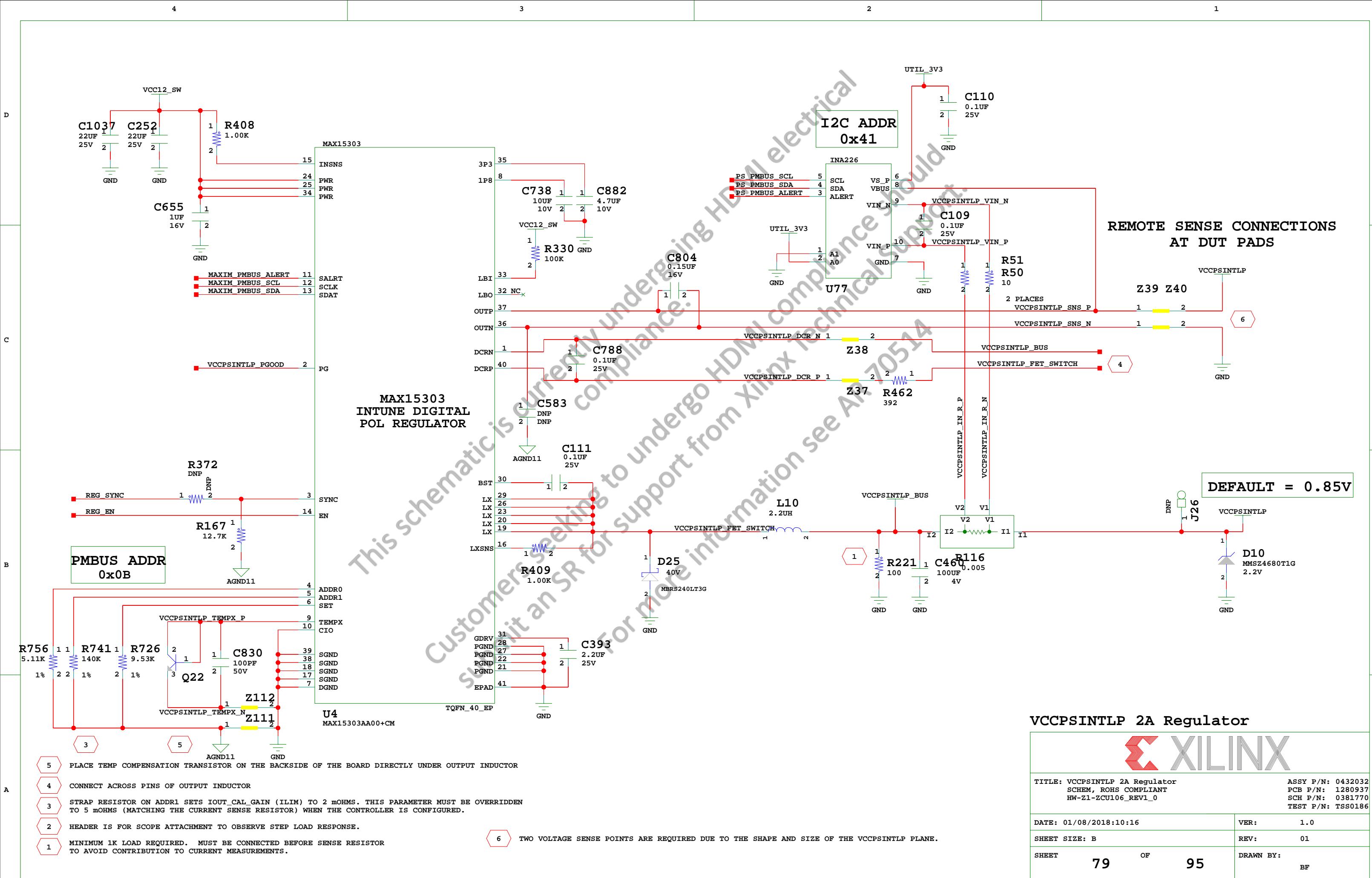
REV: 01

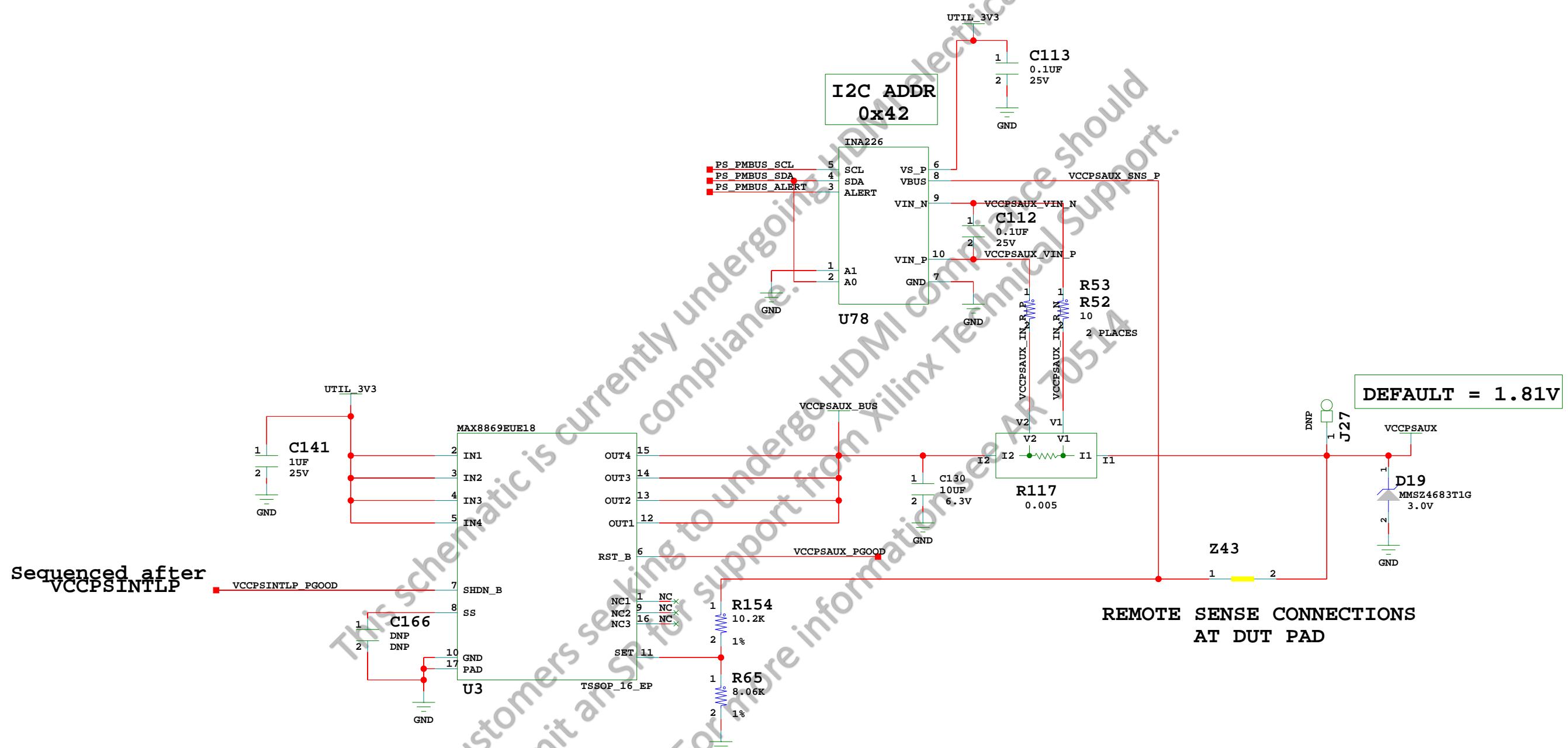
SHEET 77 OF 95

DRAWN BY:

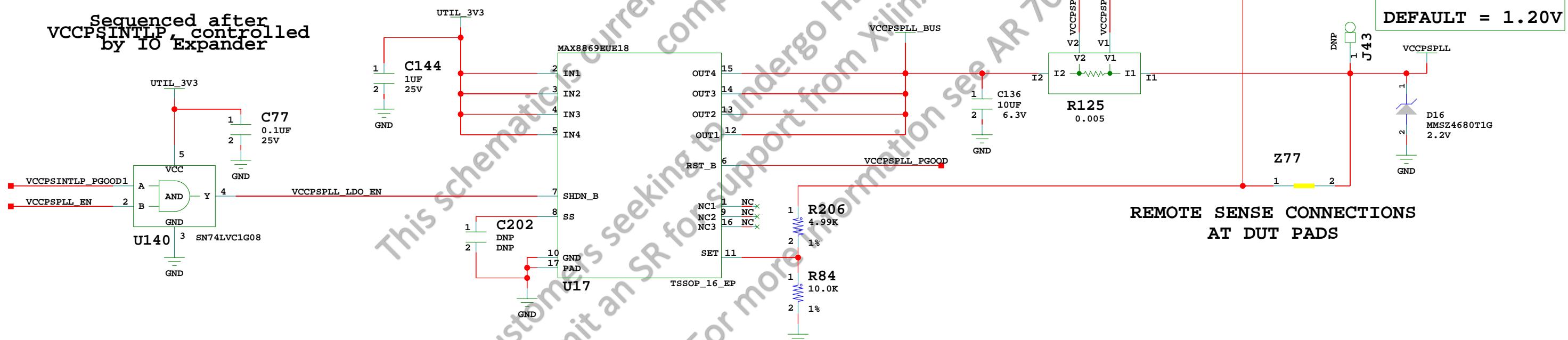
BF







Sequenced after
VCCPSINTLPC controlled
by IO Expander

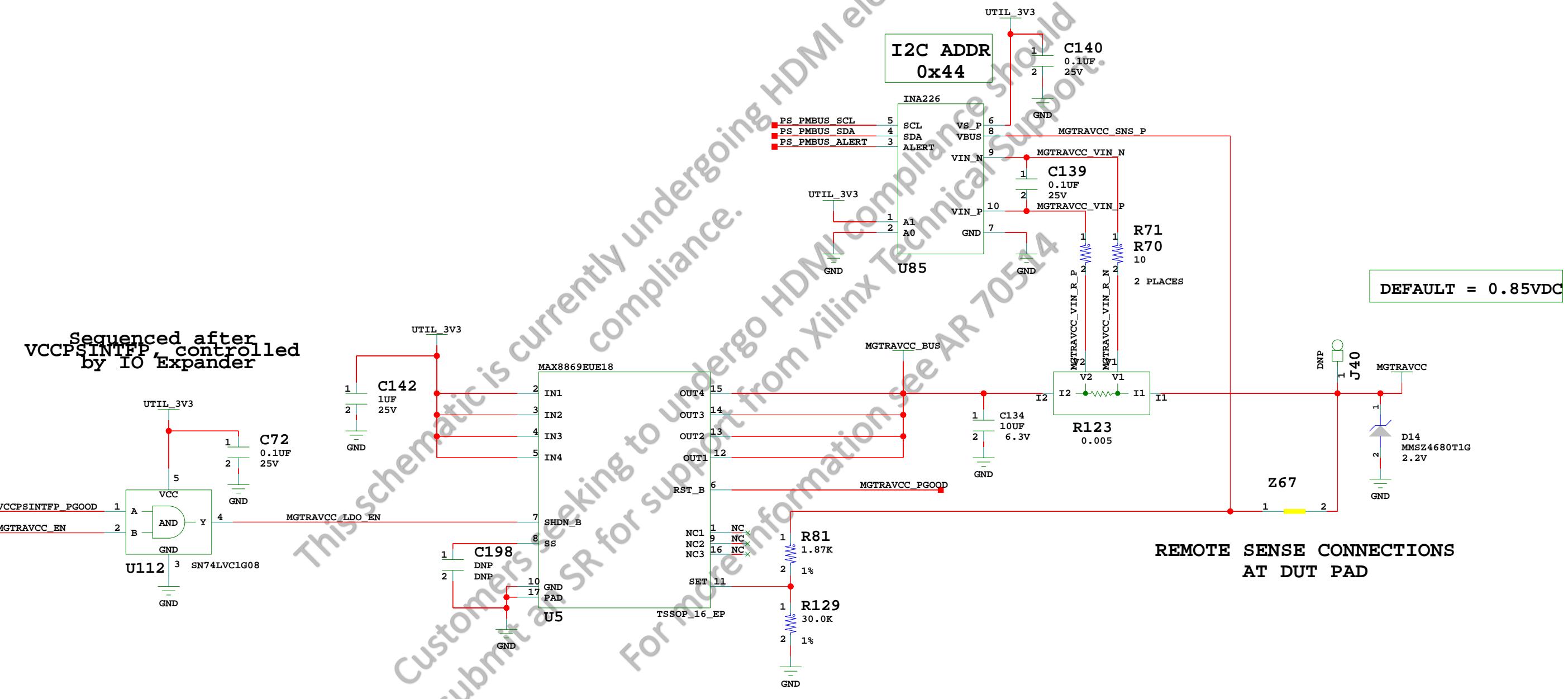


REMOTE SENSE CONNECTIONS AT DUT PADS

VCCPSPPLL 200MA Regulator



TITLE: VCCPSPPLL 200MA Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0		ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER:	1.0
SHEET SIZE: B	REV:	01
SHEET 81	OF 95	DRAWN BY: BF



MGTRAVCC 400MA Regulator

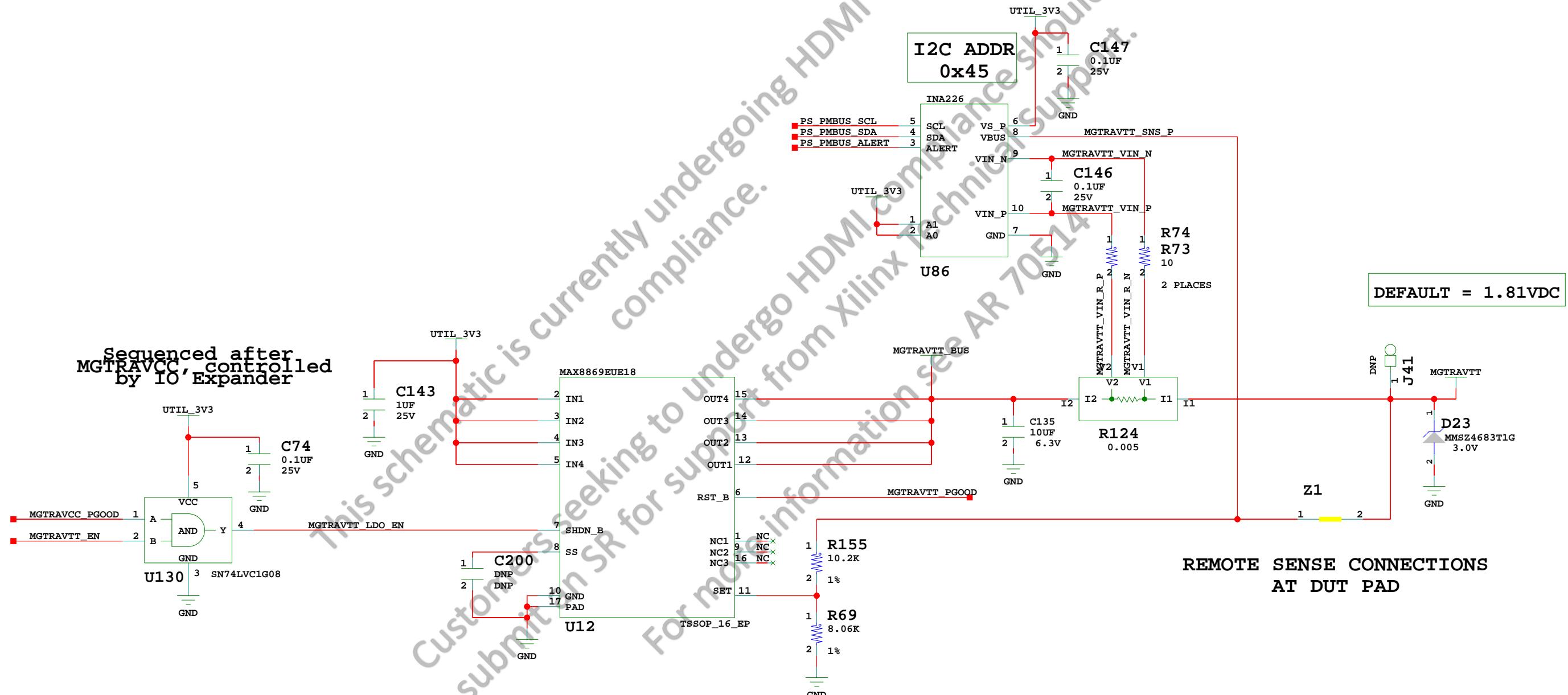


TITLE: MGTRAVCC 400MA Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 82 OF 95	DRAWN BY: BF

Sequenced after
MGTRAVCC controlled
by IO' Expander



MGTRAVTT 100MA Regulator



TITLE: MGTRAVTT 100MA Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

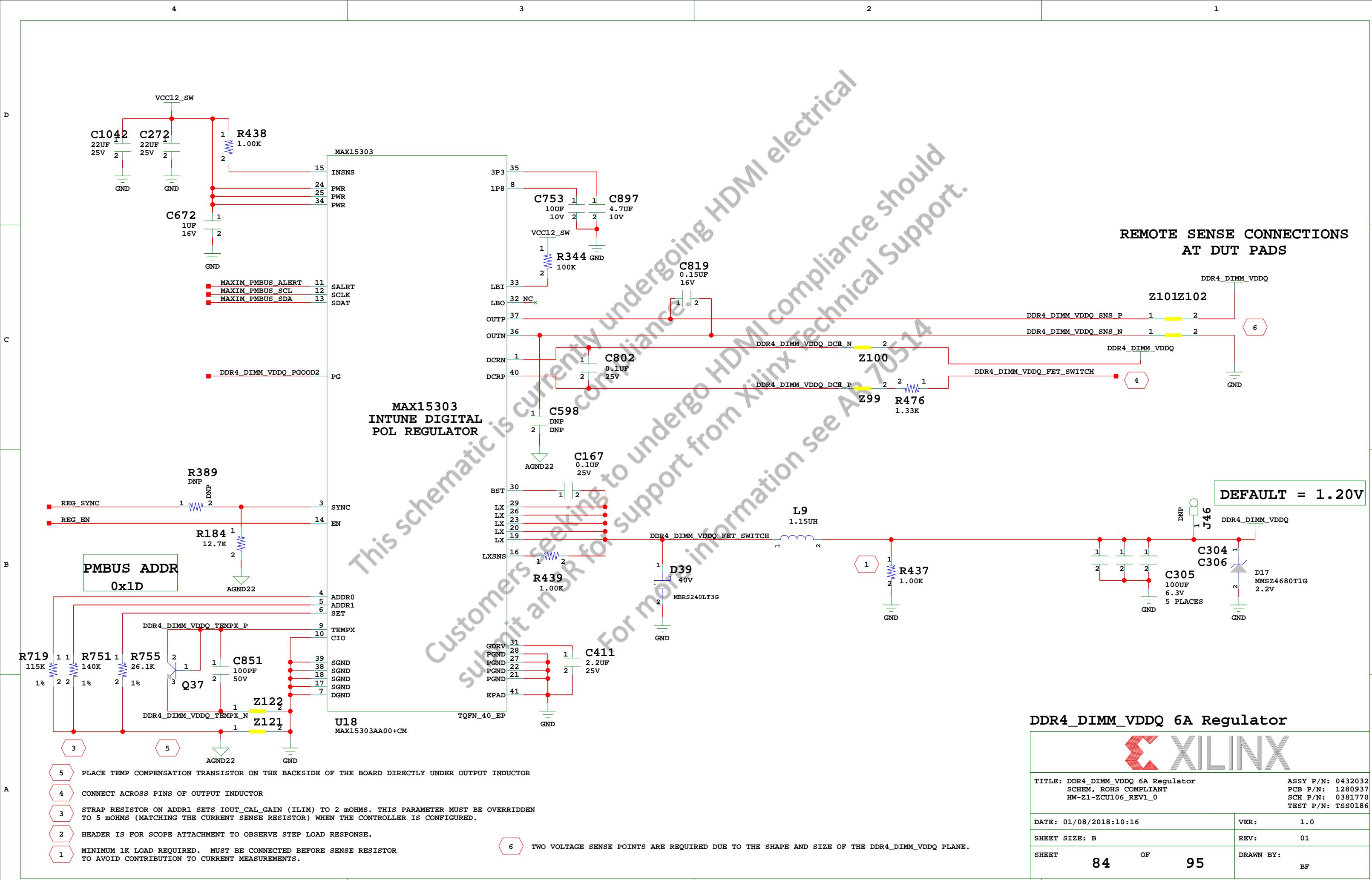
SHEET SIZE: B

REV: 01

SHEET 83 OF 95

DRAWN BY:

BF



This schematic diagram illustrates a MAX15027-based circuit configuration. The IC (U39) is a TDFN_10_3X3_EP package. Key components include:

- Power Supply:** PS_DDR4_VPP_2V5 is connected to pin 5 (EN) and pin 11 (EP).
- Feedback Path:** A 10.0K resistor (R675) connects pin 4 (IC) to ground.
- Input Path:** Pin 1 (IN) receives input from J9 (pin 2) through a 10.0K resistor (R675). Pin 2 (IN) receives input from C676 (1UF, 16V) via a 10.0K resistor (R675).
- Output Path:** Pin 10 (OUT) is connected to PS_DDR4_VPP_2V5 via R636 (40.2K, 1%) and C421 (0.022UF, 10V).
- Decoupling and Grounding:** Various capacitors (C676, C695, C421) and resistors (R284, R636) are used for power supply bypassing and noise reduction. Ground connections (GND) are present at multiple points throughout the circuit.

PS_DDR4_VPP_2V5 1A Regulator



**TITLE: PS_DDR4_VPP_2V5_1A Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106 REV1.0**

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

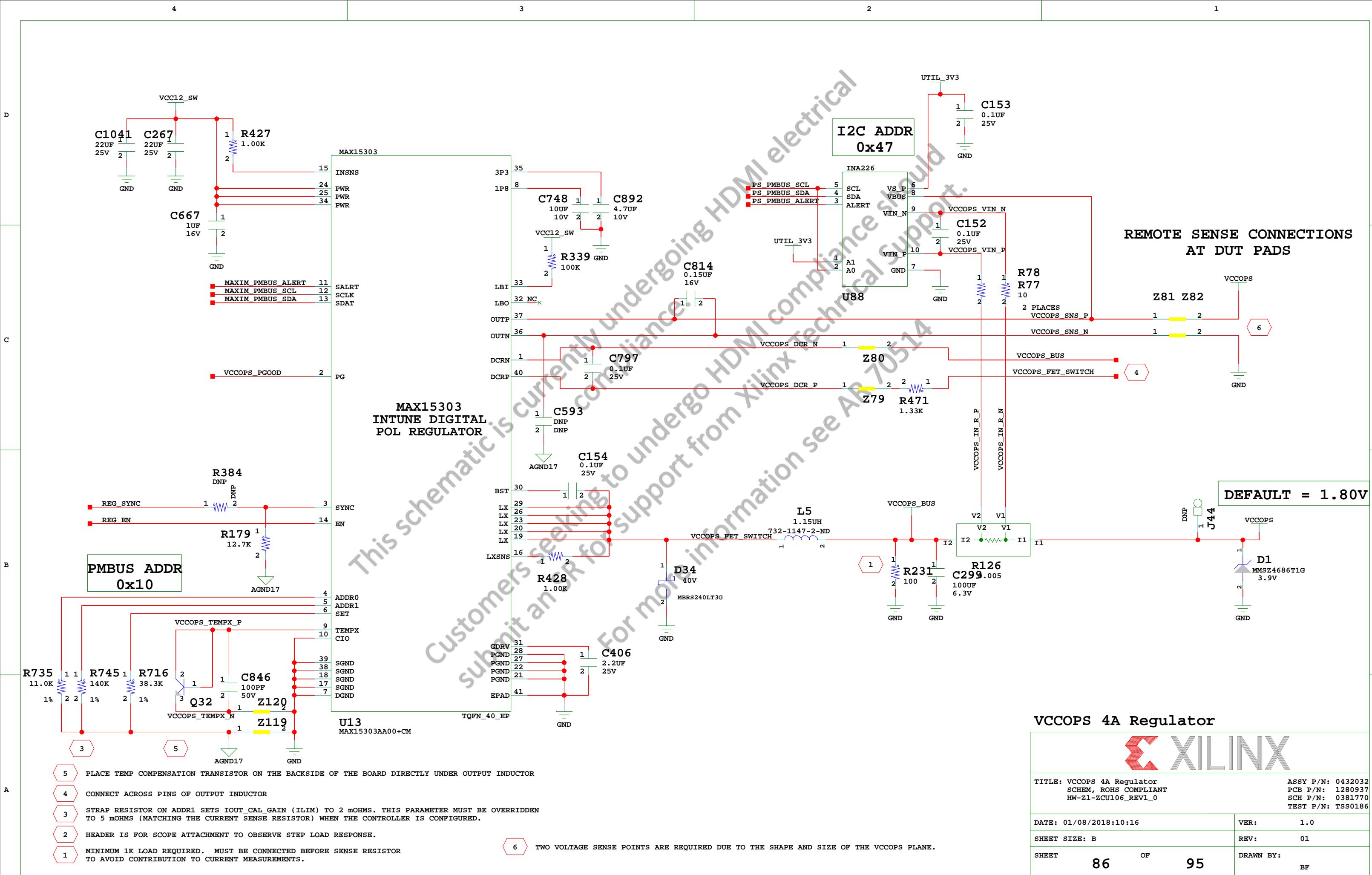
VERB: 1.0

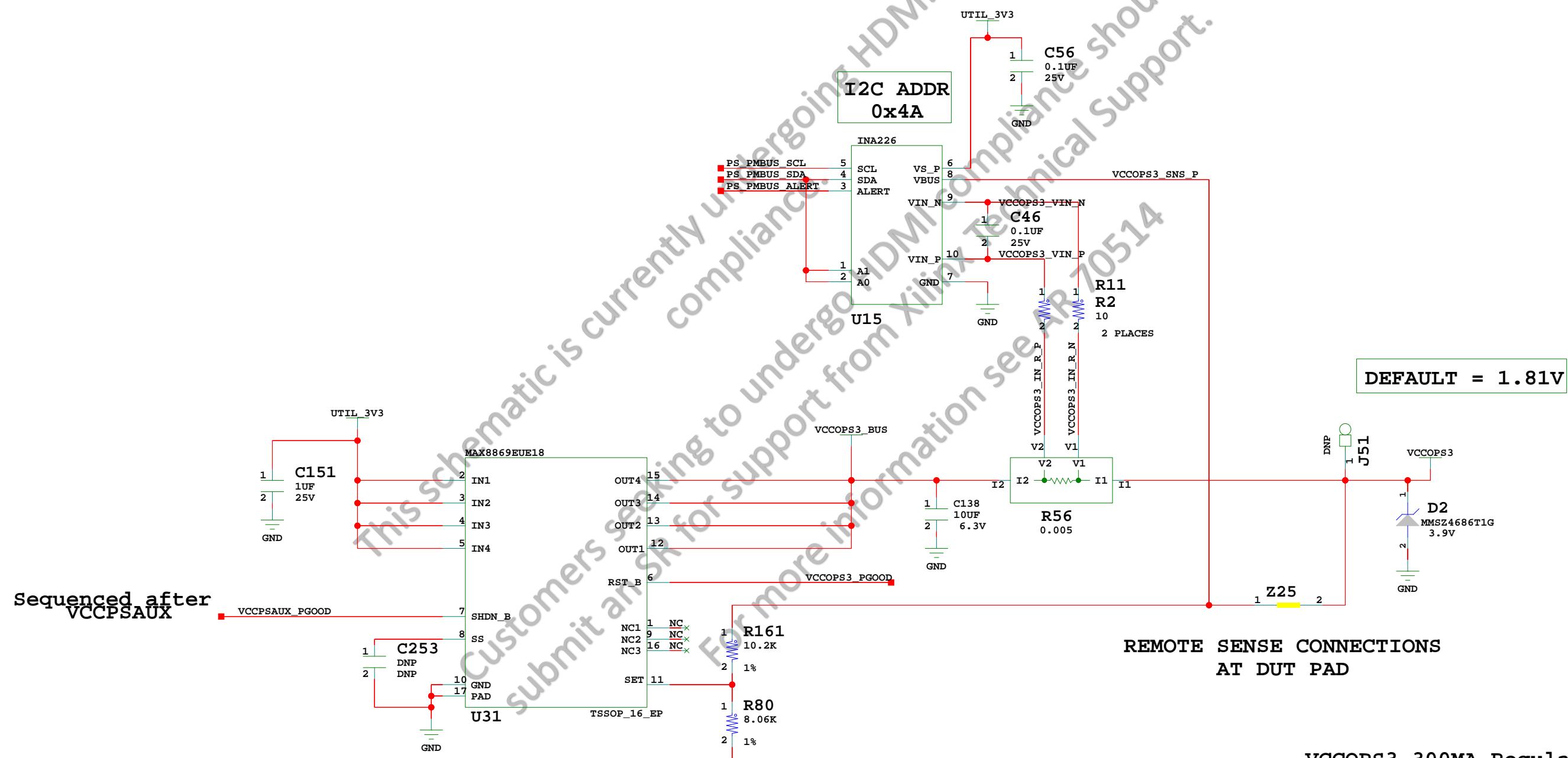
SHEET SIZE: B

REV.

SHEET 85 OF 95

DRAWN BY:





VCCOPS3 300MA Regulator



TITLE: VCCOPS3 300MA Regulator
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 87 OF 95

DRAWN BY:

BF

~~VCCPSINTFP~~ controlled
by IO Expander

The diagram illustrates a power supply network. At the top, a blue line labeled **UTIL_3V3** is connected to the **1** terminal of a component labeled **C145**. The **2** terminal of C145 is connected to ground (**GND**). The output of C145 is connected to the **1** terminal of a component labeled **C204**. The **2** terminal of C204 is also connected to ground (**GND**). A red line labeled **SDDRPLL_LDO_EN** is connected to the **1** terminal of C204. The **2** terminal of C204 is connected to ground (**GND**). The **10** terminal of C204 is connected to a green line labeled **MA**, which then branches into four parallel lines labeled **I**, **I**, **I**, and **I**. The **17** terminal of C204 is connected to ground (**GND**).

VCCPSDDRPLL_PGOOD

OUT4 15

OUT3 14

OUT2 13

OUT1 12

RST_B 6

TSSOP_16_EP

1 NC
9 NC
16 NC
NC3

SET 11

1 R157
10.2K
2 1%

1 R72
8.06K
2 1%

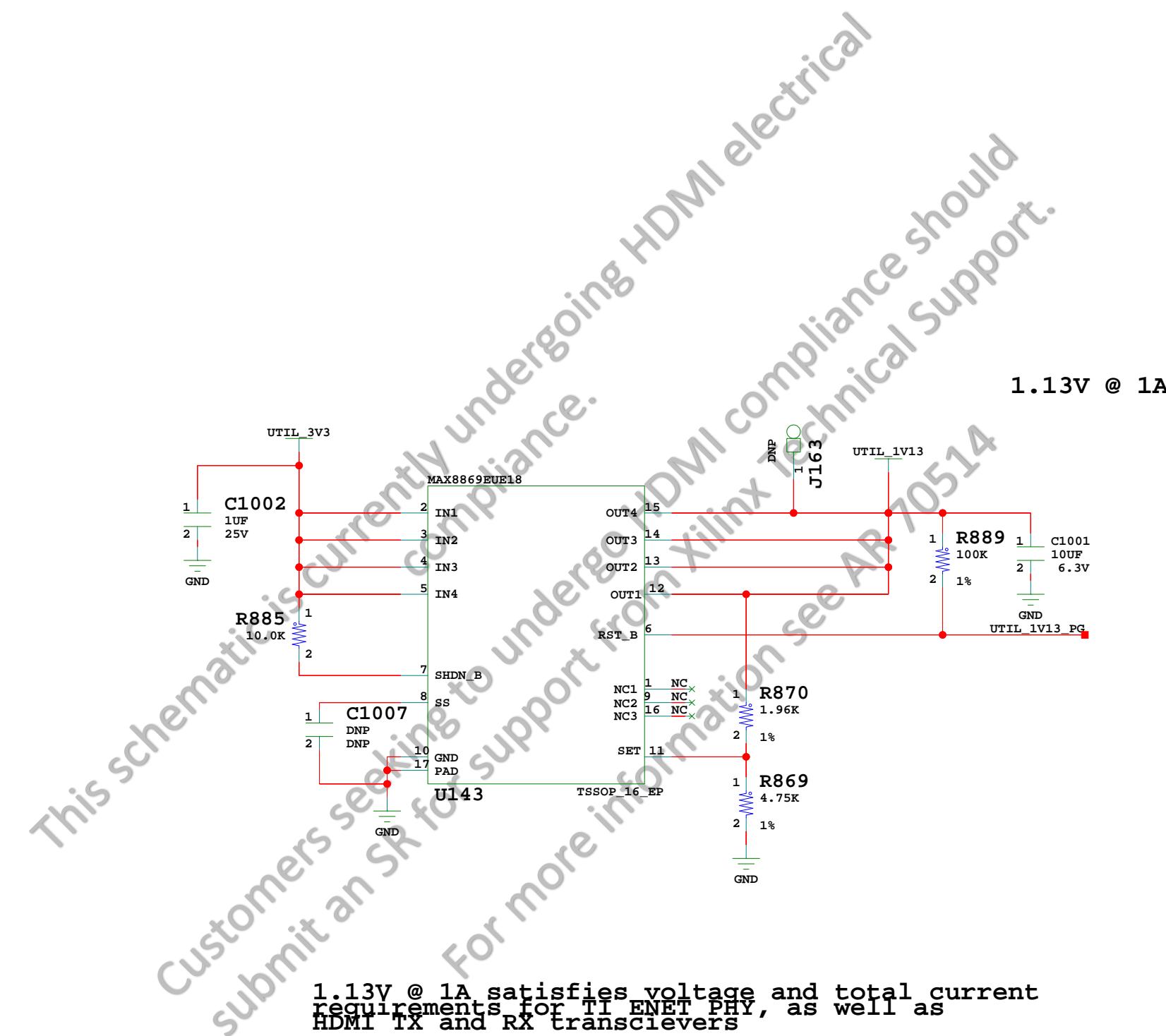
1 C137
10uF
2 6.3V

GND

VCCPSDDRPLL 100MA Regulator



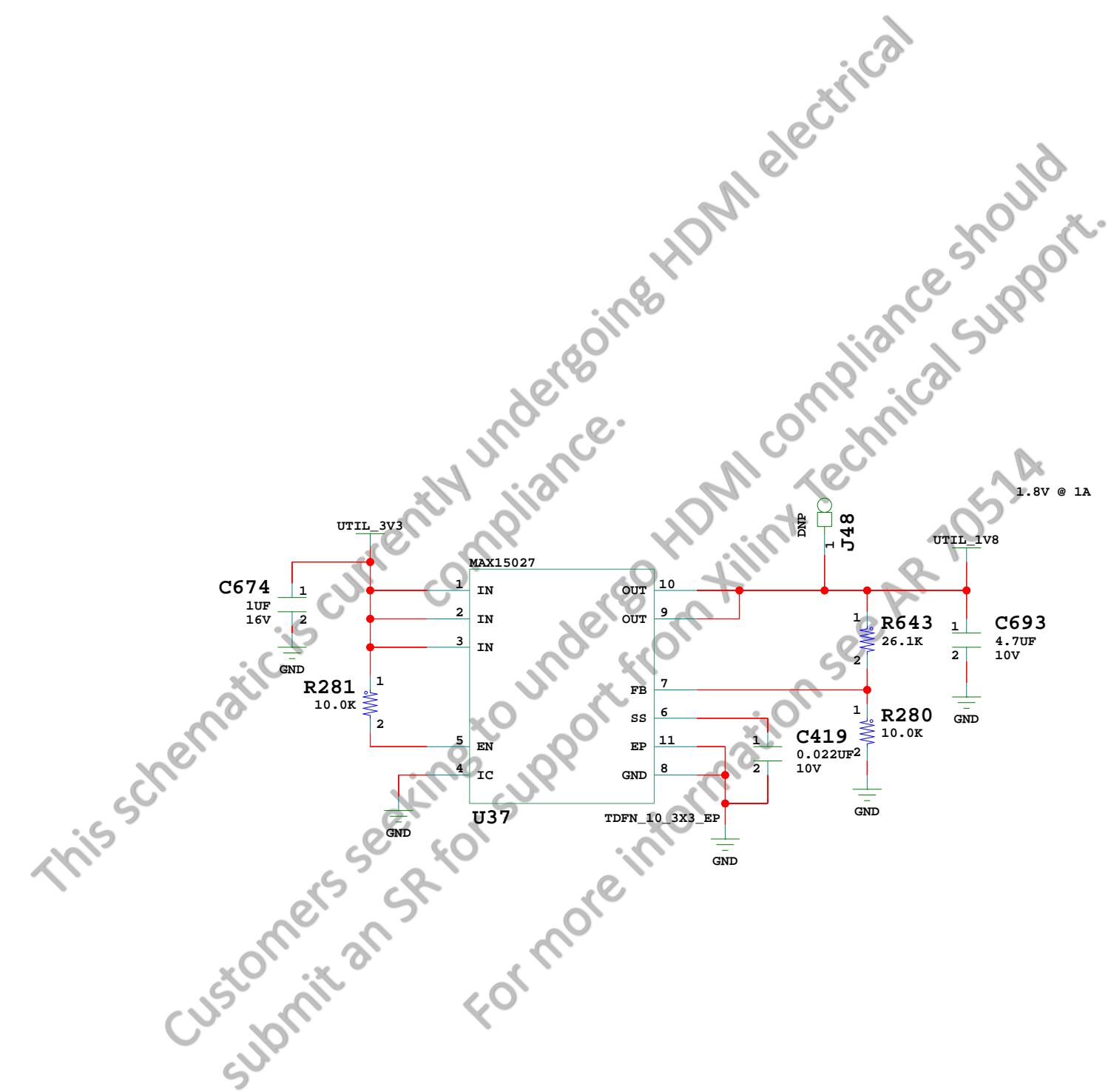
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DATE: 01/08/2018:10:16	VER:	1.0
SHEET SIZE: B	REV:	01
SHEET 88	OF 95	DRAWN BY: BF



UTIL_1V13 1A Regulator



TITLE: UTIL_1V13 1A Regulator SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 89 OF 95	DRAWN BY: BF



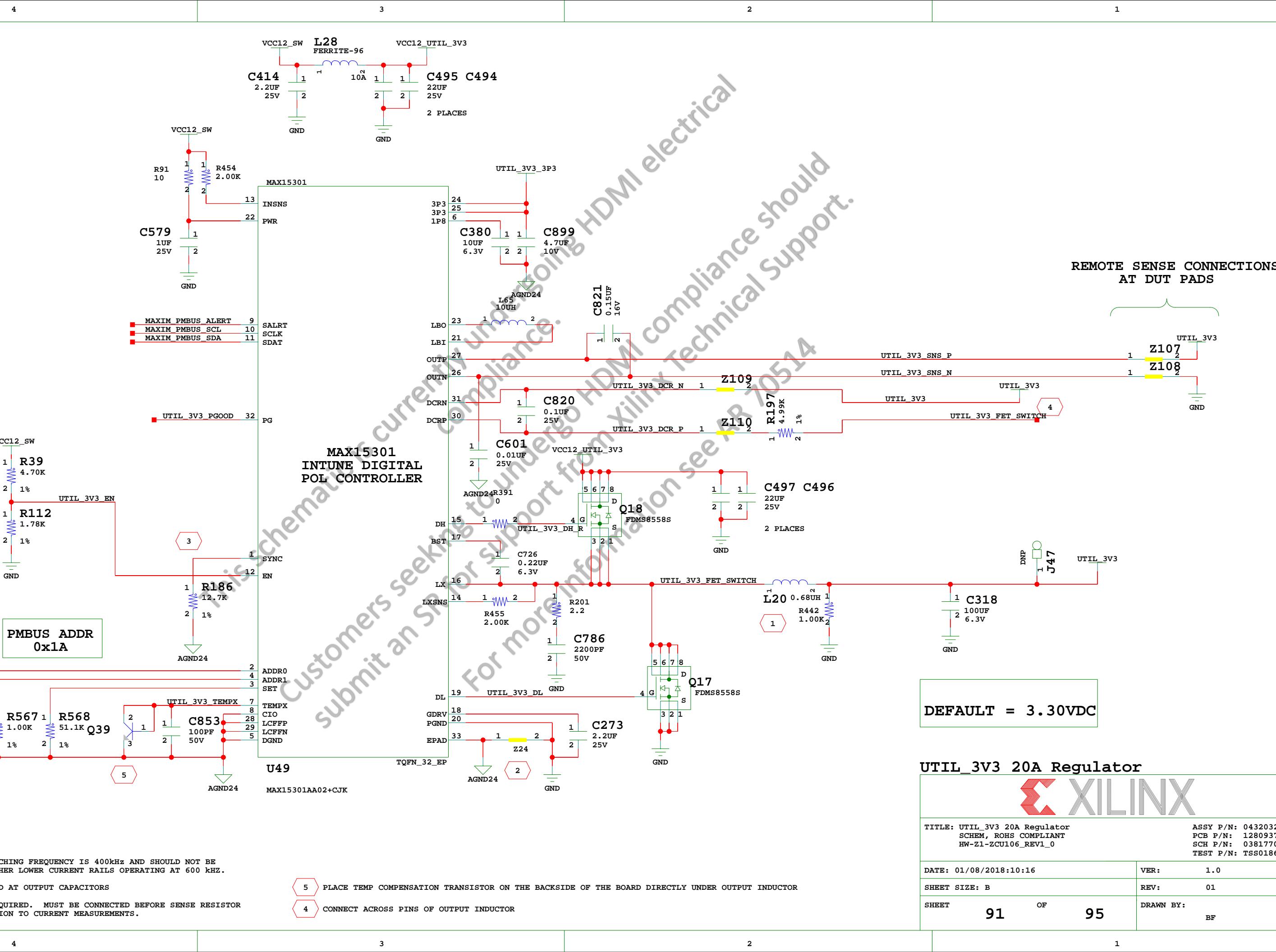
UTIL_1V8 1A Regulator

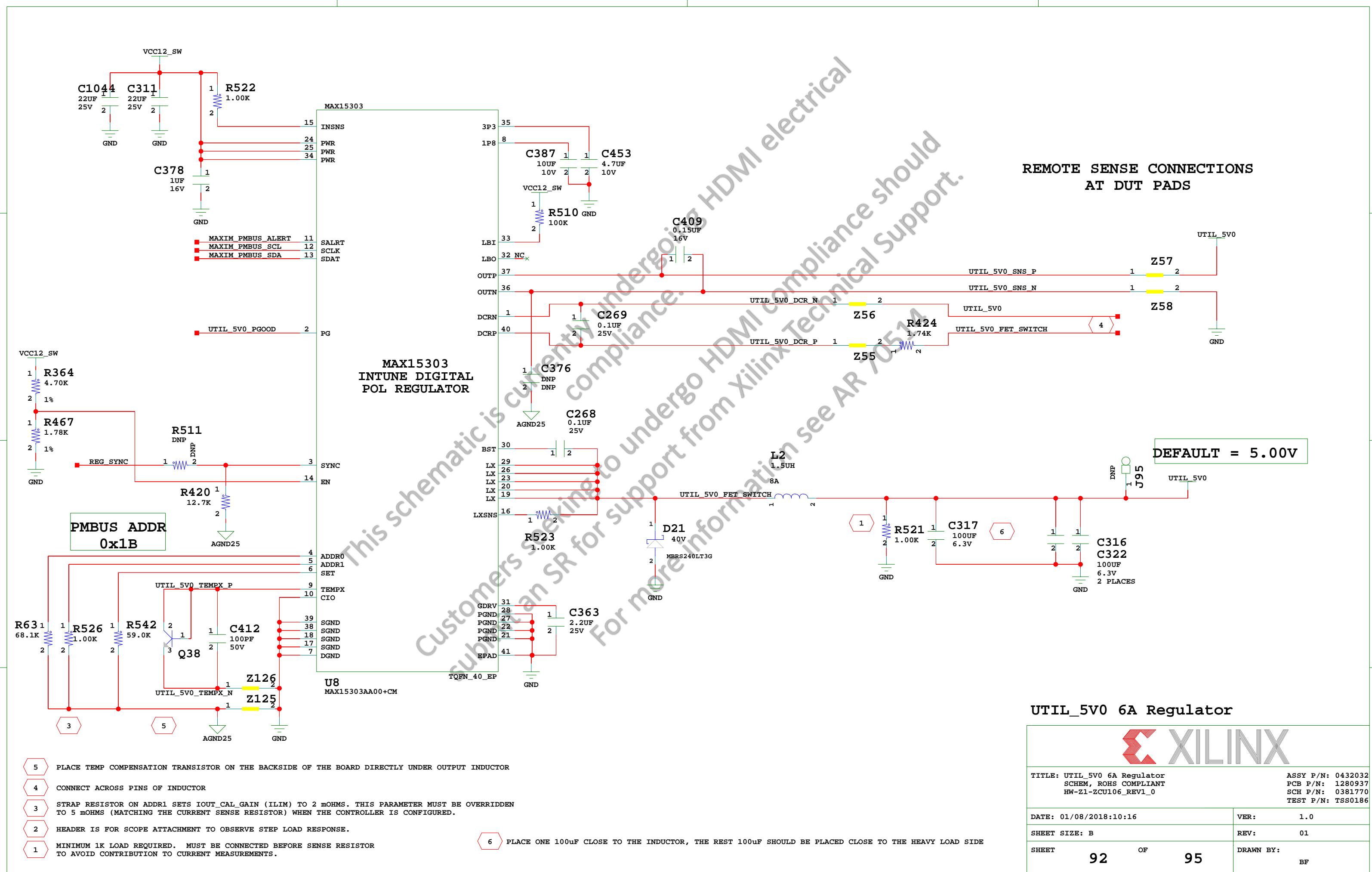


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SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

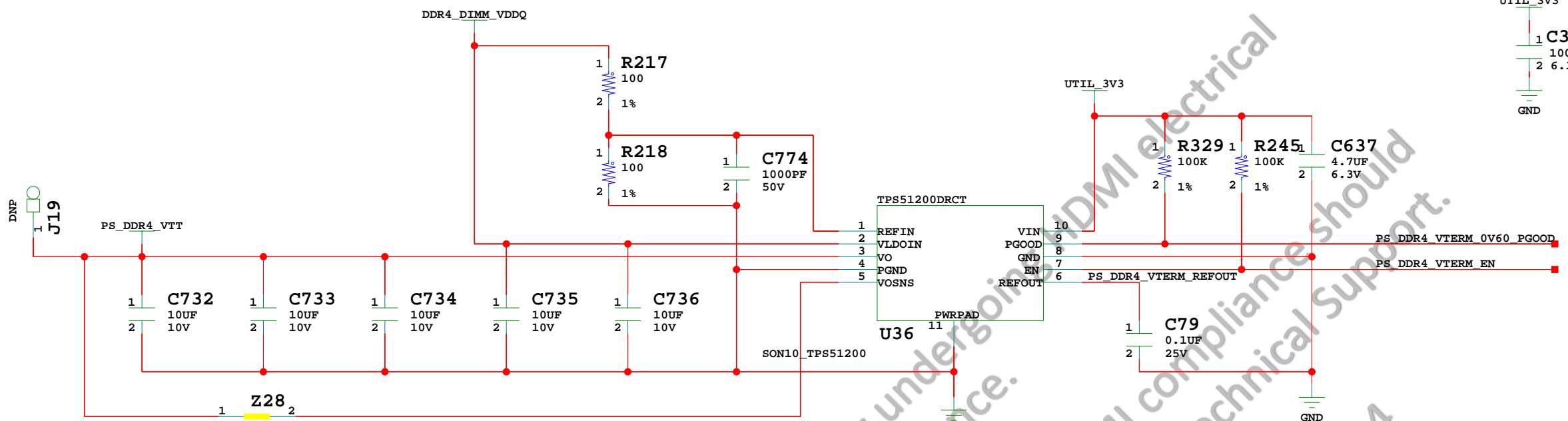
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PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 90 OF 95	DRAWN BY: BF

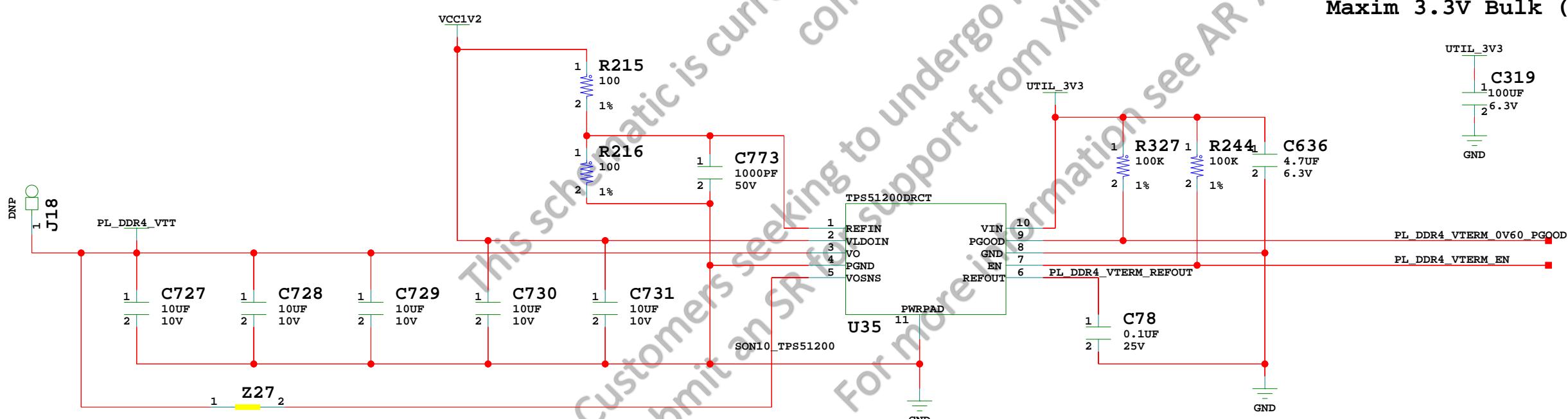




Maxim 3.3V Bulk (near PS VTT)

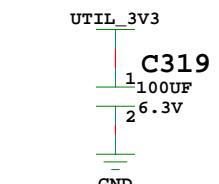


Place sense near DDR4 DIMM



Place sense near DDR4 components

Maxim 3.3V Bulk (near PL VTT)



DDR4 Termination Supply



TITLE: DDR4 Termination Supply
SCHEM, ROHS COMPLIANT
HW-Z1-ZCU106_REV1_0

ASSY P/N: 0432032
PCB P/N: 1280937
SCH P/N: 0381770
TEST P/N: TSS0186

DATE: 01/08/2018:10:16

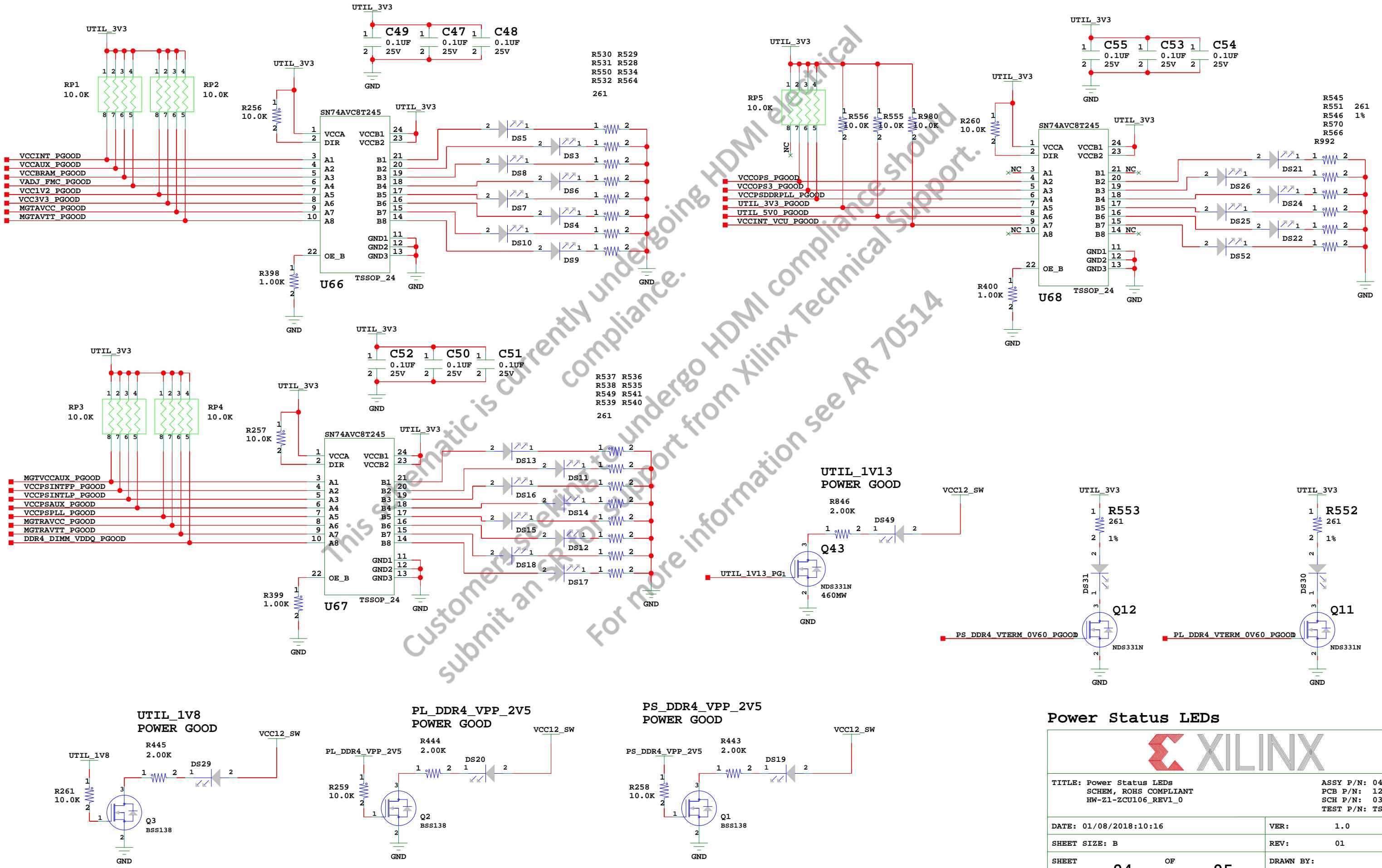
VER: 1.0

SHEET SIZE: B

REV: 01

SHEET 93 OF 95

DRAWN BY:
BF



This schematic diagram illustrates the power management and clock distribution logic for two 74AVC8T245 chips. The diagram is divided into several functional sections:

- Power Supply Section:** At the top left, there are three capacitors (C49, C47, C48) connected to GND and VCCB1/2. Each capacitor has a value of 0.1UF and a rating of 25V.
- Clock Distribution:** The 74AVC8T245 chip (labeled 261) receives its clock signals through pins 23 and 24. These signals pass through driver stages (DS5, DS3, DS8, DS6, DS7, DS4, DS10, DS9) before being distributed to the internal flip-flops (B1-B8).
- Power Good Signals:** The UTIL_3V3 section contains logic to generate power good signals for various power rails. It includes a resistor network (RP5) and a logic gate (Q43) to produce UTIL_3V3_PGOOD, UTIL_5V0_PGOOD, UTIL_VCU_PGOOD, and UTIL_VCCINT_PGOOD. A legend on the right lists these signals:
 - VCCOPS_PGOOD
 - VCCOPS3_PGOOD
 - VCCPSDDRPLL_PGOOD
 - UTIL_3V3_PGOOD
 - UTIL_5V0_PGOOD
 - VCCINT_VCU_PGOOD
- Second 74AVC8T245 Chip:** The second 74AVC8T245 chip (labeled 261) is shown below the first. It also has a power supply section with capacitors C52, C50, and C51, and a similar clock distribution and power good generation logic.
- UTIL_1V13 Power Good:** This section at the bottom right generates UTIL_1V13_PGOOD using a logic gate Q43 and a resistor R846 (2.00K).

The entire schematic is annotated with a large watermark: "Customer schematic is currently undergoing HDMI compliance support and technical support from Xilinx. For more information see AR 70514".

Power Status LEDs



**TITLE: Power Status LEDs
SCHEM, ROHS COMPLIANT
HW-71-ZCH106 REV1.0**

ASSY P/N: 04320
PCB P/N: 12809
SCH P/N: 03817
TEST P/N: TSS01

DATE: 01/08/2018:10:16

1-9

SHEET SIZE: B

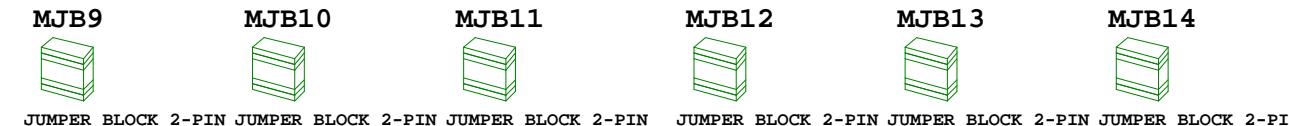
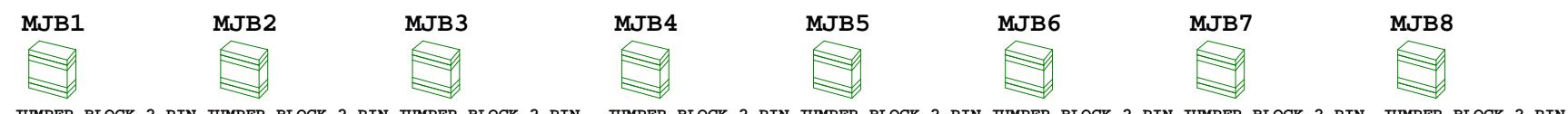
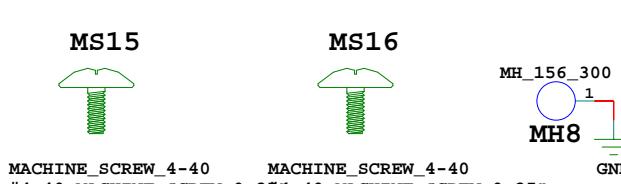
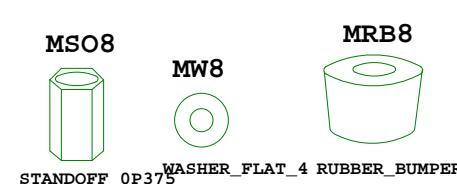
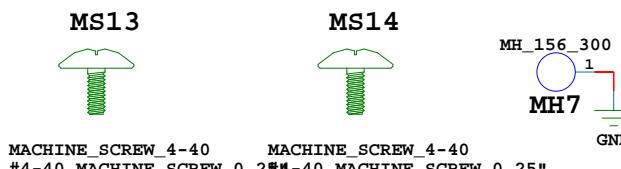
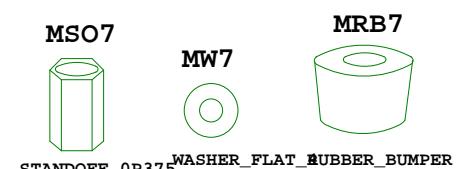
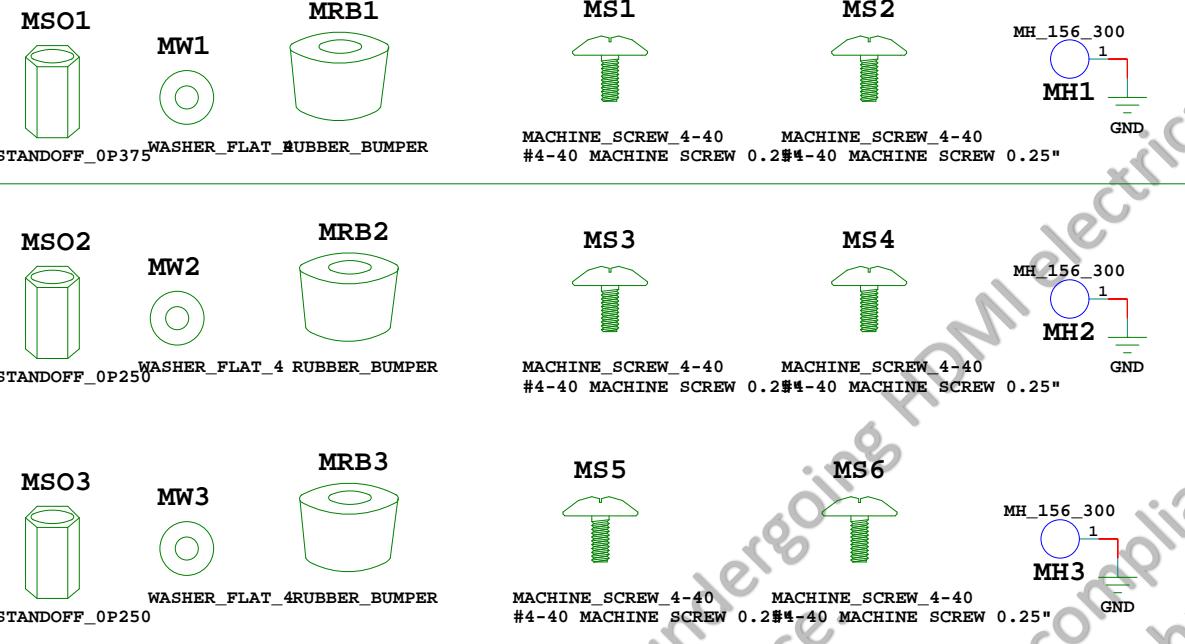
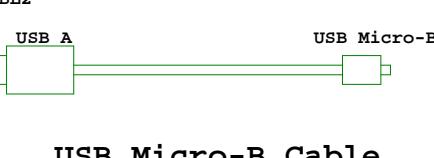
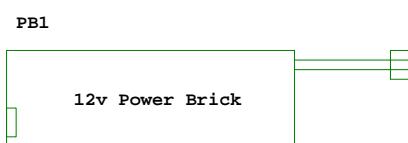
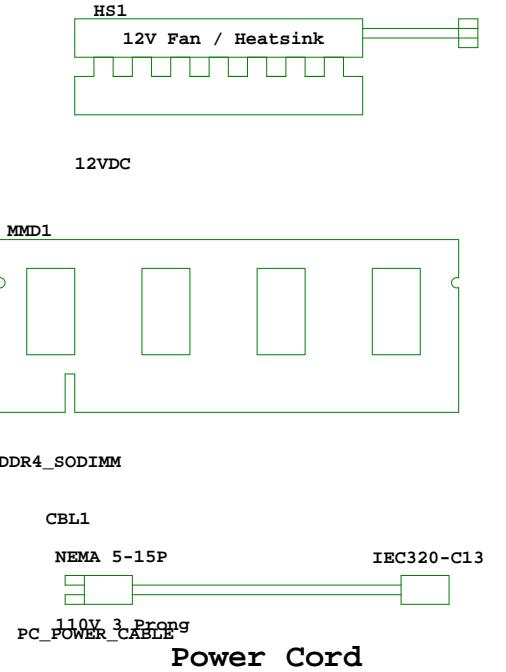
01

SHEET

Page 1

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BF



Mechanical Components

The logo consists of four large, stylized letters: 'S', 'U', 'N', and 'X'. Each letter is constructed from multiple horizontal lines of varying lengths and orientations, creating a geometric and modern appearance.

TITLE: Mechanical Components SCHEM, ROHS COMPLIANT HW-Z1-ZCU106_REV1_0	ASSY P/N: 0432032 PCB P/N: 1280937 SCH P/N: 0381770 TEST P/N: TSS0186
DATE: 01/08/2018:10:16	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 95	OF 95