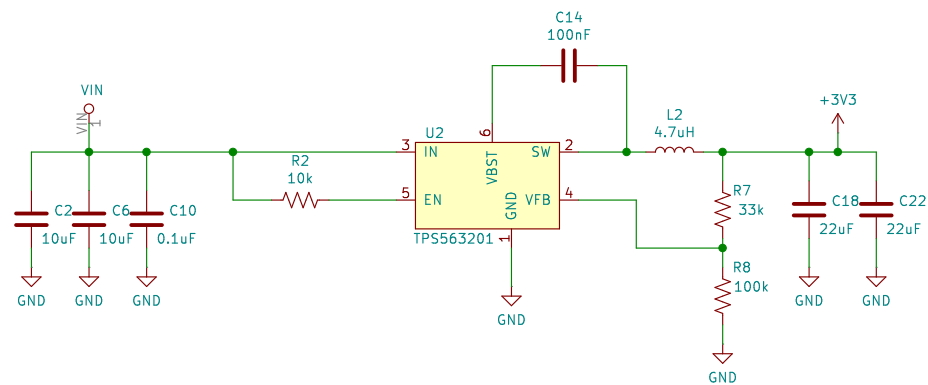
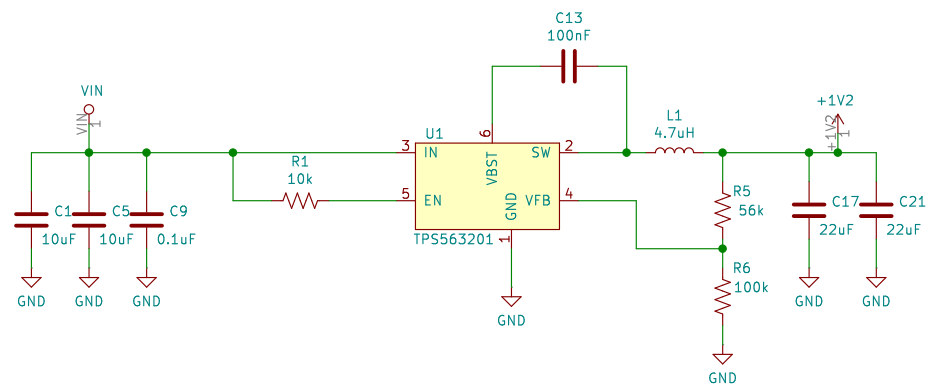
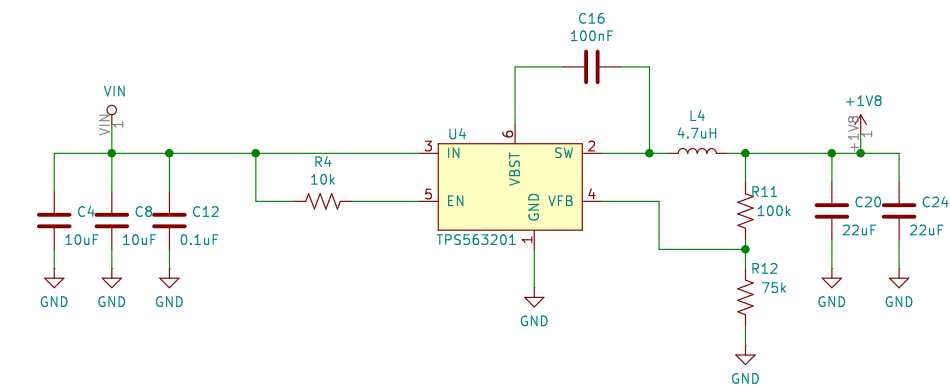
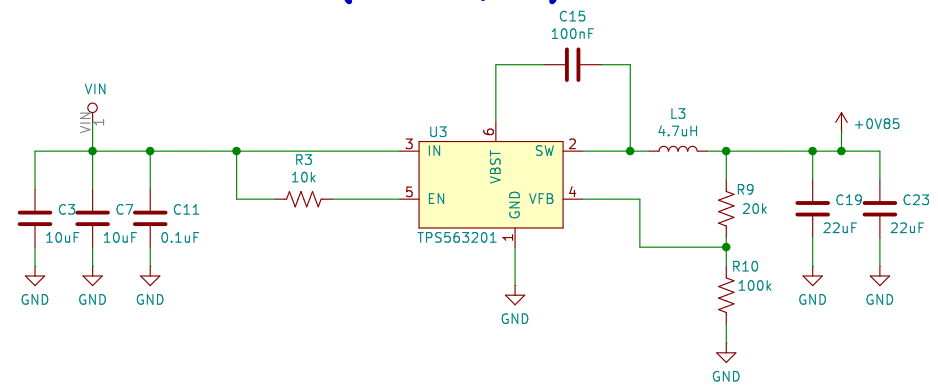


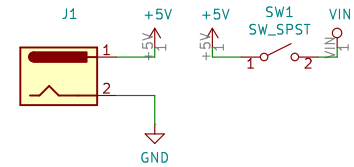
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A								
B								
C								
D								
E			<div>Sheet: alimentaciones</div> <div>File: alimentaciones.sch</div>	<div>Sheet: GND</div> <div>File: GND.sch</div>	<div>Sheet: DDR</div> <div>File: DDR.sch</div>	<div>Sheet: PINOUT</div> <div>File: PINOUT.sch</div>	<div>Sheet: MIO & REFERENCIA</div> <div>File: MIO_REFERENCIA.sch</div>	
F							<div>UAH</div> <div>Sheet: / File: esquematico_Zynq-UltraScale.sch</div> <div>Title: TFG: Guía práctica para el diseño de SoCs: Zynq UltraScale+</div> <div>Size: A3Date: KiCad E.D.A. kicad (5.1.9)–1</div> <div>Rev:Id: 1/6</div>	

TPS563201

$$V_{out} = 0,768 \times (1 + R1/R2)$$



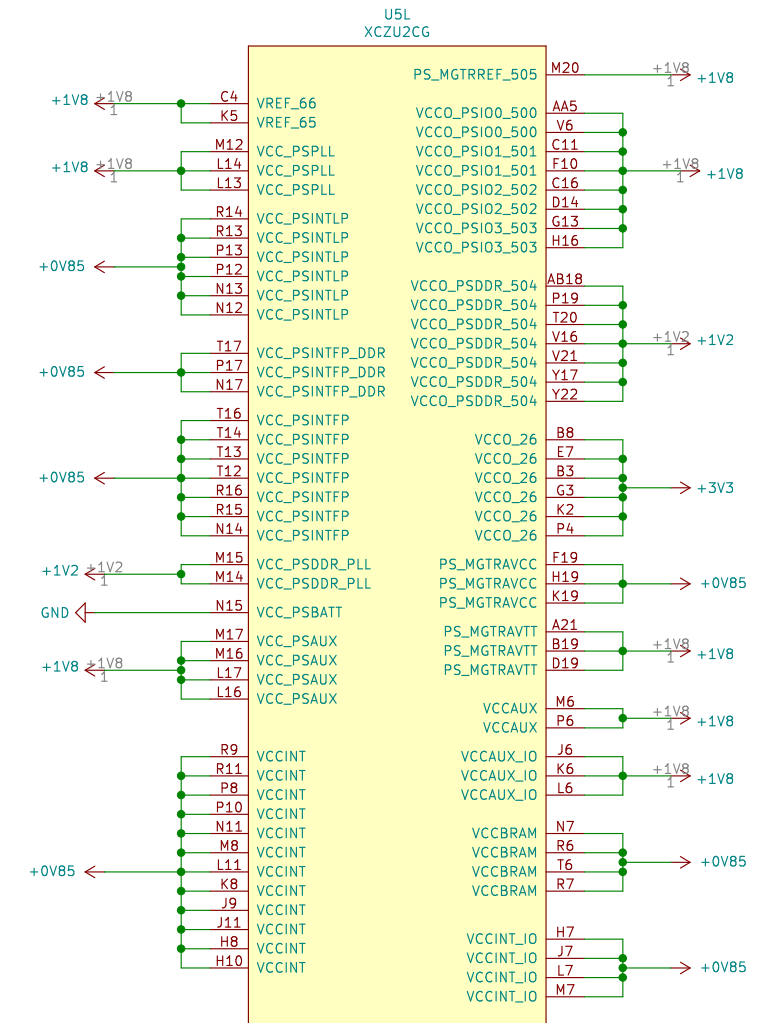
VOLTAGE INPUT



led ON



XCZU2CG



UAH

Sheet: /alimentaciones/
File: alimentaciones.sch

Title: TFG: Guía práctica para el diseño de SoCs: Zynq UltraScale+

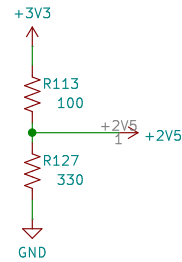
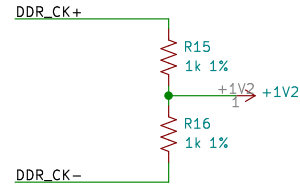
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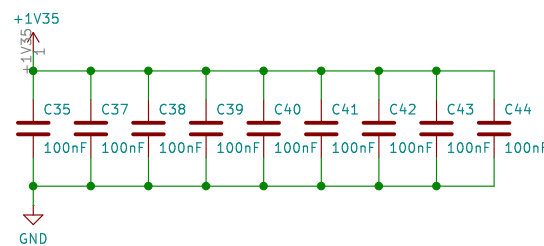
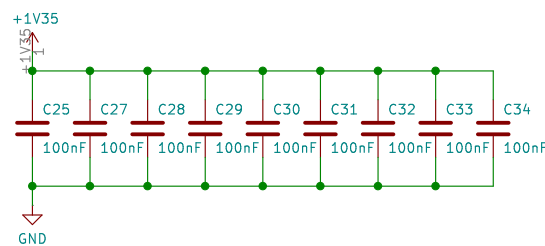
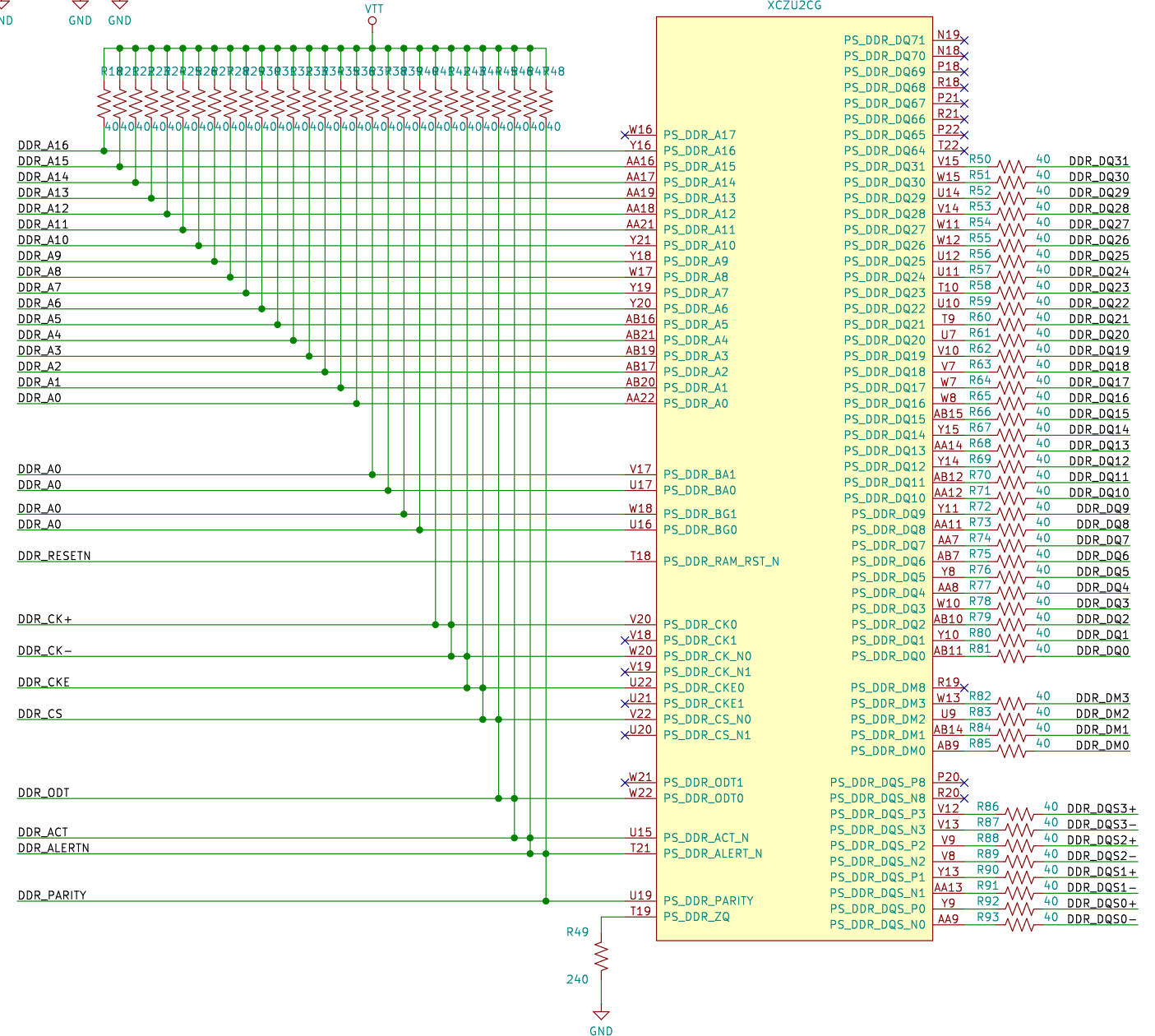
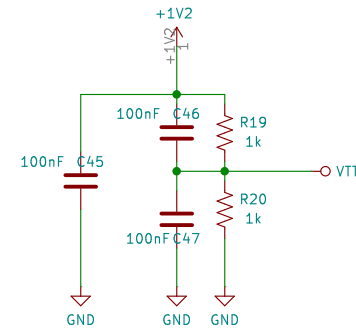
Rev:

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MT40A512M16



XCZU2CG



XCZU2CG

LEDS

BUTTON

SWITCHES

U5C
XCZU2CG

IO_T3U_N12_66

IO_L12N_T1U_N11_GC_66

IO_L12P_T1U_N10_GC_66

IO_L11N_T1U_N9_GC_66

IO_L11P_T1U_N8_GC_66

IO_T0U_N12_VRP_66

U5B
XCZU2CG

IO_L12N_AD0N_26

IO_L12P_AD0P_26

IO_L11N_AD1N_26

IO_L11P_AD1P_26

IO_L10N_AD2N_26

IO_L10P_AD2P_26

IO_L9N_AD3N_26

IO_L9P_AD3P_26

IO_L8N_HDGC_AD4N_26

IO_L8P_HDGC_AD4P_26

IO_L7N_HDGC_AD5N_26

IO_L7P_HDGC_AD5P_26

IO_L6N_HDGC_AD6N_26

IO_L6P_HDGC_AD6P_26

IO_L5N_HDGC_AD7N_26

IO_L5P_HDGC_AD7P_26

IO_L4N_AD8N_26

IO_L4P_AD8P_26

IO_L3N_AD9N_26

IO_L3P_AD9P_26

IO_L2N_AD10N_26

IO_L2P_AD10P_26

IO_L1N_AD11N_26

IO_L1P_AD11P_26

U5D
XCZU2CG

IO_L24N_T3U_N11_PERSTN0_65

IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65

IO_L23N_T3U_N9_65

IO_L23P_T3U_N8_I2C_SCLK_65

IO_L22N_T3U_N7_DBC_AD0N_65

IO_L22P_T3U_N6_DBC_AD0P_65

IO_L21N_T3L_N5_AD8N_65

IO_L21P_T3L_N4_AD8P_65

IO_L20N_T3L_N3_AD1N_65

IO_L20P_T3L_N2_AD1P_65

IO_L19N_T3L_N1_DBC_AD9N_65

IO_L19P_T3L_N0_DBC_AD9P_65

IO_T3U_N12_65

IO_T2U_N12_65

IO_L18N_T2U_N11_AD2N_65

IO_L18P_T2U_N10_AD2P_65

IO_L17N_T2U_N9_AD10N_65

IO_L17P_T2U_N8_AD10P_65

IO_L16N_T2U_N7_QBC_AD3N_65

IO_L16P_T2U_N6_QBC_AD3P_65

IO_L15N_T2L_N5_AD11N_65

IO_L15P_T2L_N4_AD11P_65

IO_L14N_T2L_N3_GC_65

IO_L14P_T2L_N2_GC_65

IO_L13N_T2L_N1_GC_QBC_65

IO_L13P_T2L_N0_GC_QBC_65

IO_L12N_T1U_N11_GC_65

IO_L12P_T1U_N10_GC_65

IO_L11N_T1U_N9_GC_65

IO_L11P_T1U_N8_GC_65

IO_L10N_T1U_N7_QBC_AD4N_65

IO_L10P_T1U_N6_QBC_AD4P_65

IO_L9N_T1L_N5_AD12N_65

IO_L9P_T1L_N4_AD12P_65

IO_L8N_T1L_N3_AD5N_65

IO_L8P_T1L_N2_AD5P_65

IO_L7N_T1L_N1_QBC_AD13N_65

IO_L7P_T1L_N0_QBC_AD13P_65

IO_T1U_N12_65

IO_T0U_N12_VRP_65

IO_L6N_T0U_N11_AD6N_65

IO_L6P_T0U_N10_AD6P_65

IO_L5N_T0U_N9_AD14N_65

IO_L5P_T0U_N8_AD14P_65

IO_L4N_T0U_N7_DBC_AD7N_65

IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65

IO_L3N_T0L_N5_AD15N_65

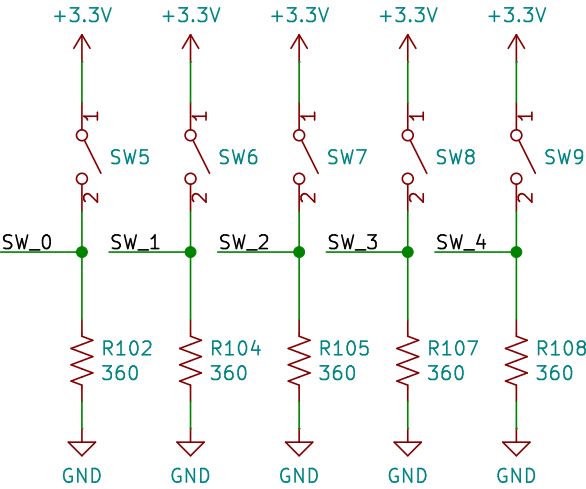
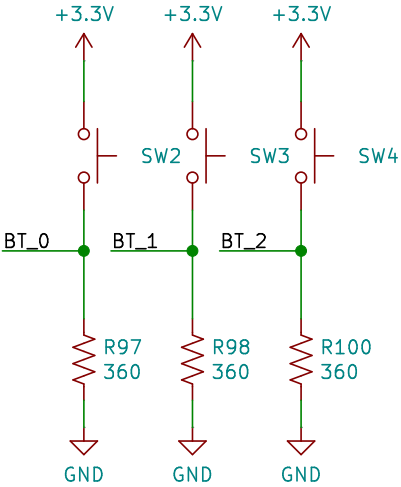
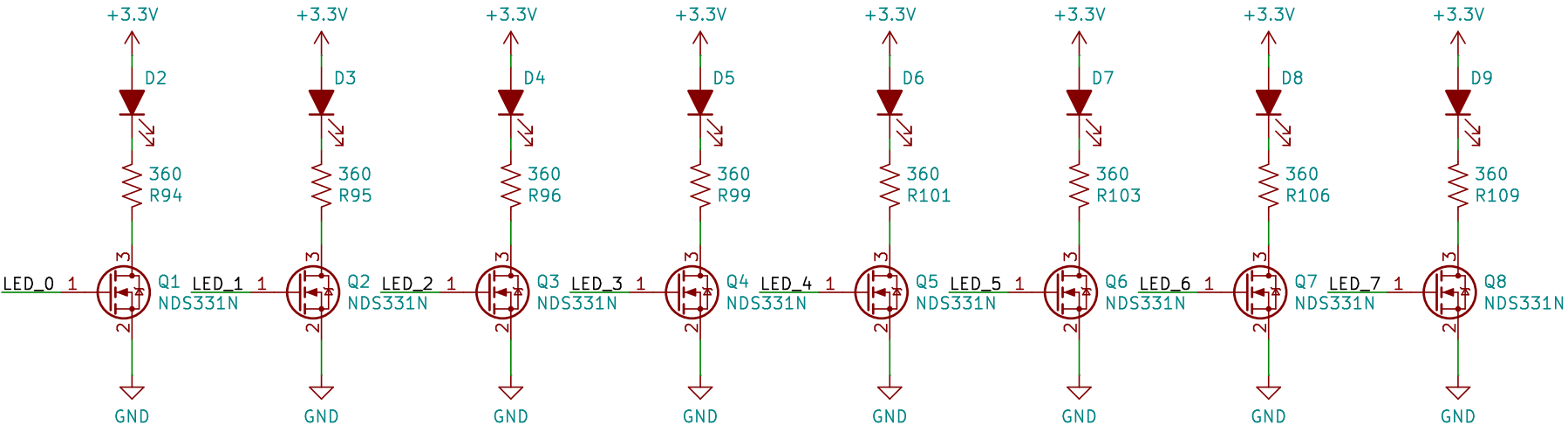
IO_L3P_T0L_N4_AD15P_65

IO_L2N_T0L_N3_65

IO_L2P_T0L_N2_65

IO_L1N_T0L_N1_DBC_65

IO_L1P_T0L_N0_DBC_65



UAH

Sheet: /PINOUT/
File: PINOUT.sch

Title: TFG: Guía práctica para el diseño de SoCs: Zynq UltraScale+

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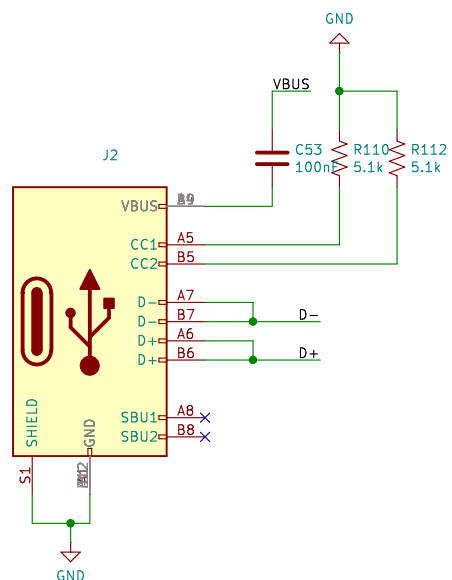
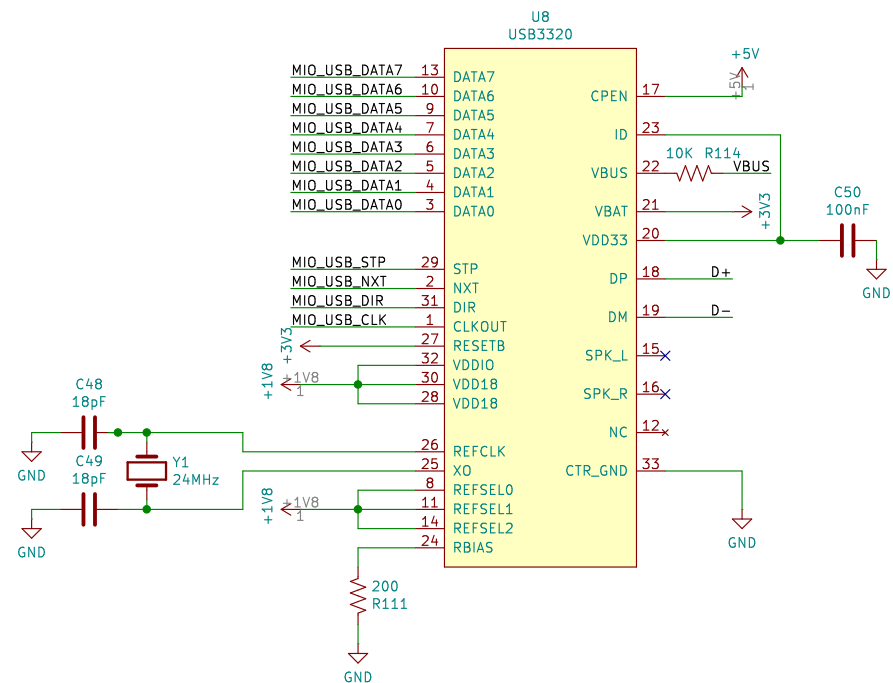
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Rev:

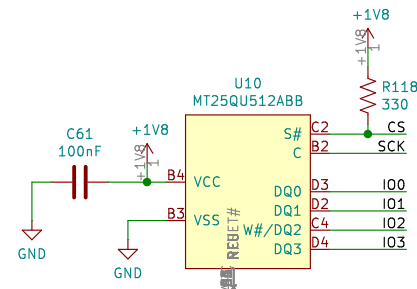
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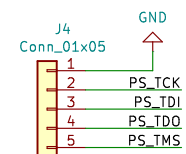
USB TIPO C



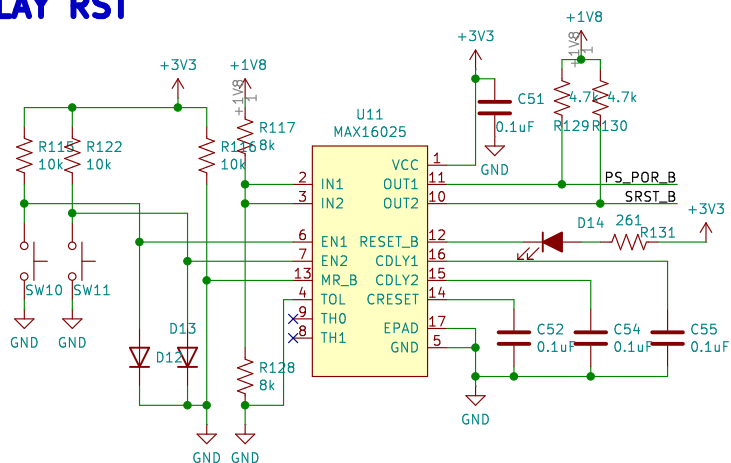
QUAD SPI FLASH



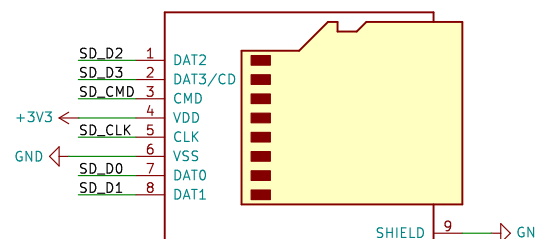
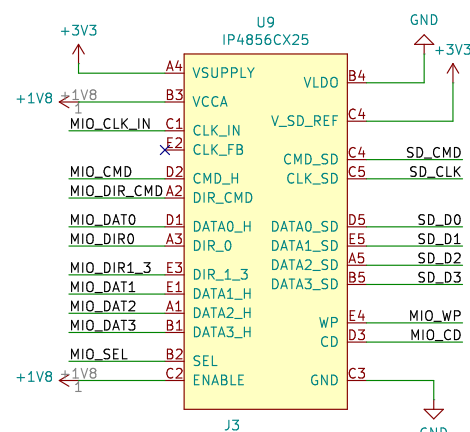
JTAG



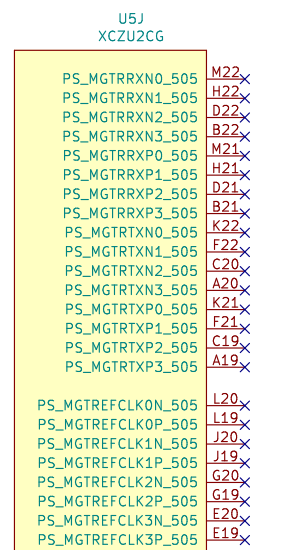
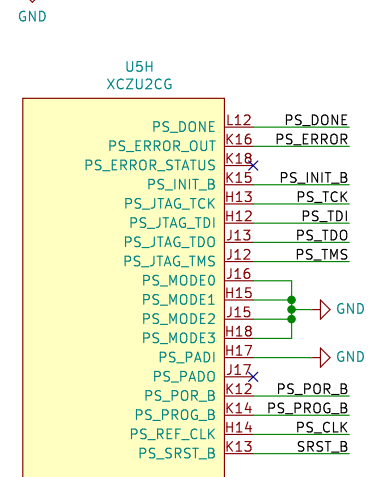
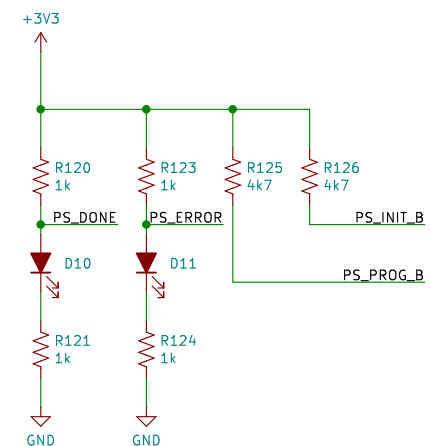
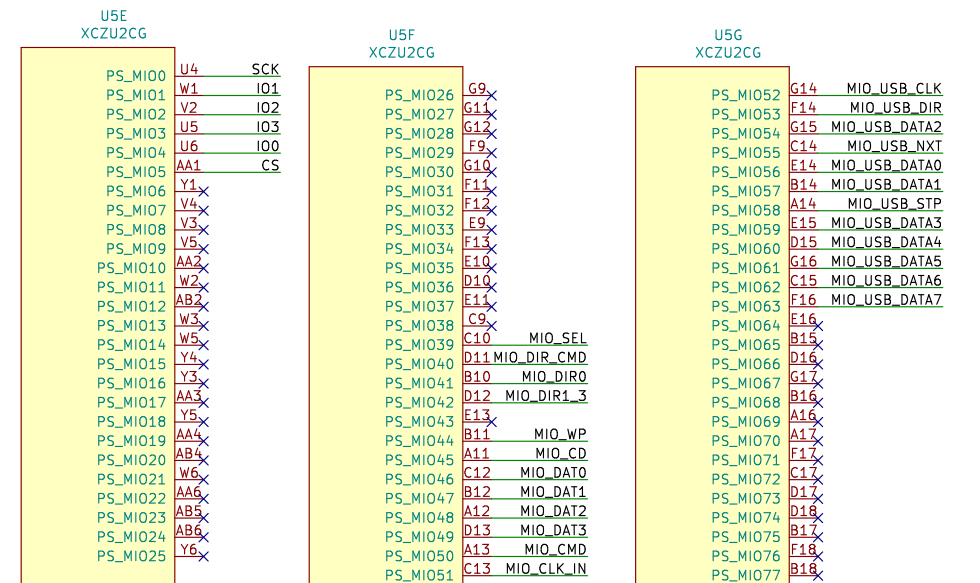
DELAY RST



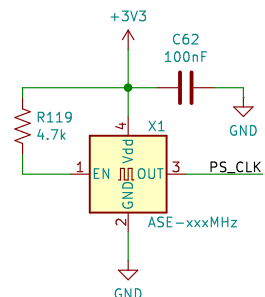
SD



XCZU2CG



OSCILLATOR 33MHz



UAH

Sheet: /MIO & REFERENCIA/
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Title: TFG: Guía práctica para el diseño de SoCs: Zynq UltraScale+

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