Decoder

Generics

- yfg6yugiukj

- U

- N

- T

- Gad

Ports

- clk <type> input <value> std_logic

: alfa

- rst <type> input <value> std_logic

: alfa

- yhmm <type> input <value> std_logic

: alfa

- Rowererererererere <type> input

: dfhdfg

- Col <type> output <value> std_logic_vector <bits> 3 downto 0

: dfhdfg1

- DecodeOut <type> output <value> std_logic_vector <bits> 3 downto 0

<value> std_logic_vector <bits> (N-1) downto (N-2)

: marcafa