Decoder

Generics

- yfg6yugiukj
- U
- N
- T
- Gad

Ports

- clk	<type> input : alfa	<value> std_logic
- rst	<type> input : alfa	<value> std_logic
- yhmm	<type> input : alfa	<value> std_logic
- Rowererrrererererrere	<type> input : dfhdfg	<value> std_logic_vector <bits> (N-1) downto (N-2)
- Col	<type> output : dfhdfg1	<value> std_logic_vector <bits> 3 downto 0
- DecodeOut	<type> output : marcafa	<value> std_logic_vector <bits> 3 downto 0