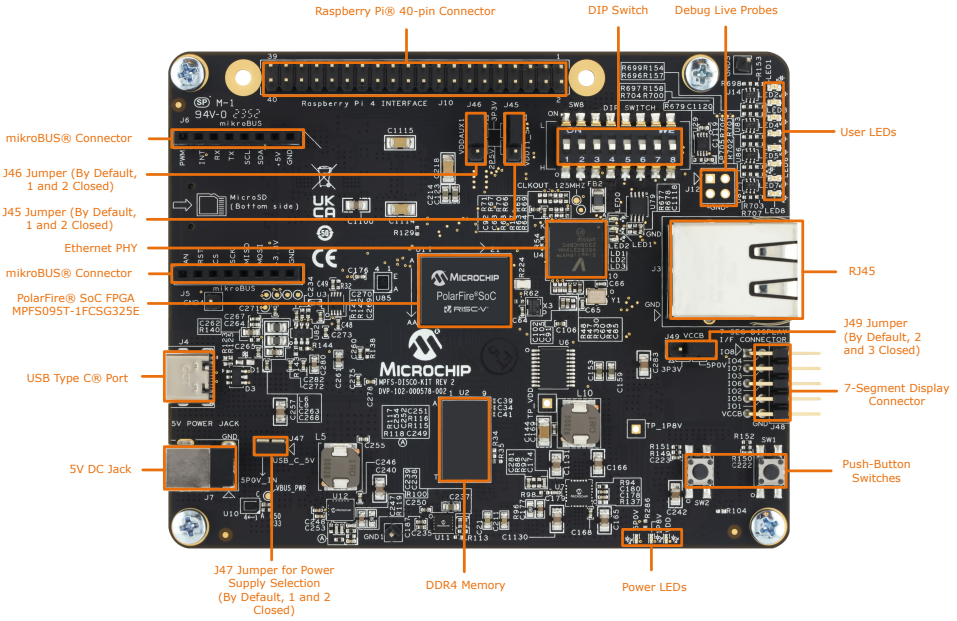
Introduction (Ask a Question)

The PolarFire® SoC Discovery Kit (MPFS-DISCO-KIT) is an RoHS-compliant, cost-optimized kit with general-purpose interfaces that enables you to evaluate features of the MPFS095T-1FCSG325E FPGA device.

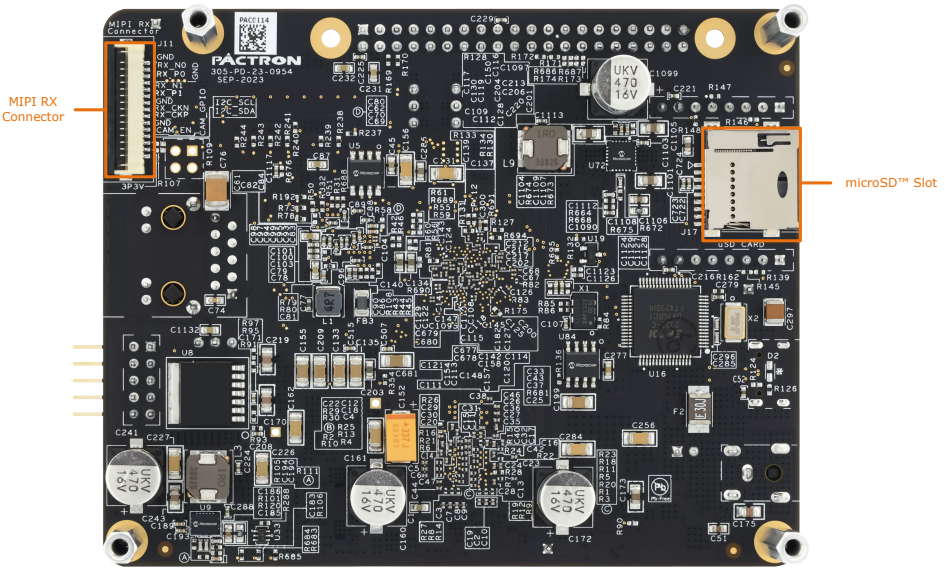
The following image highlights the top view of the PolarFire SoC Discovery Kit.

Figure 1. Board Callout (Top View)



The following image highlights the bottom view of the PolarFire SoC Discovery Kit.

Figure 2. Board Callout (Bottom View)



For more information about the PolarFire SoC Discovery Kit, see the MPFS-DISCO-KIT page.

Table of Contents

1. Getting Started (Ask a Question)

The Discovery Kit supports the following interfaces:

- microSD™ card
- DDR4
- SGMII
- USB-UART
- mikroBUS
- 40-pin Raspberry Pi 4 interface connector

The PolarFire SoC device is programmed using the onboard FlashPro5 programmer. FlashPro5 programmer is also used to debug the FPGA fabric using Identify or SmartDebug and to debug embedded applications using SoftConsole.

1.1 Kit Contents (Ask a Question)

The following table lists the contents of the PolarFire SoC Discovery Kit.

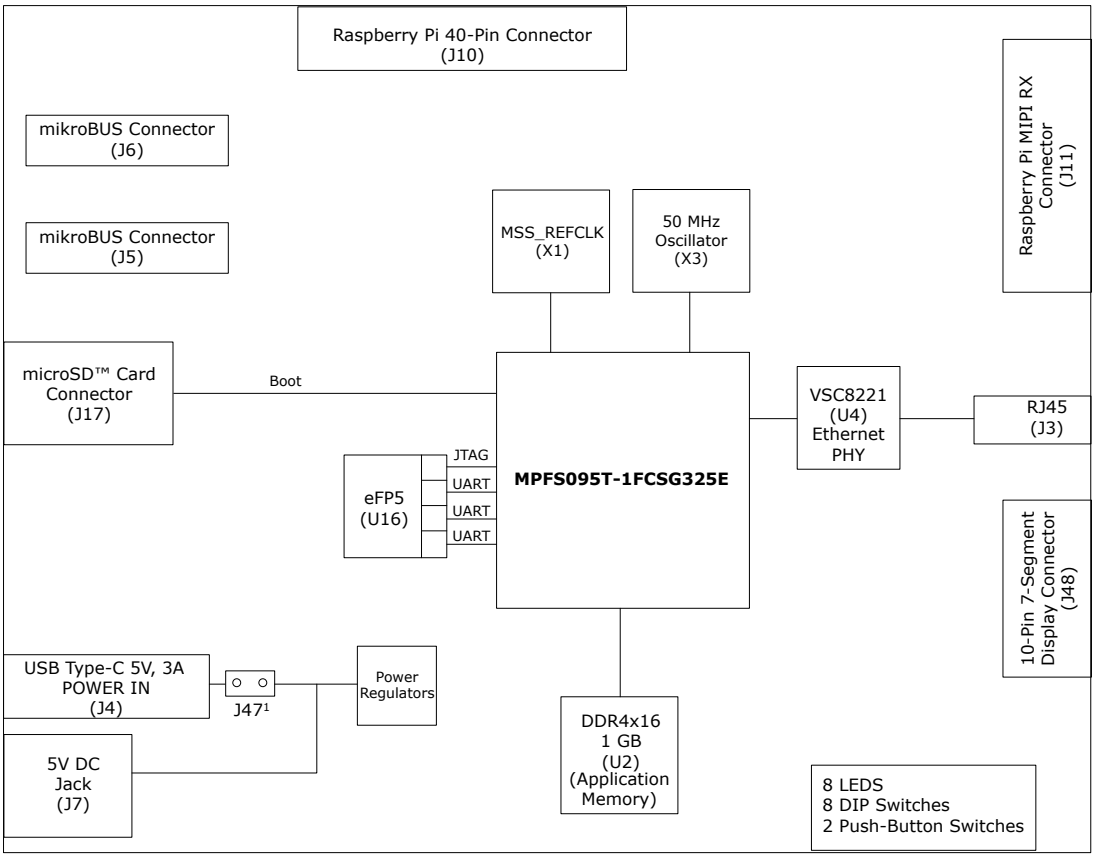
Table 1-1. Kit Contents

Item	Quantity
PolarFire® SoC Discovery Kit Board with MPFS095T-1FCSG325E	1
USB 2.0 Cable C Male to C Male 3.28' (1.00m) Shielded	1
Quickstart card	1

1.2 Block Diagram (Ask a Question)

The following block diagram shows the key components of the PolarFire SoC Discovery Kit.

Figure 1-1. Block Diagram



Note: 1. The PolarFire® SoC Discovery Kit receives power from the Type-C Port (J4) or the 5V DC Jack (J7). The J47 jumper setting determines which power source is used.

1.3 Board Overview (Ask a Question)

The PolarFire SoC Discovery Kit features an MPFS095T-1FCSG325E FPGA device. The kit supports the following capabilities:

- VSC8221 with an RJ45 connector for 10/100/1000 Mbps Ethernet
- DDR4 memory
- microSD card interface
- 40-pin Raspberry Pi 4 interface connector
- mikroBUS expansion port
- 7-Segment display connector

The following table lists the key components of the PolarFire SoC Discovery Kit.

Table 1-2. Board Components

Component	Label on Board	Description
Featured Device		
PolarFire® SoC FPGA MPFS095T-1FCSG325E FPGA	U1	See PolarFire SoC Datasheet.
Power Supply		

.....continued		
Component	**Label on Board**	**Description**
5V/3A power supply (USB Type-C)	J4	The Discovery Kit receives power from the USB Type-C port (J4) or the 5V DC Jack (J7). The J47 jumper setting determines which power source is used. See Jumper Settings.
5V DC Jack	J7	
Clocks		
50 MHz oscillator	X3	50 MHz clock oscillator with single-ended output.
125 MHz Oscillator	X1	125 MHz oscillator (differential LVDS output) which is the input to the MSS Reference clock.
FPGA Programming and Debugging		
Embedded FlashPro5 (eFP5)	U16	On-board FlashPro5 to program and debug the device through USB-to-JTAG channel.
Communication Interfaces		
Gigabit Ethernet	J3	Ethernet (RJ45) jack with built-in magnetics interfacing with VSC8221 in SGMII mode.
USB-UART	U16	FT4232HL is a USB to quad UART bridge controller. This device supports 3 UART interfaces on the board.
Memory Chips		
DDR4	U2	MT40A512M16TB-062E: R is used for DDR4 interface.
microSD™ card	J17	microSD connector
General Purpose I/O		
Debug- push buttons	SW1 to SW2	For debugging.
Dip Switches	SW8	8 dip switches for debugging.
Light Emitting Diodes (LEDs)	LED1 to LED8	Eight active-high LEDs are connected for debugging.
Expansion Interfaces		
mikroBUS	J5, J6	mikroBus connector.
Raspberry Pi 4	J10	Raspberry Pi 4 interface connector.
Raspberry Pi MIPI RX Connector	J11	Facilitates interfacing with the MIPI CSI-2 camera module.
7-Segment Display	J48	A 10-pin interface connector to support a serial 7-Seg 8-Digit Board.

1.4 Handling the Board (Ask a Question)

Handle the board with Electrostatic Discharge (ESD) precautions to avoid damage.

1.5 Operating Temperature (Ask a Question)

To be updated in a future revision.

1.6 Powering Up the Board (Ask a Question)

The PolarFire SoC Discovery Kit receives power from the Type-C Port (J4) or the 5V DC Jack (J7). The J47 jumper setting determines which power source is used, see Jumper Settings. By default, the board receives the power from Type-C port J4 (as the J47 jumper 1 and 2 pins are closed). To use the 5V DC Jack (J7) for powering-up the board, the pins 1 and 2 of the J47 jumper must be open.

To power up the board, connect the Cable C Male to C Male cable from the USB Type-C port (J4) on the Discovery Kit to the Type-C compatible (5V, 3A) port on the Host PC. The power status LEDs 5P0V, VDD, and 1P8V glow indicating that the board is powered-up.

Important: It is recommended to use a laptop or PC USB port to power up the Kit. By limiting the power input to laptop or PC USB ports, we can ensure that the Kit operates optimally without causing any compatibility issues. The power is not tested using different docking station USB ports.

The following table lists the probing points for power rails.

Table 1-3. Voltage Measurement

S. No	Power Rail	Probing Point Label on the Board	Tolerance Allowed	Expected Voltage
1	5P0V_IN	C175	±5%	5V
2	5P0V	C165	±5%	5V
3	3P3V	C123	±5%	3.3V
4	VDD	C144	±3%	1V
5	VDDA	C134	±3%	1V
6	2P5V	C153	±3%	2.5V
7	1P8V	C227	±5%	1.8V
8	1P2V_DDR4	C284	±3%	1.2V
9	0P6V_VREF_DDR4	C250	±3%	0.6V
10	3P3V_FT	C277	±5%	3.3V
11	1P8V_FT	C280	±5%	1.8V

2. Installation and Settings (Ask a Question)

This section provides information about the software and hardware settings required to run the pre-programmed demo design on the Discovery Kit.

2.1 Software Settings (Ask a Question)

Download and install the latest release of Microchip's Libero® SoC and generate your free Silver license at Microchip Portal. The Libero SoC installer includes the required device programmer drivers. See the following references:

1. For more information about the instructions about licensing and installing Libero SoC, see the Libero SoC Documentation.
2. For more information about installing SoftConsole, see the SoftConsole page.
3. For more information about downloading and installing Microchip's DirectCores on the Host PC where Libero SoC is installed, see the IP Core Tools.
4. For more information about downloading and installing Microchip's firmware drivers on the Host PC where Libero SoC is installed, see the Firmware Catalog Documentation.

2.2 Hardware Settings (Ask a Question)

This section provides information about jumper settings, test points, and Power LEDs available on the Discovery Kit.

2.2.1 Jumper Settings (Ask a Question)

Connect the jumpers according to the settings specified in the following table.

Table 2-1. Jumper Settings

Jumper	Description	Pin	Default Setting
J45	Jumper to select Bank 1 and Bank 5 voltages (VDDI1_5)	• Close pins 1 and 2 for 3.3V (For Rpi GPIO and mikroBus operation). • Close pins 2 and 3 for 2.5V (For MIPI RX and Ethernet operation).	1 and 2 closed
J46	Jumper to select the VDDAUX1 Voltage	• Close pins 1 and 2 for 3.3V. • Close pins 2 and 3 for 2.5V.	1 and 2 closed
J47	Jumper to select the power source for the board	• Close pins 1 and 2 to receive power from the USB Type-C port (J4). • Open pins 1 and 2 to receive power from the 5V DC Jack (J7).	1 and 2 closed
J49	Jumper to select the voltage for 7-Segment display	• Close pins 1 and 2 for 3.3V. • Close pins 2 and 3 for 5V.	2 and 3 closed

Important:
If VDDI1_5 is set to 2.5V by closing 2 and 3 pins of J45, VDDAUX1 must also be set to 2.5V by closing 2 and 3 pins of J46.

2.2.2 Power Supply LEDs (Ask a Question)

The following table lists the power supply LEDs available on the Discovery Kit.

Table 2-2. Power Supply LEDs

LED	Description
VDD	1V rail (Core voltage)
1P8V	1.8V rail
5P0V	5V rail

2.2.3 Test Points (Ask a Question)

The following table lists the test points available on the PolarFire SoC Discovery Kit.

Table 2-3. Test Points

Test Point	Description
GND1	Test point for GND
GND4	Test point for GND
GND5	Test point for GND
TP_VDD	Test point for 1V (core voltage rail)
TP_1P8V	Test point for 1.8V

2.2.4 Power Sources (Ask a Question)

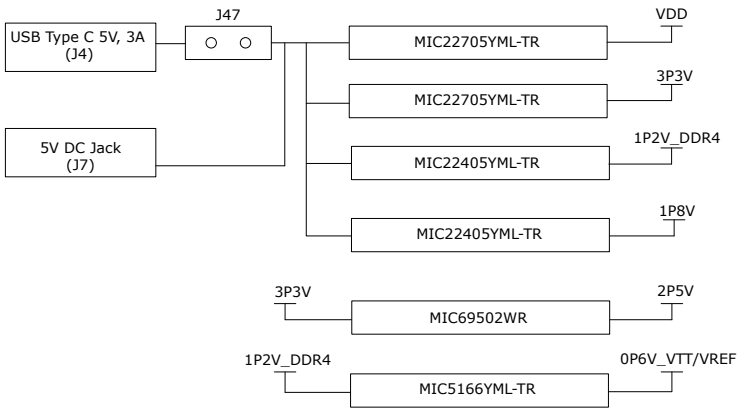
The PolarFire SoC Discovery uses Microchip power supply devices. For more information about these power supply devices, see Microchip's Power Management Devices. The following table lists the key voltage rails required for a normal operation of the PolarFire SoC Discovery kit.

Table 2-4. I/O Voltage Rails

Bank	I/O Rail	Voltage
Bank 0 (HSIO)	1P8V	1.8V
Bank 1 (GPIO)	VDDI1_5	2.5V, 3.3V
Bank 2 (MSS I/O)	3P3V	3.3V
Bank 3 (JTAG)	3P3V	3.3V
Bank 4 (MSS SD)	1P8V	1.8V
Bank 5 (MSS SGMII)	VDDI1_5	2.5V, 3.3V
Bank 6 (MSS DDR)	1P2V_DDR4	1.2V

The following figure shows 5V, 3.3V, 2.5V, 1.8V, 1.2V, and 1.0V (VDD) voltage rails available on the Discovery Kit.

Figure 2-1. Power Supply Topology



The following table lists the power regulators recommended for PolarFire SoC Discovery kit voltage rails.

Table 2-5. Power Regulators

Voltage Rail	Part Number	Description	Current
VDD (1.0V)	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A	7A
1P2V_DDR4	MIC22405YML-TR	IC REG BUCK ADJUSTABLE 3A	4A
1P8V	MIC22405YML-TR	IC REG BUCK ADJUSTABLE 3A	4A
2P5V	MIC69502WR	IC REG LINEAR POS ADJ 5A	5A
3P3V	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A	7A
VTT/VREF	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3A

3. Board Component and Operations (Ask a Question)

This section describes the key components of the PolarFire SoC Discovery kit and provides information about important board operations. For more information, see the PolarFire SoC Datasheet.

3.1 DDR4 Memory Interface (Ask a Question)

The DDR4 memory is connected to MSS BANK 6. The DDR4 memory specification is as follows:

- Part number: MT40A512M16TB-062E: R
- Manufacturer: Micron
- Frequency range: 800 MHz
- Memory size: 1 GB

3.2 microSD Interface (Ask a Question)

The Kit has one microSD card connector and it is interfaced to MSS BANK 4 I/Os. The microSD card connector specification is as follows:

- Part number: MEM2075-00-140-01-A
- Manufacturer: GCT

The microSD interface is connected using a voltage translator between the SD card connector and FPGA silicon.

3.3 Communication Interfaces (Ask a Question)

The Discovery Kit supports the following interfaces for communication:

- Ethernet - SGMII interface: The Kit supports a low-power single-port Ethernet 10/100/1000BASE-T PHY device and the part number of the PHY device is VSC8221. The PHY SGMII signals connected on MSS SGMII Bank 5.
- USB-to-UART interface: The Kit supports a USB-to-quad UART bridge controller device, which supports 3 UART interfaces. The specifications are as follows:
  - Part number: FT4232HL
  - Manufacturer: FTDI
  - UART_B and UART_C interfaces are connected to MSS BANK 2 I/Os.
  - UART_D interface hooked to HSIO BANK 0.

Important: To detect and view the UART COM ports in your **Host PC** > **Device Manager**, install the FT4232H drivers.

3.4 Expansion Capabilities (Ask a Question)

PolarFire SoC Discovery Kit has the following expansion capabilities.

3.4.1 Raspberry Pi 40-Pin Connector (Ask a Question)

The PolarFire SoC Discovery kit has a 40-pin Raspberry connector.

- Raspberry Pi signals are interfaces to GPIO BANK 1 and MSS I/O Bank 2
- SPI, I2C Signals (7) are interfaced to MSS I/O Bank 2
- UART, one pair of I2C, and other GPIO Signals (21) are connected to GPIO Bank 1.
- Part number: 61204021621

- Manufacturer: Wurth Elektronik

3.4.2 mikroBUS Connector (Ask a Question)

The PolarFire SoC Discovery kit has a 16-pin mikroBUS interface connector. It supports interfaces like UART, SPI, and I2C. mikroBUS signals are interfaced to GPIO BANK 1. For more information on available Click Boards, see www.mikroe.com/.

3.4.3 7-Segment Display (Ask a Question)

The PolarFire SoC Discovery kit has a 10-pin interface connector to support a Serial 7-Seg 8-Digit Board. Display signals are connected to HSIO Bank 0.

3.5 Debug Circuitry (Ask a Question)

The Kit is equipped with 2 push button switches, eight dip switches, and eight debug LEDs. Switches and LEDs (1-7) are connected to HSIO BANK 0, and LED 8 is connected to MSS I/O Bank 2. Three LEDs are for power indication and eight LEDs are for debugging purposes.

The following table lists the debug LED to FPGA pin connection.

Table 3-1. Debug LEDs Connections

LED Number	Bank	FPGA Pin
LED1	Bank 0	T18
LED2	Bank 0	V17
LED3	Bank 0	U20
LED4	Bank 0	U21
LED5	Bank 0	AA18
LED6	Bank 0	V16
LED7	Bank 0	U15
LED8	Bank 2	E1

The Kit also has provision for live probes access (J12) and debug Reset. Debug live probes are connected to GPIO Bank and the debug Reset signal is connected to Bank 3.

3.6 Programming Scheme (Ask a Question)

The Discovery kit supports the JTAG programming through an on-board FlashPro5 programmer. For more information about programming the PolarFire SoC device, see Appendix A: Programming the PolarFire SoC FPGA Using the Onboard FlashPro5.

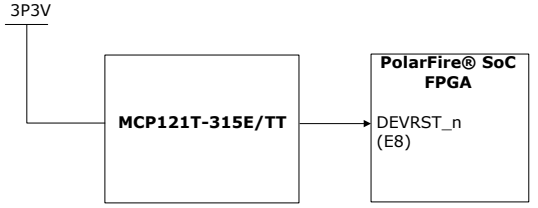
3.7 Form Factor (Ask a Question)

The form factor of the PolarFire SoC Discovery Kit is 4.15 x 3.3 inches approximately.

3.8 System Reset (Ask a Question)

DEVRST_n is an input-only reset pad that allows a full reset of the chip to be asserted. The following figure shows a sample reset circuit that uses a Microchip MCP121T-315E/TT device.

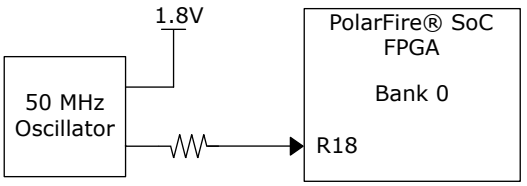
Figure 3-1. Reset Circuit



3.9 50 MHz Oscillator (Ask a Question)

A 50 MHz clock oscillator with an accuracy of ±10 ppm is available on the board. This clock oscillator is connected to the FPGA fabric through the R18 pin to provide a system reference clock as shown in the following figure.

Figure 3-2. 50 MHz Oscillator

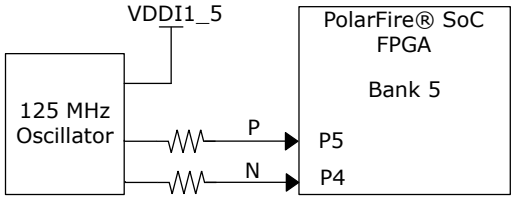


For more information, see the board-level schematics on the PolarFire SoC Discovery Kit Documentation.

3.10 125 MHz Oscillator (Ask a Question)

A 125 MHz clock oscillator with an accuracy of ±10 ppm is available on the board. This clock oscillator is connected to the Bank 5 through P5 and P4 pins to provide a reference clock to the MSS block as shown in the following figure.

Figure 3-3. 125 MHz Oscillator



For more information, see the board-level schematics on the PolarFire SoC Discovery Kit Documentation.

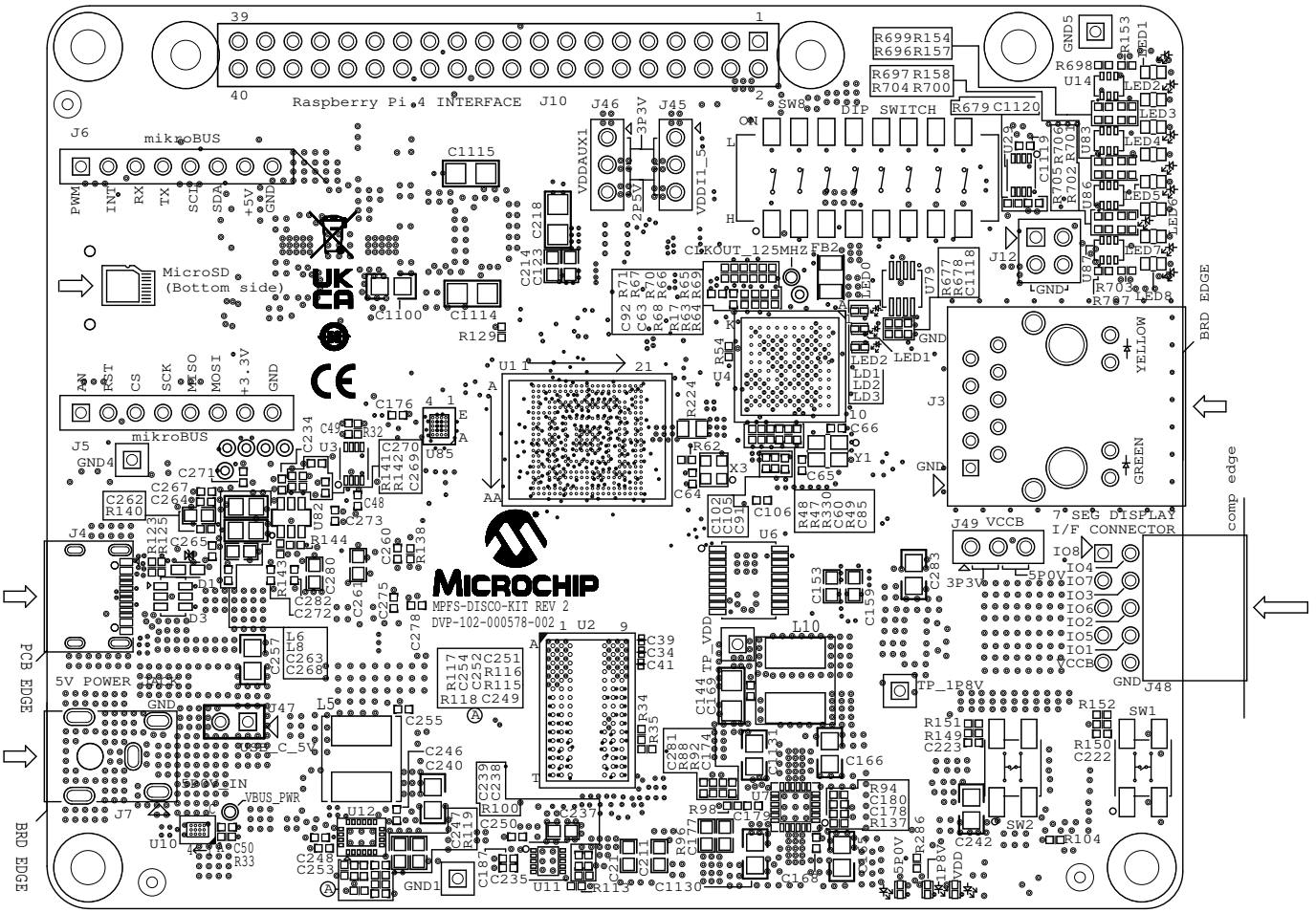
3.11 Pin List (Ask a Question)

For more information about all PolarFire SoC package pins, see Package Pin Assignment Tables (PPATs).

4. Board Components Placement (Ask a Question)

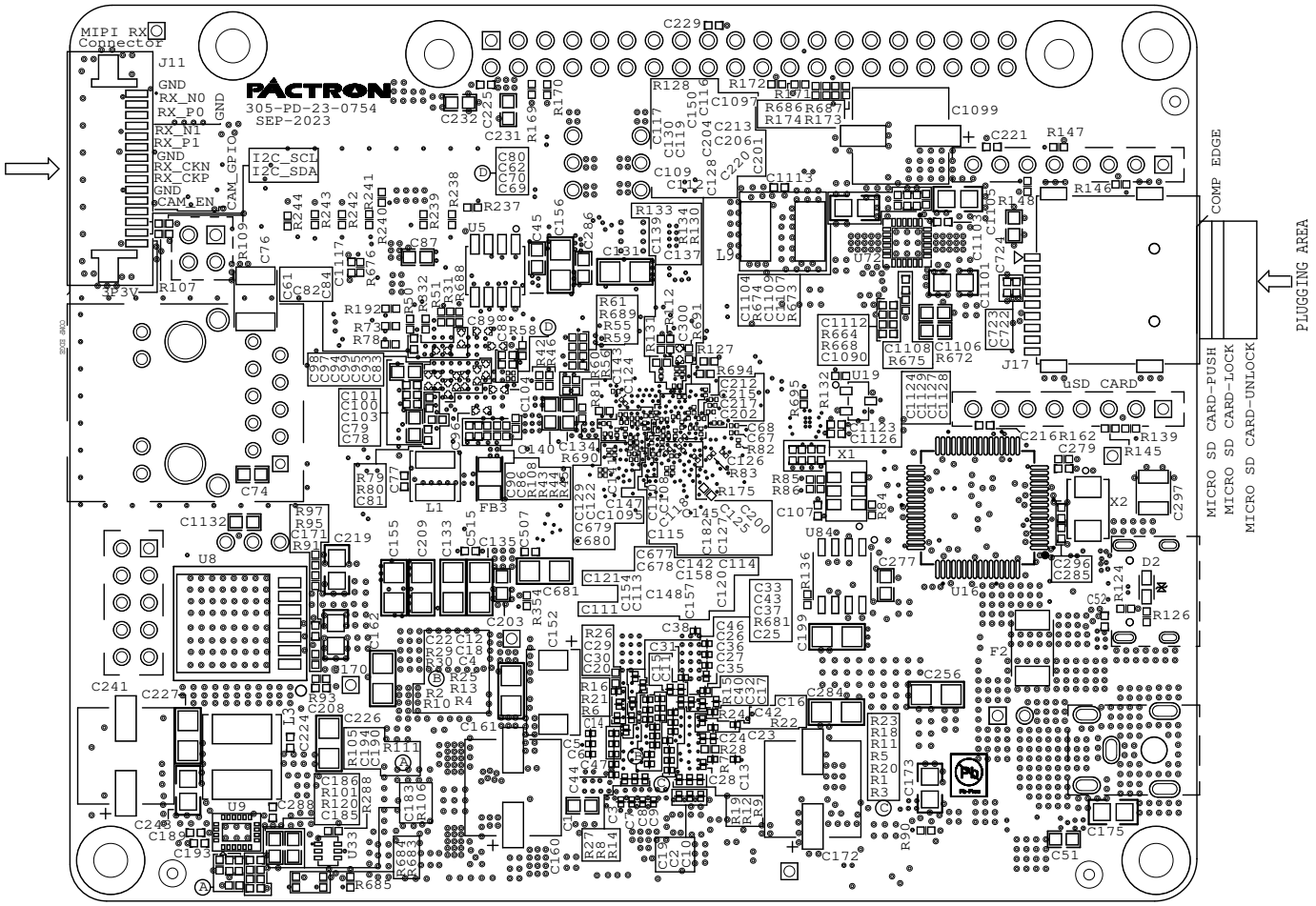
The following silkscreen shows the top view of the placement of various components on the board.

Figure 4-1. Silkscreen (Top View)



The following silkscreen shows the bottom view of the placement of various components on the board.

Figure 4-2. Silkscreen (Bottom View)



5. Demo Design (Ask a Question)

The PolarFire SoC Discovery Kit is pre-loaded with a Finite Impulse Response (FIR) Filter demo design. For information about the demo design and running it, see AN5165: PolarFire SoC DSP FIR Filter Demo.

6. Appendix A: Programming the PolarFire SoC FPGA Using the Onboard FlashPro5 (Ask a Question)

The PolarFire SoC Discovery Kit includes an onboard FlashPro5 programmer. Therefore, external programming hardware is not required to program the PolarFire SoC device. The device is programmed with a programming job file using the FlashPro Express software installed on the host PC. As a prerequisite, ensure to download the latest version of FlashPro Express on the host PC.

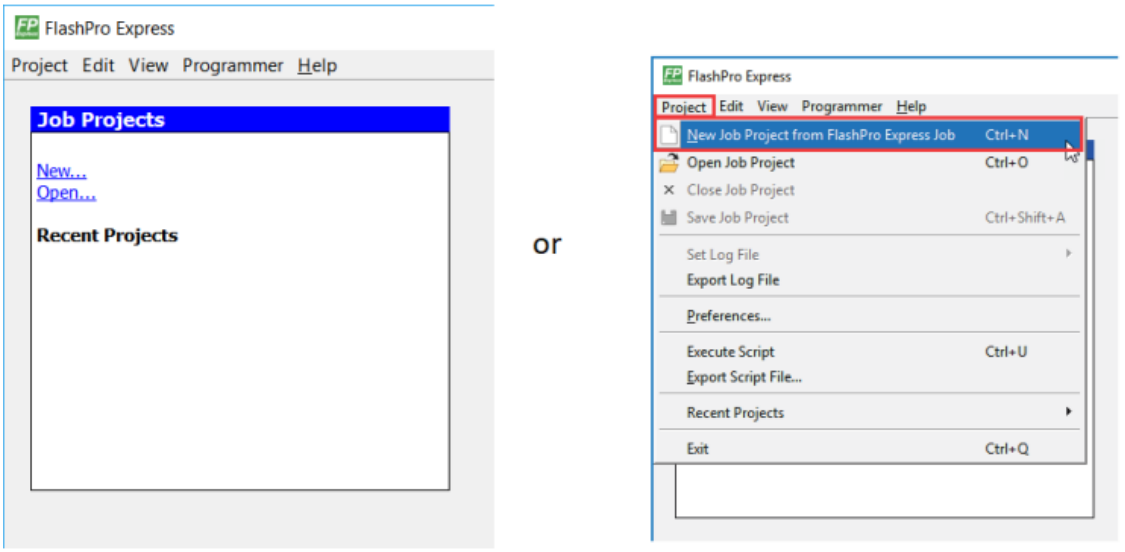
To program the PolarFire SoC device, perform the following steps:

1. Connect the USB Type-C cable from the host PC to the J4 connector on the board.
2. Ensure that the desired power source is selected for the board using the J47 jumper setting.
3. When the board is successfully powered up, the power status LEDs glow.

Follow these steps to program the PolarFire SoC device:

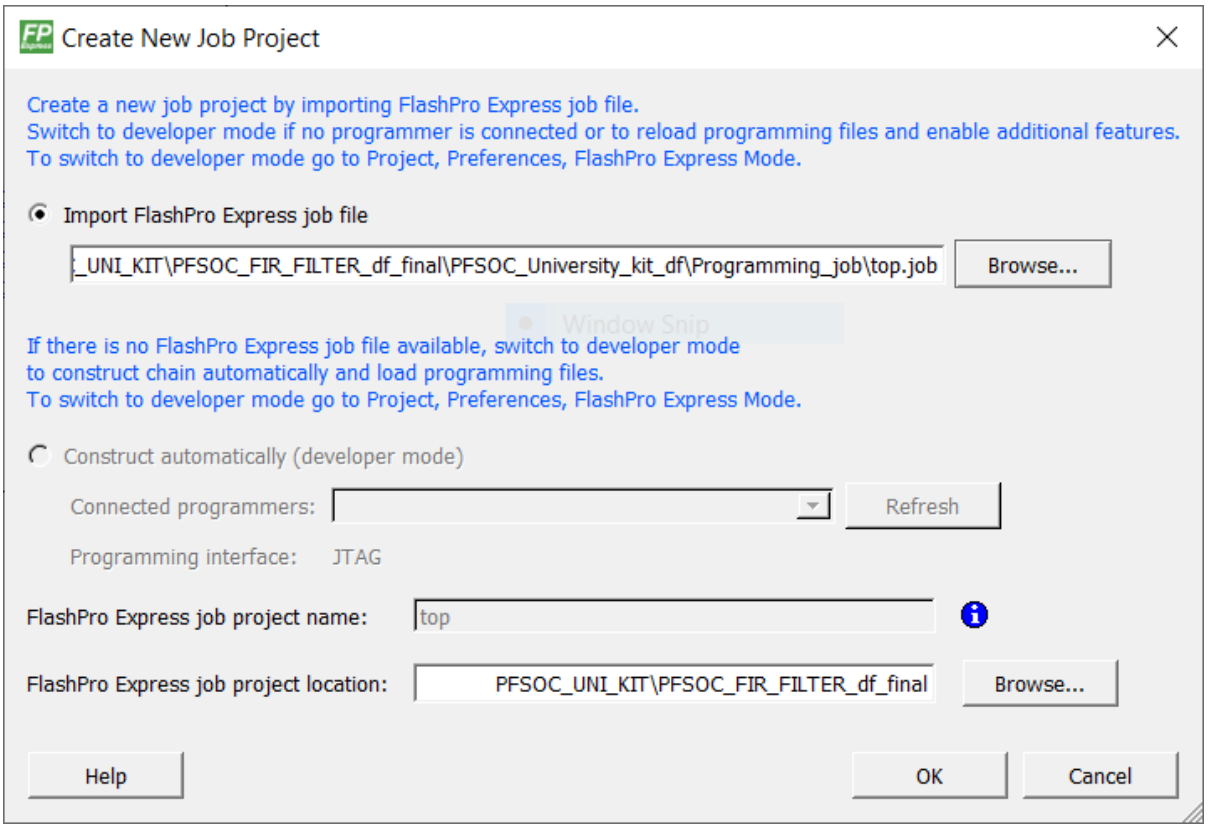
1. On the host PC, launch FlashPro Express.
2. Click **New** or select **Project** > **New Job Project from FlashPro Express Job** to create a new job project as shown in the following figure.

Figure 6-1. New Job Project Creation



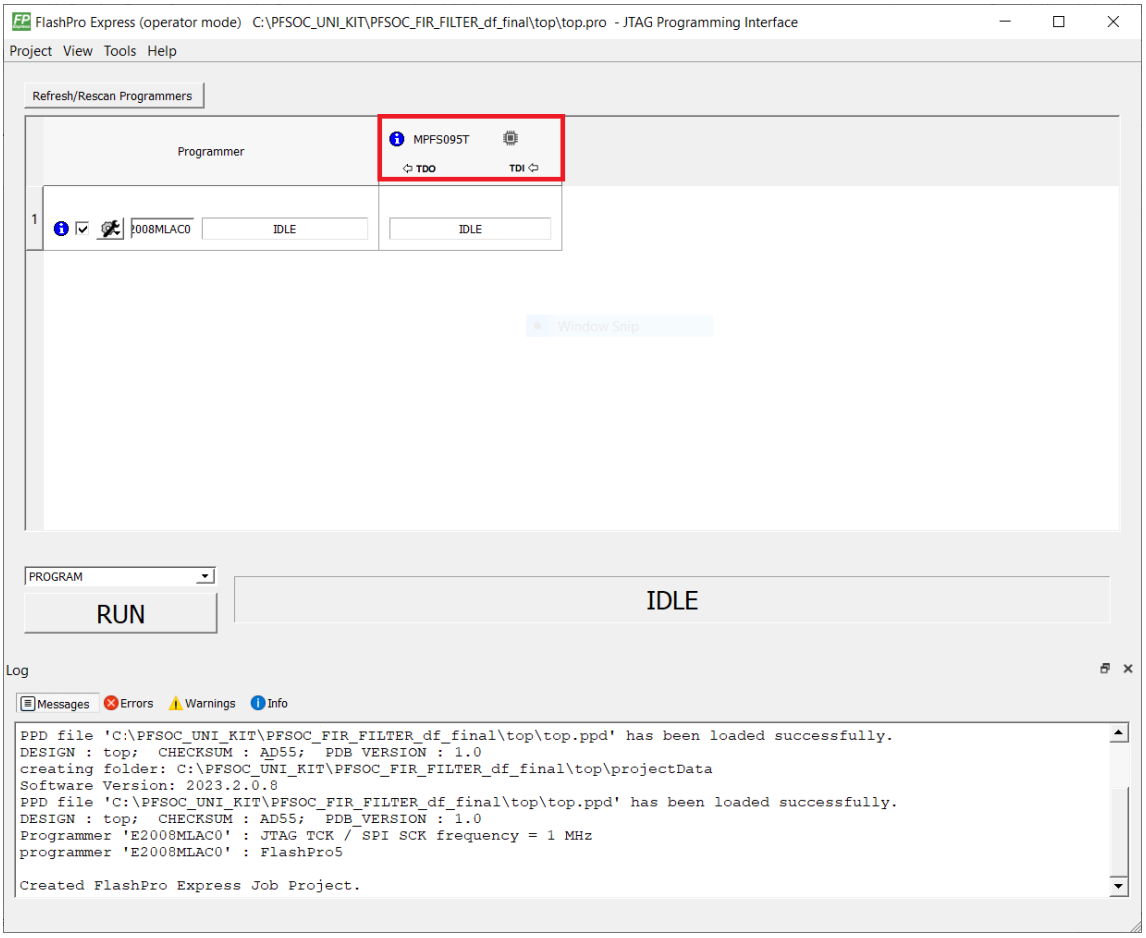
3. **Create New Job Project** dialog box appears, enter the following:
   - In **Import FlashPro Express job file**:
     i. Click **Browse**.
     ii. Select the `.job` file
   - In **FlashPro Express job project location**:
     i. Click **Browse**.
     ii. Select the location to save the project.

Figure 6-2. Selecting the Programming Job File



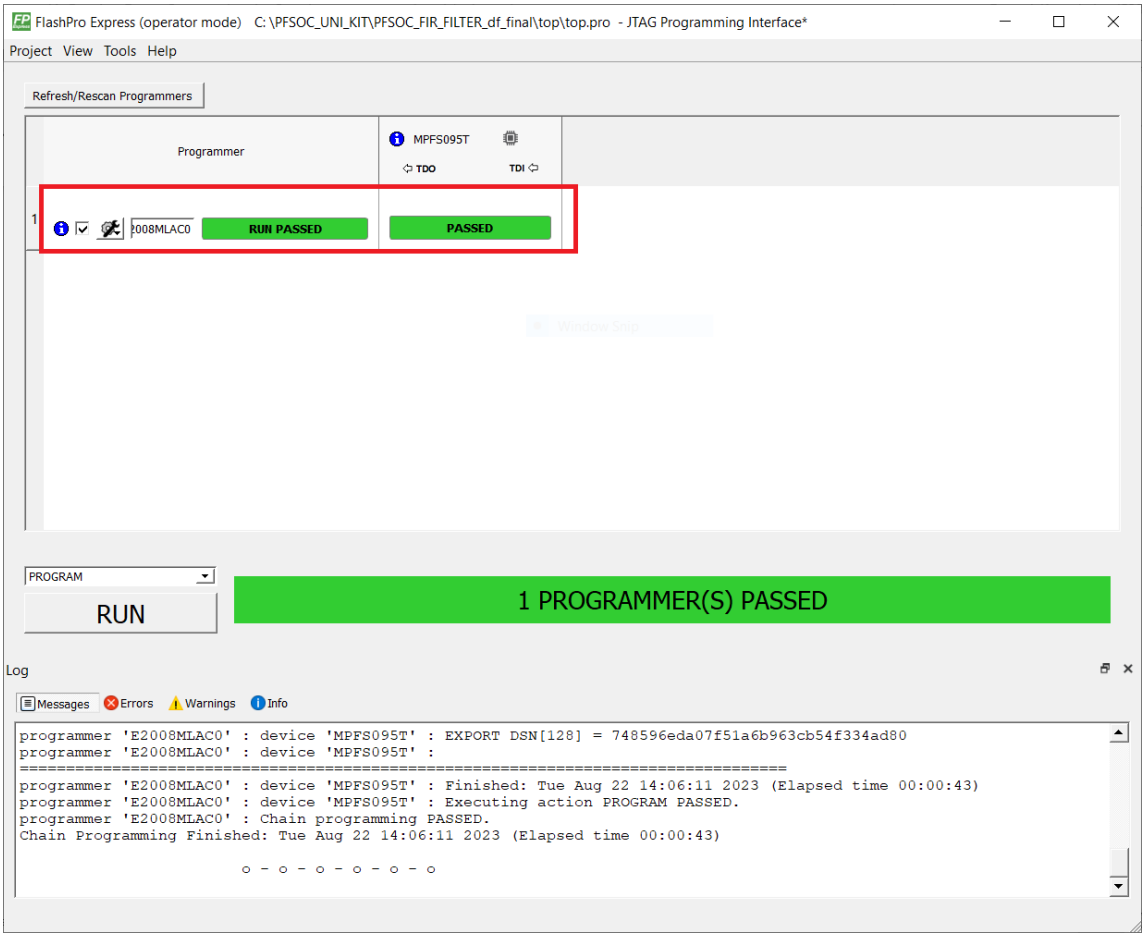
4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
5. Verify that a programmer number appears in the **Programmer** box. If it does not show, verify the board connections, and click **Refresh/Rescan Programmers**.

Figure 6-3. Refresh/Rescan Programmers



6. Click **RUN** to program the device. When the device is programmed successfully, a `RUN PASSED` status is displayed as shown in the following figure.

Figure 6-4. RUN PASSED



This concludes programming the PolarFire SoC device.

7. Appendix B: User Hardware Pinout (Ask a Question)

The following table lists the Raspberry Pi Connector Pinout (J10) pinout.

Table 7-1. Raspberry Pi Connector Pinout (J10)

Left		Right	
FPGA	Raspberry Pi Pin		FPGA
3.3 V	1	2	5 V
E18	3	4	5 V
F18	5	6	GND
E12	7	8	A20
GND	9	10	B21
G18	11	12	E10
F21	13	14	GND
F20	15	16	E21
3.3 V	17	18	F19
A4	19	20	GND
B4	21	22	A19
D6	23	24	D5
GND	25	26	B2
D1	27	28	C2
D17	29	30	GND
D18	31	32	B20
A15	33	34	GND
B19	35	36	B15
B17	37	38	B14
GND	39	40	E13

The following table lists the Debug Switch (SW8) pinout.

Table 7-2. Debug Switch (SW8) Pinout

SW8 Pin	FPGA
1	U17
2	Y16
3	R17
4	AA15
5	AA20
6	Y20
7	V21
8	AA19

The following table lists the Debug LED pinout.

Table 7-3. Debug LED Pinout

LED	FPGA
1	T18
2	V17
3	U20
4	U21

.....continued	
LED	**FPGA**
5	AA18
6	V16
7	U15
8	E1

The following table lists the mikroBUS socket pinout.

Table 7-4. mikroBUS Socket

Left (J5 Pinout)		Right (J6 Pinout)	
Pin	**FPGA**	**Pin**	**FPGA**
1	G12	1	D13
2	B16	2	G17
3	C16	3	E14
4	E17	4	E15
5	A18	5	D11
6	E11	6	D12
7	3.3 V	7	5V
8	GND	8	GND

The following table lists the MIPI RX Connector (J11) pinout.

Table 7-5. MIPI RX Connector (J11)

Pin	FPGA
1	GND
2	B11
3	C11
4	GND
5	A10
6	B10
7	GND
8	B12
9	A12
10	GND
11	Y14
12	Y17
13	T21
14	T20
15	3.3 V

The following table lists the microSD Connector (J17) pinout.

Table 7-6. microSD Connector (J17)

Pin	FPGA
1	M5
2	L5
3	M4
4	3.3V
5	L2

.....continued	
Pin	**FPGA**
6	GND
7	L3
8	K1
9	K2

The following table lists the 7 Segment Display (J48) pinout.

Table 7-7. 7 Segment Display (J48)

Left		Right	
FPGA	**Pin**	**Pin**	**FPGA**
T17	2	1	Y15
Y19	4	3	V15
W20	6	5	AA17
V18	8	7	W16
GND	10	9	VCCB

8. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
C	11/2024	The following changes are made in this revision. • Added Appendix B: User Hardware Pinout.
B	04/2024	The following is a summary of the changes made in this revision: • Updated Figure 1 and Figure 2. • Replaced “2-Position Terminal Block” with “5V DC Jack” throughout the document. • Added Table 3-1. • Added 125 MHz Oscillator. • Updated Figure 3-1 to include the FPGA pin name. • Updated Figure 4-1 and Figure 4-2.
A	12/2023	Initial Revision

Microchip FPGA Support

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