How to use Libero’s graphical logic gate designer

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Blog post: https://soceame.wordpress.com/2025/03/11/how-to-use-liberos-graphical-logic-gate-designer/

Blog: https://soceame.wordpress.com/

GitHub: https://github.com/DRubioG

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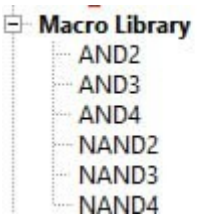
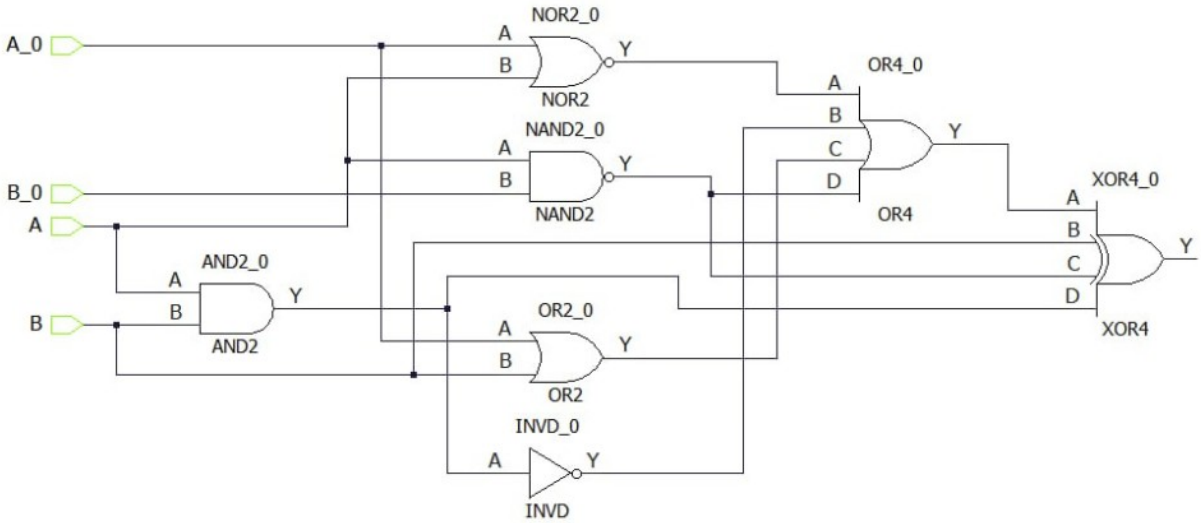
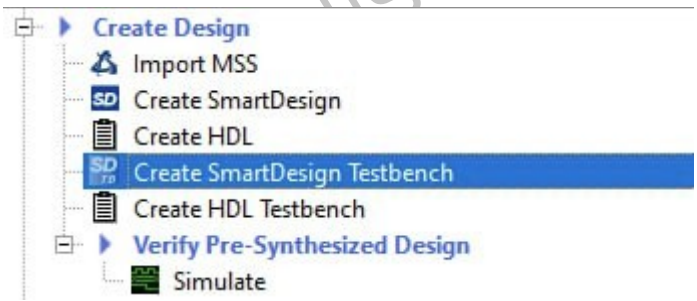
To design a model using logic gates in Libero, you first have to create a SmartDesign, and then go to the *Catalog* to the *Macro Library*, where you will find all the logic gate models that Libero includes.



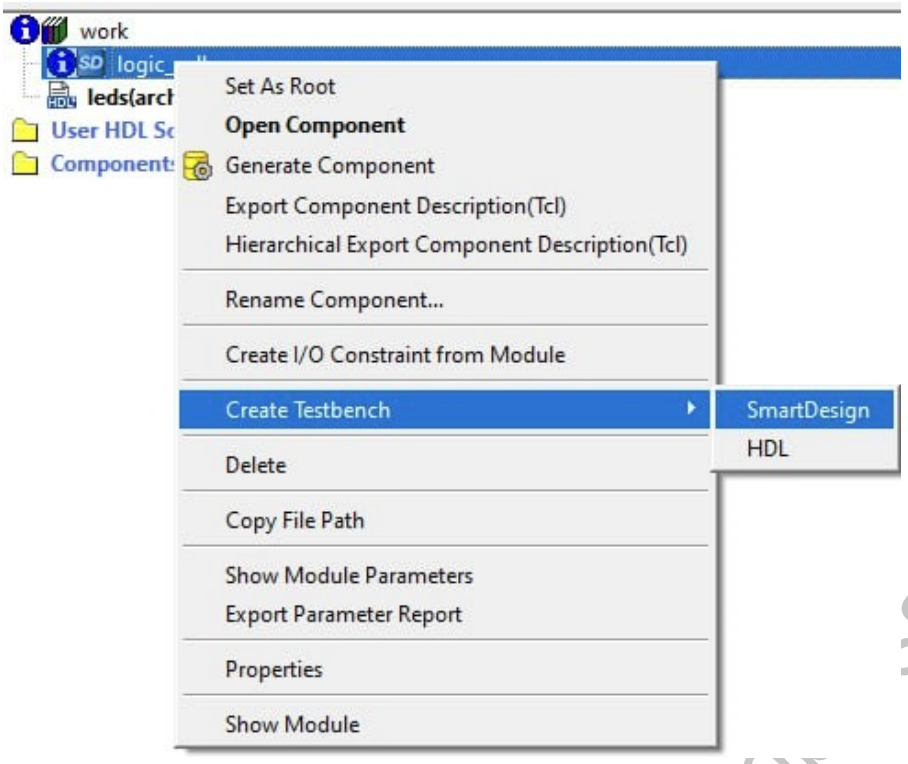
With these models, all you have to do is model the logic gate design you want.



Now, all you have to do is create a Testbench for the SmartDesign.

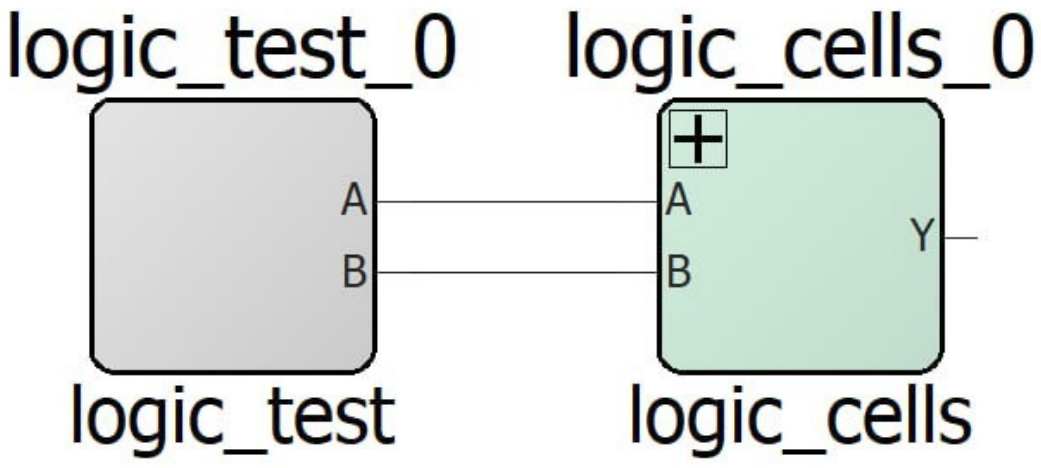


You can also do this by right-clicking.



NOTE: to create a testbench, you have to mark the file you want to create the testbench for as Root.

This model behaves the same as a normal SmartDesign, so you would only need to attach a simulation FW module for the inputs *(you can also force the values in the simulator, to do this, right-click on the signal whose value you want to change, click on the Force option and select the value and the time that the change you have made should last)*.



Now, you only have to simulate the model, you can use this entry as a reference.

https://soceame.wordpress.com/2025/03/11/simulation-in-modelsim-libero/