Pinout del Polarfire SoC Discovery Kit de Microchip

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Entrada: https://soceame.wordpress.com/2024/11/22/pinout-del-polarfire-soc-discovery-kit-de-microchip/

Blog: https://soceame.wordpress.com/

GitHub: https://github.com/DRubioG

Fecha última modificación: 23/02/2025

Este es el pinout del Polarfire SoC Discovery Kit.

También tienes un documento y el pinout (PDC) en mi GitHub:
https://github.com/DRubioG/PolarFire_SoC_FPGA_Discovery_Kit_Pinout

FPGA Pinout

Pin Name	Pin Number	Direction	Voltage	FPGA bank
CLK_50MHz	R18	In	1.8V	0
LED1(LOW LEVEL ACTIVE)	T18	Out	1.8V	0
LED2(LOW LEVEL ACTIVE)	V17	Out	1.8V	0
LED3(LOW LEVEL ACTIVE)	U20	Out	1.8V	0
LED4(LOW LEVEL ACTIVE)	U21	Out	1.8V	0
LED5(LOW LEVEL ACTIVE)	AA18	Out	1.8V	0
LED6(LOW LEVEL ACTIVE)	V16	Out	1.8V	0
LED7(LOW LEVEL ACTIVE)**	U15	Out	1.8V	0
SWITCH1 (LOW LEVEL ACTIVE)	T19	In	1.8V	0
SWITCH2 (LOW LEVEL ACTIVE)	U18	In	1.8V	0
DIP1 (LOW LEVEL ACTIVE)	U17	In	1.8V	0
DIP2 (LOW LEVEL ACTIVE)	Y16	In	1.8V	0
DIP3 (LOW LEVEL ACTIVE)	R17	In	1.8V	0
DIP4 (LOW LEVEL ACTIVE)	AA15	In	1.8V	0
DIP5 (LOW LEVEL ACTIVE)	AA20	In	1.8V	0
DIP6 (LOW LEVEL ACTIVE)	Y20	In	1.8V	0
DIP7 (LOW LEVEL ACTIVE)	V21	In	1.8V	0
DIP8 (LOW LEVEL ACTIVE)	AA19	In	1.8V	0
IO1	V18		1.8V	0
IO2	W20		1.8V	0
IO3	Y19		1.8V	0
IO4	T17		1.8V	0
IO5	W16		1.8V	0
IO6	AA17		1.8V	0
IO7	V15		1.8V	0

IO8	Y15		1.8V	0
UART_TX	W21	Out	1.8V	0
UART_RX	Y21	In	1.8V	0
RPI_GPIO3	E18		2.5V/3.3V (J45)*	1
RPI_GPIO5	F18		2.5V/3.3V (J45)*	1
RPI_GPIO7	E12		2.5V/3.3V (J45)*	1
RPI_GPIO8	A20		2.5V/3.3V (J45)*	1
RPI_GPIO10	B21		2.5V/3.3V (J45)*	1
RPI_GPIO11	G18		2.5V/3.3V (J45)*	1
RPI_GPIO12	E10		2.5V/3.3V (J45)*	1
RPI_GPIO13	F21		2.5V/3.3V (J45)*	1
RPI_GPIO15	F20		2.5V/3.3V (J45)*	1
RPI_GPIO16	E21		2.5V/3.3V (J45)*	1
RPI_GPIO18	F19		2.5V/3.3V (J45)*	1
RPI_GPIO22	A19		2.5V/3.3V (J45)*	1
RPI_GPIO29	D17		2.5V/3.3V (J45)*	1
RPI_GPIO31	D18		2.5V/3.3V (J45)*	1
RPI_GPIO32	B20		2.5V/3.3V (J45)*	1
RPI_GPIO33	A15		2.5V/3.3V (J45)*	1
RPI_GPIO35	B19		2.5V/3.3V (J45)*	1
RPI_GPIO36	B15		2.5V/3.3V (J45)*	1
RPI_GPIO37	B17		2.5V/3.3V (J45)*	1
RPI_GPIO38	B14		2.5V/3.3V (J45)*	1
RPI_GPIO40	E13		2.5V/3.3V (J45)*	1
MIKROBUS_AN	G12		2.5V/3.3V (J45)*	1
MIKROBUS_RST(PULL-UP)	B16		2.5V/3.3V (J45)*	1
MIKROBUS_CS(PULL-UP)	C16		2.5V/3.3V (J45)*	1
MIKROBUS_SCK	E17		2.5V/3.3V (J45)*	1
MIKROBUS_MISO	A18		2.5V/3.3V (J45)*	1
MIKROBUS_MOSI	E11		2.5V/3.3V (J45)*	1
MIKROBUS_PWM	D13		2.5V/3.3V (J45)*	1
MIKROBUS_INT(PULL-UP)	G17		2.5V/3.3V (J45)*	1
MIKROBUS_RX	E14		2.5V/3.3V (J45)*	1

MIKROBUS_TX	E15		2.5V/3.3V (J45)*	1
MIKROBUS_SCL(PULL-UP)	D11		2.5V/3.3V (J45)*	1
MIKROBUS_SDA(PULL-UP)	D12		2.5V/3.3V (J45)*	1
ETH_MDC(PULL-UP)	D15	Out	2.5V/3.3V (J45)*	1
ETH_MDIO(PULL-UP)	D16	Out	2.5V/3.3V (J45)*	1
ETH_MDINTB(PULL-UP)	A13	Out	2.5V/3.3V (J45)*	1
ETH_RESETn(PULL-UP)	A14	Out	2.5V/3.3V (J45)*	1
ETH_RXLOS	A17	Out	2.5V/3.3V (J45)*	1
ETH_TXDISn(PULL-UP)	E20	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_N0	B11	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_P0	C11	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_N1	A10	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_P1	B10	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_CKN	B12	Out	2.5V/3.3V (J45)*	1
GPIO_MIPI_RX_CKP	A12	Out	2.5V/3.3V (J45)*	1
CAM_EN	Y14	In	1.8V	0
CAM_I2C_SDA(PULL-UP)	T20	In	1.8V	0
CAM_I2C_SCL(PULL-UP)	T21	In	1.8V	0
CAM_GPIO	Y17	In	1.8V	0

*
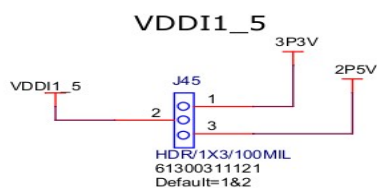
VDDI1_5 and VDDAUX1
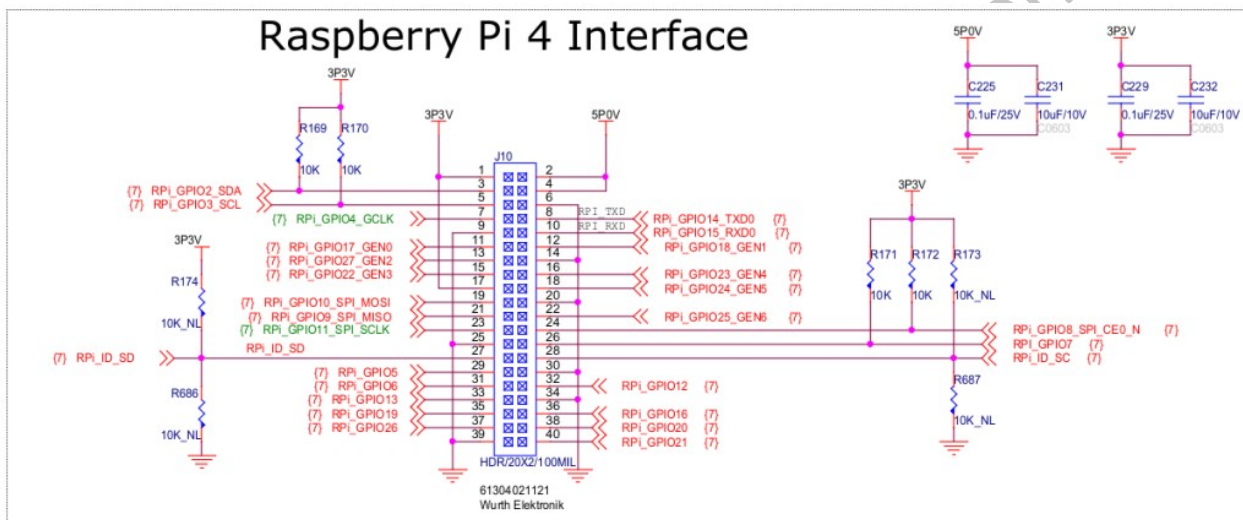2.5V for MIPI and Ethernet PHY operation
3.3V for RPI and MikroBus operation
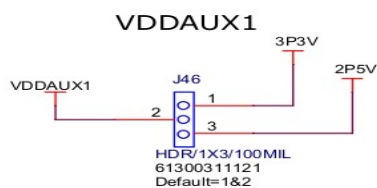
** *LED8 controlled by MSS with 3.3V*

Live Probes (J12). *Debugging pins:*

Pin	Name	Function
1	LPRB_B *(C20)*	Live Probe B
2	LPRB_A *(C21)*	Live Probe A
3	GND	
4	GND	

Raspberry Pi 4 Interface

PIN CONNECTOR	PIN FPGA	TYPE PIN	VOLTAGE	BANK
1		SOURCE	3.3V	
2		SOURCE	5V	
3	E18	HSIO	2.5V/3.3V (J45)	1
4		SOURCE	5V	
5	F18	HSIO	2.5V/3.3V (J45)	1
6		SOURCE	GND	
7	E12	HSIO	2.5V/3.3V (J45)	1
8	A20	HSIO	2.5V/3.3V (J45)	1
9		SOURCE	GND	

10	B21	HSIO	2.5V/3.3V (J45)	1
11	G18	HSIO	2.5V/3.3V (J45)	1
12	E10	HSIO	2.5V/3.3V (J45)	1
13	F21	HSIO	2.5V/3.3V (J45)	1
14		SOURCE	GND	
15	F20	HSIO	2.5V/3.3V (J45)	1
16	E21	HSIO	2.5V/3.3V (J45)	1
17		SOURCE	3.3V	
18	F19	HSIO	2.5V/3.3V (J45)	1
19	A4	MSS	3.3V	2
20		SOURCE	GND	
21	B4	MSS	3.3V	2
22	A19	HSIO	2.5V/3.3V (J45)	1
23	D6	MSS	3.3V	2
24	D5	MSS	3.3V	2
25		SOURCE	GND	
26	B2	MSS	3.3V	2
27	D1	MSS	3.3V	2
28	C2	MSS	3.3V	2
29	D17	HSIO	2.5V/3.3V (J45)	1
30		SOURCE	GND	
31	D18	HSIO	2.5V/3.3V (J45)	1
32	B20	HSIO	2.5V/3.3V (J45)	1
33	A15	HSIO	2.5V/3.3V (J45)	1
34		SOURCE	GND	

35	B19	HSIO	2.5V/3.3V (J45)	1
36	B15	HSIO	2.5V/3.3V (J45)	1
37	B17	HSIO	2.5V/3.3V (J45)	1
38	B14	HSIO	2.5V/3.3V (J45)	1
39		SOURCE	GND	
40	E13	HSIO	2.5V/3.3V (J45)	1

MIKROBUS
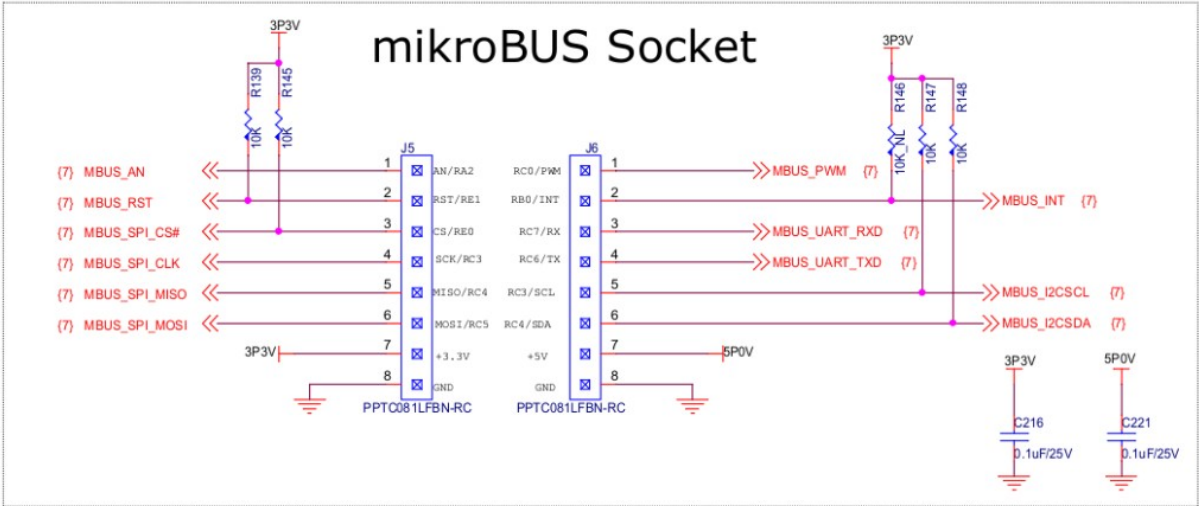
CONNECTOR	PIN	NAME	FPGA PIN	VOLTAGE	BANK
J5	1	MIKROBUS_AN	G12	2.5V/3.3V (J45)	1
J5	2	MIKROBUS_RST(PULL-UP: 3V3)	B16	2.5V/3.3V (J45)	1
J5	3	MIKROBUS_CS(PULL-UP: 3V3)	C16	2.5V/3.3V (J45)	1
J5	4	MIKROBUS_SCK	E17	2.5V/3.3V (J45)	1
J5	5	MIKROBUS_MISO	A18	2.5V/3.3V (J45)	1
J5	6	MIKROBUS_MOSI	E11	2.5V/3.3V	1

				(J45)	
J5	7	3V3			
J5	8	GND			
J6	1	MIKROBUS_PWM	D13	2.5V/3.3V (J45)	1
J6	2	MIKROBUS_INT(PULL-UP: 3V3)	G17	2.5V/3.3V (J45)	1
J6	3	MIKROBUS_RX	E14	2.5V/3.3V (J45)	1
J6	4	MIKROBUS_TX	E15	2.5V/3.3V (J45)	1
J6	5	MIKROBUS_SCL(PULL-UP: 3V3)	D11	2.5V/3.3V (J45)	1
J6	6	MIKROBUS_SDA(PULL-UP: 3V3)	D12	2.5V/3.3V (J45)	1
J6	7	5V			
J6	8	GND			

ETHERNET *(GPIO & MSS Pins)*

PHY address[4:0]: 01011
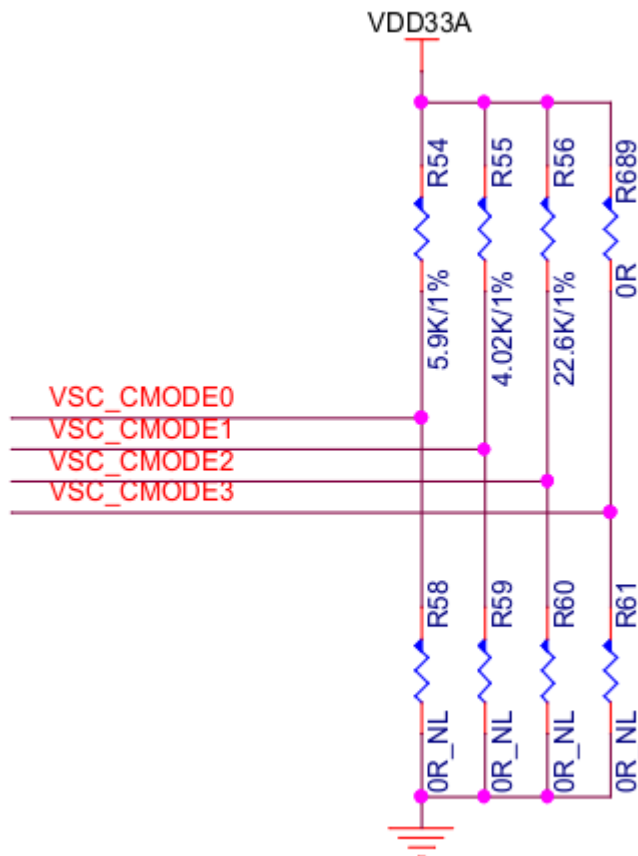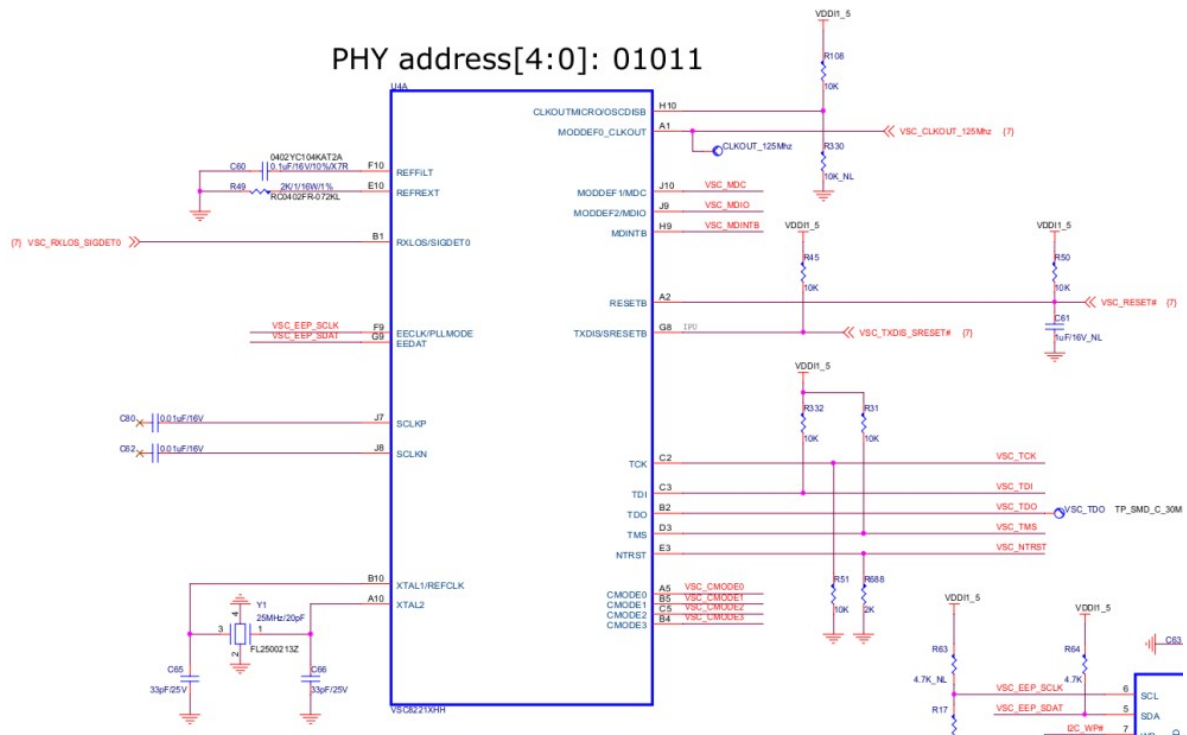
*R58, R59, R60, R61 : NM → **CMODE: 2***

	bit 3	bit 2	bit 1	bit 0	Connection
CMODE 0	Phy address[3]	Phy address[2]	Phy address[1]	Phy address[0]	
	1	0	1	1	5.90k tied to VDD33A
CMODE1	SFP Mode Disable	PHY Address[4]	SiGDET pin direction	SerDes Line impedance	
	1	0	1	0	4.02k tied to VDD33A
CMODE 2	PHY Operating Mode[3]	PHY Operating Mode[2]	PHY Operating Mode[1]	PHY Operating Mode[0]	
	1	1	1	1	22.6k tied to VDD33A
CMODE3	LED Control[1]	SQE Enable	Reserved	Auto-negotiation Advertisement Control[1]	
	1	0	0	0	0k tied to VDD33A
	LED[2:0] = {Link/Activity, Link/Activity, Fault}			10/100/1000BASE-T HDX, FDX	

Name	FPGA Pin	Type	Voltage	Bank
ETH_MDC(PULL-UP)	D15	Out	2.5V/3.3V (J45)	1
ETH_MDIO(PULL-UP)	J9	Out	2.5V/3.3V (J45)	1
ETH_MDINTB(PULL-UP)	A13	Out	2.5V/3.3V (J45)	1
ETH_RESETn(PULL-UP)	A14	Out	2.5V/3.3V (J45)	1
ETH_RXLOS	A17	Out	2.5V/3.3V (J45)	1
ETH_TXDISn(PULL-UP)	E20	Out	2.5V/3.3V (J45)	1

… Other pins are MSS pins
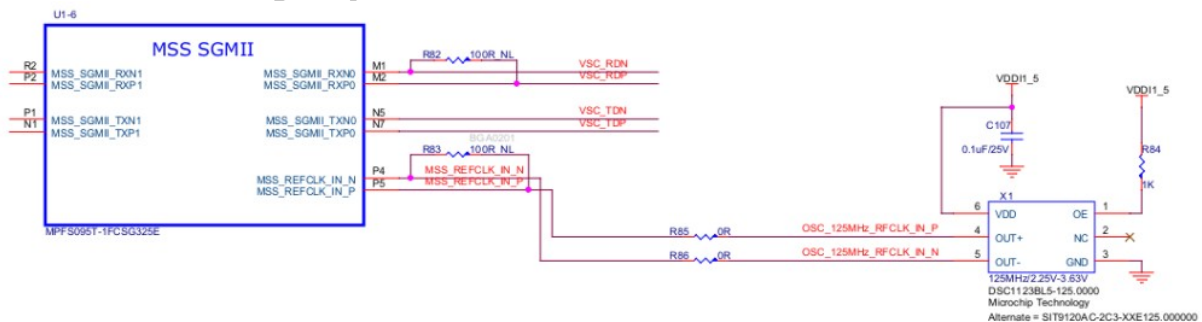
MIPI Conector
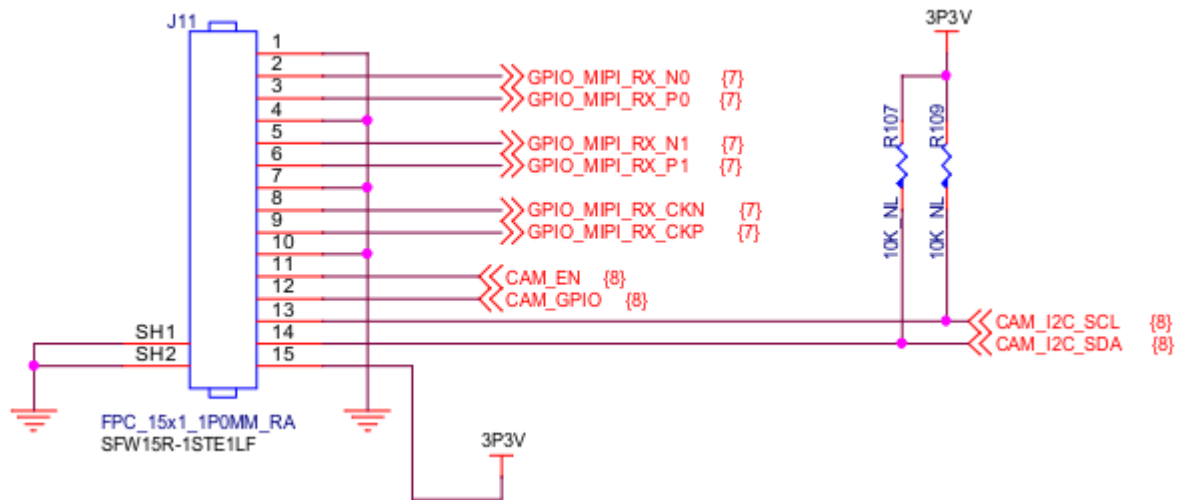
Pin	Name	FPGA Pin	Type	Voltage	Bank
1	GND				
2	GPIO_MIPI_RX_N0	B11	Out	2.5V/3.3V (J45)	1
3	GPIO_MIPI_RX_P0	C11	Out	2.5V/3.3V (J45)	1
4	GND				
5	GPIO_MIPI_RX_N1	A10	Out	2.5V/3.3V (J45)	1
6	GPIO_MIPI_RX_P1	B10	Out	2.5V/3.3V (J45)	1
7	GND				
8	GPIO_MIPI_RX_CKN	B12	Out	2.5V/3.3V (J45)	1
9	GPIO_MIPI_RX_CKP	A12	Out	2.5V/3.3V (J45)	1
10	GND				
11	CAM_EN	Y14	In	1.8V	0
12	CAM_GPIO	Y17	In	1.8V	0
13	CAM_I2C_SDA(PULL-UP)	T20	In	1.8V	0
14	CAM_I2C_SCL(PULL-UP)	T21	In	1.8V	0

| 15 | GND | | | | |

7 Segment Display
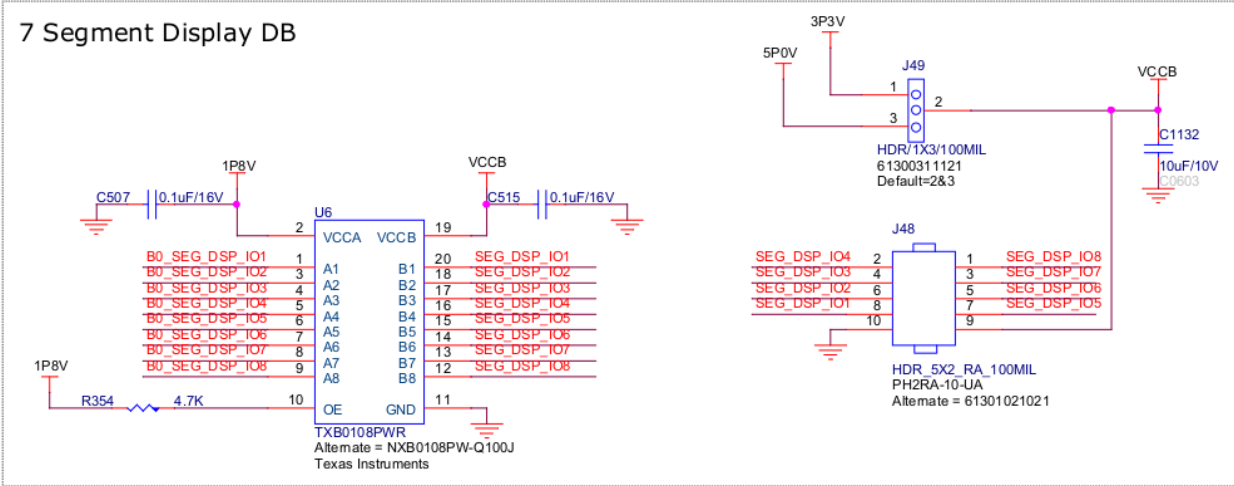
FPGA Output voltage: 1.8V → Pin voltage: 3V3 / 5V (J49)

Name	FPGA PIN	Type	Voltage	FPGA Bank
IO1	V18	Out	1.8V	0
IO2	W20	Out	1.8V	0
IO3	Y19	Out	1.8V	0
IO4	T17	Out	1.8V	0
IO5	W16	Out	1.8V	0
IO6	AA17	Out	1.8V	0
IO7	V15	Out	1.8V	0
IO8	Y15	Out	1.8V	0

SD CARD (*MSS Pins*)

SD_CD#

J17   9   S3 S4

SD_CLK   5   CLK   Card Det   SH3 SH4

SD_DAT3   2   CD/DAT3
SD_DAT2   1   DAT2   MEM2075-00-140-01-A
SD_DAT1   8   DAT1   GCT
SD_DAT0   7   DAT0

uSD CARD

SD_CMD   3   CMD   VDD   VSS1   SH1 SH2

         4   6   S1 S2

PART_NUMBER =

3P3V

	C722	0.1uF/25V
	C723	0.1uF/25V
	C724	4.7uF/16V

VDDI4 = 1.8V

U1-7

MSSIO-B4

SD_LT_CLK	L2	MSSIO0B4	MSSIO7B4	H2
SD_LT_CMD	M4	MSSIO1B4	MSSIO8B4	L7 SD_LT_POW
SD_LT_DATA0	L3	MSSIO2B4	MSSIO9B4	K7 SD_LT_SEL
SD_LT_DATA1	K1	MSSIO3B4	MSSIO10B4	H1
SD_LT_DATA2	M5	MSSIO4B4	MSSIO11B4	K4
SD_LT_DATA3	L5	MSSIO5B4	MSSIO12B4	K5
SD_CD#	K2	MSSIO6B4	MSSIO13B4	J1

MPFS095T-1FCSG325E