How to assign a decimal value to a std_logic_vector

Created by: David Rubio G.

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Blog: https://soceame.wordpress.com/

GitHub: https://github.com/DRubioG

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Many times we have wanted to assign a decimal value to a *std_logic_vector* and we have not been able to do it directly and we have had to declare a *constant* with a fixed value and then assign the value of that constant to the signal we want.

Well, there is a way to do that assignment without having to go through a constant.

The normal assignment method is:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity borrar is
    port(
       a : in std_logic;
       b : out std_logic_vector(9 downto 0)
    );
end entity;
architecture arch_borrar of borrar is
-- the classic way to define a constant is to define all
-- the fields:
-- constant twelve : unsigned(9 downto 0) := to_unsigned(12,
-- but it can also be done in a summarized way:
constant twelve : unsigned(b'range) := to_unsigned(12, b'length);
begin
    process(a)
    begin
    if a = '1' then
        b <= std_logic_vector(twelve);</pre>
           b <= (others
     end if;
      end process;
end architecture;
Well, the other way we avoid having to declare a constant is to use '<signal> <=
std logic vector(to unsigned(<value>, <signal>'length));'
This example illustrates its use:
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity borrar is
    port(
        a : in std_logic;
        b : out std_logic_vector(9 downto 0)
```

```
);
end entity;

architecture arch_borrar of borrar is

begin
    process(a)
    begin
    if a = '1' then
        b <= std_logic_vector(to_unsigned(12, b'length));
    elsif a = '0' then
        b <= (others=>'0');
    end if;
end process;

end architecture;
```

And with this we avoid having to declare a constant for the assignment of a decimal value.

Also, comparisons can be made with this format, for example:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity borrar is
    port(
        a : in std_logic_vector(9 downto 0);
        b : out std_logic
    );
end entity;
architecture arch_borrar of borrar
begin
    process(a)
    begin
        if a = std_logic_vector(to_unsigned(12, b'length))then
        end if;
    end process;
end architecture;
```

Note

You should always use the 'numeric_std' library