What is DEVRST_N and how does it work on Microchip FPGAs?

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Blog post: https://soceame.wordpress.com/2025/03/11/what-is-devrst_n-and-how-does-it-work-on-microchip-fpgas/

Blog: https://soceame.wordpress.com/

GitHub: https://github.com/DRubioG

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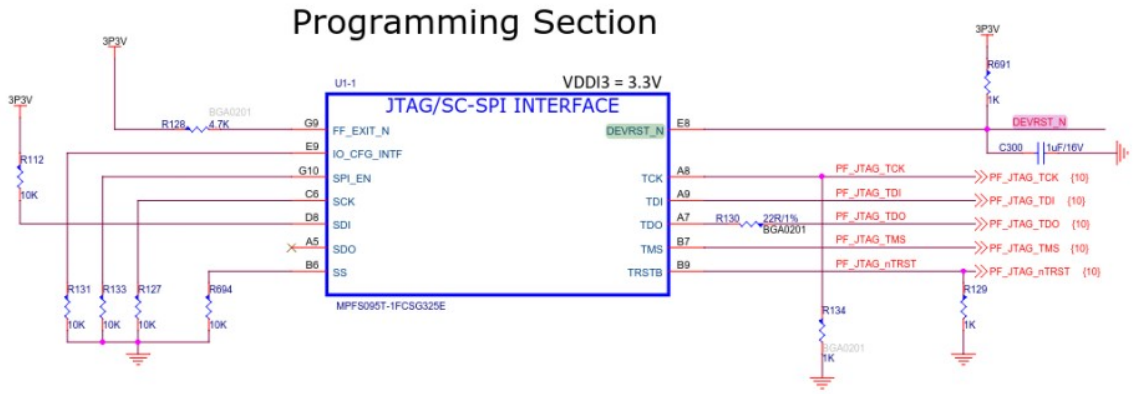
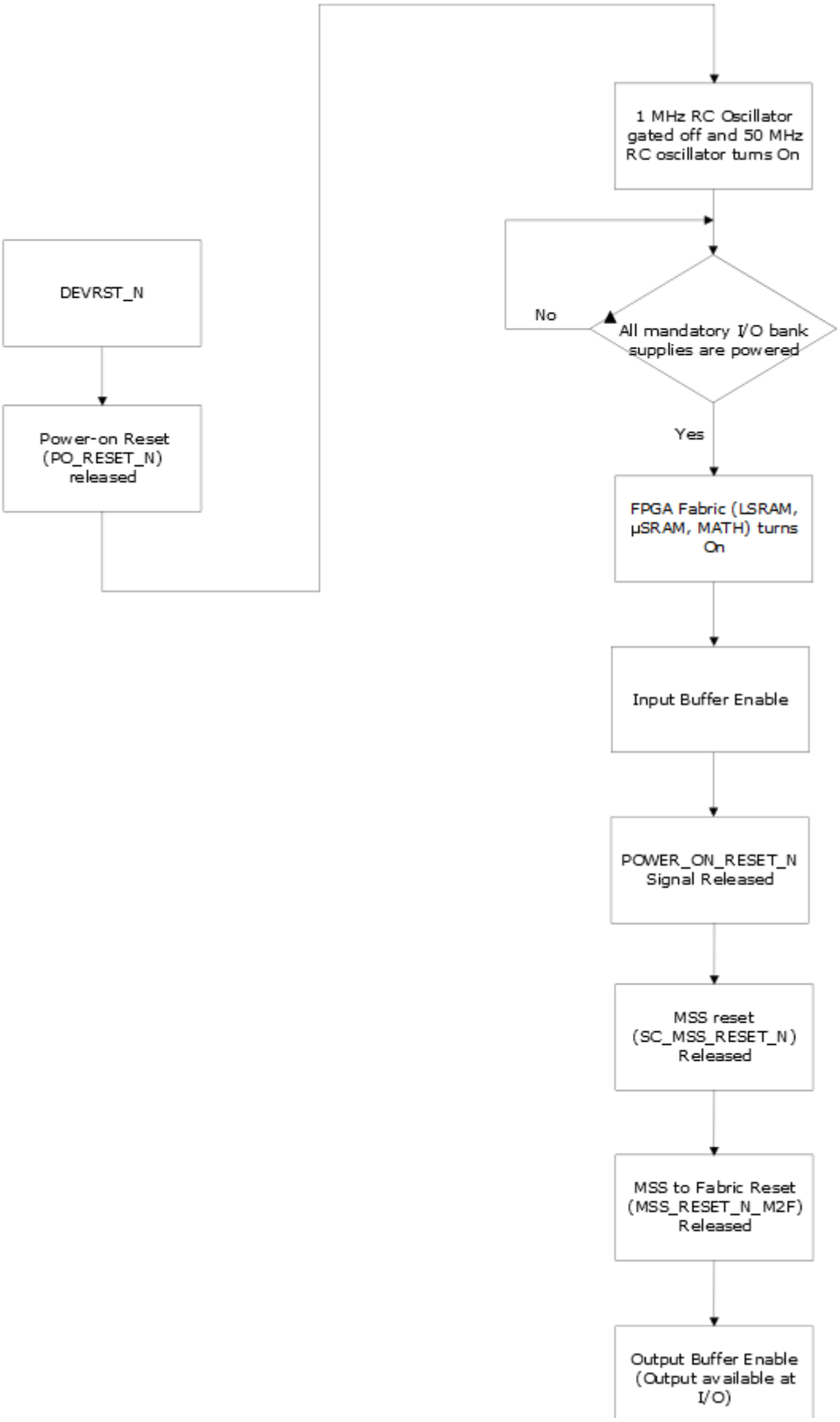
A very common question about Microchip FPGAs/SoCs is what is the DEVRST_N pin used for?

The DEVRST_N pin is a pin that Microchip includes in its FPGAs, but this pin could be similar to those that other FPGA manufacturers have to erase the bitstream of their FPGAs, but it is not.

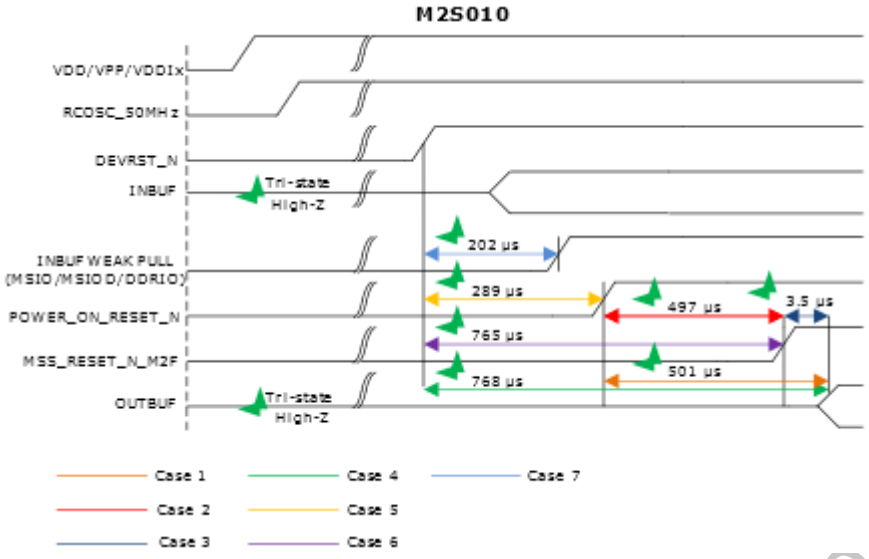


The function of this pin is to cut off the enabling of the FPGA logic, because since this type of FPGA is Flash type, the bitstream is not erased.

The manufacturer publishes the state machine that manages the DEVRST_N when activated. So, it can be seen that in no case does it reset or reload the FPGA bitstream, the only thing it does is enable the internal logic of the FPGA.


1 MHz RC Oscillator gated off and 50 MHz RC oscillator turns On
DEVRST_N
No
All mandatory I/O bank supplies are powered
Yes
Power-on Reset (PO_RESET_N) released
FPGA Fabric (LSRAM, µSRAM, MATH) turns On
Input Buffer Enable
POWER_ON_RESET_N Signal Released
MSS reset (SC_MSS_RESET_N) Released
MSS to Fabric Reset (MSS_RESET_N_M2F) Released
Output Buffer Enable (Output available at I/O)

If you look at the timing curves published by the manufacturer, you can see that the DEVRST_N is activated before the logic, but after the power supplies come into use.



How to Use

The DEVRST_N pin is not selectable for use in firmware, so the only way to do so is through the *SYSRESET* block. This block is linked to the logic only for booting an MSS core in a SmartFusion2.