How to access the synthesis model in Libero

Created by: David Rubio G.

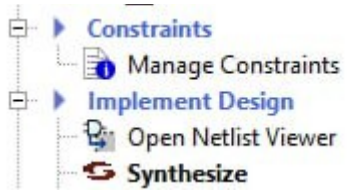
Blog post: https://soceame.wordpress.com/2025/03/11/how-to-access-the-synthesis-model-in-libero/

Blog: https://soceame.wordpress.com/

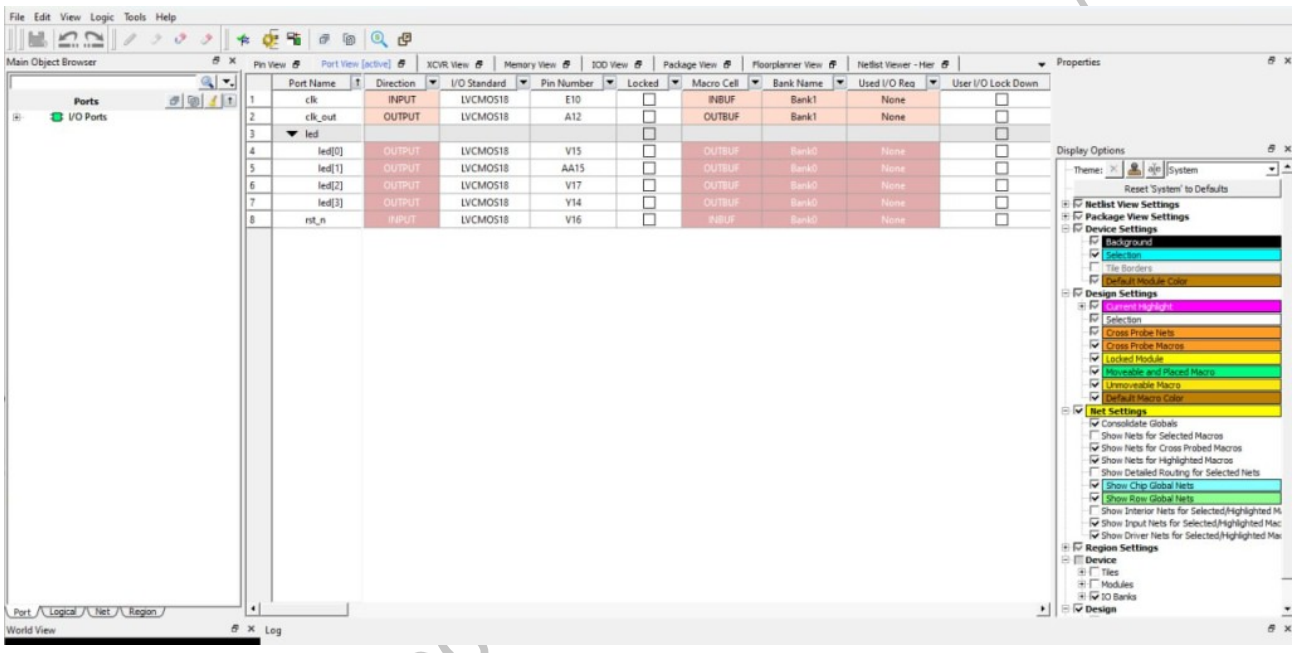
GitHub: https://github.com/DRubioG

Last modification date: 11/03/25

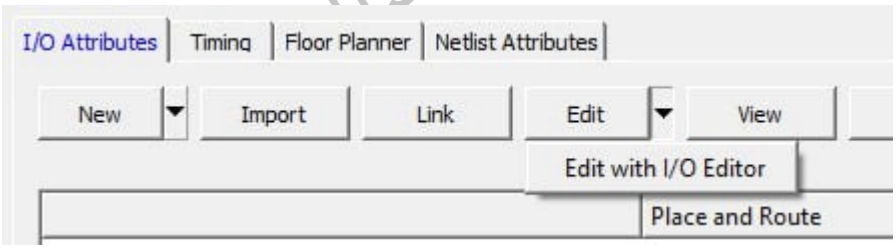
To access the synthesis models you must first have the FW implementation done. Then you have to go to the *Manage Constraints* tab.



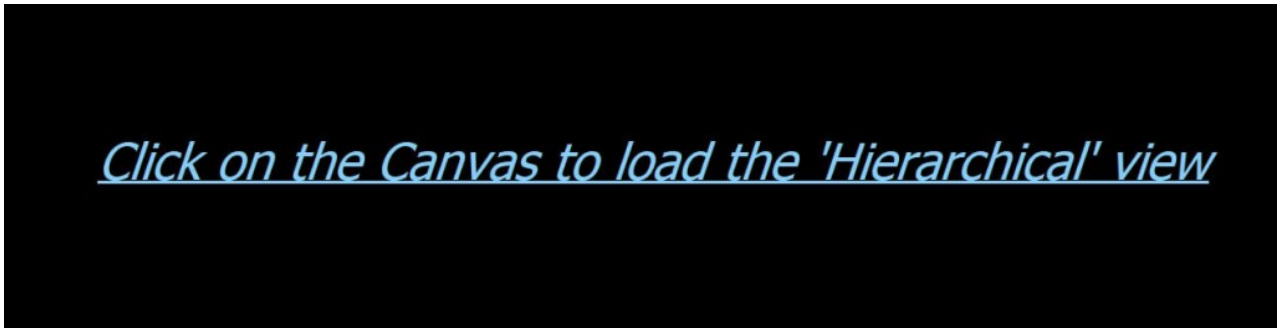
A tab will open for you to edit it.



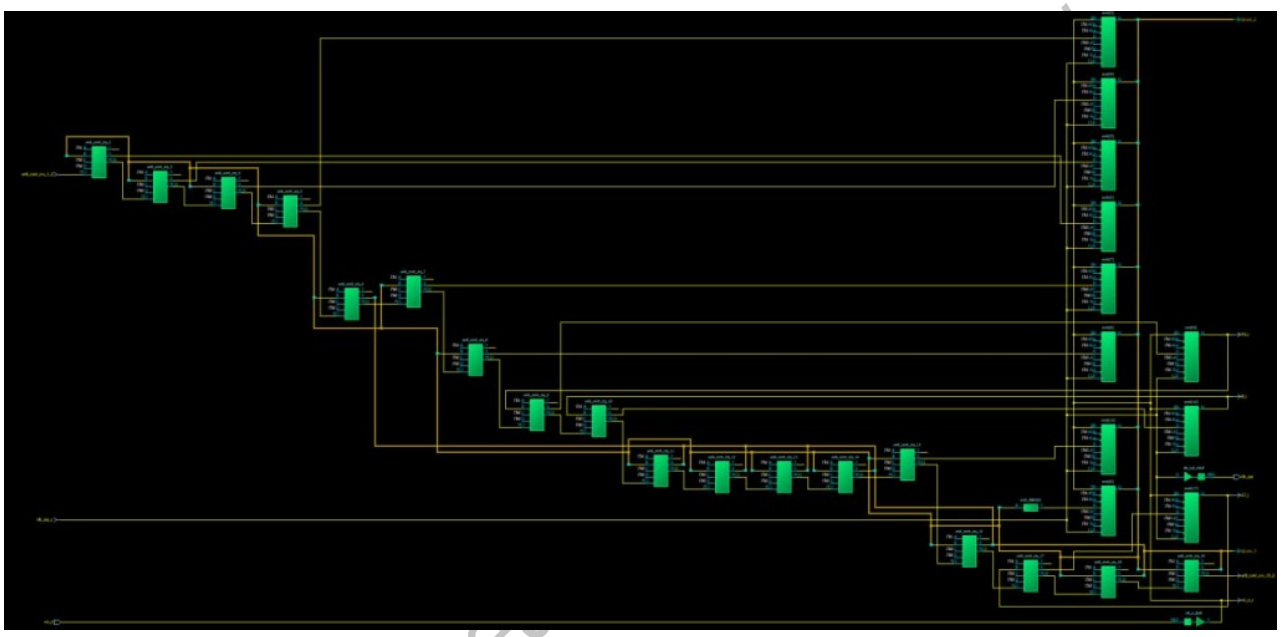
In the *I/O Attributes* tab you have to click *Edit with I/O Editor.*



If you go to the **Netlist Viewer – Hier** tab a message like the following appears.

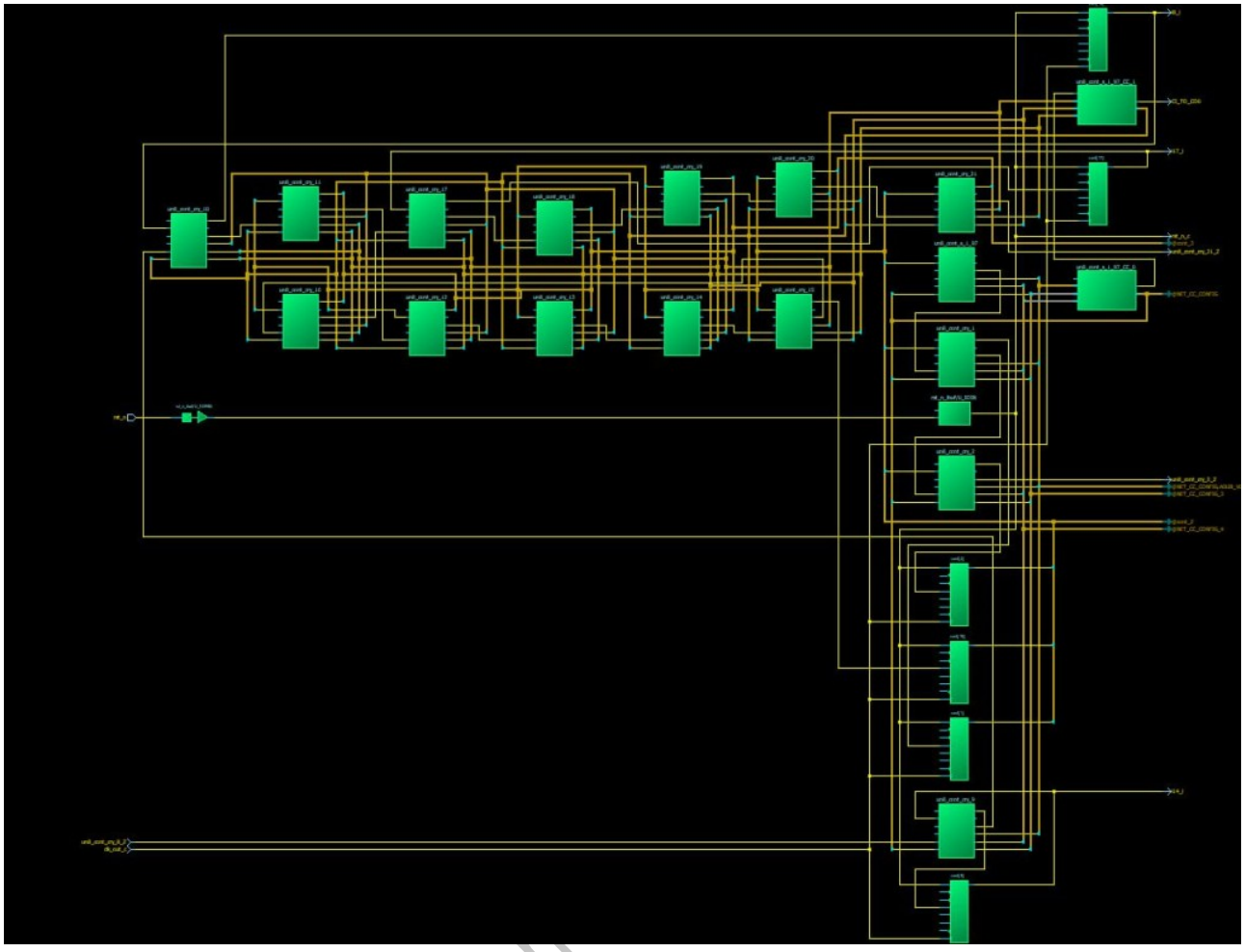


You just have to click on it and the synthesis model will open.

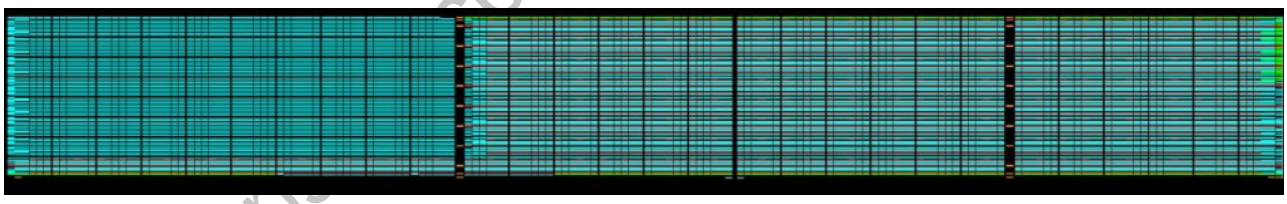


In the tab next to **Netlist Viewer – Flat** another message like this appears.

Just click on it as before.



In the **Floorplanner View** tab you have the FPGA/SoC implementation model.



Finally in the **Package View** tab you have the model to configure the package pins.