How to generate a .xdc file

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Blog post: https://soceame.wordpress.com/2025/03/09/how-to-generate-a-xdc-file/

Blog: https://soceame.wordpress.com/

GitHub: https://github.com/DRubioG

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An XDC file is a pin assignment file on a Xilinx board. This file determines the input or output port on the board, the physical pin to which the port is to be assigned, and the power bank.

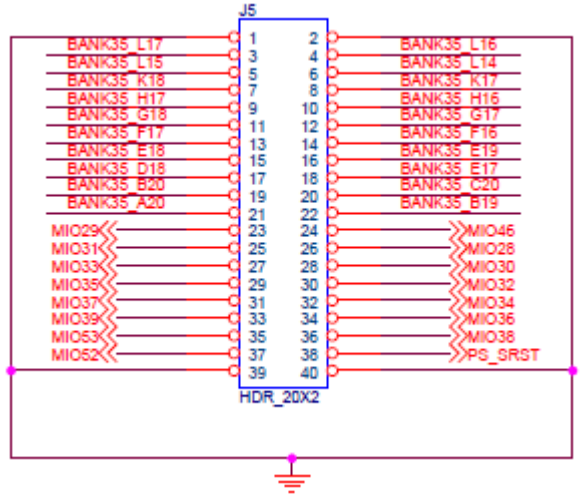
Input/Output Signals

These are the signals that have been determined in the code to be input or output to the system. For example, in VHDL they are the in and out ports.

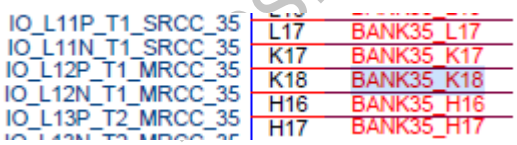
Physical Pins on the Board

These pins are the ones on the board that are connected to the real FPGA. To locate these pins you have to go to the datasheet and look at how the manufacturer has assigned the output pins.

For example, on the board I have, the manufacturer in the datasheet gives me these output pins



So, to use pin 7 I have to follow the BANK35_K18 signal to find out which chip pin it uses.



Pin 7 is assigned to pin K18 and this is the one that will be used to generate the xdc.

> Many times the manufacturer calls the outputs on the board and the outputs of the FPGA chip in the same way. In the previous example you can see that the BANK35_K18 signal already includes the K18 output

Power bank

The power bank is what allows you to vary the maximum input voltage of the pins.

For example, to output a signal with a voltage of 3.3V you have to use the LVCMOS33 bank.

Generating XDC

To generate a basic XDC, at least two lines of code are needed.

```
set_property IOSTANDAR <Power bank> [get_ports <port name>];
set_property PACKAGE_PIN <pin name>[get_ports <port name>];
```

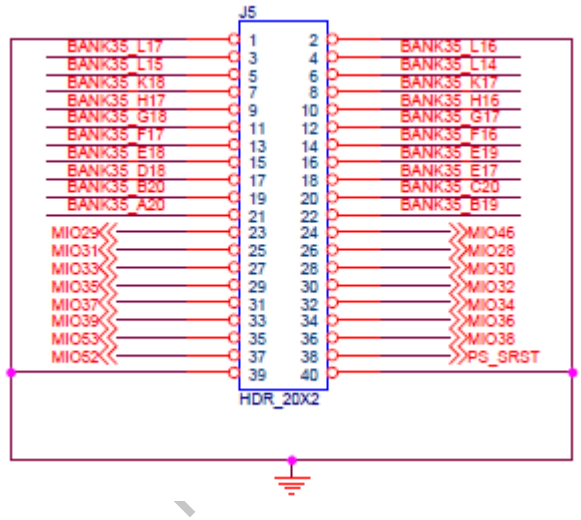
The first line assigns a reference voltage to the port, and the second assigns the output pin to the port

> If instead of single-signal output ports, they are multi-signal ports, each bit of the signal must be declared separately using the scheme:
> set_property PACKAGE_PIN <pin name> [get_ports {<port name>[<port bit>]}];

Example

You want to output a signal called two_bits (which has two output bits) of 3.3V through pins 7 and 8 of a board with the XC7Z010 chip.

First, you look for output pins 7 and 8 of the FPGA.



The output pins are K18 and K17. So, since you already have the three things that you have to output, you proceed to generate the XDC.

```
set_property IOSTANDAR LVCMOS33[get_ports {dos_bits[0]}]; #pin 7
set_property IOSTANDAR LVCMOS33 [get_ports {dos_bits[1]}]; #pin 8

set_property PACKAGE_PIN K18 [get_ports {dos_bits[0]}]; #pin 7
set_property PACKAGE_PIN K17 [get_ports {dos_bits[1]}]; #pin 8
```

** This file goes in the Constraints section of Vivado

Here is a link to the XDC of a XC7Z010-CLG400 from QMTECH

Another way to generate an XDC is through the Pin Planner, which will be discussed in another entry.

NOTE: There is an extension of this entry

https://soceame.wordpress.com/2025/03/09/how-to-generate-a-xdc-file-updated-and-expanded/

NOTE 2: You can also create an XDC using Vivado

https://soceame.wordpress.com/2025/03/09/how-to-create-an-xdc-from-vivado/