

# How to create a BIF interface in Libero

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Blog post: <https://soceame.wordpress.com/2025/03/11/how-to-create-a-bif-interface-in-libero/>

Blog: <https://soceame.wordpress.com/>

GitHub: <https://github.com/DRubioG>

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If you have come this far it is because you have not found the necessary documentation to be able to create a BIF connector in Libero, which are essential for the creation of IP blocks in Libero, because if not, the connectors cannot be joined with the different connections.

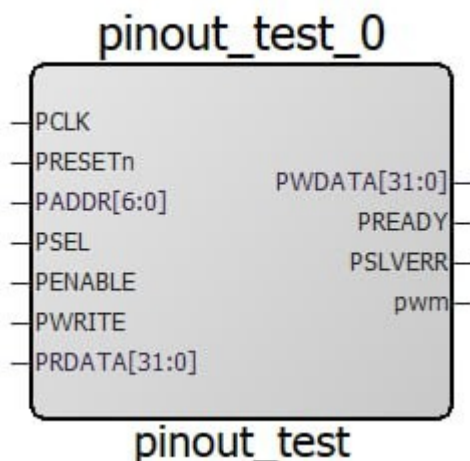
In this post I will explain how to create a BIF for APB. Based on this information in a future post I will explain how to create an IP block for Libero.

## BIF for APB

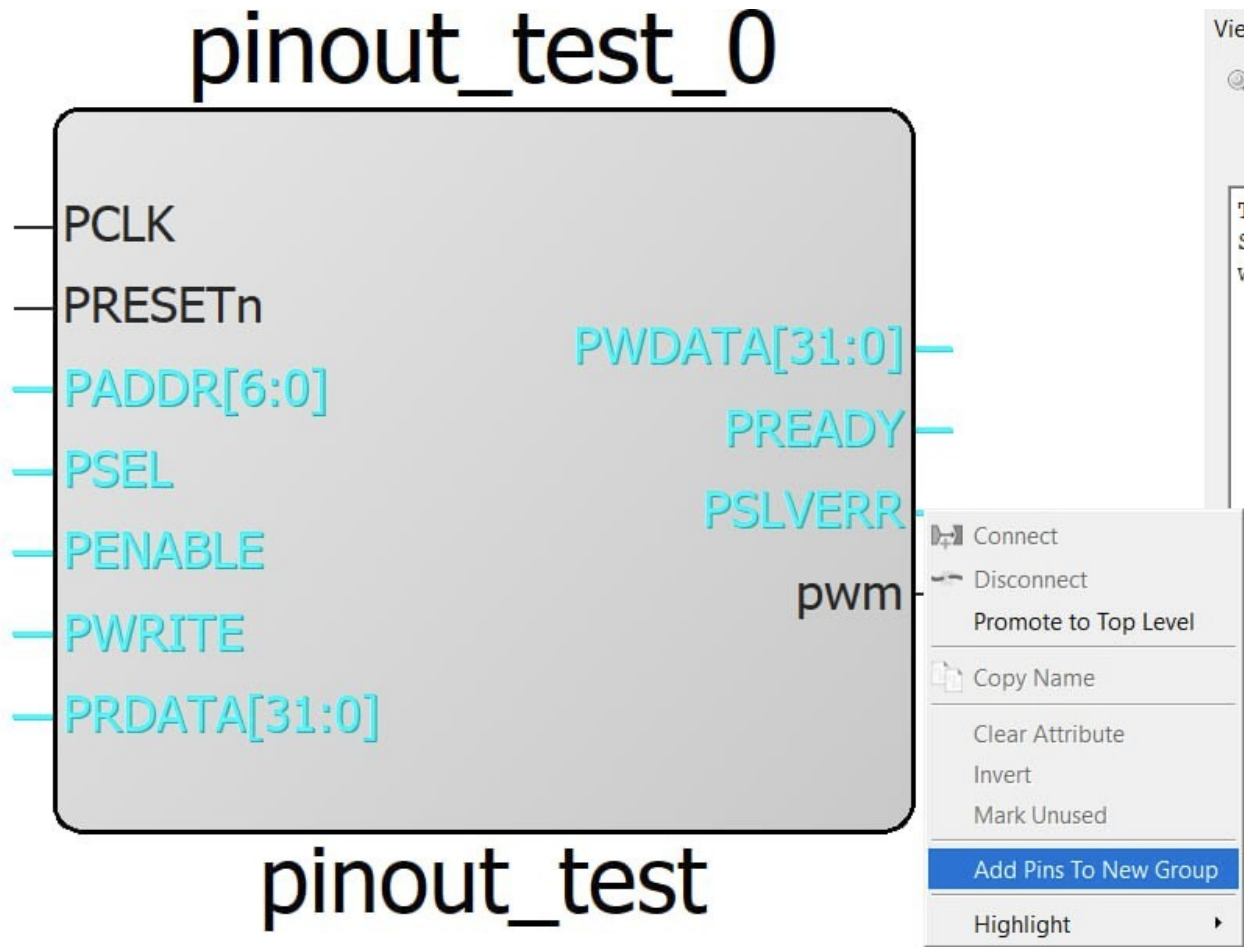
To create a BIF for AMBA 3 you have to have the following ports in the module:

PADDR	7 BITS
PSEL	1 BIT
PENABLE	1 BIT
PWRITE	1 BIT
PRDATA	32 BITS
PWDATA	32 BITS
PREADY	1 BIT
PSLVERR	1 BIT

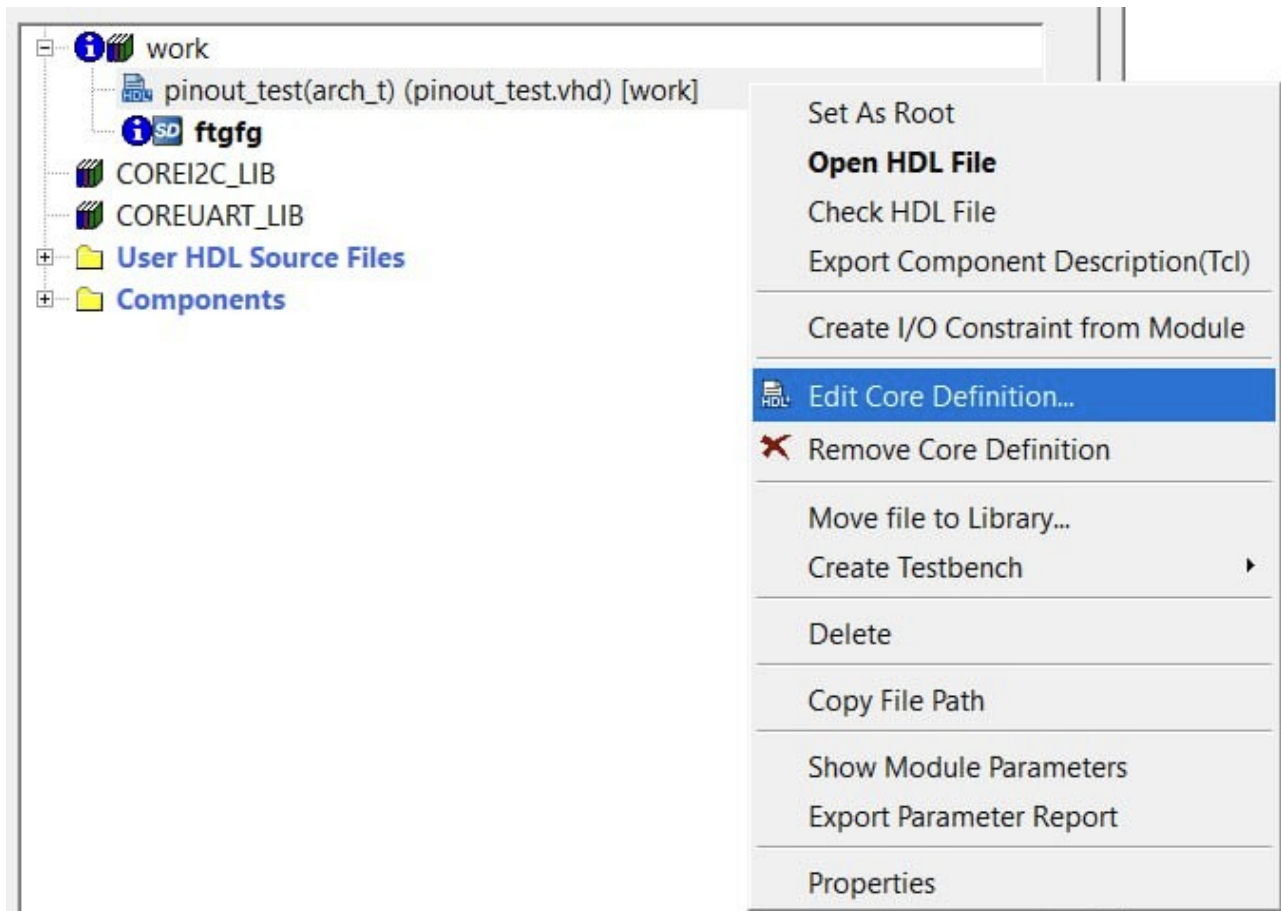
An example of an IP block is like the following, in addition to the APB ports a clock and a reset are needed, and finally the specific pins of the project, in my case the pwm port as an example.



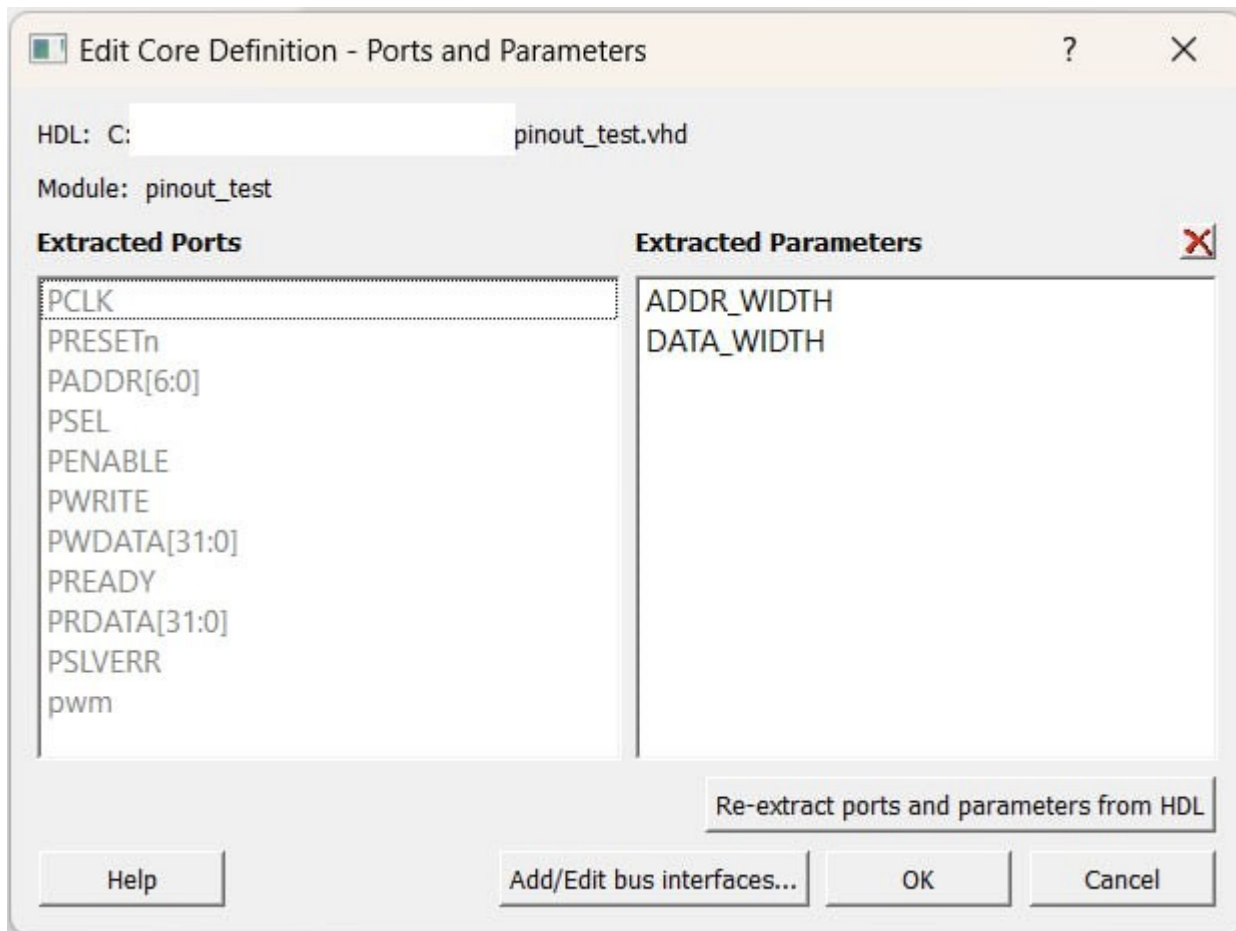
**NOTE:** to create a BIF you do **NOT** have to create a group



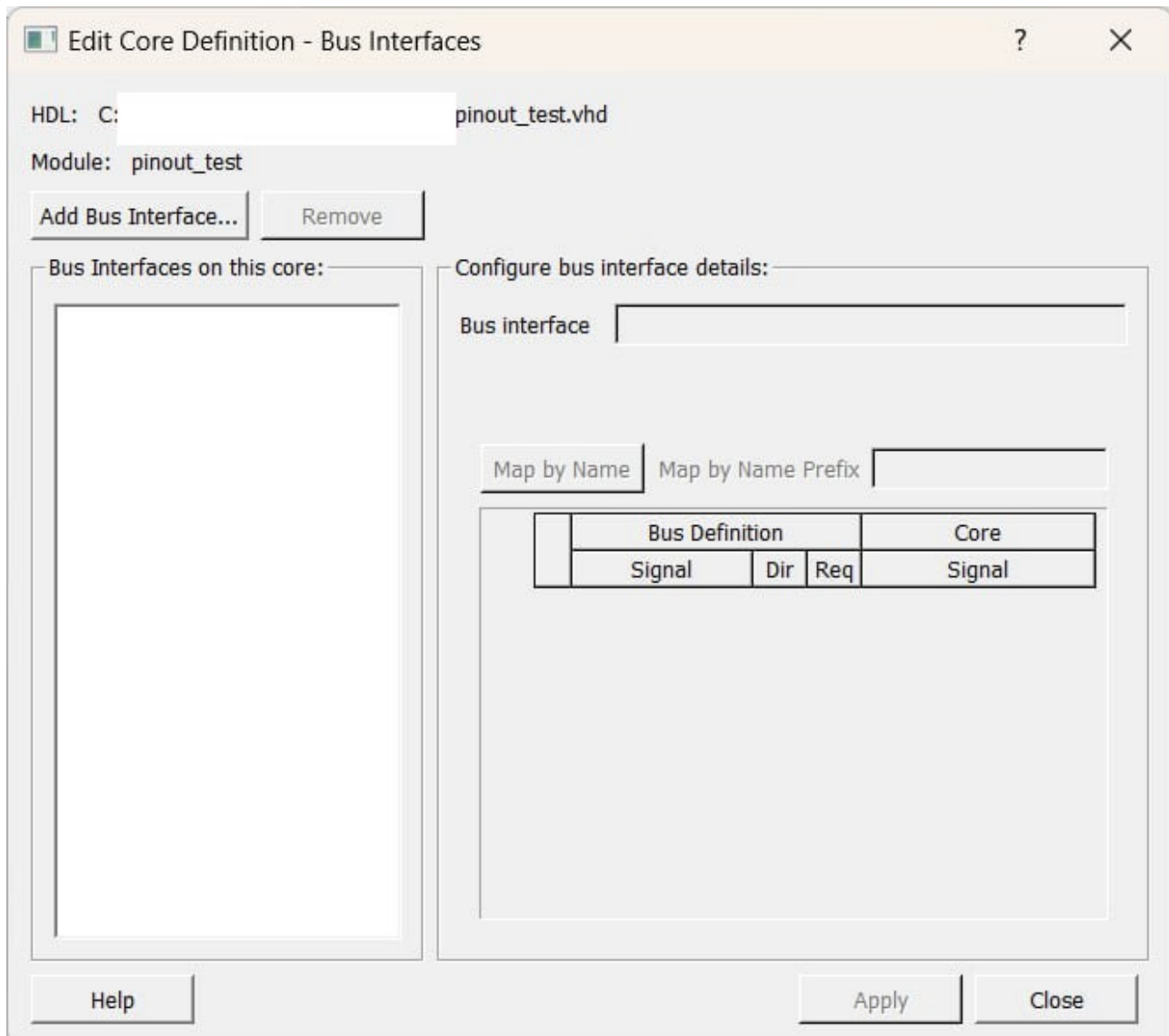
To create an interface we have to act as if we were going to create an IP block, so we right click on the file in which we want to create an interface and click on the *Edit Core Definition* option.



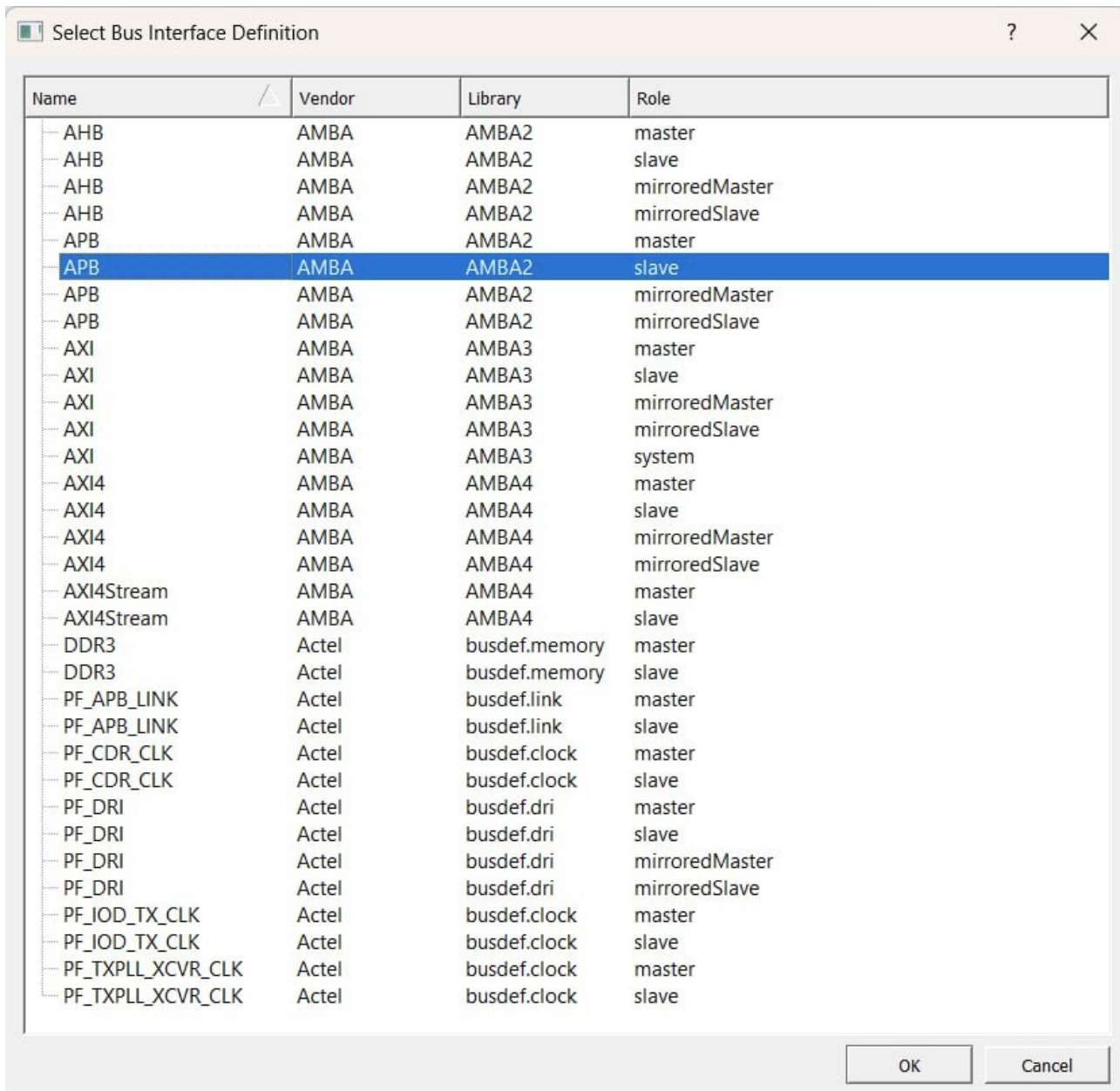
Now a tab opens where the generics that the module has appear on the right and the ports of the module on the left.



Now we have to click on the Add/Edit bus interfaces option, and a new tab opens where the buses already created appear, in my case there are none yet.



Now we click on the *Add Bus Interface...* option and a tab opens with all the protocols supported by Libero. In my case I am going to create an APB slave type interface.



Once we click on it, it automatically assigns ports by name, so if we have a port called PADDR it automatically assigns it to the PADDR of the APB. The rest have to be entered by hand. You can also change the name of the BIF.


Module: pinout\_test

Add Bus Interface... Remove














Bus Interfaces on this core:

BIF\_1

Configure bus interface details:

Bus interface (APB):  BIF\_1

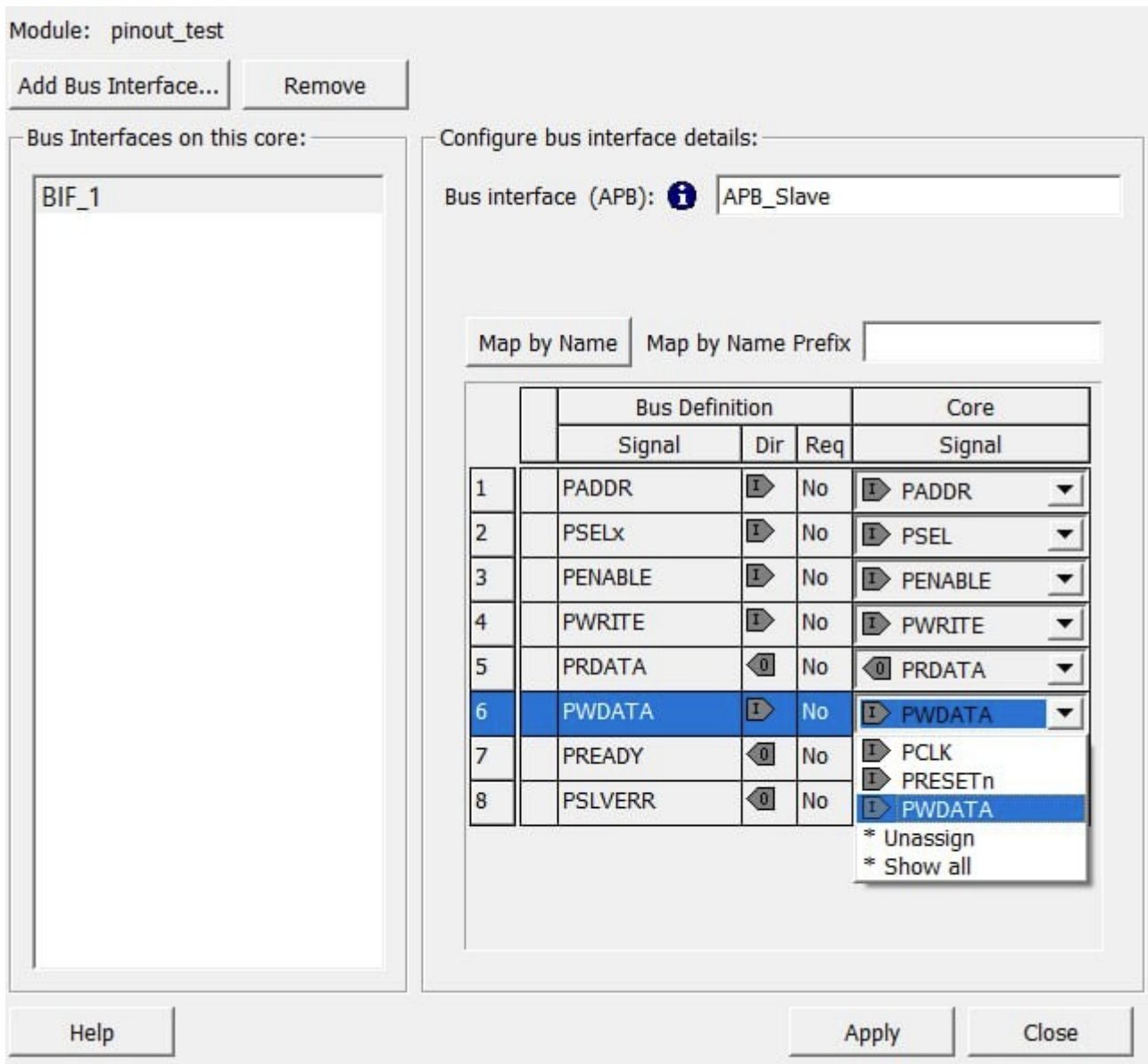
Map by Name Map by Name Prefix

	Bus Definition			Core
	Signal	Dir	Req	Signal
1	PADDR		No	 PADDR ▼
2	PSELx		No	▼
3	PENABLE		No	 PENABLE ▼
4	PWRITE		No	 PWRITE ▼
5	PRDATA		No	▼
6	PWDATA		No	▼
7	PREADY		No	 PREADY ▼
8	PSLVERR		No	 PSLVERR ▼

Help Apply Close

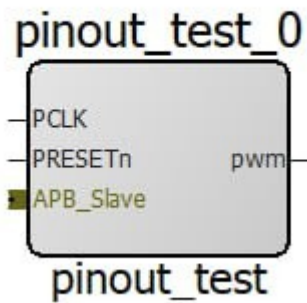
Now the pins are assigned and the interface is renamed to *APB\_Slave*.



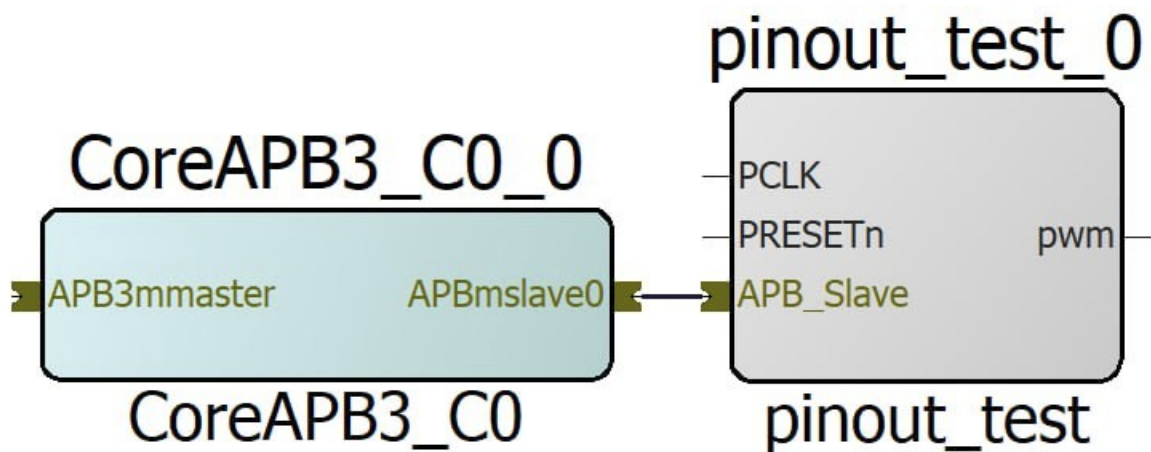


Now click *Apply* and close this tab. Next, click *OK* and return to the Libero tab.

If I now drag the module to a SmartDesign, I can see that the interface has been created in the module.



And now this interface can be connected to any *APB master* interface.



Just as you can do for the APB interface, you can do it for any other interface.

**NOTE:** It is important to keep in mind that importing an IP block is quite complex, so it is recommended to create the interface in those files that are going to be used as final files to avoid having to recreate the interfaces again.