

How to create an XDC from Vivado

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Blog post: <https://soceame.wordpress.com/2025/03/09/how-to-create-an-xdc-from-vivado/>

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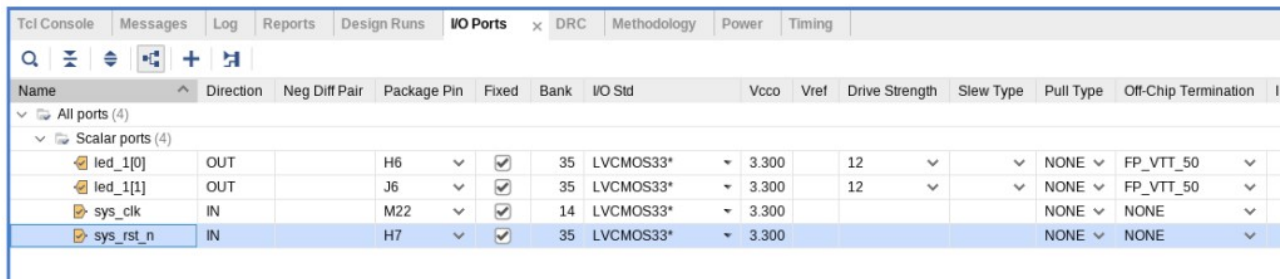
GitHub: <https://github.com/DRubioG>

Last modification date: 09/03/25

In previous posts I explained how to make an XDC by hand, now I'll explain how you can create your own from Vivado.

The first thing you have to do is implement it. With the implementation done, open the profile and in the upper tab of Window an option called I/O Ports appears.

In this tab you have to follow what the schematic of the board dictates.



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination
All ports (4)												
Scalar ports (4)												
led_1[0]	OUT		H6	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12		NONE	FP_VTT_50
led_1[1]	OUT		J6	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300		12		NONE	FP_VTT_50
sys_clk	IN		M22	<input checked="" type="checkbox"/>	14	LVC MOS33*	3.300				NONE	NONE
sys_rst_n	IN		H7	<input checked="" type="checkbox"/>	35	LVC MOS33*	3.300				NONE	NONE

Here you can select the pin you want for the port, and the voltage of the pin, in our case 3.3V.

Once you have the pins created you have to save them.

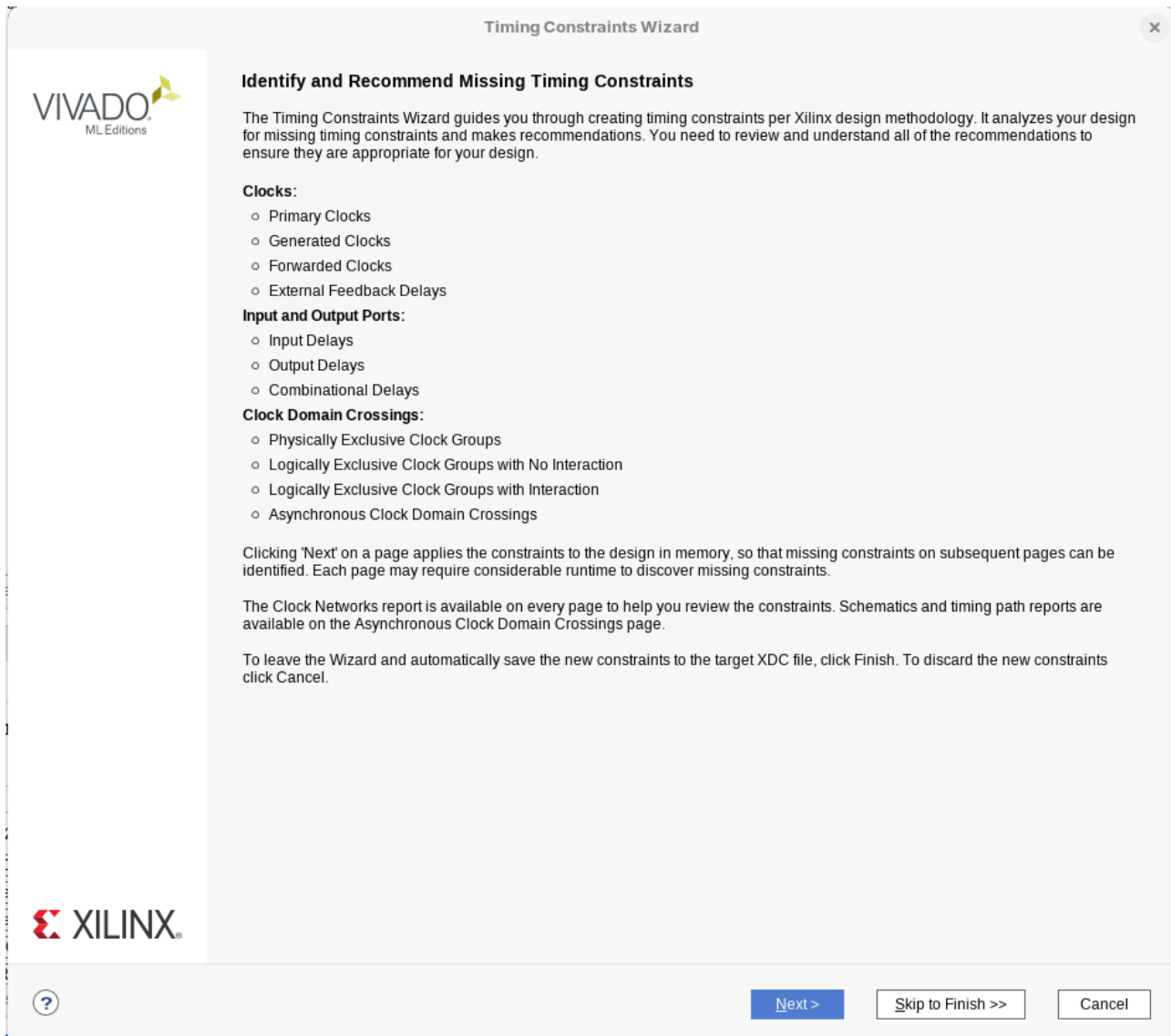


Then, Vivado will ask you if you want to create a new one, or overwrite an XDC you already have.

Create a clock

To create a clock and just like in the previous step, in Tools, an option called **Timing Constraints Wizard** appears.

When you click on it, a tab opens, to configure the profile you want.




In this tab you choose the primary clocks you want

Timing Constraints Wizard

Primary Clocks

Primary clocks usually enter the design through input ports. Specify the period and optionally a name and waveform (rising and falling edge times) to describe the duty cycle if not 50%. [More info](#)

Recommended Constraints

<input checked="" type="checkbox"/>	Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
<input checked="" type="checkbox"/>	 sys_clk	sys_clk	100.000	10.000	0.000	5.000	

Constraints for Pulse Width Check Only

<input type="checkbox"/>	Object	Name	Frequency (MHz)	Period (ns)	Rise At (ns)	Fall At (ns)	Jitter (ns)
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Tcl Command Preview (1)

Existing Create Clock Constraints (0)

create_clock -period 10.000 -name sys_clk -waveform {0.000 5.000} [get_ports {sys_clk}]

?

<Back

Next >

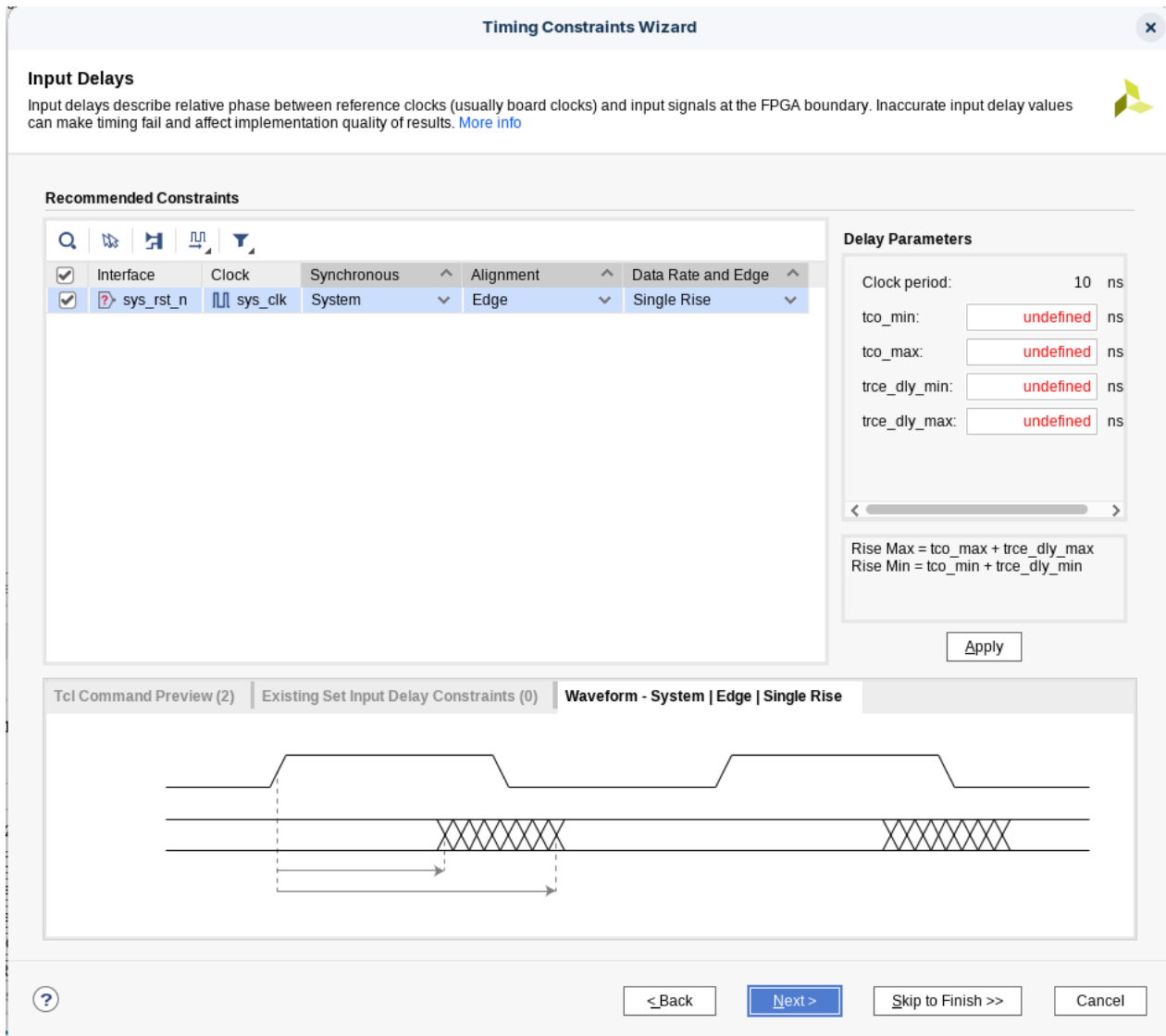
Skip to Finish >>

Cancel

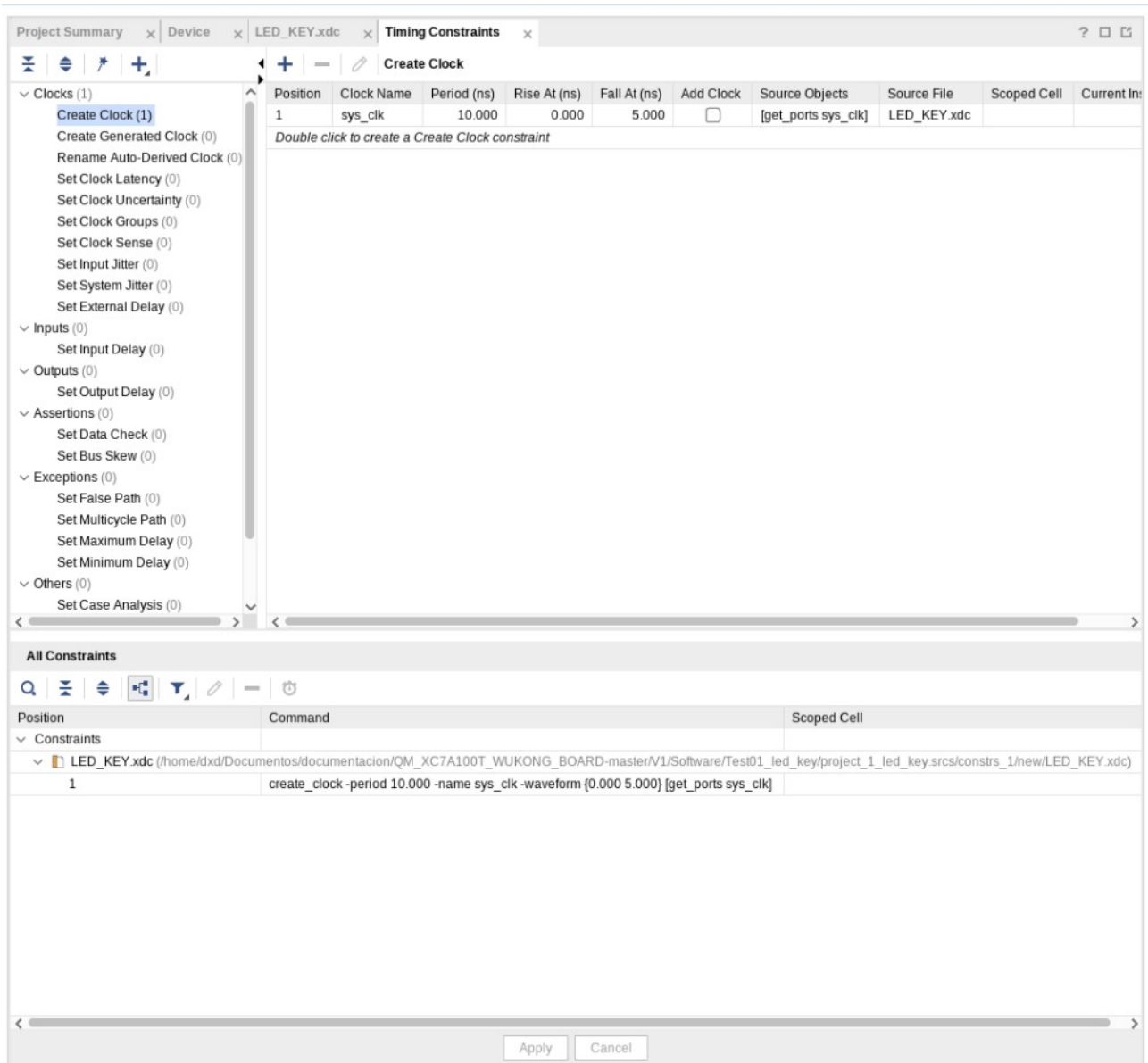
It also allows you to add delays to the clock, although it is not necessary to give it delays.

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Once done in Timing Constraints the created clock will appear



And in the XDC the clock that has been created will appear

```
13 |
14 | create_clock -period 10.000 -name sys_clk -waveform {0.000 5.000} [get_ports sys_clk]
15 |
```