

XCELLE

Issue 10
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THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS



The Programmable Logic CompanySM

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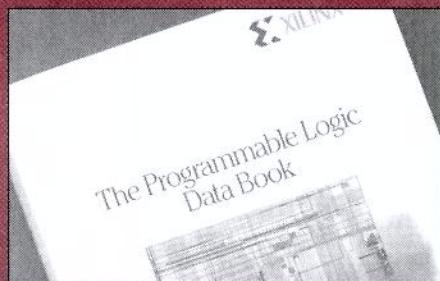
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GENERAL FEATURES



1993 Data Book Available

Everything you ever wanted to know about Xilinx products and much, much more...

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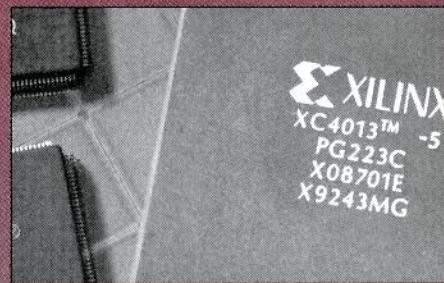
PRODUCT INFORMATION

New Product:

The XC4013

Xilinx creates world's highest-capacity FPGA with 576 Configurable Logic Blocks...

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DEVELOPMENT SYSTEMS



CD-ROM

Power

Soon all Xilinx development system software will be available on CD-ROM...

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DESIGN TIPS & HINTS

XC4000 Timing Parameters

Tips on determining pin-to-pin timing parameters for the XC4000 family...

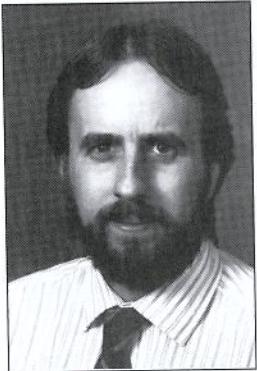
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Welcome to The New XCELL

By BRADLY FAWCETT ♦ Editor

As you may have noticed, the *XCELL* newsletter has taken on a new look starting with this issue. This new look reflects a renewed commitment to provide you, our customers, with the latest information regarding Xilinx products and their applications.



First and foremost, *XCELL* will continue to include "application-oriented" articles describing design techniques and helpful hints that aid you in getting the most

out of Xilinx technology. For example, articles in this issue show how to embed ROMs within XC3000 series designs, discuss XC4000 timing parameters, and provide guidelines for clocking asynchronous data. A new regular column contains questions and answers selected from the queries that we receive on our "applications hotline."

In response to your requests, we have expanded our coverage of new product introductions. The pace of innovation continues to accelerate here at Xilinx. In the past several months, we have introduced more new IC products than our cumulative total over Xilinx's first seven years! Several new devices are described in this issue, including the XC4013 (the world's highest-capacity FPGA), higher-speed versions of the XC4000 FPGA family, the architecturally-enhanced XC3000A family,

and the new XC7336 CPLD.

Additions to our development system product line also will be highlighted; this issue focuses on products supporting high-level logic synthesis.

Items of general interest about Xilinx and the programmable logic market will be included regularly in *XCELL*, such as listings of available literature and products, news of upcoming conferences, and, for the fiscally-minded, a summary of the previous quarter's financial results. We also will highlight the company's strategies and directions with "guest editorials." This

“*XCELL* will continue to include “application-oriented articles” describing design techniques and helpful hints that aid you in getting the most out of Xilinx technology.”

issue features an article about FPGA component costs by **Bernie Vonderschmitt**, founder and President of Xilinx.

Each issue of *XCELL* is directed toward Xilinx's most important asset -- you. Simply put, the information here is intended to help you use Xilinx products. Please let us know how we're doing by sending in your comments and suggestions. You can contact us

Continued on the next page

XCELL

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XILINX®

FROM THE FAWCETT

Continued from the previous page

by mail, telephone, FAX, or electronic mail (via Internet). Consider using the FAX-back form in this newsletter. We're looking forward to hearing from you. Perhaps we may be able to add a "Letters to the Editor" column!

PLD Design Conference

It's time to start thinking about next year's PLD Design Conference (*San Jose Convention Center, April 11-13, 1994*). Sponsored by CMP Publications, the publisher of *EE Times* magazine, this is the industry's largest conference dealing exclusively with programmable logic and its applications. This conference is an excellent chance to gain recognition from your peers by submitting papers about your EPLD and FPGA design experiences. Abstracts are due by Oct. 22. If you have an interesting topic or application you would like to present, but lack the skills or resources to prepare an abstract and/or manuscript, please contact us as soon as possible. We'll try to help. We would love to see a good showing of leading-edge, Xilinx-based designs at the conference.

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If this newsletter is not addressed to you and you would like to get on the mailing list, please fill out and FAX or mail the form in the back of this issue. ♦

FROM THE PRESIDENT**Why FPGAs are Cost-Effective**

By Bernie Vonderschmitt

President, Xilinx, Inc.

The same economics that created the burgeoning FPGA market nine years ago still exist today, only in spades. Time-to-market pressures are greater, product life spans are shorter, design complexity is higher and costs must be driven lower. Reducing the cost of FPGA devices is a primary mission at Xilinx as it represents the greatest opportunity for growth.

FPGAs often are viewed as a high-cost solution when, in fact, increased unit volume, submicron technology and new architectures have enabled FPGA suppliers to reduce costs by 30 percent per year over the past five years. These savings have subsequently been passed along to the customer and, as a result, FPGAs have been used in increasingly higher volumes at the expense of gate arrays.

Dataquest, a San Jose, CA market research firm, believes that the choice of an FPGA solution may increase margin dollars by more than 25 percent over those attainable with a masked gate array solution. This is based



Continued on the next page

FROM THE PRESIDENT

Continued from the previous page

on a model using a 6,000 gate device in a system with 5,000 units shipped per month over a 12-month market window. Gate arrays can take at least three months to reach production status once the final design is completed and prototyped. Because FPGA-based systems can be introduced to market first, the systems manufacturer is able to achieve higher prices and product margins before competition enters the market.

Illustrating this point is the accelerating abandonment by gate array suppliers of the low end of this market. About one third of U.S. CMOS ASIC designs are less than 10,000 gates, a density level achievable with today's FPGA devices.

However, the 80/20 rule applies to the distribution curve of total unit production; 80 percent of the total unit volume is represented by the 20 percent of designs that are produced in the highest volume. Many of these ASIC

designs that are not the highest-volume business are a money losing area for gate array suppliers and an obvious target for FPGA technology. FPGA suppliers are actually doing gate array vendors a favor by enabling them to concentrate on more profitable business.

Confusing this issue is the obvious disparity in prices between various FPGAs. The highest-density, highest-speed FPGAs can cost hundreds of dollars at introduction. The lowest-speed, lower-density FPGAs can cost only a few dollars. New process technology, higher volumes and more efficient FPGA architectures are driving the cost of FPGAs down rap-

idly. In 1986, Xilinx introduced its first product, the XC2064, on a 2.0 μ CMOS process using four-inch wafers. Volume pricing was about \$35. Seven years later, the same device is now manufactured on a 0.8 μ process with six-inch wafers and prices closer to \$4 in volume quantities, representing almost a tenfold price reduction over this period. Process miniaturization, coupled with the introduction of more-efficient architectures will drive the high-density devices (e.g. the XC4000 family) to achieve a tenfold reduction in a reduced period of only about five years.

Leading-edge FPGAs are expected to be in production on 0.6 μ processes and below beginning in 1994, further driving down the cost of FPGAs and, more importantly, reducing the price gap with gate arrays. Some argue that gate arrays will go down the same cost curves and, therefore, will hold onto their price edge. Unfortunately for the gate array suppliers, this will not happen because gate arrays already have a small die size; less than 20 percent of total product cost can be attributed to silicon area in a typical gate array. The remainder is assembly/packaging/test and overhead costs. For typical FPGAs, the silicon portion represents up to 80 percent of the total product cost. As FPGAs move to smaller process geometries to reduce silicon area, FPGAs will get a larger percentage cost reduction than gate arrays. In this regard, the relative disparity in silicon area gives FPGAs a distinct built-in advantage. This will allow a greater number of designers to realize the many benefits of FPGAs and put further pressure on the viability of the lower-density segment of the CMOS gate array business. ♦

**“FPGAs
will get a larger
percentage cost
reduction than
gate arrays.”**

Semaphore Simplifies Design Cycle By Targeting VHDL Design to Xilinx FPGAs

Logic design using a Hardware Description Language (HDL) is rapidly gaining acceptance in the engineering community. As a method of design entry, an industry-standard HDL offers high productivity and technology-independence. Because FPGAs can condense large designs into a small area while providing a very efficient development and debug environment, they are a logical implementation choice.

Semaphore Communications (Santa Clara, CA), a Xerox Company, completed a design that was entered entirely in VHDL and targeted to Xilinx FPGAs. Semaphore manufactures the Network Security System, which provides end-to-end data protection on both local and wide area networks, and consists of a RISC processor and two Xilinx XC4005 FPGAs. The processor controls an encryption process while the FPGAs are used to interface to the processor and data paths.

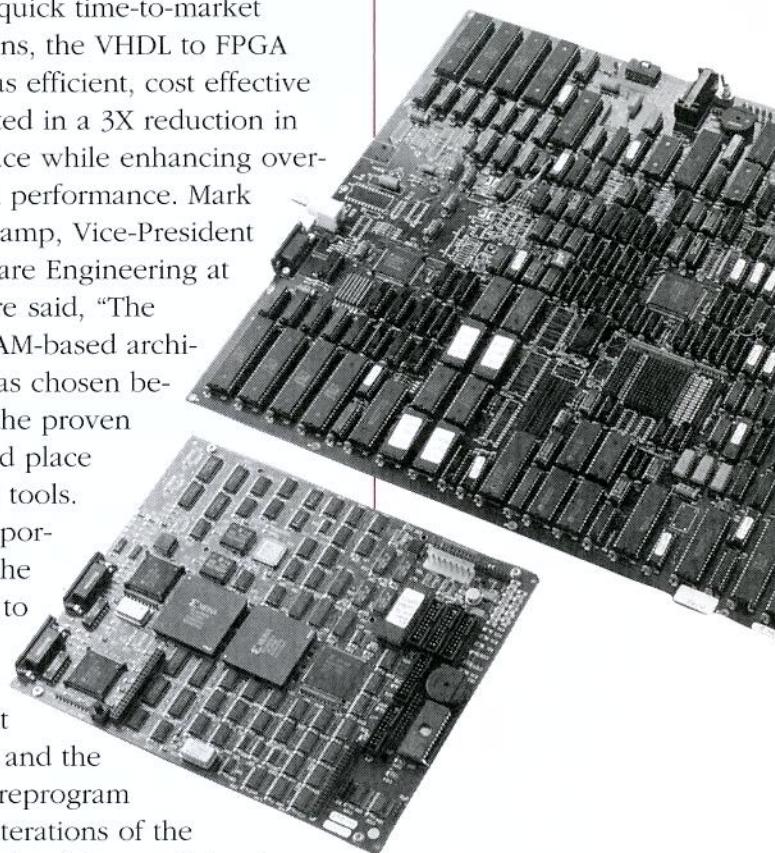
A prototype circuit board was designed using numerous SSI/MSI and PLD devices. The logic was described using PGA Designer from MINC (Colorado Springs, CO). After proving the product concept, the board needed to be redesigned into a smaller form factor before beta testing. Xilinx FPGAs accomplished this task.

For the new board design, Semaphore chose a tool set from Viewlogic Systems (Marlboro, MA) that provided a tightly-integrated design environment at a cost-effective price. After translating the first

version of the board design into VHDL at the register transfer level, a top level schematic containing VHDL modules was developed for each FPGA. Viewlogic's VHDL interface converted the design into a schematic file that was then compiled using Xilinx FPGA software.

Because FPGAs are ideally suited to quick time-to-market applications, the VHDL to FPGA design was efficient, cost effective and resulted in a 3X reduction in board space while enhancing overall system performance. Mark Vondemkamp, Vice-President of Hardware Engineering at Semaphore said, "The Xilinx SRAM-based architecture was chosen because of the proven silicon and place and route tools. Just as important was the flexibility to use non-proprietary front end tools and the ability to reprogram different iterations of the design in the debug and development environment."

The product is now in the final beta site test phase. Within the time constraints of the project, the combination of VHDL and FPGAs proved very successful for Semaphore Communications. *If you are interested in having your company featured in a future issue of XCELL, please fill out and FAX the form in the back of this newsletter.* ♦



Xilinx Literature

Get the latest information on Xilinx products and services through our extensive library of product literature. A selection of product overviews, databooks and white papers is listed below with the newest items in *italics*. To order, please contact your local Xilinx sales representative.

Title	Description	Part Number
Overview Pieces		
• Product Description and Selection Guide #0010130	Xilinx product overview	
• <i>1993 Databook</i> #0401096	Technical data on FPGAs, EPLDs, PROMs, development systems, application notes	
• <i>A Systems Perspective on Interpreting</i> #0010171 <i>the PREP™ benchmarks</i>	White paper	
• University Information Guide #0010168	University program description	
• Xilinx Training Schedule and Brochure #0010134	Training course description	
• Xilinx 1993 Annual Report	Yearly financial report	#100066
XC3000/XC3100 FPGAs		
• XC3000A FPGA family data sheet	Technical data	#0010163
• XC3100 FPGA family overview	Features/benefits	#0010155
• XC3100 Performance Benchmarks	White paper	#0010152
XC4000 FPGAs		
• XC4000 FPGA family overview	Features/benefits	#0010137
• XC4000H FPGA family overview	Features/benefits	#0010156
FPGAs - General		
• <i>ZERO+ Family Data Sheet</i>	Technical data	#0010165
EPLDs		
• XC7200 Family overview	Features/benefits	#0010144
• XC7300 Family overview	Features/benefits	#0010164
• <i>PAL Conversion Guide</i>	Technical data	#0401077
HardWire Gate Array		
• HardWire Gate Array overview	Features/benefits	#0010124
• HardWire Gate Array databook	Technical data	#0010064
Military		
• Xilinx FPGAs: The Ideal Logic Device For Military Multichip Modules & Hybrids	Features/benefits	#0010111
• Xilinx FPGAs: The Ideal Logic Device For Military Applications	Features/benefits	#0010071
Packaging		
• <i>Plastic Surface Mount Packaging overview</i>	Features/benefits	#0010169
• TQFP overview	Features/benefits	#0010136
Development Systems		
• <i>Base Development System overview</i>	Features/benefits	#0010154
• XACT Development System overview	Features/benefits	#0010101
• X-BLOX Module Synthesis overview	Features/benefits	#0010107
• Xilinx ABEL overview	Features/benefits	#0010116
• Designing Xilinx FPGAs and EPLDs with OrCAD	Features/benefits	#0010135
• Designing Xilinx FPGAs with Mentor Graphics	Features/benefits	#0010067
• Designing Xilinx FPGAs with Synopsys	Features/benefits	#0010145
• Designing Xilinx FPGAs with Viewlogic	Features/benefits	#0010066

1993 Xilinx Data Book Available

The 600-page *1993 Xilinx Data Book* combines detailed product information about *all* Xilinx devices: FPGAs, EPLDs and Serial PROMs. The electrical and timing parameters for the various subfamilies (XC4000A, XC4000H, XC3000A, XC3000L, XC2000L) are clearly separated.

The package information now has its own chapter.

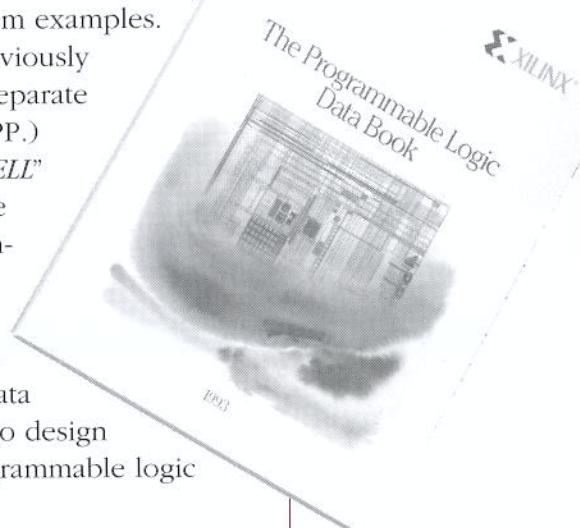
We have improved the organization, grouped related topics better, and provided extensive cross-references. Military data was deleted, and will be covered in a separate book.

Some AC timing parameters for the XC4000-4, XC3000A, XC3000L and XC2000L families were not yet available when the book went to

press in July '93. There are 160 pages of detailed applications information, from general design hints to completely documented subsystem examples. (These were previously published in a separate book called XAPP.) "The Best of XCELL" and an extensive index are also included.

We hope that this comprehensive source of data makes it easier to design with Xilinx programmable logic devices.

For copies of the 1993 Xilinx Data Book, contact your local sales representative. ♦



RECORD REVENUE IN FIRST HALF OF 1993

Good Customers + Good Products = Financial Success

Thanks to our customers, Xilinx Inc. continues to enjoy excellent financial results, reflecting the strength of our product line and the continued growth of the programmable logic market. For the quarter ending July 3, 1993, Xilinx's sales revenues were a record \$54.4 million, an increase of eight percent from the previous quarter and 39 percent from the same quarter last year.

Fiscal 1993 marked another year of substantial progress for Xilinx. (Our fiscal year runs from April 1 to March 30; thus, the current quarter (July - September, 1993) is actually the 2nd quarter of fiscal year 1994.) In fiscal 1993 (ending March 30, 1993), Xilinx achieved \$178 million in sales revenues, up 31 percent from the previous year.

Since our founding in 1984, Xilinx has shipped more than 20 million programmable logic ICs and more than 15,000 development systems to electronic equipment suppliers worldwide. We have grown to become the world's leading supplier of CMOS programmable logic. ♦

COMPONENT AVAILABILITY CHART - AUGUST 1993

◆ = Product currently shipping or planned

XILINX RELEASED SOFTWARE STATUS - AUGUST 1993

PRODUCT CATEGORY	PRODUCT DESCRIPTION	PRODUCT FUNCTION	XILINX PART NUMBER	LAST VER. REL.	PLATFORM					LAST UPDATE
					PC1 3.30	NC2 3.30	SN2 4.1.x	AP1 10.4	HP7 9.01	
XILINX INDIVIDUAL PRODUCTS										
CORE FPGA	XC2,3,4K SUPPORT	CORE IMPLEMENTATION	DS-502-XXX	1.41	1.42	1.42	1.42	1.42	1.42	07/93
CORE EPLD	XC7K SUPPORT	CORE IMPLEMENTATION	DS-550-XXX	3.10	4.00		4.00			08/93
MENTOR ¹	V7.00	I/F AND LIBRARIES	DS-343-XXX	4.00				4.10		02/93
MENTOR ¹	V8.20	I/F AND LIBRARIES	DS-344-XXX	1.00			1.10	1.10	1.10	07/93
OrCAD ²		I/F AND LIBRARIES	DS-35-XXX	4.22A	4.23	4.20				06/93
SYNOPSYS ¹		I/F AND LIBRARIES	DS-401-XXX	2.00			3.01	3.01	3.01	09/93
VIEWLOGIC ²	VIEWDRAW	I/F AND LIBRARIES	DS-390-XXX	4.14	4.15					06/93
VIEWLOGIC ²	VIEWSIM	I/F AND LIBRARIES	DS-290-XXX	4.14	4.15					06/93
VIEWLOGIC ²		I/F AND LIBRARIES	DS-391-XXX	4.14	4.15		5.01			06/93
XABEL ²		ENTRY, SIM, LIB, OPT.	DS-371-XXX	1.01	1.03					10/92
X-BLOX ¹		ARCHITECTURAL SYNTHESIS	DS-380-XXX	1.03	1.04	1.04	1.04	1.04	1.04	10/92
XILINX PACKAGES										
MENTOR 8	STANDARD		DS-MN8-STD-XXX	1.00			1.10	1.10	1.10	07/93
MENTOR 8	EXTENDED		DS-MN8-EXT-XXX	1.00			1.10	1.10	1.10	07/93
MENTOR 7	STANDARD		DS-MN7-STD-XXX	1.00				1.10		07/93
MENTOR 7	EXTENDED		DS-MN7-EXT-XXX	1.00				1.10		07/93
OrCAD	BASE		DS-OR-BAS-XXX	1.01	1.10					07/93
OrCAD	STANDARD		DS-OR-STD-XXX	1.01	1.10					07/93
SYNOPSYS	STANDARD		DS-SY-STD-XXX	1.00			1.10	1.10	1.10	09/93
VIEWLOGIC	BASE		DS-VL-BAS-XXX		1.10	1.10				07/93
VIEWLOGIC	STANDARD		DS-VL-STD-XXX		1.10	1.10				07/93
VIEWLOGIC	EXTENDED		DS-VL-EXT-XXX		1.10	1.10				07/93
VIEWLOGIC/S	BASE		DS-VLS-BAS-XXX		1.10					08/93
VIEWLOGIC/S	STANDARD		DS-VLS-STD-XXX		1.10					08/93
VIEWLOGIC/S	EXTENDED		DS-VLS-EXT-XXX		1.10					08/93
XILINX HARDWARE										
PROM PGMR.	CONF. PROM. PGMR.	SOFTWARE	HW-112	3.30	3.31					04/93
PROGRAMMER	CONF. PGMR.		HW-120	3.14						
THIRD PARTY PRODUCTION SOFTWARE VERSIONS										
CADENCE	COMPOSER	SCHEMATIC ENTRY	N/A				4.20	4.20	4.20	N/A
CADENCE	VERILOG	SIMULATION	N/A				1.60	1.60	1.60	N/A
CADENCE (VALID)	CONCEPT	SCHEMATIC ENTRY	N/A				1.50			N/A
CADENCE (VALID)	RAPIDSIM	SIMULATION	N/A				1.50			N/A
MENTOR	NETED	SCHEMATIC ENTRY	N/A					7.XX		N/A
MENTOR	QUICKSIM	SIMULATION	N/A					7.XX		N/A
MENTOR	DESIGN ARCHITECT	SCHEMATIC ENTRY	N/A	8.10			8.20	8.20	8.20	N/A
MENTOR	QUICKSIM	SIMULATION	N/A	8.10			8.20	8.20	8.20	N/A
OrCAD	STD	SCHEMATIC ENTRY	N/A		4.00	4.00				N/A
OrCAD	VST	SIMULATION	N/A		4.00	4.00				N/A
OrCAD	STD 386+	SCHEMATIC ENTRY	N/A		1.00					N/A
OrCAD	VST 386+	SIMULATION	N/A		1.00					N/A
SYNOPSYS	FPGA/DESIGN COMP.	SYNTHESIS	N/A	2.2B			3.00b	3.00b	3.00b	N/A
VIEWLOGIC	VIEWDRAW	SCHEMATIC ENTRY	N/A		4.00	4.00	5.00			N/A
VIEWLOGIC	VIEWSIM	SIMULATION	N/A		4.00	4.00	5.00			N/A
XABEL	ABEL COMPILER	ENTRY AND SIMULATION	N/A		4.12		4.12			N/A

NOTE: ¹FPGA Only ²FPGA and EPLD

Xilinx Presents Technical Papers at Industry Forums

Look for information on the newest Xilinx products at the following industry conferences.

International Workshop on Field Programmable Logic

September 8-10

University of Oxford, Oxford, UK

The third in a series of annual workshops, this conference brings together designers from around the world. Xilinx engineers will be presenting three papers at this year's event.

Wescon

September 28-30

San Francisco, CA

Moscone Convention Center

This year's Wescon technical program includes several sessions on the newest developments in programmable logic devices and software. Xilinx will participate in three sessions:

Tuesday, September 28

Session 4: 9:30 - 11:30 a.m.

*"The State-of-the-Art" in Digital Logic
Simulation*

Wednesday, September 29

Session 13: 12:30-2:30 p.m.

*"SRAM-Based Field Programmable
Gate Arrays"*

Wednesday, September 29

Session 19: 3 - 5 p.m.

*"Complex Programmable Logic
Devices"*

IDEA '93

September 28-30

San Francisco, CA

Moscone Convention Center

Co-located with Wescon, the IDEA '93 technical program is oriented toward applications of programmable logic, ASIC devices and EDA tools. Xilinx will participate in the following technical session:

Thursday, September 30

2 - 3 p.m.

"Applications of Reconfigurable Logic"

Call for Papers:

PLD Design Conference

April 11-13, 1994

San Jose, CA

San Jose Convention Center

The "Call for Papers" for 1994's Fourth Annual PLD Design Conference should be issued by the time this newsletter is mailed. Abstracts are due on October 22, 1993, and, if accepted, completed papers will be due February 27, 1994. Designers with compelling success stories or interesting applications involving the use of programmable logic are encouraged to submit papers to the industry's largest conference dedicated to PLD technology.

Please contact Jan Houts or Brad Fawcett if you would like to receive a copy of the official "Call for Papers," or if you require assistance preparing your abstract or manuscript.

For more information on these events, contact Jan Houts:
Telephone (408) 879-5164
FAX (408) 879-4676 ♦

Schedule of Training Classes for Products Now Available

Xilinx Training Classes allow you to get up-to-speed on the latest Xilinx products quickly and efficiently. Xilinx offers a variety of classes worldwide; we also can bring classes to your own facility. Early enrollment is advised. For a list of the classes planned in the U.S. for the remainder of 1993 or more information, please contact **Candace Blackwell** (Telephone 408-879-5090; FAX 408-879-4676) or your local Xilinx Sales Office. ♦

The XC4013™ FPGA:

The World's Highest Capacity PLD

Xilinx continues to set records in density for FPGAs with the introduction of the XC4013 device this past spring. The XC4013 is the newest addition to Xilinx's third generation XC4000 family, and features 576 Configurable Logic Blocks (an increase of 44 percent over the XC4010™) in a 24 by 24 array, and 192 I/O Blocks.

The XC4013 FPGA delivers more than 13,000 usable gates for logic-only designs. A memory-intensive design that uses 11 percent of the CLBs' function generators as memory cells (2K bits of embedded RAM) and the remaining CLBs for logic would achieve the equivalent of 20,000 gates. Measurements by the industry standard PREP™ benchmarks reveal that the XC4013 FPGA is up to 60 percent larger in density than any other previously available programmable logic device, achieving an average of 53 instances over the nine benchmarks (*see table*).

The XC4013 FPGA is available now in pin grid array and quad flat



pack packages. It is expected to follow the same cost curves as Xilinx's XC4010 and XC3090®. The XC3090 has dropped in price by more than 70 percent since 1989. The XC4013 has already dropped in price by 50 percent in its first year of production. Process enhancements are underway that will allow Xilinx to deliver a 20,000 gate device by early 1994. ♦

BENCHMARK	NUMBER OF INSTANCES	
	XC4010	XC4013
1. Datapath*	30	48
2. Timer/Counter	30	48
3. Small State Machine	36	52
4. Large State Machine	15	22
5. Multiply/Accumulator	25	36
6. 16-bit Accumulator	50	72
7. 16-bit Counter	40	72
8. 16-bit Prescaled Counter	40	72
9. Memory Map*	40	57

*Fully Implemented



PRELIMINARY,
UNCERTIFIED. XC4013
data is not certified by
PREP, but is derived
according to PREP PLD
Benchmark Suite #1, Ver-
sion 1.2, dated 3/28/93.

XILINX

NEW PRODUCT PREVIEW

XC4000-4 Specifications Available Now

In response to market demand for faster XC4000 devices, Xilinx has made enhancements to the 0.8µm process that will allow delivery of a new speed grade, the XC4000-4. For early evaluation of this new speed grade, designers can reference the advance information specifications printed in the 1993 Data Book. Limited quantities of the XC4005-4 are available now.

For more information about XC4000-4 product availability and a preliminary speeds file, please contact your local Xilinx sales office. ♦

Timing Parameter Description	-6	-5	-4
Combinatorial Delay (T_{ILO})	6.0	4.5	4.0
Combinatorial Delay (with H function generator)	8.0	7.0	6.0
Pad to Direct In	4.0	3.0	2.8
Clock to Pad, Output (Fast slew rate)	7.5	7.0	6.5
Wide Edge Decoders	10.0	9.0	6.0

Example worst case timing parameters in nanoseconds for three XC4000 speed grades

D-Series PROMs Offered In Three Versions

Xilinx's new D-Series Serial Configuration PROMs are now available in three versions: the XC1718D™, the XC1736D™ and the XC1765D™. These products replace the existing XC1736A™ and XC1765™ and deliver three significant benefits: lower cost devices, improved ESD protection, and a new, small surface-mount packaging option.

The D-series also adds a new, lower-density device -- the XC1718D. This device provides enough memory to configure a single XC2064®, XC2018™ or XC3020™, and is available at a lower price than any previous serial configuration PROM. Combined with low-cost Xilinx FPGAs, you can now get all the benefits of FPGAs in even the most cost-sensitive applications.

The ESD (electrostatic discharge) protection circuitry on the D-series is significantly improved, providing protection to more than 8,000 volts per pin. Good ESD protection is especially important on a PROM, since they are subjected to extra handling while being inserted into a device programmer.

All of these new devices are now available in the thin, space-saving SO8 small outline package. This package has the same pin-out as the 8-pin DIP package, but is about one-half the length, one-half the width, and one-third the height. The SO8 package is only 1.4 mm. thick, and is an excellent choice to use in space- and height-restricted applications (such as PCMCIA cards), along with Xilinx FPGAs offered in the new TQFP and VQFP packages.

The new PROMs can be programmed on a wide variety of device programmers, including the Xilinx DS112, as well as programmers from Data I/O, Advin, BP Microsystems, Link, Red Square, SMS and many other programmer manufacturers. ♦

New Device Breaks the XC3x00 Density Ceiling

Featuring a 22-by-22 array of configurable logic blocks (CLBs) and 176 user-defined I/O Blocks (IOBs), the XC3195™ sets a new standard for XC3x00 family logic capacity. The XC3195 is available in six different packages and three speed grades.

The new XC3195 FPGA is:

- the fastest device in production at this density level (~7000 usable gates).
- a cost-effective high-density alternative to the XC4000 family, when the XC4000 architecture's system-level features are not required.
- the ideal density migration path for XC3090® and XC3190™ designs.
- ideal for I/O intensive designs, with 176 available I/O.
- available in six package options, four of which are pin-compatible with the XC3090 and XC3190.

The XC3195 has 50 percent more CLBs than either a XC3090 or XC3190. This larger array allows for a significantly higher logic capacity. Conservative estimates (pending the completion of XC3195 PREP™ benchmarks) indicate that the XC3195 has more than 35 percent more logic capacity than the XC3x90.

The XC3195 FPGA is ideal for experienced XC3000 or XC3100 users who need additional device density or I/O capability.

Footprint and pin-out compatible with the XC3190 and XC3090 for packages up through 175 pins, the XC3195 can be dropped into a XC3x90 socket with no board redesign.

The XC3195 is shipping now in three speed grades and six different packages. ♦

XC3195 Package	Usable I/Os	Footprint Compatible with XC3x90
PC84 - 84-pin plastic leaded chip carrier	70	YES
PQ160 - 160-pin plastic quad flat pack	138	YES
PG/PP175 - 175-pin ceramic/plastic pin grid array	144	YES
PQ208 - 208-pin plastic quad flat pack	176	NO
PG223 - 223-pin plastic pin grid array	176	NO

	XC3190	XC3195	Diff.
CLBs	320	484	+50%
I/Os	144	176	+22%
Flip-flops	928	1,320	+42%
Horizontal longlines	40	44	+10%
TBUFs per Horizontal Long Line	17	23	+35%
Packages	PC84, PQ160, PP175, PG175, PQ208	Same as XC3x90 plus PG223	

Standard Military Drawings (SMDs) Available for XC4000 FPGAs

Xilinx is now offering the XC4010™ and the XC4005® FPGAs as Standardized Military Drawings (SMDs). Both products conform to MIL-STD-883 Class B processing requirements and the "one part -- one part number" system that was recently established by the Defense Electronics Supply Center (DESC), and both are available now in two speed grades and two ceramic packages. ♦

Xilinx Part Number	SMD Number
XC4005-10PG156B	5962-9225201MXX
XC4005-10CB164B	5962-9225201MZX
XC4005-6PG156B	5962-9225202MXX
XC4005-6CB164B	5962-9225202MZX

Xilinx Part Number	SMD Number
XC4010-10PG191B	5962-9230501MXX
XC4010-10CB196B	5962-9230501MZX
XC4010-6PG191B	5962-9230502MXX
XC4010-6CB196B	5962-9230502MZX

New XC3000A Family Delivers Enhanced Features

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“The XC3000A devices offer new features and improved routability for new designs, as well as significant production benefits as XC3000 replacements.”

As part of our strategy to constantly improve our current product offerings, Xilinx has introduced the XC3000A family of FPGAs, an evolutionary improvement upon the popular XC3000 family. The XC3000A devices offer new features and improved routability for new designs, as well as significant production benefits as XC3000 replacements.

New Design Benefits

XC3000A enhances the usability and efficiency of the XC3000 architecture in new designs.

- Improved routing resources allowed easier connection between the output of IOBs and CLBs to the internal three-state buffers (TBUFs). Also, improved access is provided from long line routing resources to both TBUFs and the CLB's Clock Enable input. In bus oriented designs, these changes can increase available local interconnect resources by up to 40 percent.
- Optimized Automatic Placement and Routing (APR) algorithms better utilize these new resources, resulting in more routable designs overall.

Additionally, with the XACT V® release coming later this year, two more software products will support XC3000A architecture. The new XACT-Performance™ software will offer schematic-level performance predictability. The new X-BLOX™ software will offer improved design entry ease-of-use along with more

optimized placement implementations.

- Up to 10 percent higher performance than the equivalent XC3000 devices is obtained through our advanced 0.8µ CMOS process.

Existing Design Benefits

The XC3000A Family offers a number of significant production benefits over the current XC3000 family. By providing footprint, package, density and bitstream compatibility with the XC3000 family, you can take full advantage of all these benefits at no additional cost.

- Over 50 percent more ESD protection is realized through enhanced I/O structures and other circuit modifications.
- A bitstream error-checking feature verifies the locations of stop bits in the bitstream, offering an extra level of assurance during device programming. (*See related article, page 26.*)
- Lower ground bounce at system power-up is achieved through “Soft Start-up.” This feature activates all IC outputs in slew rate-limited mode to avoid excessive ground bounce, and then allows the outputs to adopt the user-defined slew rate option.
- A 25 percent reduction in power dissipation compared with the 1.0µ XC3000 device is realized due to the smaller geometry of the XC3000A devices. A software update is available on request for implementing new XC3000A designs. (Order #ES3KA).

Please contact your local Xilinx sales representative or Field Applications Engineer for further information, samples, datasheets and the development system update. ♦

ZERO+ Family Delivers Low Power Logic

The ZERO+ family is a complete line of 3.3-Volt FPGAs which combine ultra-low power dissipation, advanced packaging, a wide range of densities, and all of the established benefits of Xilinx programmable logic. The ZERO+ family is an ideal solution for leading-edge designs requiring very low power consumption and 3.3-Volt operation.

The ZERO+ line consists of the XC2000L, XC3000L, and XC1700L families. They have the same device densities, pin-outs, features, and design methodology as the XC2000, XC3000A and XC1700 families, but are designed for low power operation at 3.3 Volts.

10µA Standby Power

The ZERO+ name derives from the fact that the parts consume nearly zero power in standby

	XC2000	XC2000L	XC3000A	XC3000L
Quiescent current (I_{CC0})	5 mA	20 µA	500 µA	20 µA
Powerdown (I_{CCPD})	500 µA	10 µA	50 µA	10 µA

mode. The CMOS SRAM-based technology of Xilinx FPGAs already delivers operating power consumption lower than any other programmable logic technology, and the ZERO+ family was designed to add even further power conservation.

Very low operating power

Based on the typical elements of LCA power consumption, the ZERO+ family can reduce power consumption by as much as 69 percent from comparable 5-Volt devices. Power savings over other programmable logic technologies will be even greater. Consult the *Xilinx Programmable Gate Array Data Book* (pp. 2-27, 2-28, and 6-10) for details on the usage of these figures and general FPGA power calculation methods. ♦

Power Dissipation (mW/MHz)

	XC3042 (@5V)	XC3042A (@5V)	XC3042L (@3.3V)
One CLB driving three local interconnects	0.25	0.17	0.07
One global clock buffer and clock line	2.25	1.40	0.50
One device output with a 50 pF load	1.40	1.40	0.70

Design Example

	XC3042 (@5V)	XC3042A (@5V)	XC3042L (@3.3V)
Three outputs at 5 MHz	21.0	21.0	10.5
20 outputs at 0.1 MHz	2.8	2.8	1.4
Global clock at 20 MHz	45.0	28.0	10.0
10 CLBs at 5 MHz	12.5	8.5	3.5
40 CLBs at 0.2 MHz	2.0	1.4	0.6

XC3042A power savings over XC3042 26%

XC3042L power savings over XC3042A 58%

XC3042L power savings over XC3042 69%

The XC7300 Family: The Best Solution for PAL® Conversion

The XC7300 family was developed as the second generation of EPLD products from Xilinx. Containing an innovative new architecture called Dual Block™, this product family addresses the need for high performance and high density in a single complex programmable logic device. The combination of PAL-like architecture and software that directly translates industry-standard PAL equations and descriptions to an EPLD

provide maximum logic density and system-level features to implement complex functions with predictable timing for adders and accumulators, wide functions and state machines requiring large numbers of product terms.

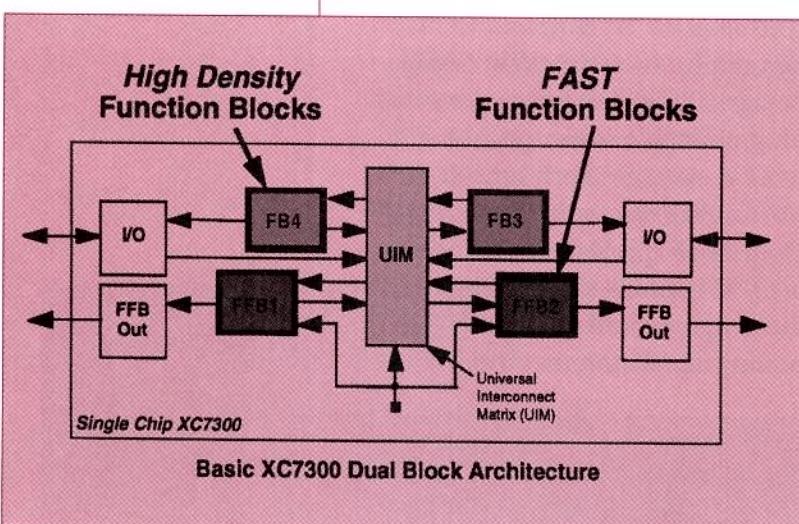
In addition to FFBs and HDFBs, the XC7300 architecture employs 100 percent routing capability through the patented Universal Interconnect Matrix (UIM™). This means that *any* UIM input (coming from a function block or from a chip pin) can be programmed to connect to *any* UIM output (which are connected to function block inputs).

The delay through the interconnect is constant regardless of the apparent routing distance and complexity, as well as fan-out or fan-in. Constant interconnect delays simplify device timing and guarantee design performance regardless of logic placement within the chip.

This guaranteed routing capability delivers up to 100 percent logic utilization of on-chip resources, the highest usable logic of any complex PLD today. Based on switch matrix limitations, other EPLD suppliers only claim 70-80 percent utilization.

The XC7300 family contains a number of unique system features that provide a clear upgrade path for PAL designers:

- 3.3 volt I/O allows direct interface to 3.3 and 5 volt devices without performance degradation



provides the best solution for customers interested in converting multiple PALs into a complex PLD.

The Dual Block architecture allows designers to take advantage of high-speed paths when required, without sacrificing the ability to also implement complex functions and without giving up timing predictability. Fast Function Blocks (FFBs) provide fast pin-to-pin speed and logic throughput for critical decoding of ultra-fast state machine applications. High Density Function Blocks (HDFBs)

- Each macrocell contains a dedicated Arithmetic Logic Unit (ALU) and fast carry logic for maximum performance of arithmetic functions and logical comparison.
- Input latches and registers are included to provide additional registered storage and synchronization of input signals.
- Programmable power management allows you to specify high-performance or low-power operation on a macrocell-by-macrocell basis.

The XC7336™ consists of only FFBs for ultra high-speed applications, and does not include ALUs or input registers.

The XC7300 family spans a broad range of densities, speeds, and packaging options. Total pin-counts range from 44 to 184 pins and the number of function blocks range from four to 16. In addition, the larger XC7300 devices provide footprint compatibility, a unique feature in complex PLDs. This feature allows easy upward migration among parts while maintaining the same package and pin-out.

The XC7300 family is supported by the Xilinx EPLD Translator (XEPLD™) software. XEPLD is

designed to work with industry standard PAL logic compilers and languages such as ABEL, CUPL and PALASM and offers an efficient and easy path to convert multiple PALs

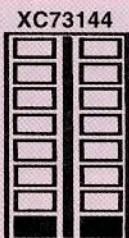
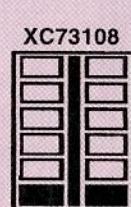
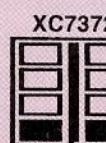
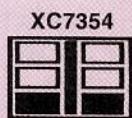
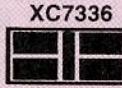
into a single high-density EPLD. A design using PALs such as 22V10s and 20V8s can be imported and directly converted with XEPLD acting as an automatic partitioner and fitter, taking the design description and mapping it into the chosen EPLD. This lets the designer concentrate on the functionality of the design, not its physical implementation.

The XC7300 family, based on an innovative Dual Block architecture, addresses both high-speed and high-density requirements on one complex programmable logic chip. The basic architecture along with easy-to-use conversion software and a broad family of devices and packages provide the best solution for PAL conversions. ♦

“The XC7300 family contains a number of unique system features that provide a clear upgrade path for PAL designers.”

The XC7300 Family of EPLDs.

■ High-Density FB
■ FAST FB



Equiv. PALs	3-4	6	8	12	16
Registers	36	108	126	198	234
t_D	7.5ns	10ns	10ns	12ns	10ns
t_{CYC}	125MHz	100MHz	100MHz	80MHz	100MHz
Packages	44 PLCC	44/68 PLCC	68/84 PLCC	84 PLCC 144 PGA 160 PQFP	184 PGA

The XC7336™: 7.5ns and 100 Percent Routable GUARANTEED

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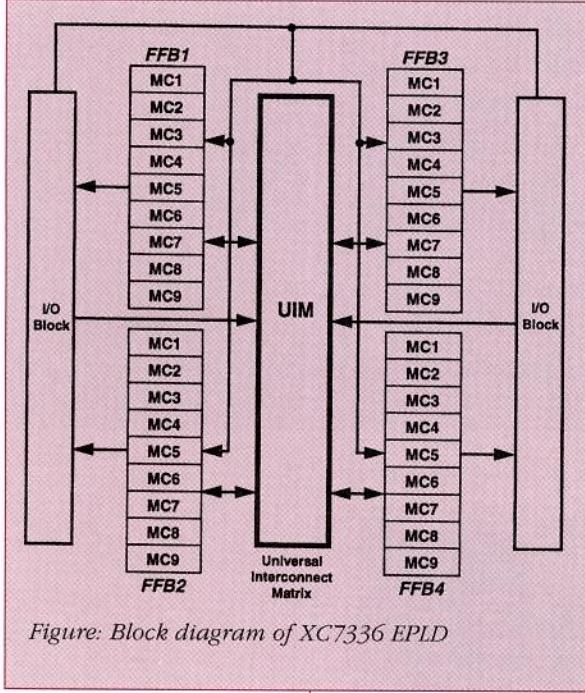


Figure: Block diagram of XC7336 EPLD

The PAL-like logic block includes 24 inputs, an AND array generating 45 product terms, and nine outputs. The high ratio of inputs to outputs ensure maximum use of the logic block, while an average of five product terms per output provides high performance.

The XC7000 EPLD family, best known for its industry-leading Dual Block™ architecture and 100 percent routable Universal Interconnect Matrix (UIM™), is getting a new high-performance addition.

The new Xilinx XC7336 offers 7.5ns pin-to-pin speeds, clock-to-output delays of 4.5ns and 125 MHz clock rates, rivaling the industry's fastest low-density PALs and GALs. This 36-macro-cell CMOS device integrates the equivalent functionality of three-to-four 22V10-type PLDs into a single 44-pin PLCC while also offering significant power and board space savings. This makes the XC7336 an excellent fit for high-speed applications such as memory address decoders and multi-plexers.

The XC7336 consists of four Fast Function Blocks (FFBs), each with nine macrocells (see figure), designed to address the highest speed requirements of any performance-related application.

Any UIM input (coming from a FFB output or an I/O pin) can connect to any FFB's input. The delay through the UIM is constant (regardless of the apparent routing distance and complexity) and independent of fan-out and fan-in. With guaranteed routing capability and predictable interconnect delays, XC7336 users achieve nearly 100 percent on-chip logic resource utilization.

Each output is capable of driving a full 24mA, eliminating the need for external bus drivers. Also, a built-in 3.3V/5V logic and level shifting feature allows for easy, direct interface for systems that require a mix of 3.3 and 5 volt logic. This 3.3V I/O operation is achieved without any loss in performance while eliminating the need for "speed-robbing" discrete level translation buffers.

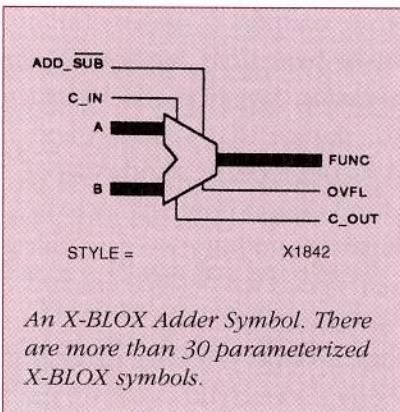
Designs are supported by the Xilinx EPLD translator software, XEPLD™. This easy-to-use tool is designed to work with industry-standard logic compilers such as ABEL, CUPL and PALASM, offering an efficient, productive path to high-density logic integration. For example, a design using PALs such as 22V10s and 20V8s can be imported and directly converted with XEPLD acting as a fitter, taking the design description and mapping it into the XC7336.

The XC7336 will be available in 44-pin PLCC/CLCC in November 1993 for both commercial (0°C to +70°C) and industrial (-40°C to +70°C) temperature ranges. Military temperature (-55°C to +125°C) and MIL-STD-883 versions packaged in the 44-pin CLCC are targeted for 1Q94 and 1Q95 availability, respectively. ♦

X-BLOX Boosts HDL Synthesis Performance

Optimal data path synthesis for XC4000

You're probably familiar with X-BLOX™ as a graphical 'synthesis' tool for schematic-based designs. You capture X-BLOX symbols in your schematic and X-BLOX then synthesizes and optimizes your design using the special system features of the XC4000 FPGA architecture: dedicated fast-carry logic, on-chip RAM, flip-flops in the I/O, global clock buffers, and global reset. The result is faster and more area-efficient designs.



But did you know that X-BLOX can also be used with designs entered with VHDL and Verilog/HDL? Synthesis tools from Synopsys, Viewlogic, Cadence Design Systems, IBM, Mentor Graphics, Exemplar Logic, and Racal-Redac can or will soon be able to work in conjunction with X-BLOX to yield better synthesis performance.

HDL Synthesis Design Flow with X-BLOX

In a typical HDL-based design flow with X-BLOX, you first enter your design as HDL code. Your synthesis tool creates a netlist with a combination of X-BLOX modules and Xilinx primitives. The X-BLOX modules may be "inferred" automatically. For example, the signal assignment "A<= B + C;" could infer an X-BLOX adder. Logic that cannot be inferred to X-BLOX modules is synthesized to Xilinx primitives.

Next, X-BLOX synthesizes the X-BLOX modules to Xilinx macros that use the XC4000's system-integration features. These features automatically come into play when you use X-BLOX, resulting in synthesis performance improvements.

Not all third party HDL synthesis tools have the ability to infer X-BLOX modules. Instead, they may use X-BLOX modules via explicit structural instantiation. In the example above, "A <= B + C;" inferred the creation of an X-BLOX adder. With structural instantiation, you explicitly call out an X-BLOX adder from an HDL package. For example, "XB_ADD_SUB (A => A, B => B, C_OUT => C)." Different third party HDL synthesis tools support one or both methods.

Inferred and instantiated methods of using X-BLOX modules each have advan-

tages. With inferred modules, your HDL code stays completely technology-independent, permitting you to synthesize the same HDL code to any technology. With instantiated modules, you can explicitly define any X-BLOX module giving you greater control in determining how your design will synthesize.

X-BLOX HDL Debut in '94

To meet the needs of both schematically-based and HDL-based X-BLOX users, a new X-BLOX add-on will be available in mid-1994: **X-BLOX HDL**.

X-BLOX will continue to be improved to support gate-level simulation with schematic back-annotation. Over time, more graphical modules like multipliers will be added.

X-BLOX HDL will be better integrated into HDL synthesis tool environments, adding support for the Library of Parameterized Modules (LPM) standard. By supporting LPM, X-BLOX will be able to communicate with your synthesis tool, exchanging constraint, area, and timing information to yield better results. Both X-BLOX and X-BLOX HDL will add support for the XC3000 FPGA family.

So whether your method of Xilinx design entry is drawing schematics or typing HDL code, X-BLOX products can boost your chip performance. ♦

Demand for HDL Synthesis Tools for Xilinx FPGAs Increasing

Today, many engineers are exploring the use of high-level design languages and logic synthesis to gain faster time-to-market, reusable designs and technology-independent files that are transferable from project to project and engineer to engineer.

However, there are trade-offs. There is a learning curve associated with Hardware Description Languages (HDLs), the languages for composing designs that are the input files to synthesis tools. To be an effective designer, one must first learn the language and then learn to design with the HDL.

Historically, synthesis has been used for ASIC and gate array designs. As a result, synthesis optimization algorithms were created to support

those gate-oriented architectures. New technologies, such as FPGAs, have since been introduced with very different architectures. Using ASIC algorithms that synthesize to gates for an FPGA will yield less-efficient results than an algorithm tailored to the FPGA architecture. Xilinx is addressing this by providing synthesis vendors with information on X-BLOX™ technology.

X-BLOX

The first of its kind, X-BLOX allows a standard library of high-level blocks to feed FPGA synthesis tools. The X-BLOX optimizer helps designs make use of on-chip system features, such as carry logic, wide decoders, global clock buffers and RAM/ROM. Knowledge of the CLB architecture enables it to efficiently partition logic

“Many engineers are exploring the use of high-level design languages and logic synthesis to gain faster time-to-market.”

into CLBs and place them in a way that will achieve the fastest performance. It is more efficient to synthesize logic into X-BLOX functions rather than gates. Many synthesis vendors are adding X-BLOX support to their synthesis products.

Vendors can concentrate on synthesizing a design to these high-level blocks and let Xilinx concentrate on implementation efficiency.

Xilinx Syndicate Program

To address the growing demand for synthesis, Xilinx has introduced the Syndicate program to help its users achieve optimal FPGA designs when using HDL synthesis. Xilinx and its Syndicate partners (*Compass Design, Exemplar Logic, IBM, Mentor Graphics, Racal-Redac, Synopsys and Viewlogic*) aim to entwine HDL synthesis and FPGA layout tools. A standardized, high-level design flow will increase productivity and improve gate utilization and speed for designs entered with an HDL.

Xilinx product offerings include Viewlogic's ViewSynthesis™ on the PC and a Synopsys interface and libraries for workstations (*Sun, HP7XX*).

ViewSynthesis

ViewSynthesis offers all the capabilities of the Viewlogic software, but is restricted to Xilinx libraries. It is available as part of the Xilinx stand-alone package of Viewlogic software called the Extended Package (DS-VLS-EXT-PC1). The VHDL input format can be simulated as well as synthesized. The libraries support XC2000, XC3000, XC3000A, XC3000L, XC3100 and XC4000 family devices.

ViewSynthesis can instantiate X-BLOX modules, which means the X-BLOX functions can be directly

called using structural VHDL. This makes the design file technology-dependent, but it increases the efficiency of the synthesis result.

Xilinx Synopsys Interface

The Synopsys interface and libraries contain support for XC3000, XC3000A, XC3000L, and XC4000 devices. Version 3.01 of the DS401 software supports both the Design Compiler and FPGA Compiler. The FPGA Compiler contains specific architecture optimization algorithms for the XC4000 devices that increase the efficiency of the synthesis results. To increase efficiency further, the Xilinx-Synopsys Interface also includes a library of X-BLOX modules (currently, they include adders, subtracters and comparators). When specified in the .synopsys file, the Synopsys synthesizer automatically selects the appropriate X-BLOX modules as it processes the HDL code. Both the Design Compiler and FPGA Compiler support automatic I/O insertion.

Future Plans for Synthesis

Viewlogic-ViewSynthesis: By the end of 1993, ViewSynthesis will synthesize directly to X-BLOX modules. This will eliminate the need for direct instantiation and provide a technology-independent file while reaping the benefits of X-BLOX technology.

By 2Q94, ViewSynthesis will provide automatic I/O insertion and XACT-PerformanceTM support.

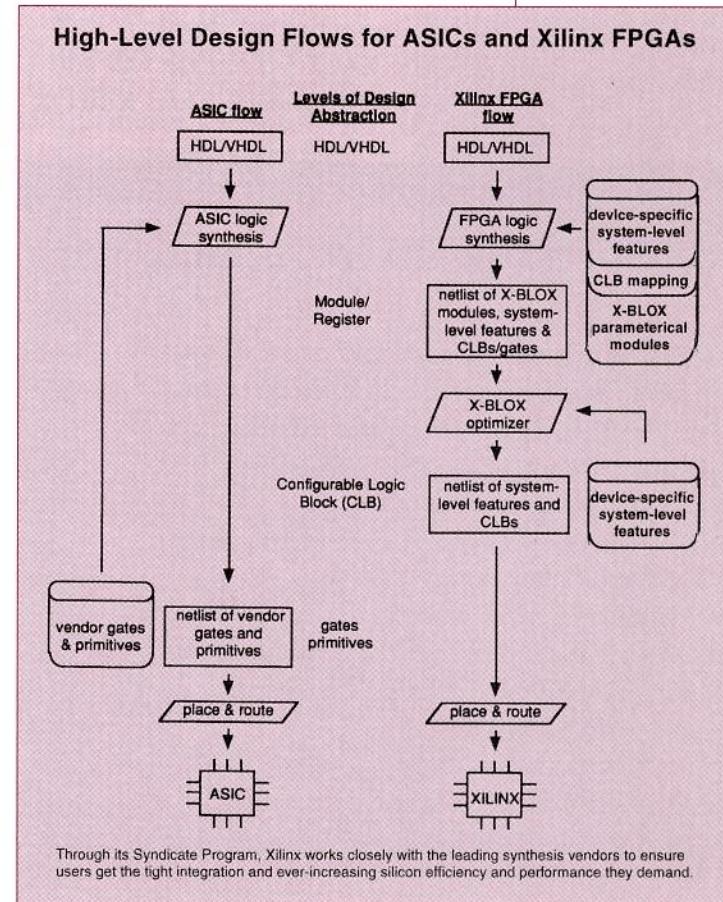
Synopsys-FPGA Compiler and Design Compiler: By 1Q94, Version 3.1 of the FPGA Compiler will support:

- Forward annotation of timing constraints to layout (support for XACT-Performance)
- Back-annotation of post-layout timing via XNF and SDF

- Automatic mapping to negative-edge flip-flops
- Mapping to sequential I/O cells
- Synthesizing to XC4000 Clock Enable logic

Summary

Xilinx plans to increase the efficiency of implementations resulting from synthesis by using X-BLOX technology. X-BLOX has the knowledge of the Xilinx FPGA architecture that maximizes efficiency and performance. Today, many synthesis vendors are supporting X-BLOX and more will continue to do so through the Syndicate program, a Xilinx alliance group of synthesis vendors. Although synthesis is not a panacea for all design issues, Xilinx and synthesis vendors are working to improve synthesis results so that the benefits can be realized in all types of designs. ♦



XACT 5.0® Release Offers Unified Library, Ease-of-Use

The next release of our XACT software will round out our software offerings across families. To start, we will be shipping a unified library that contains common symbols across all Xilinx programmable logic families -- XC7000 series CPLDs as well as XC2000, XC3000 and XC4000 FPGAs.

For the XC4000 series, XACT 5.0 will include incremental/iterative design capability similar to that already available in the XC2000/XC3000 family. Simulating XC4000 series design will be significantly easier, especially those which include either X-BLOX™ modules or hard macros. XACT 5.0 will support the use of XC4000 carry-logic and relative location constraints from the schematic level.

The XACT 5.0 release will add XACT-Performance™ and X-BLOX

support for the XC3000A family. XACT-Performance allows designers to specify their performance requirements up front. The software places and routes the design to meet those requirements, focusing its effort on the critical paths of the design instead of trying to make the entire design fast.

All software in the XACT 5.0 release will be DPMI-compliant, allowing DOS tools to be called from within Windows.

The XACT 5.0 release also will offer significant improvements in routability and performance -- especially for larger devices such as the XC4010™ and the XC4013™.

XACT 5.0 is scheduled to ship on the PC and Sun platforms by year's end. Other platforms will follow. Look for more information on the upcoming XACT 5.0 release in next quarter's *XCELL!* ♦

NEW PRODUCT PREVIEW

Xilinx Software To Be Available on CD-ROM Media

Xilinx is riding the wave of the future. Starting in early 1994, Xilinx software and updates will be available on CD-ROM media for the PC and most workstations (Sun and HP 9000 / 700 Series). Here are some of the benefits :

- Faster Installation. No more wasting your time, feeding floppy after floppy into your PC. No more waiting for your workstation tapes to spin, looking for the proper data. Installing or updating your Xilinx software is as easy as popping in one CD-ROM disk.
- Software Compatibility. With CD-ROM, all Xilinx software for your platform is on the same disk. New install utilities will monitor your soft-

ware configuration, ensure executable version compatibility, and update only the necessary files to keep your software up-to-date. Saving old versions of XACT software is as easy as storing one CD-ROM disk.

- Future Improvements. Xilinx will eventually add on-line documentation, tutorials, and product demonstrations.

To start getting your updates on ISO 9660 standard CD-ROM, simply FAX a letter to Xilinx Customer Service at (408) 559-0115. Indicate the serial numbers of each of the products required on CD-ROM. ♦

Letters and Numbers:

FPGA, LCA, CPLD, PLD

FPGA (Field Programmable Gate Array) is the generic name for all channel-routed, user-programmable logic devices such as the XC2000, XC3000 and XC4000 families.

LCA (Logic Cell Array)™, a reference to the Xilinx FPGA architecture, is a Xilinx trademark, and should, therefore, only be used as an adjective (e.g., LCA device, LCA architecture).

EPLDs (Erasable Programmable Logic Devices) are more-structured, coarse-grained devices based on a PAL® architecture (PAL is an AMD trademark) like the XC7300 family.

CPLD (Complex Programmable Logic Device) is used as a generic-sounding synonym for EPLD.

PLD (Programmable Logic Device) describes all programmable logic, from the smallest PAL device to the largest FPGA. (To confuse matters, the trade press and some vendors will use FPGA and/or CPLD as an all-encompassing label for both channel-routed and PAL-structured high-density PLDs.)

XC2064 to XC4013

The XC2064® was the first Xilinx device and the first FPGA. There was no XC1000 family. XC has become the recognized Xilinx prefix, as with i for Intel or Am for AMD.

The very first device was called XC2064 to describe its $8 \times 8 = 64$ CLB structure. This nomenclature was never used again; all later Xilinx FPGAs use the two trailing digits to describe the claimed gate density (expressed in multiples of 100 gates for the XC2000 and XC3000 families and in multiples of 1000 gates for the XC4000 family). The XC2000 and XC3000 families count the highest number of gates that can be

implemented, assuming that all function generators and flip-flops are being used. A typical gate-count value is 40 percent lower because some function generators may be used to implement simple logic, some flip-flops may be unused, and some CLBs may not be routable. The XC4000 family uses a more conservative method of counting gates. A typical design will pack the claimed number of gates, and substantially more when some function generators are used as RAM.

XC3100 describes a speed-enhanced version of the XC3000 family, with identical functionality and bitstream compatibility. The XC3195™ is a new member with 50 percent higher CLB count than the XC3090® or XC3190™.

XC2300, XC3300 and XC4300 are HardWire™ derivatives of the respective FPGA families, offering lower cost for volume production.

XC7000

XC7000 describes the Xilinx EPLD offerings. The original devices are the XC7236™ and XC7272™, with 36 and 72 macrocells respectively. The new devices using the Dual Block™ Architecture are called the XC7336™ through XC73108™, again listing the number of macrocells after the leading two digits.

What about the A?

Different product lines use the suffix A for different purposes.

- **XC3000A** is a new, functionally enhanced variation of the XC3000 family. It has better connectivity, bitstream error checking, and a better start-up behavior. Any

*A Guide to
Xilinx Part
Numbers*

“XC has
become the
recognized Xilinx
prefix, as with i
for Intel or Am
for AMD.”

XC3000/ XC3000A/ XC3000L Bitstreams Compatible

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Comparable density devices in the XC3000 and XC3100 families are totally bitstream compatible.

XC3000A devices have additional switches in the routing controlled by bit locations in the bitstream which are unused in the XC3000 devices. So, bitstreams generated for an XC3000 FPGA can be successfully downloaded into the corresponding XC3000A device, but the additional routing resources would not be used. However, bitstreams generated from XC3000A designs should not be loaded into an XC3000 device. In other words, the XC3000A is upward-compatible with XC3000 bitstreams, but not downward-compatible.

The internal architecture of the XC3000L is identical to the

XC3000A, so their bitstreams are compatible. The XC3000L is upward-compatible with XC3000 bitstreams *with one exception*. In XC3000L designs, due to internal loading considerations, horizontal long lines cannot be connected to both of their available pull-up resistors; only one pull-up per long line is allowed. (Pull-up resistors often are associated with long lines that are used to implement wide wired-AND or wired-multiplexer circuits.)

So, if the XC3000 or XC3000A design contains long lines with both pull-up resistors connected, the design will need to be modified to connect only one pull-up resistor per long line and a new bitstream generated in order to migrate the design to an XC3000L device. ♦

A GUIDE TO XILINX PART NUMBERS -- CONTINUED FROM THE PREVIOUS PAGE

XC3000 design can be upgraded to the XC3000A with no change, not even to the bitstream.

- **XC4000A** describes the smaller members of the XC4000 family which do not need the generous interconnect structure of the larger devices. Only the XC4005® exists in both flavors: the XC4005A™ has the optimized-interconnect structure and is less expensive, while the XC4005 has the full-interconnect structure and is more expensive. Though not bitstream-compatible, both devices come in the same packages and with the same pin-out. (The XC4003™ is an early device, not recommended for new designs. Use the XC4003A™ instead.)
- **XC7236A™** and **XC7272A™**. The “A” parts are functionally identical to the original parts, but are manufactured using a more advanced process, requiring a different programming algorithm with a lower programming voltage. This mandates a new part number, although the “A” parts behave identically in the user application.
- **XC1736A™**. The XC1736™ was the original serial PROM. When it was changed to a more advanced process, the programming algorithm and voltage changed. This mandates a new

part number, although the “A” part behaves identically in the user application.

The new, redesigned and unified family of XC17000 devices uses the suffix “D”, since “A” was already used for the XC1736A. The suffix “B” denotes military devices, and “C” is overused to indicate commercial temperature or ceramic packages.

Speed designations

Early Xilinx FPGAs (XC2000 and XC3000 families) describe device speed by the guaranteed worst-case toggle rate of the CLB flip-flops. As devices become faster, this toggle frequency approaches 300 MHz and is no longer a meaningful indicator. The newer families, starting with XC4000 and XC3100, use the combinatorial delay through a function generator (T_{ILO}) expressed in nanoseconds to designate speed. “-5” describes a device with a T_{ILO} of 4.7 ns, roughly equivalent to a -100 in the older designation.

EPLDs designate device speed by the fastest combinatorial delay from input pin to output pin in ns. There is no speed designation in the Serial PROM part number. See the data sheet for details. ♦

8 mA Outputs in XC3000A OK in Some Cases

While XC3000A devices have their output sink current (I_{OL}) specified as 4 mA, some device/package combinations can easily handle 8 mA. Xilinx has long indicated that individual outputs can be used to sink higher currents. Sinking 8 mA, or even 10 mA, cannot damage an output, although it may cause a slight increase in output voltage. It is only when a large number of outputs sink high currents that damage can occur. In some low-pin-count packages, however, all of the available outputs can sink 8 mA without damage because so few are made available.

Three factors determine the usable sink current (*see figure*). The most obvious factor, although not the most critical, is the pull-down transistor. This transistor is much larger than I_{OL} would suggest. It is designed for transition speed, and must supply the high instantaneous current needed to discharge the load capacitance. Consequently, the voltage drop for small currents is only 20 mV per mA; an increase from 4 mA to 8 mA changes the output voltage by only 80 mV.

The second factor that limits the output sink current is the voltage created when the combined sink current of all outputs flows through the ground metal on the chip, the bond wires and the package ground pins. The sum of this voltage and the transistor voltage must remain less than the output Low voltage, V_{OL} .

The magnitude of the combined sink currents in the ground metal is the last and usually most critical

factor. In absolute terms, the cross-section of the ground metal on any chip is very small. Consequently, currents as low as 10s of mA can cause metal migration. Over a long period of time, the current moves metal around on the chip, slowly degrading it.

All Xilinx FPGAs are designed for worst-case conditions; it is assumed all device outputs will sink their full I_{OL} simultaneously. While unlikely in any package, this condition is physically impossible in low-pin-count packages because many outputs are left unbonded and cannot sink current.

If only half the outputs are bonded and these are uniformly distributed around the chip, 8 mA sink current can only create the same total ground current and voltage as all outputs would sinking 4 mA. The additional transistor voltage is not a significant problem if not all bonded IOBs are used as outputs, and if those that are do not all go Low simultaneously and sink the full I_{OL} . Furthermore, Xilinx devices are rated extremely conservatively.

It is possible, therefore, to treat some XC3000A device/package combinations as having a higher I_{OL} . The following combinations have sufficiently few bonded IOBs that an 8 mA I_{OL} can be assumed: XC3030APC44, XC3064APC84, and XC3090APC84. ♦

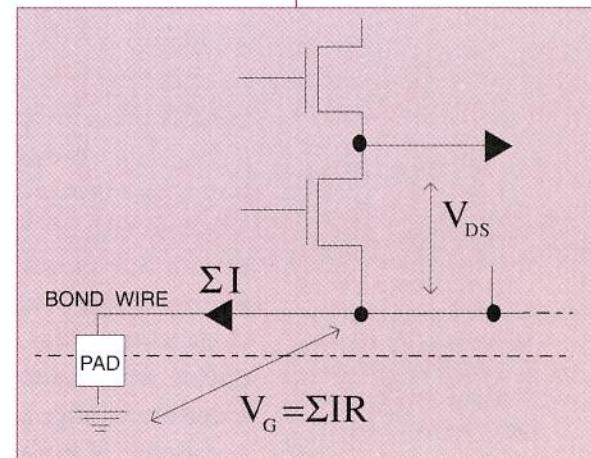


Figure : Three factors determine usable sink current: the voltage drop across the output transistor, the voltage drop caused by the intrinsic resistance of the bond wire and ground pad and the magnitude of the total sink current in the ground metal.

Bitstream Error Checking in XC3000A Improved Over XC3000

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

XC3000 and XC3000A start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000 devices do not check for the correct stop bits, but XC3000A devices check that the last three bits of any frame are actually 111.

Under normal circumstances, the XC3000 and XC3000A FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done, but with incorrect configuration and the possibility of internal contention.

An XC3000A device starts any new frame only if the three preceding bits are all ones. If this check fails, the XC3000A pulls INIT Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 μ s Low level on RESET.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges. A separate modification slows down the RESET input during configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond glitches on RESET during configuration and simplifies the "Short Power-on Delay" application described in *XCELL #8*.

The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only). ♦

Cavity Up or Cavity Down? Die Placement Affects Heat Flow

Most Xilinx devices attach the die against the inside bottom of the package (i.e. against the outside surface that does not carry the Xilinx logo and device designation). This is called "cavity-up" and has been the standard assembly method for more than 25 years, even though it is not ideal from a thermal point of view.

Large Xilinx Pin Grid Arrays (>130 pins) and Ceramic Quad Flat Packs are assembled differently. The die is attached to the inside top of the package. For an illustration, see the back cover of all Xilinx Data Books, 1989 through 1992, showing the XC3090® with the bottom lid taken off. Attaching the die against the inside top of the package optimizes heat transfer to the ambient air.

Continued on the next page

Implementing ROM in XC3000 Devices

The RAM/ROM feature of the XC4000 CLB is well-known and supported by software. XC4000 CLBs, though, only differ from other CLBs in their ability to write data, thus providing a RAM. All LCA™ function generators can be used as ROMs, including those in the XC3000.

While table entry, such as provided by MEMGEN, is not supported in XC3000, two new Xilinx library symbols permit convenient entry of ROM data in the schematic. In addition to the expected address inputs and data outputs, the new symbols have 32 data inputs, one for each bit of ROM. Data is entered into the ROM by simply connecting these inputs to VCC or GND as desired.

Internally, the 16x2 ROM macro (see figure) is a dual 16:1 multiplexer. Connecting VCC and GND to the multiplexer inputs creates a function that is logically equivalent to the required ROM. A CLBMAP in the macro causes XACT® to

implement the multiplexer in a single CLB. The VCC and GND connections are absorbed into the function-generator lookup table, leaving only the address inputs and data outputs. Data inputs to the macro should only be connected to VCC and GND.

Other signals will prevent the conversion to a single CLB.

The ROM access time is T_{IL} , the combinatorial delay of the device. Viewlogic symbols are available for both 16x2 and 32x1 ROMs. They are named X3K_16X2 and X3K_32X1 and may be downloaded from the Xilinx Technical Bulletin Board Service (408-559-9327). ♦

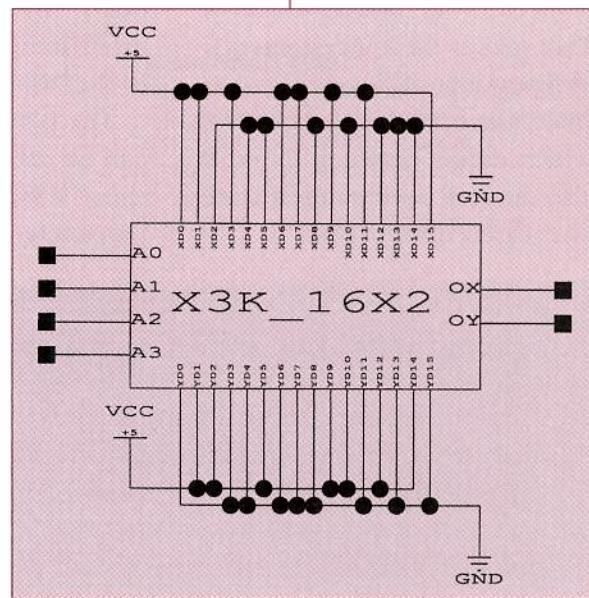


Figure: 16 x 2 ROM macro for the XC3000 series showing example connections of VCC and GND to the multiplexer inputs.

Continued from the previous page

For most packages, this information may be of only academic interest because the user has no choice. For Ceramic Quad Flat Pack (CQFP) packages, however, it may influence the way the user forms the leads. For the best heat transfer to the surrounding air, these packages should be attached to the PC board in such a way that the surface with the logo faces up, away from the PC board, with the metal lid facing the PC board.

Obviously, both the orientation of the die in the package and the orientation of the package on the PC board have a profound impact on the PC board layout.

PLCC and PQFPs count pins in a *counterclockwise* direction when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin #1 in the center of the beveled edge, while PQFPs have pin #1 in one corner.

CQFPs count pins in a *clockwise* direction when viewed from the surface with the Xilinx logo; and, they have pin #1 in the center of one edge. The user can make the pin count run in the more conventional counterclockwise direction, but that means forming the leads in such a way so that the logo mounts against the PC board, impairing the heat flow to the surrounding air. ♦

XC4000 Specifies Pin to-Pin Timing Parameters

Input setup and hold times, as well as output delays, are traditionally specified with respect to the internal clock. That makes these parameters independent of device size, since it is only the clock delay which differs between different size devices of one family and one speed designation.

To arrive at the real pin-to-pin values, the user has to include the on-chip clock delay by adding it to the output delay, subtracting it from the input setup time, and adding it to the hold time value.

The pin-to-pin setup time can be difficult to assess because it is not obvious what percentage of the clock delay

should be subtracted. Subtracting 100 percent of the worst-case value would be overly optimistic, assuming perfect delay tracking on the chip. Xilinx recommends that the user subtract 70 percent of the guaranteed maximum clock delay. This may be overly conservative, but it is a safe

Continued on the next page

Avoiding the Pitfalls of Asynchronous Clocking in FPGAs

Wherever possible, FPGA designs should be fully synchronous with one clock. Such designs are most easily understood, the least error-prone and fit well in Xilinx FPGA architectures. While asynchronous inputs cannot always be avoided, they can easily be accommodated if a few simple guidelines are followed.

Clocking asynchronous input data into a flip-flop creates problems when the data changes within the set-up/hold-time window around the clock edge. Either the old or the new data can be captured, and, in rare instances, a metastable condition arises.

In its metastable state, a flip-flop pauses in an indeterminate state for a short period before either returning to its previous state or attaining its new state. If a few extra nanoseconds are allowed for clock-to-output delay, analysis of XC3000 devices* shows that the mean time between metastability events can be thousands of years. These extra nanoseconds are usually available because worst-case devices and conditions are seldom encountered. XC4000 devices should be less metastable prone than XC3000 devices.

The uncertainty of capturing new or old data is not really a problem. The data is arriving asynchronously, so new data that

is not captured early enough by one clock is guaranteed to be captured by the next. In practice, propagation delays require active steps to ensure this happens

Guidelines

- **Only transfer serial data.** If more than one bit is transferred in parallel across an asynchronous interface, differences in data delay and exact capture times can create hybrid data that contains bits from both the old and new data. In this case, transfer serial data; a single old/new-data decision, while arbitrary, is always self-consistent.
- **Capture data in one place only.** If an asynchronous signal is captured in more than one flip-flop, some may get the new data while others get the old data. This inconsistency is resolved by capturing the data only once, and distributing the result, be it old or new data.
- **Transmit data from only one source.** Glitches or other transitory conditions can be captured by an asynchronous clock and be treated as data. Unless combinatorial data is guaranteed to be glitch-free, register the data before transmission across an asynchronous interface.

* See XAPP 024 in Chapter 8 of the 1993 Data Book:
Additional XC3000/XC3100 Data ♦

Continued from the previous page
method which understates device performance.

For XC4000 devices, the 1993 *Data Book* now publishes tested and guaranteed pin-to-pin parameters. These published values are slightly better than the values calculated from the speeds files. The user can be assured that

these 100 percent tested pin-to-pin values are more authentic than the calculated values. This is the only case where the Data Book numbers have a higher authority than the data in the speeds files and other simulation and report files.

Here are two examples, using the XC4005-5®:

Clock-to-Output Delay:

*calculated by adding worst-case T_{OKPOF} (clock-to-pad delay, fast slew rate) and T_{PG} (global clock delay):
 $7.0\text{ ns} + 6.0\text{ ns} = 13.0\text{ ns}$
measured and guaranteed: 13.0 ns
(g.e., same as calculated)*

Input Setup Time:

*calculated by subtracting 70 percent of T_{PG} (global clock delay) from T_{PICKD} (setup time, pad-to-clock [IK] with delay):
 $24.0\text{ ns} - (0.70 * 6.0\text{ ns}) = 19.8\text{ ns}$
measured and guaranteed: 18.0 ns
(g.e. 1.8 ns better than calculated) ♦*

RESET Polarity on the XC1736D

Question: *Since the XC1736D™ has RESET polarity, and the XC1736A™ doesn't, can I use the same PROM files for the XC1736D as I did for the XC1736A?*

Answer: YES, you can!!! The files are the same.

The PROM files for the XC1736A and XC1736D will be the same. The reason for this is related to the way the RESET polarity bits are programmed. The basic PROM file (that is output from MAKEPROM) does NOT contain any information regarding the RESET polarity (MAKEPROM doesn't know anything about it). Therefore, it doesn't matter at this point whether the target device has programmable RESET polarity or not.

So how is the RESET polarity specified? It's all done at the programmer level when the devices are actually programmed. Let's look at examples of what happens with two different programmers:

- **Xilinx DS112™ PROM programmer:** This programmer is supplied with the XPP™ software. The user selects the device to be programmed from the available device list. When the device is selected, the software checks to see if that particular device has programmable RESET polarity. If it does, the user is asked if the RESET polarity is to be High (default) or Low. The programmer then sets the appropriate memory locations and programs devices that way until a new device is selected or a new file is downloaded.

If the user selects the default, the device operates exactly the same way as the XC1736A

- **Data I/O Unisite:** After selecting the desired device from the menu, the user must explicitly set specific memory locations. The RESET polarity bits on the XC1736D are at memory locations 2000H-2003H. The user must access those specific locations and either fill them with all 1s (for active High) or all 0s (for active Low). This data must be entered manually.

If the user doesn't go in and set the appropriate memory locations, the programmer will attempt to use whatever data is already there. If the programmer had already been used to program a different device, the data at those addresses could be random.

In all cases, regardless of the specific method of setting the RESET polarity bits, it is done at the time of programming, and is NOT part of the bitstream. Therefore, the PROM files are identical for the XC1736D and XC1736A so there is no need for the user to generate new bitstreams. ♦

General

Q: While trying to invoke a command from XDM™ the following message is encountered: "command <command name> failed, rc= -1". What causes this?

A: This error is normally due to a problem with the PATH statement in the AUTOEXEC.BAT file. Typically, this error is introduced when, during the install process, the customer has modified the AUTOEXEC.BAT manually, rather than allowing the Xilinx install program to make the modification automatically. Usually, the customer has accidentally added a semicolon to the end of the PATH statement. Remove this semicolon and the error should go away.

Q: While attempting to run the Xilinx tools on my workstation, I encounter the message, "cannot connect to license server." Why?

A: Typically, the customer is experiencing network problems. However, in some cases, the customer may be experiencing one or more of the following:

1. The Highland license server, lmgrd, and the Xilinx daemon, XXACTD, may be different version numbers.
2. The hostid of the host machine, as understood by the license manager, may be wrong.
3. The TCP/IP software may not be running.

Two programs, xlmcn and xlmlg, can help the user determine the source of the error. These programs provide information about

the license manager and the license.dat file in addition to displaying all license manager activity. See the "Checking the Installation" section in the blue Xilinx Release Note for more information on these commands.

Q: In my XC4000 design, why are my signals that use the global buffers, BUFGP and BUFGS, using CLB feedthroughs?

A: While the XC4000 family does have up to eight global buffers available, these eight buffers compete for four vertical long lines with the secondary buffers having more flexibility. In addition, only the K pin on the CLB will always connect to a global long line, while the F3, G1, C1, and the C3 pins might connect to a global long line with intelligent partitioning and placement. As a matter of fact, do not expect PPR to connect the F3, G1, C1, or C3 pins directly to global long lines without intelligent floor-planning.

Q: The Xilinx databooks do not include all of your package pin-outs and dimensions.

Where can I get this info?

A: Information on the new package types has been included in Chapter 4 of the new 1993 Data Book. If not, your local sales representative or FAE should be able to provide this information to you. Finally, most new package information usually is placed on the Xilinx Bulletin Board Service.

Our Xilinx BBS phone number is (408) 559-9327. See the "Technical Support" section of the Data Book (Chapter 6) for instructions on using the Xilinx BBS.

Q: How can I determine the version number of a program that I am running?

A: There are two ways to determine the version number:

1. Invoke the program executable without any arguments from the DOS or UNIX command line.
2. Invoke the "Utilities/Version" command from within XDM.

Mentor Graphics

Q: While using Mentor V7 and attempting to back annotate to a schematic that has X-BLOX™ modules or hard macros, MBA2EREL is run creating the error message, "<instance> not found in DFI table."

A: This error is caused because the original schematic contains elements that make back annotation impossible. If a design has hard macros, X-BLOX modules, XABEL modules, or any other modules that do not have underlying schematics, then

the back annotated .xnf file will contain logic that is not represented directly on the schematic. The workaround is to run GEN_SCH, which will create a new schematic that contains all of the instances.

Q: Will the Xilinx DS-344™ v1.01 Interface work with Mentor V8.2?

A: No. Many program options have been changed in Mentor v8.2; therefore, the Xilinx scripts within the DS-344 interface had to be modified.

Viewlogic

Q: While running XNF2WIR, the following error message is encountered: "error 214: XNF pin names for <instance> do not match Viewlogic symbol."

A: This error message indicates that XNF2WIR has found a symbol in the .xnf file that it does not understand. Some likely causes and their workarounds:

1. The design may contain hard macros. (You may search the .xnf file for "DEF=HM" to determine if your design contains hard macros.) If the design contains hard macros, run PPR with the "justflatten=true" option. Note, however, that this is not a complete run of PPR, as only an unrouted, but flat, version of the design is produced. Then run LCA2XNF with the "-g" option to convert the hard macro to representative gates.

2. Improper setup of the viewdraw.ini file. At the end of the viewdraw.ini file, only the primary, appropriate part family, and the built-in libraries (in this order) should be uncommented (the “!” in the first column is a comment). It is very important that the primary library be first and the built-in library be last. An example viewdraw.ini file is shown (the directory paths will vary!):

```
(beginning of file deleted)
DIR [p] .                                (primary)
IDIR [m] \workview\x2000                  (x2000)
IDIR [m] \workview\mx2000                 (mx2000)
IDIR [m] \workview\x3000                  (x3000)
IDIR [m] \workview\xttl                   (xttl)
IDIR [m] \workview\mx3000                 (mx3000)
DIR [m] c:\workview\x4000                  (x4000)
DIR [m] c:\workview\mx4000                 (mx4000)
DIR [m] c:\workview\hm4000                 (hm4000)
DIR [m] c:\workview\xblox                  (xblox)
DIR [m] c:\workview\builtin                (builtin)
```

Synopsys

Q: I am not clear about the support within the Xilinx Synopsys Interface (XSI). Could you please review this with me?

A: Xilinx has three XSI packages: DS401 v2.0, ES401 v3.0, and DS401 v3.01, summarized below:

DS401™ v2.0

- Supports Design Compiler 2.2b or 3.0
- Does not support "insert_pads". IBUFs and OBUFs must be instantiated.

ES401™ v3.0

- Supports Design Compiler 3.0 or FPGA Compiler

- Supports "insert_pads" for IBUFs, OBUFs, OBUFTs, and BUFGPs.
- Uses the DesignWare library for the XC4000 family. Two Xilinx hard macros are included.

DS401 v3.01

- Supports Design Compiler 3.0 or FPGA Compiler
- Supports "insert_pads" for IBUFs, OBUFs, OBUFTs, and BUFGPs.
- Uses the DesignWare library for the XC4000 family. X-BLOX adder/subtractor and comparator macros are included. X-BLOX will use the IOB registers and global buffers for high fanout nets.

XABEL

Q: I cannot perform functional simulation on my design which contains XABEL modules. Why not?

A: The Synthx program within XABEL will create fmap, hmap, or eqn records when optimizing. Simulation modules for these records do not exist. Synthx needs to be executed with the "mapped_xnf=false" option to prevent the use of fmap, hmap, or eqn records. This is accomplished by adding the following line to the XACTINIT.DAT file in the project directory: /synthx/mapped_xnf=false. Functional simulation can then be performed.

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Cadence

Q: How do I add properties to symbols in Composer?

A: The procedures are described in the *Cadence User Interface Guide*, pp. 5-11. The main points to note are:

1. The filename must be of type "sym_prop."
2. The type must be "string."
3. The value field must contain the entire property description, i.e. for a hard macro property, the following string must be in the value field: 'DEF=HM.'

Xilinx users with technical questions can call the Xilinx hotline at 800-559-7778 between 8 a.m. and 5 p.m. Pacific time, send E-mail to hotline @xilinx.com, or send a FAX to 408-879-4676 ♦

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